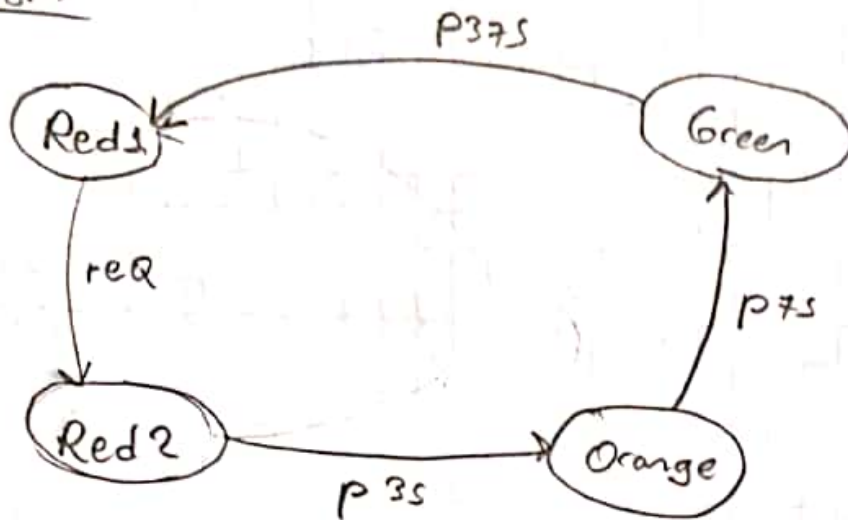


* CSE 234 Lab 5

* inputs = req, p35, p75, p375

* outputs = resetT, redL, orangeL, greenL

1) FSM



* 4 states = 2 bit registers (s1, s0) + 4 inputs

* 2 bit register for the next state (n1, n0) + 4 outputs

3) s1 s0
 0 0 → Red1
 0 1 → Red2
 1 0 → Orange
 1 1 → Green

4)

s1	s0	A req	B p35	C p75	D p375	n1	n0	resetT	redL	orangeL	greenL
0	0	1	X	X	X	0	1	1	1	0	0
0	1	X	1	X	X	1	0	0	0	1	0
1	0	X	X	1	X	1	1	0	0	0	1
1	1	X	X	X	1	0	0	1	1	0	0

$$* \text{reset } T = s_1's_0' + s_1s_0 D$$

$$* \text{red } L = s_1's_0'A + s_1s_0D$$

$$* \text{org } L = s_1's_0B$$

$$* \text{green } L = s_1s_0'C$$

$$* n_1 = s_1's_0B + s_1s_0'C$$

$$* n_0 = s_1's_0'A + s_1s_0'C$$