CSE234 Lab 4 - Yeşim Yalçın - 200104004034

1-) States $(s_0, s_1, s_2, s_3) = 4$ states $= 2$ bit register
- → 2 bit for the next state
- → 2 inputs : a, b
- → 1 output : x

2-) States: $S_0 = 00$, $S_1 = 01$, $S_2 = 10$, $S_3 = 11$

3-) State Table

	C	Q	a	b	X	n1	n0
S_0	0	0	0	0	0	0	0
	0	0	0	1	0	0	0
S_0	0	0	1	0	0	0	1
	0	0	1	1	0	0	0
S_1	0	1	0	0	0	0	0
	0	1	0	1	0	0	0
S_1	0	1	1	0	0	1	1
	0	1	1	1	0	1	0
S_2	1	0	0	0	1	1	0
	1	0	0	1	1	1	1
$i2$	1	0	1	0	1	0	0
	1	0	1	1	1	1	0
S_3	1	1	0	0	1	0	0
	1	1	0	1	1	1	1
S_2	1	1	1	0	1	0	0
	1	1	1	1	1	1	1

* $X = CD'a'b' + CD'a'b + CD'ab' + CD'ab + CDa'b' + CDa'b + CDab' + CDab$

* $n1 = C'Dab' + C'Dab + CD'a'b + CD'a'b + CD'ab + CDa'b + CDab$

* $n0 = C'D'ab' + C'Dab' + CD'a'b + CDa'b + CDab$

* Karnough Map of X

CD \ ab	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

* $X = C$

* Karnough Map of n1

CD \ ab	00	01	11	10
00	0	0	0	0
01	0	0	1	1
11	0	1	1	0
10	1	1	1	0

* $n1 = Cb + C'Da + CD'a'$

* Karnough Map of n0

CD \ ab	00	01	11	10
00	0	0	0	1
01	0	0	0	1
11	0	1	1	0
10	0	1	0	0

* $n2 = CDb + C'ab' + Ca'b$