CSE 234 Logic Circuits and Digital Design

Lab 5 – Traffic Light Controller

Lab Session (Exact Duration: 75min):

You will design an FSM for a traffic light controller with following input and output signals:

req (input): this is pedestrian request button to cross the street. 1 means there are pedestrians who want to cross and 0 means there is no one.

p3s (input): it is the timer signal which shows that 3 seconds have passed.

p7s (input): it is the timer signal which shows that 7 seconds have passed.

p37s (input): it is the timer signal which shows that 37 seconds have passed.

resetT (output): if 1, the timer initializes to zero.

redL (output): if 1, red led is turned on otherwise it is off.

orangeL (output): if 1, orange led is turned on otherwise it is off.

greenL (output): if 1, green led is turned on otherwise it is off.

Assume you have these signals, therefore do not design your timer. During simulation you will give input signals by hand. Connect the led outputs to leds in right color in Logisim.

If there is a pedestrian who pushed the button and made **req** signal 1, then after *three seconds* the traffic light turns to orange and waits there for *four seconds*. Then it turns to green and waits there for *30 seconds* and then turns to red.

(*Hint look at the time differences in between three pXs signals. It can be easily implemented with 4 states.*)

a. First draw the finale state diagram for this problem.
b. Then draw state table for next state logic.
c. Then write down and simplify the Boolean expression for next state bits.
d. Design your resultant simplified circuit using Logisim.

Demo Session:

During demo, explain and simulate each step of your design. Do not forget you only have at most 4 minutes for that. Also you will answer any questions asked by the TA.