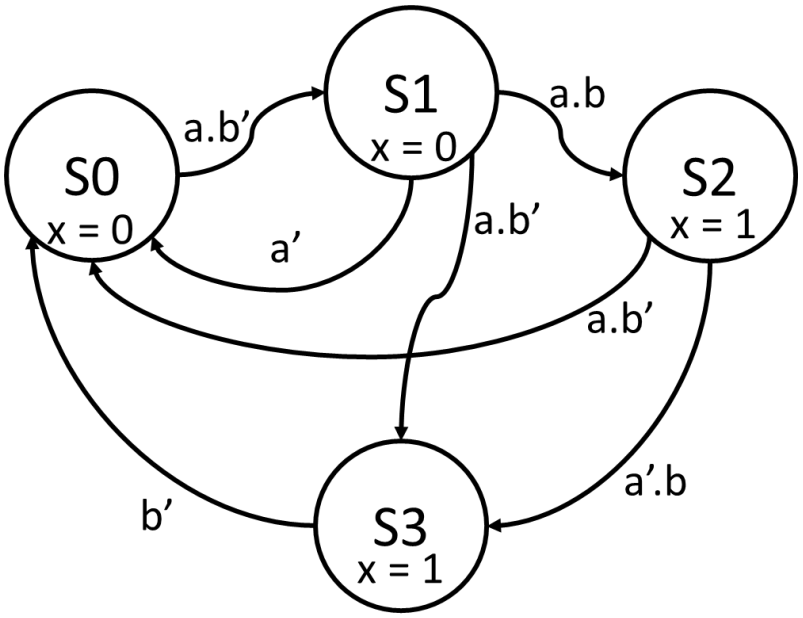
CSE 234 Logic Circuits and Digital Design

Lab 4

Lab Session (Exact Duration: 60min):

You will design the following FSM in this lab session:



Assume if any one of the transition conditions is not satisfied, then the FSM stays at its current state.

a and b are input signals and x is the output signal for that FSM. Connect x signal to a red led. a and b will be the input pins for your FSM.

a. Draw the state table for this FSM.
b. Extract and simplify Boolean equations for next state logic using your table.
c. Design and simulate your FSM in Logisim. Do not forget to observe the state when different inputs come to the FSM.

Demo Session:

During demo, explain and simulate each step of your design. Do not forget you only have at most 4 minutes for that. Also you will answer any questions asked by the TA.