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Revision History

REV	DESCRIPTION
0.1	EVT1.0 first release for review

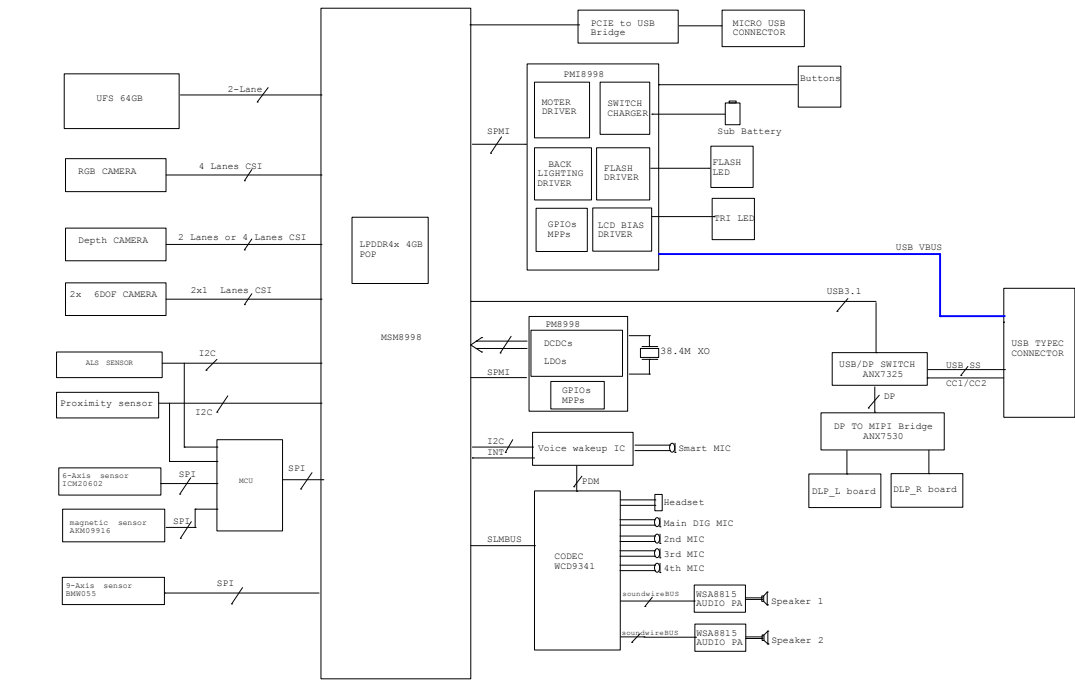
Board Change History

SCHEMATIC MCN	HW VERSION	REVISION	DESCRIPTION OF CHANGE

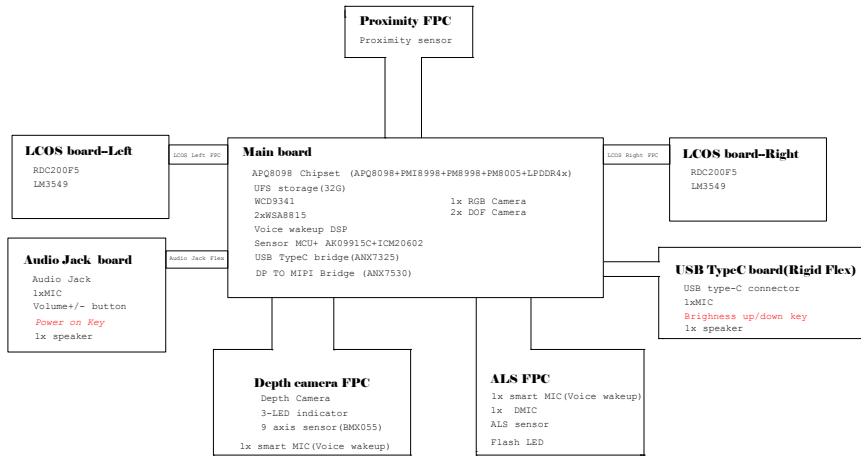
Revision History



Schematic Block Diagram



PCB split definition:



Block Diagram



Rev	1.0
Date	2023-08-01
Author	flex
Checker	flex
Approver	flex

MSM8998 GPIO Configuration for Irongate HMD					
GPIO_0	ANX7401_INTF	GPIO_41	6DOF_FRAME_SYNC	GPIO_82	MCU_SPI1_MISO
GPIO_1	ANX7401_RESET_N	GPIO_42	6DOFL_STROBE	GPIO_83	MCU_SPI1_CS
GPIO_2	BLSP1_I2C_SDA	GPIO_43	VOICE_LCD_I2C6_SDA	GPIO_84	MCU_SPI1_SCK
GPIO_3	BLSP1_I2C_SCL	GPIO_44	VOICE_LCD_I2C6_SCL	GPIO_85	VOICE_SPI_MOSI
GPIO_4	MSM_UART_TX	GPIO_45	NC	GPIO_86	VOICE_SPI_MISO
GPIO_5	MSM_UART_RX	GPIO_46	ANX7325_INTF_TO_AP	GPIO_87	VOICE_SPI_CS_N
GPIO_6	ANX7530_FWR_EN	GPIO_47	MICRO_USB_VBUS_EN	GPIO_88	VOICE_SPI_CLK
GPIO_7	ANX7530_RST_EN	GPIO_48	MICRO_USB_VBUS_OCB_EN	GPIO_89	VOICE_RESET_N
GPIO_8	ANX7401_FWR_EN	GPIO_49	NC	GPIO_90	ANX7401_1P8_EN
GPIO_9	ANX7401_CABLE_DET	GPIO_50	USBC_DET_TO_AP	GPIO_91	VOICE_WAKE_UP_N
GPIO_10	BLSP4_I2C_SDA	GPIO_51	NC	GPIO_92	NC
GPIO_11	BLSP4_I2C_SCL	GPIO_52	CAM_6DOF_2P8_EN	GPIO_93	CAM_6DOF_1P8_EN
GPIO_12	NC	GPIO_53	CODEC_INT2	GPIO_94	ANX7325_PWR_EN
GPIO_13	CAM_MCLK0	GPIO_54	CODEC_INT1	GPIO_95	NC
GPIO_14	CAM_MCLK1	GPIO_55	APFS_I2C7_SDA	GPIO_96	NC
GPIO_15	CAM_MCLK2	GPIO_56	APFS_I2C7_SCL	GPIO_97	NC
GPIO_16	CAM_MCLK3	GPIO_57	FORCE_USB_BOOT	GPIO_98	NC
GPIO_17	CCI_I2C_SDA0	GPIO_58	LED_L_FAULT	GPIO_99	NC
GPIO_18	CCI_I2C_SCL0	GPIO_59	LED_R_FAULT	GPIO_100	NC
GPIO_19	CCI_I2C_SDA1	GPIO_60	BLSP11_I2C_SDA	GPIO_101	GRFC4
GPIO_20	CCI_I2C_SCL1	GPIO_61	BLSP11_I2C_SCL	GPIO_102	GRFC5
GPIO_21	TOF_START	GPIO_62	MCU_SOC_INT	GPIO_103	GRFC6
GPIO_22	FL_STROBE_TRIG	GPIO_63	ANX7530_INT	GPIO_104	GRFC7
GPIO_23	TOF_EN_ILUM	GPIO_64	CODEC_RESET_N	GPIO_105	NC
GPIO_24	TOF_VSEL_EN	GPIO_65	CODEC_SPI_S_DIN	GPIO_106	NC
GPIO_25	DEP_1V5_EN	GPIO_66	CODEC_SPI_S_DOUT	GPIO_107	NC
GPIO_26	NC	GPIO_67	CODEC_SPI_S_CSN	GPIO_108	NC
GPIO_27	NC	GPIO_68	CODEC_SPI_S_CLK	GPIO_109	GPIO109_WSA_R_EN
GPIO_28	CAM2_RSTN	GPIO_69	NC	GPIO_110	NC
GPIO_29	CAM1_STBYN	GPIO_70	LPASS_SLIMBUS_CLK	GPIO_111	GPIO111_WSA_L_EN
GPIO_30	CAM1_RSTN	GPIO_71	LPASS_SLIMBUS_DATA0	GPIO_112	NC
GPIO_31	LED_L_EN	GPIO_72	LPASS_SLIMBUS_DATA1	GPIO_113	UIM_BATT_ALARM
GPIO_32	LED_R_EN	GPIO_73	NC	GPIO_114	NC
GPIO_33	MCU_RST_N	GPIO_74	NC	GPIO_115	CONFIG_PWR_1P8
GPIO_34	6DOF_ULPM	GPIO_75	HARDWARE_ID_1	GPIO_116	NC
GPIO_35	PCIE_RESET_N	GPIO_76	HARDWARE_ID_2	GPIO_117	NC
GPIO_36	PCIE_CLKREQ_N	GPIO_77	HARDWARE_ID_3	GPIO_118	NC
GPIO_37	PCIE_WAKE_N	GPIO_78	NC	GPIO_119	NC
GPIO_38	CC_DIR (GND)	GPIO_79	NC	GPIO_120	PS_INT_N
GPIO_39	USB_BRIDGE_RESET_N	GPIO_80	NC	GPIO_121	NC
GPIO_40	6DOFR_STROBE	GPIO_81	MCU_SPI1_MOSI	GPIO_122	NC

GPIO_123	NC
GPIO_124	ALS_INT_N
GPIO_125	BRI_UP_KEY
GPIO_126	BRI_DOWN_KEY
GPIO_127	GRFC3_MDM
GPIO_128	NC
GPIO_129	NC
GPIO_130	NC
GPIO_131	L_RDC200_BOOT_FINISH
GPIO_132	L_RDC200_RSTB
GPIO_133	R_RDC200_BOOT_FINISH
GPIO_134	R_RDC200_RSTB
GPIO_135	NC
GPIO_136	NC

GPIO_137	NC
GPIO_138	NC
GPIO_139	NC
GPIO_140	NC
GPIO_141	NC
GPIO_142	NC
GPIO_143	ANX7530_1P0_EN
GPIO_144	NC
GPIO_145	NC
GPIO_146	PCIE_FWR_EN
GPIO_147	NC
GPIO_148	6DOFL_SHUTDOWN_L
GPIO_149	6DOFR_SHUTDOWN_R

PMI8998 GPIO Configuration for Irongate HMD

GPIO_1	NC	GPIO_6	NC	GPIO_11	NC
GPIO_2	NC	GPIO_7	NC	GPIO_12	DIV_CLK3
GPIO_3	NC	GPIO_8	NC	GPIO_13	NC
GPIO_4	NC	GPIO_9	GND	GPIO_14	NC
GPIO_5	NC	GPIO_10	NC		

PM8998 GPIO Configuration for Irongate HMD

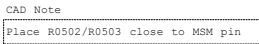
GPIO_1	UIM_BATT_ALARM	GPIO_12	NC	GPIO_23	NC
GPIO_2	NC	GPIO_13	NC	GPIO_24	Option
GPIO_3	NC	GPIO_14	DIV_CLK2	GPIO_25	Option
GPIO_4	SSC_PWR_EN	GPIO_15	NC	GPIO_26	PM_SLB
GPIO_5	NC	GPIO_16	DIV_CLK3		
GPIO_6	VOL_UP_N	GPIO_17	NC		
GPIO_7	NC	GPIO_18	NC		
GPIO_8	NC	GPIO_19	NC		
GPIO_9	NC	GPIO_20	CAM_REAR_ON		
GPIO_10	NC	GPIO_21	NC		
GPIO_11	NC	GPIO_22	NC		

WCD9341 GPIO Configuration for Irongate HMD

GPIO_0	GND	GPIO_2	WSA_R_EN	GPIO_4	GND
GPIO_1	WSA_L_EN	GPIO_3	GND		

GPIO TABLE





CAD Note

=====

90ohm Diff Imp routing for USB

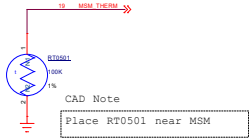
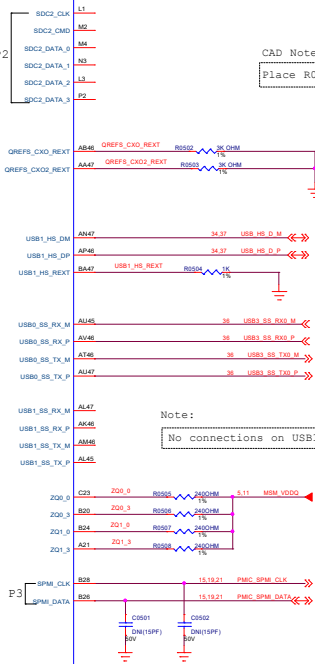
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CAD Note

Place R0504 close to MSM pin

Note:

No connections on USB1 PHY

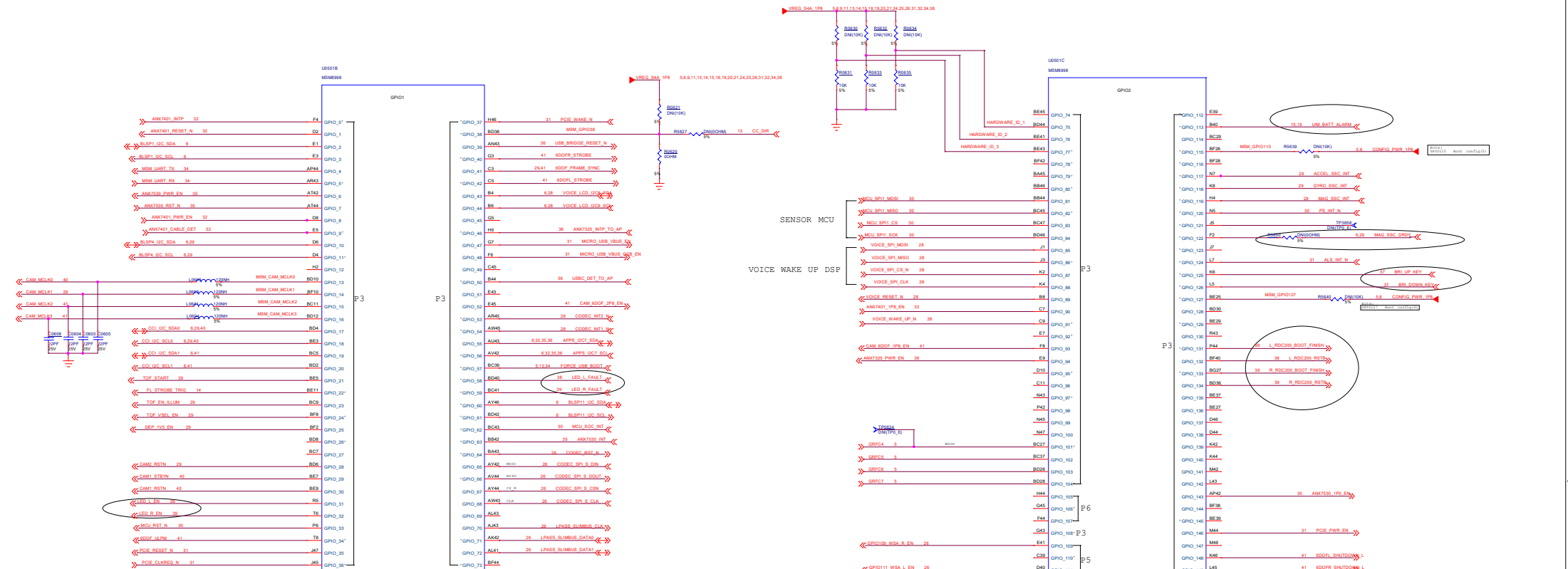


GPIOs	BOOT_CONFIG
GPIO_101	BOOT 0 - Enable 1 - Disable
GPIO_102	BOOT_CONFIG[1]
GPIO_103	BOOT_CONFIG[2]
GPIO_104	BOOT_CONFIG[3]
GPIO_114	BOOT_CONFIG[4]

ROOT_CONFID[411]	ROOT_CONFID
00000 (Y/N) 000000	000 -> RD SEC2 -> RD/RA/PP URM 00 URM3.1
00001	RD SEC2 -> WFF
00010	SEC2
00011	RD/RA/PP URM 00 URM3.1

MSM8998 CONTROL



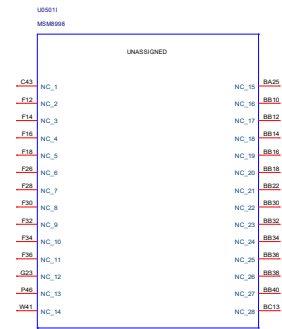
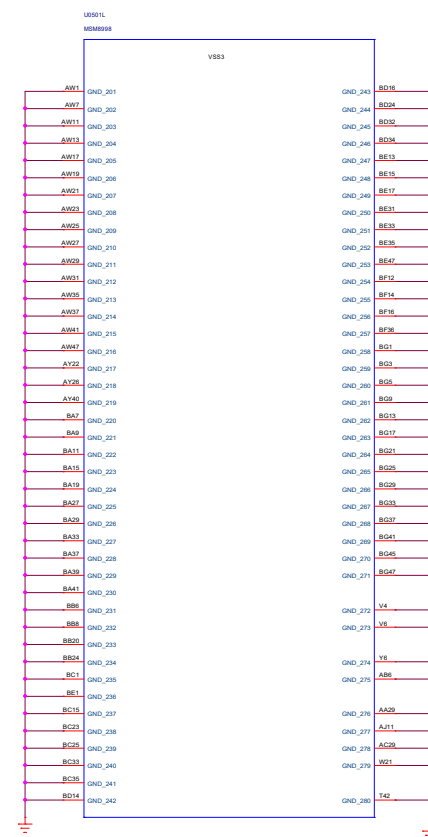
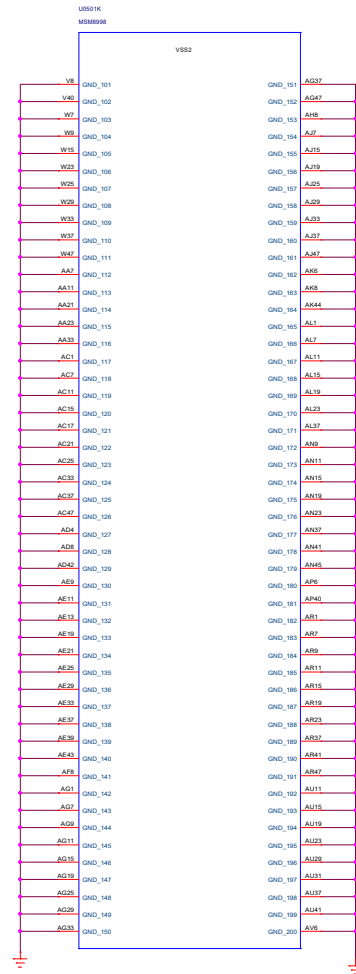
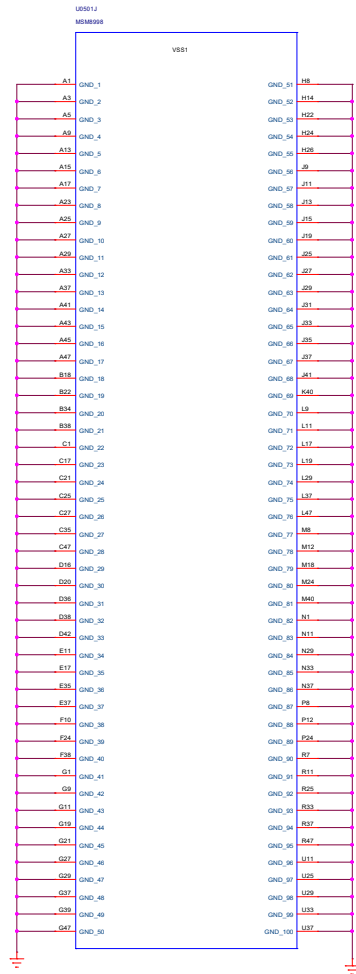


Note:
Ensure SW sets these GPIOs (Sensor, CTP and Camera I2C bus) to inout pull down when the peripherals are powered off to eliminate leakage.

MSM8998 GPIO



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MSM8998 GND

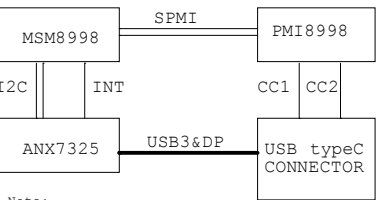


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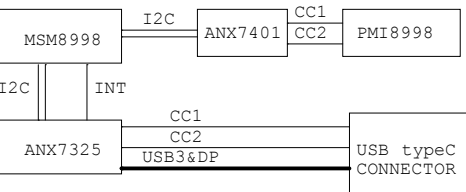
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graph TD
    MSM8998[MSM8998] --- SPI[SPI] --- PMI8998[PMI8998]
    MSM8998 --- I2C[I2C] --- ANX7325[ANX7325]
    MSM8998 --- INT[INT] --- ANX7325
    MSM8998 --- CC1[CC1] --- USB[USB typeC CONNECTOR]
    MSM8998 --- CC2[CC2] --- USB
    MSM8998 --- USB3DP[USB3&DP] --- USB
  
```

USB TYPE-C BACKUP SOLUTION 1

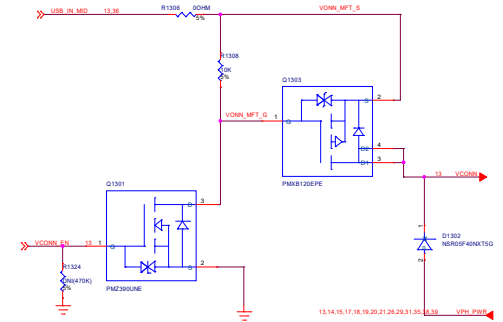
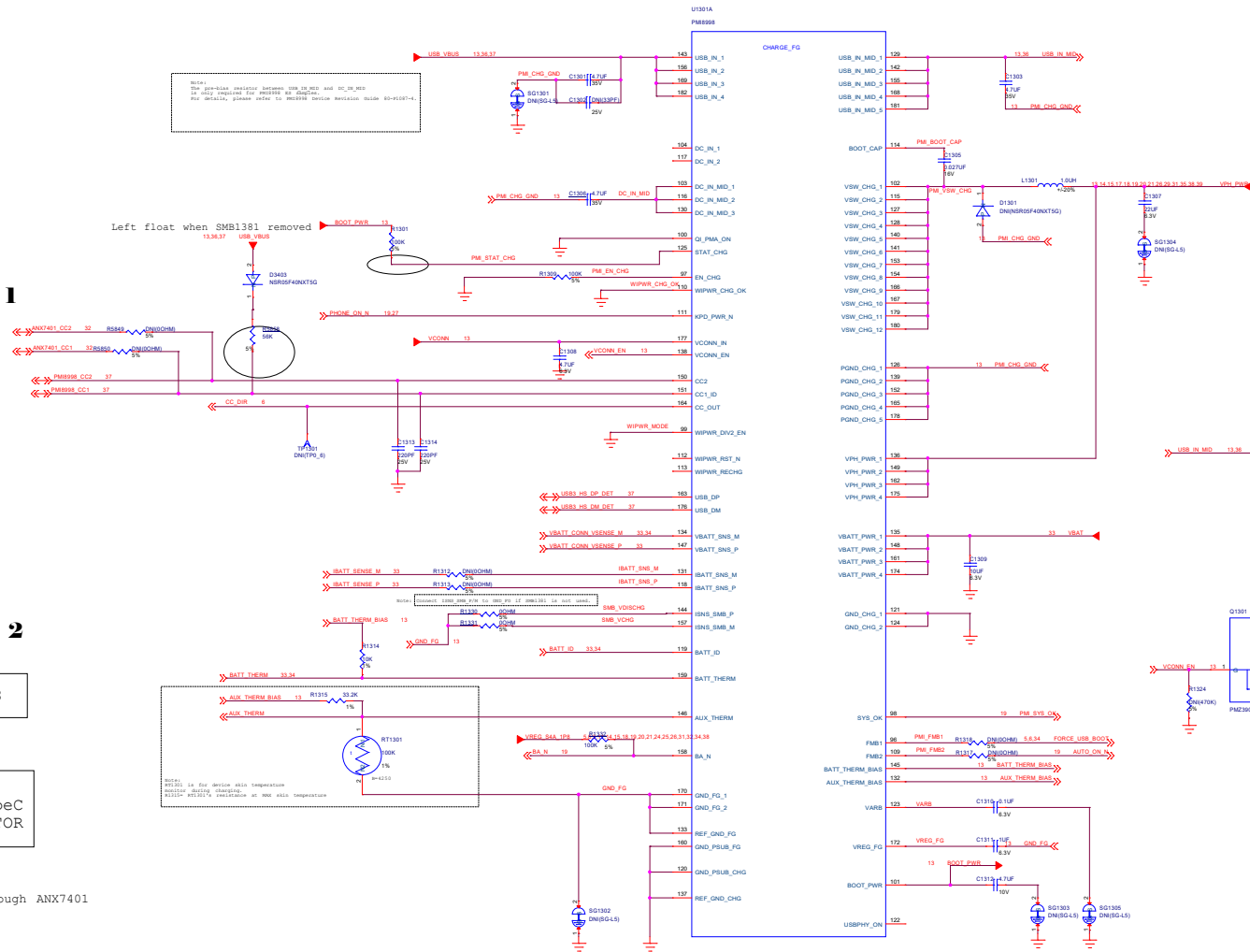


USB TYPE-C BACKUP SOLUTION 2



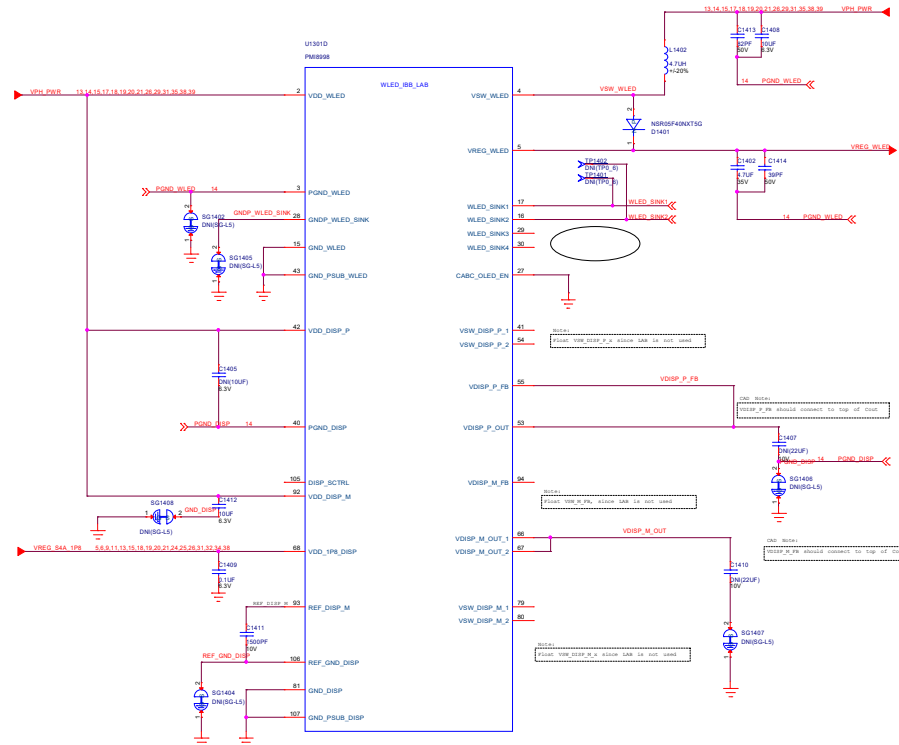
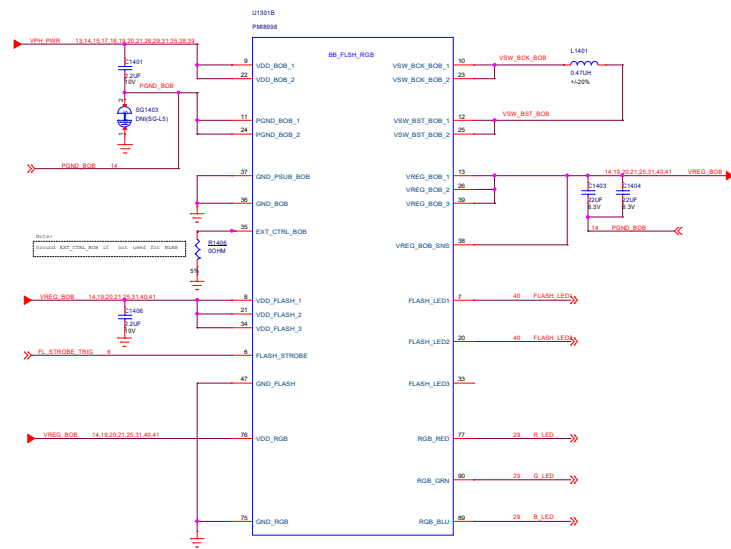
Note:

1. PMI8998 working under TypeC mode
2. Float PMI8998 GPIO4
3. ANX7325 forward the PD information to PMI8998 through ANX7401



PMI8998_Charge_FG

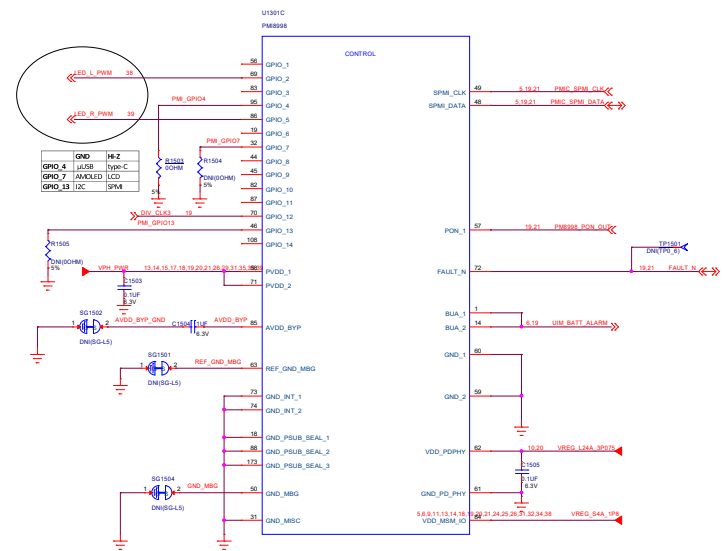




PMI8998_Buck_Boost_Flash



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2	Updated to Rev 1.1	PMI8998_Buck_Boost_Flash	1.1



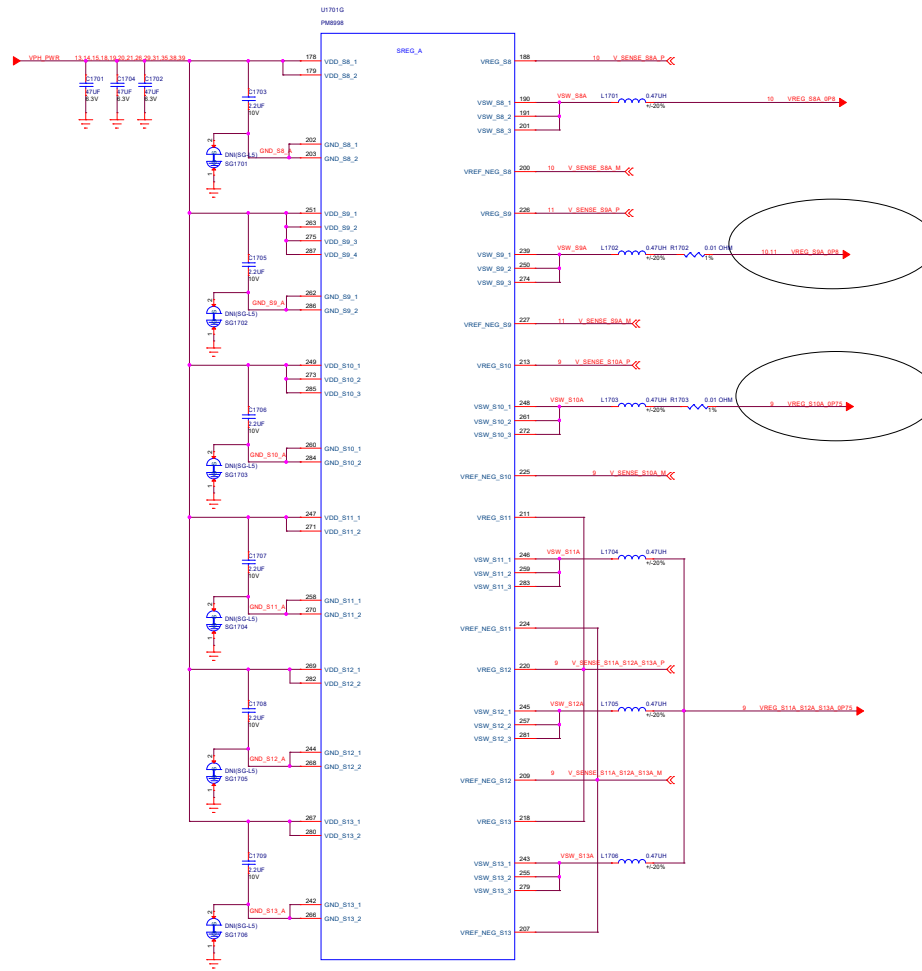
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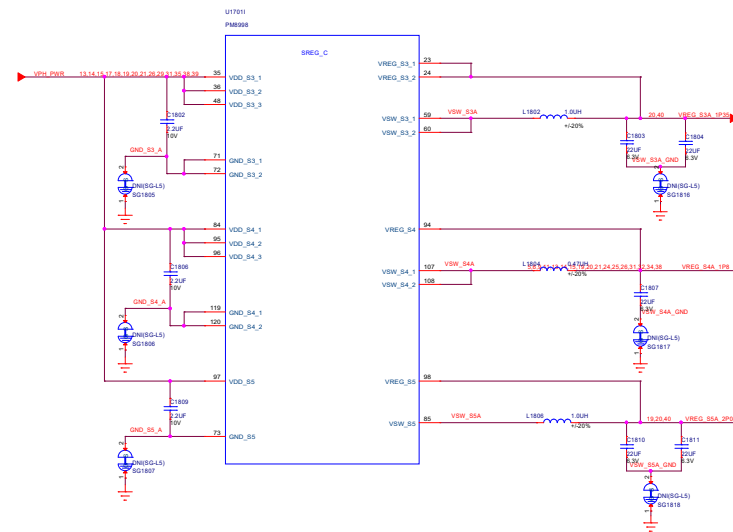
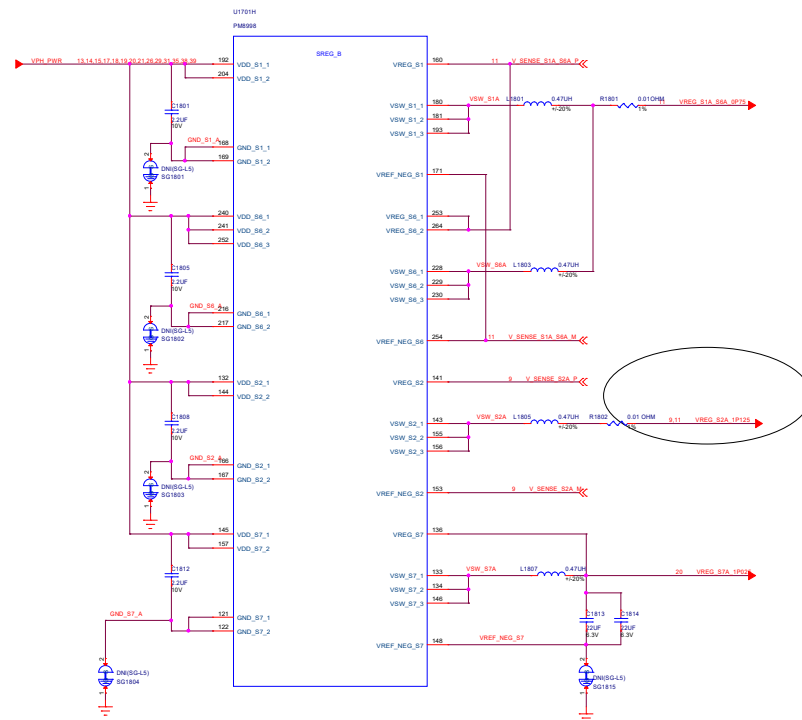
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PM8998 Bucks (1 of 2)



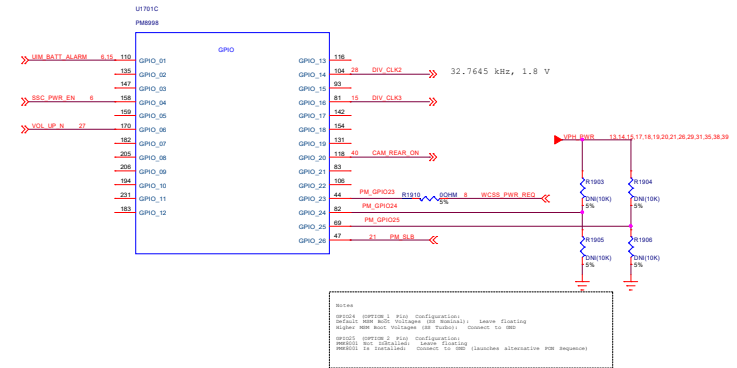
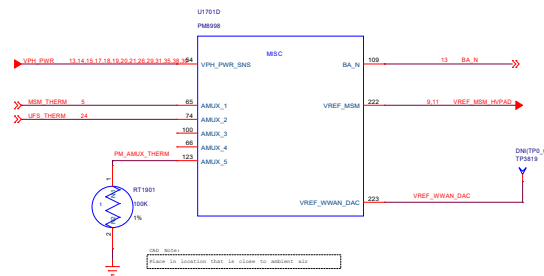
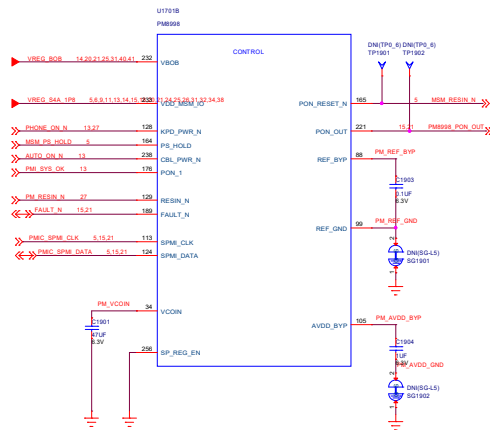
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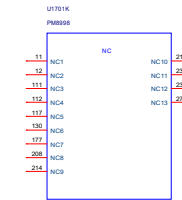
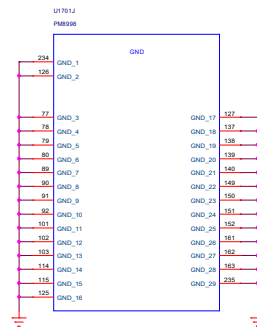
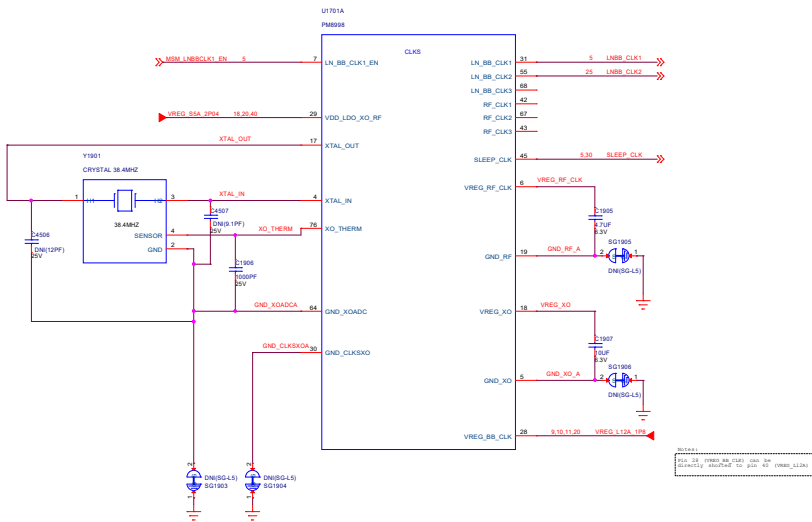
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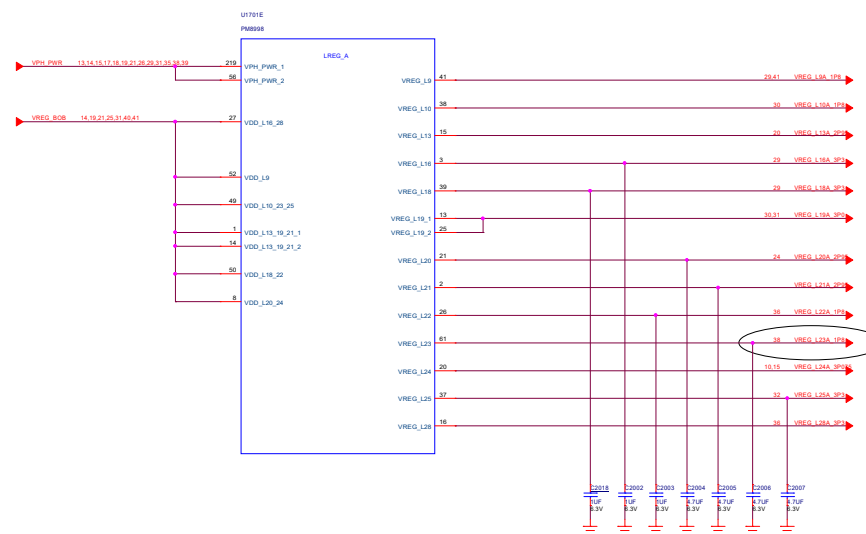
Memory suggested	PM8998	PM8998	PM8998	Notes
U701A	NC	GPIO 10	GPIO 10	PM8998 is NOT in the Boot sequence
U701A	Connect to PM8998	GPIO 10	GPIO 10	PM8998 is NOT in the Boot sequence
U701A	Connect to PM8998	GPIO 10	GPIO 10	PM8998 is NOT in the Boot sequence



PM8998 Control



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Rev	«Doc»	«Rev»	«Rev»



2035 VREG_L12A_1P8 20 VREG_L13A_2P35

C2016 C2017

1UF 1UF

0.3V 0.3V

Add C2016, C2017 to meet Pseudo-capless LDO requirement in QM09998 08X3 PCB

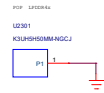
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PM8939B	PON trigger
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PM8939B	PON_CU1T
PM8939B	VREG_05
PM8939B	VREG_XO
PM8939B	VREG_B0B8
PM8939B	VREG_3V3/REG_31/VREG_SE
PM8939B	VREG_37
PM8939B	VREG_111
PM8939B	VREG_144
PM8939B	VREG_M0M
PM8939B	VREG_17
PM8939B	VREG_15
PM8939B	VREG_117
PM8939B	VREG_125
PM8939B	REF_CLK
PM8939B	BT_C1C2
PM8939B	EXP104
PM8939B	VREG_112
PM8939B	N_BB_C1C3
PM8939B	VREG_52
PM8939B	EXP26A
PM8939B	VREG_52C
PM8939B	VREG_12
PM8939B	VREG_11
PM8939B	VREG_124
PM8939B	VREG_120
PM8939B	VREG_126
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PM8939B	VREG_51D
PM8939B	PON_RESET_N

flex

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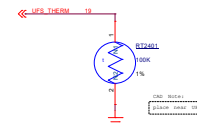
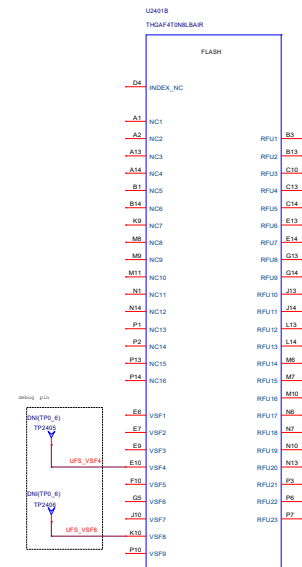
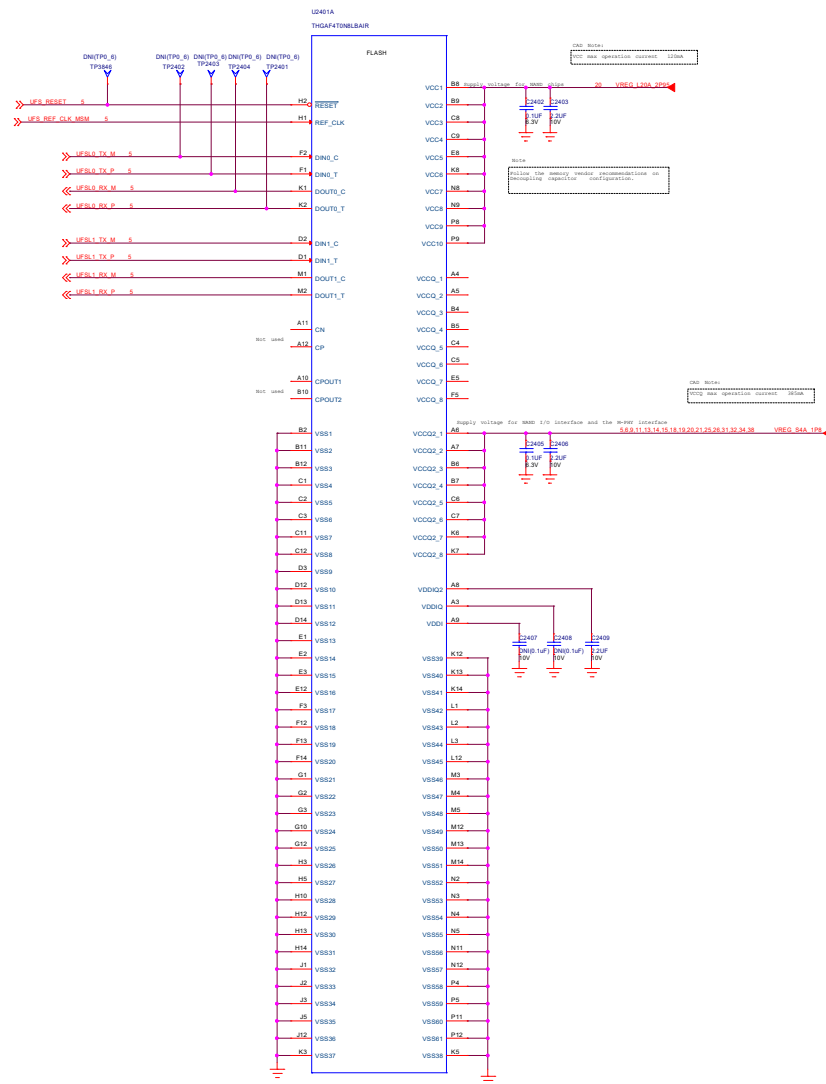
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LPDDR4x



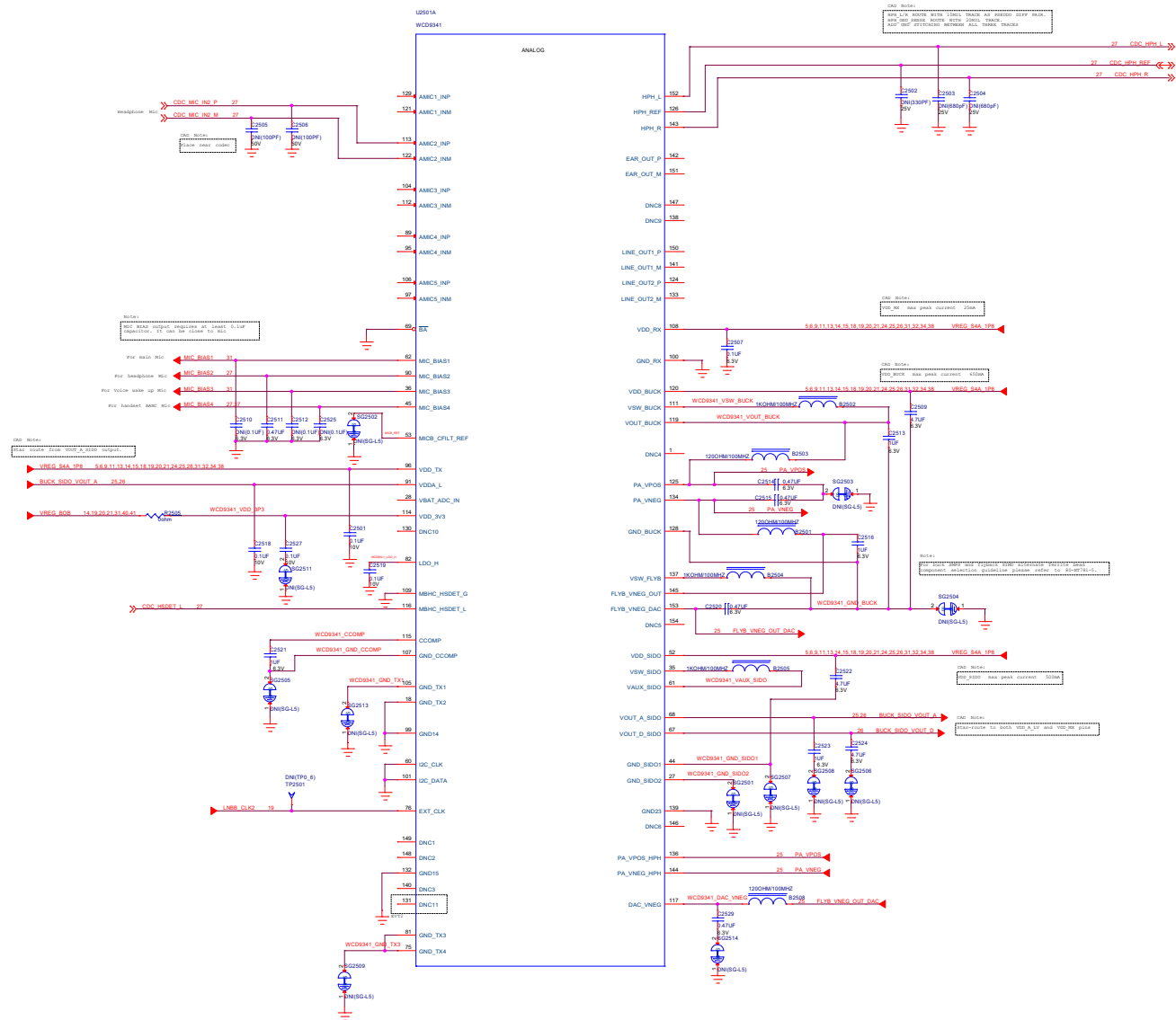
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MEMORY UFS



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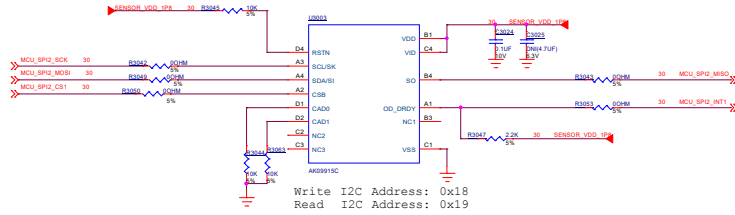
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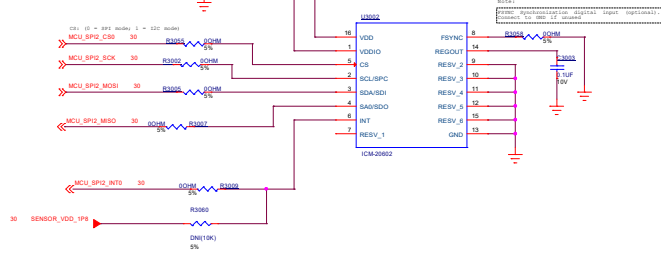
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Sensors

Magnetic Sensor

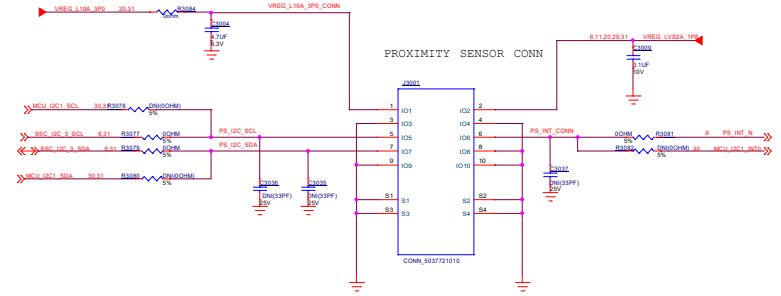


Accelerator and Gyro Sensor



BOOT1	BOOT0	BOOT MODE
X	0	Main Flash memory
0	1	System memory
1	1	Embedded SRAM

ALS sensor on camera board

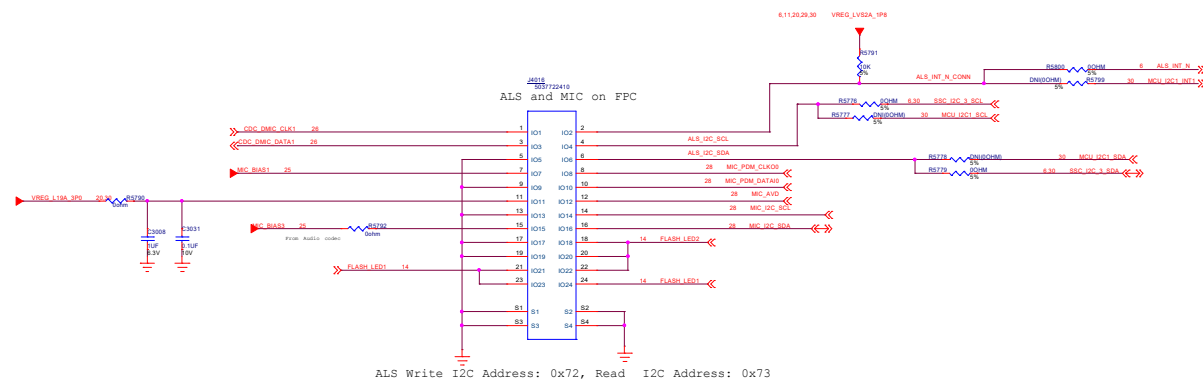
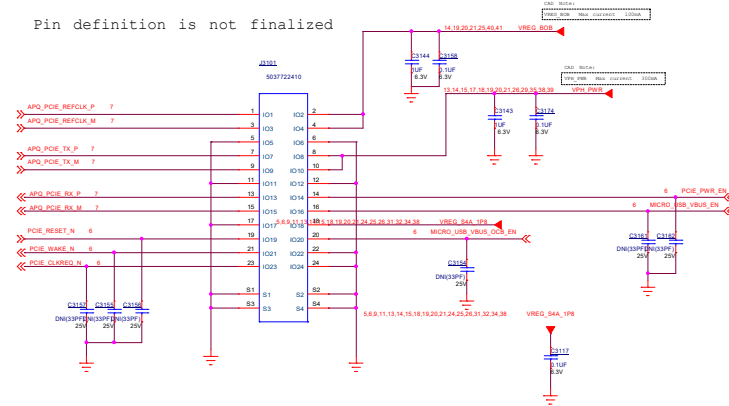


SENSORS&MCU



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Pin definition is not finalized



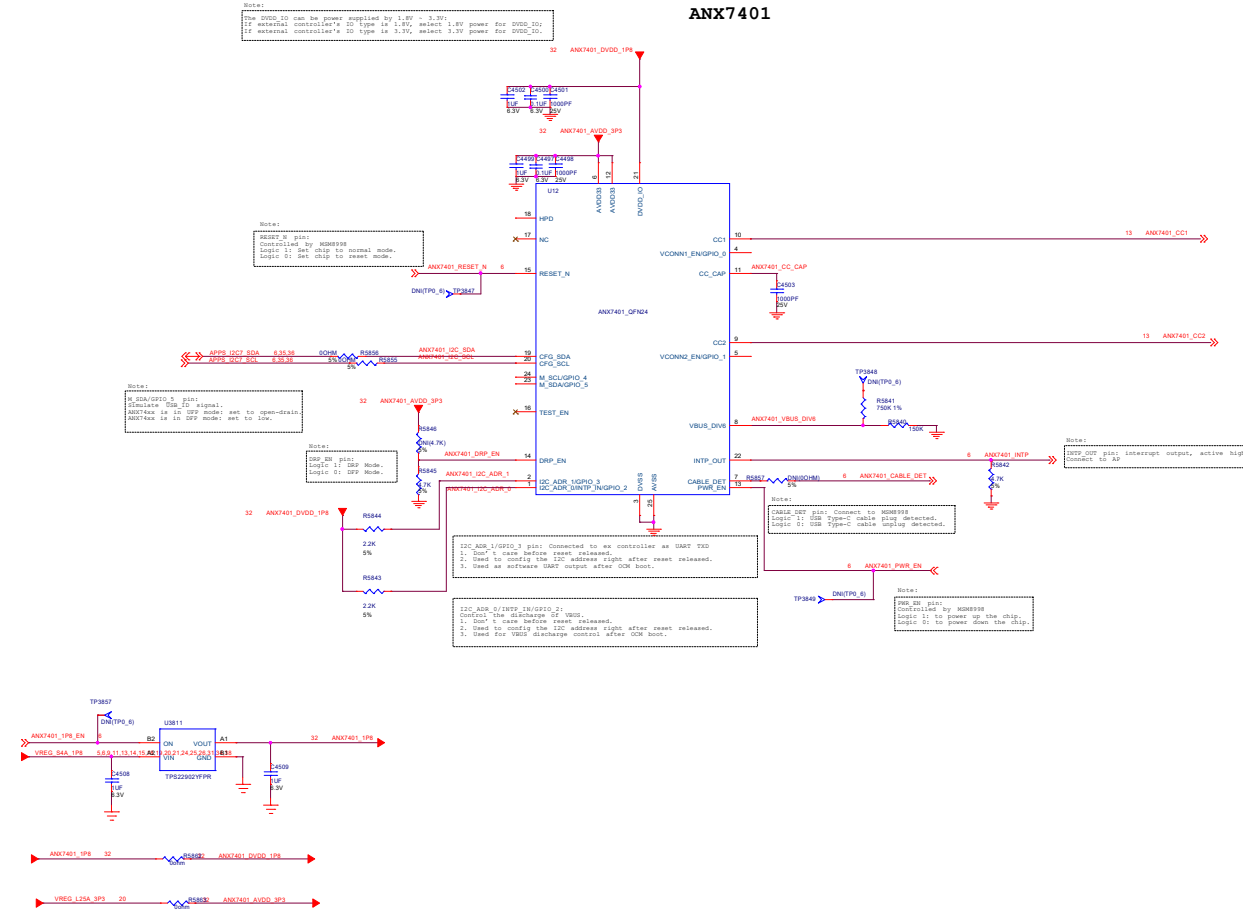
Need to add another Smart Dmic on ALS_FPC

PCIE to USB Bridge Conn



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ANX7401



ANX7401



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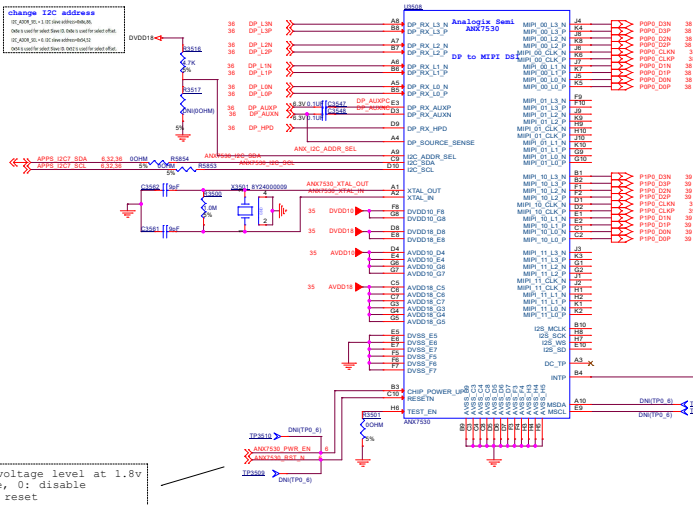


Test point/GND/Shields



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ANX7530



Note

```
From MSM8998, input voltage level at 1.8v
Pwr_Enable: 1: enable, 0: disable
Rst_N: 1: Normal, 0: reset
```

CAD Note

Decoupling capacitors close to ANX7530 PIN

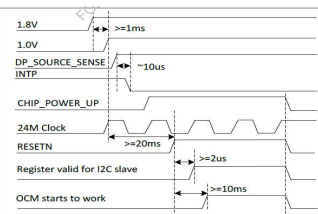
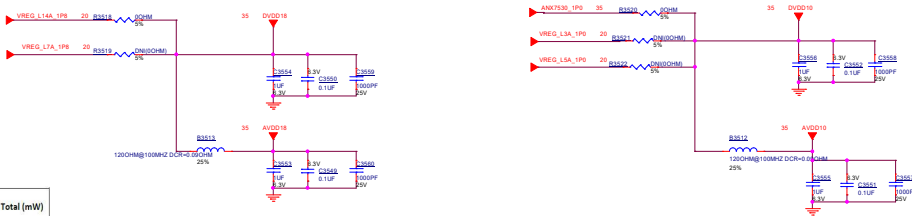


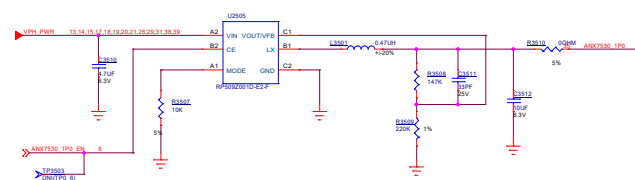
Table 6-6 Power Consumption in Active Mode

Input Video Clock	Current (mA)				Total (mW)
	AVDD10	AVDD18	DVDD18	DVDD10	
390MHz	178.00	77.00	1.00	88.00	406.40
524MHz	175.00	78.00	1.00	94.00	411.20
619MHz	175.00	78.00	1.00	101.00	418.20



CAD Note

DVDD10 & AVDD10	276mA
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DP to MIPI Bridge ANX7530



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Symbol	Parameter	Min	Typ	Max	Units
SVDD_IO	Digital supply voltage	1.7	3.3	3.83	V
AVDD11	Analog supply voltage	3.14	3.3	3.46	V

[illegible]

I2C_ADR_1	I2C_ADR_0	I2C_Addr
Logic 0	Logic 0	0x30
Logic 2	Logic 1	0x72
Logic 1	Logic 0	0x70
Logic 1	Logic 1	0x80

I2C_ADR_1 and I2C_ADR_0 pins:

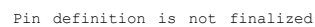
1. The 'I2C address' is determined approximately 500ns after RESET_N turns from 0 to 1, these two pins' input should be kept at a stable value during this period.
2. There are internal pull-down resistors on I2C_ADR_0 and I2C_ADR_1 pins.
3. If external pull-up resistor is not populated, the I2C_ADR_0 or 'I2C_ADR_1 is logic 0.
4. If external pull-up is populated, the I2C_ADR_0 or I2C_ADR_1 is logic 1.

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CAD Note:
Ensure R3710 and R3713 isolation resistor placed close to the Sub board connector.

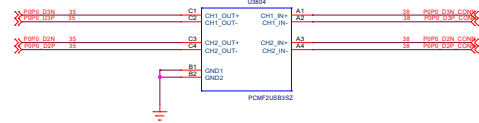
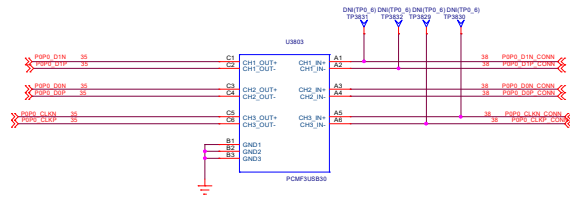
Note:
To reduce the capacitive loading of DP/DM lines if required
change R3711 and R3714 to ferrite beads



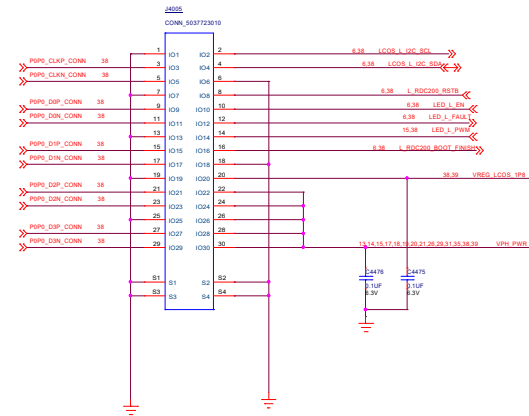
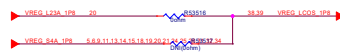
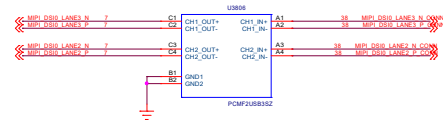
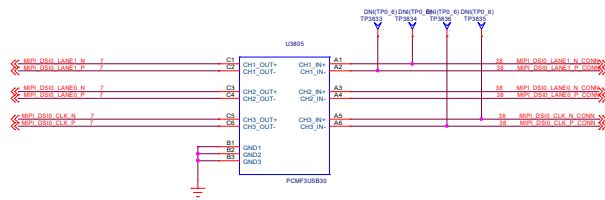
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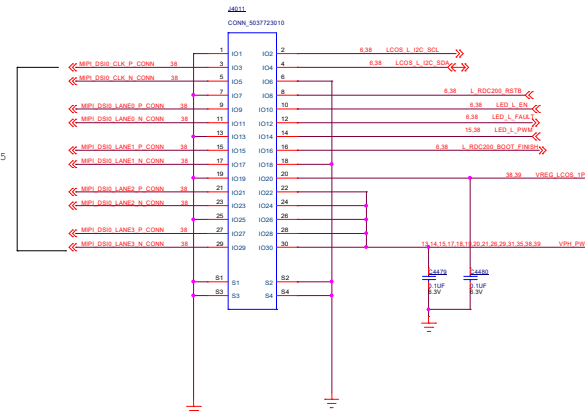
CAD Note:
Place Test points on the trace, No stub



CAD Note:
Place Test points on the trace, No stub



MIPI from HMD SD835

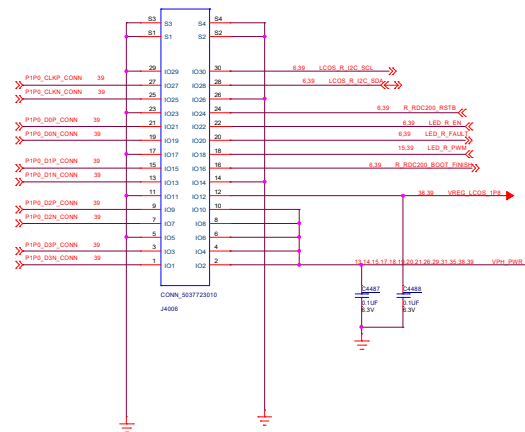
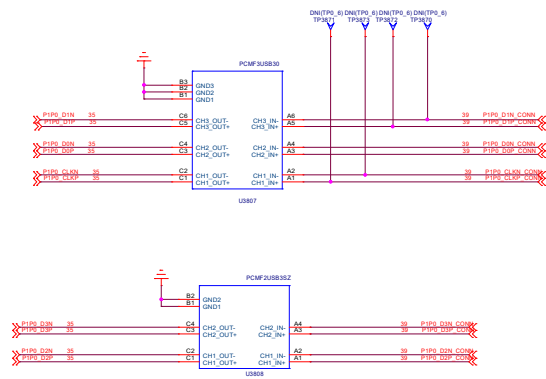


Left DLP board connector

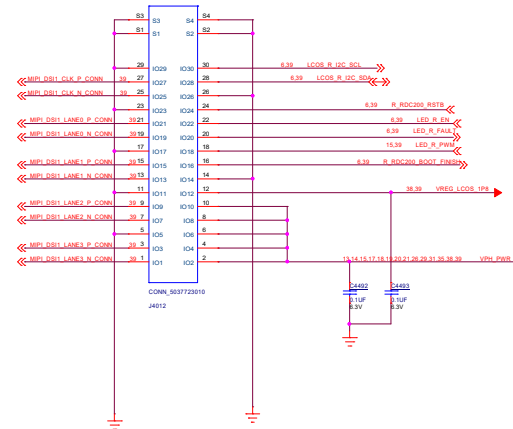
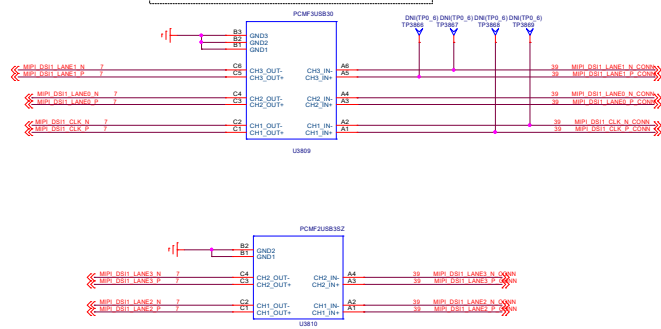



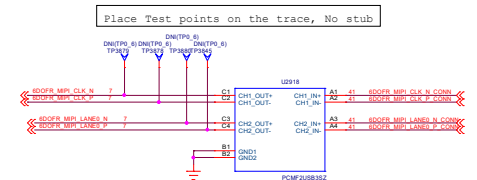
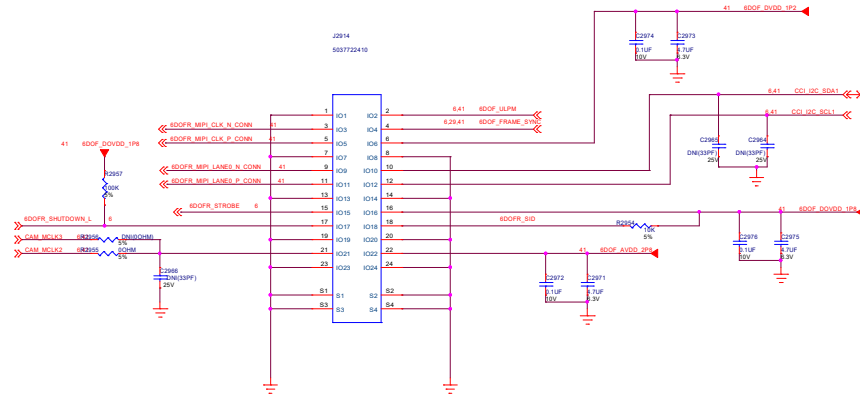
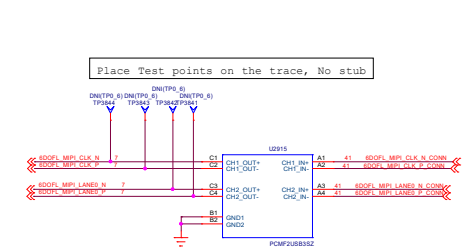
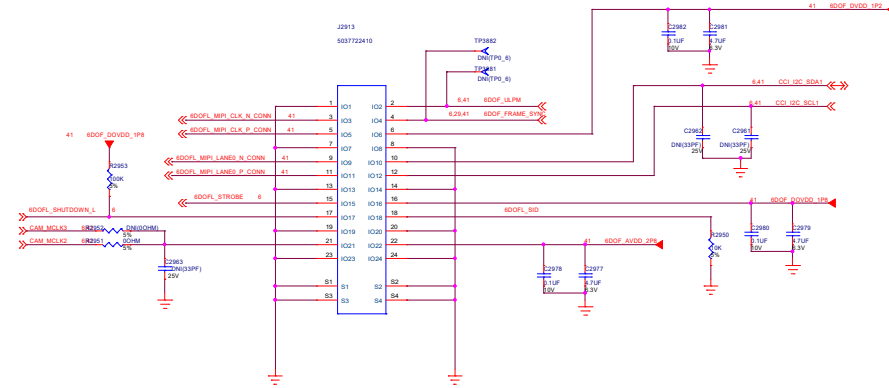
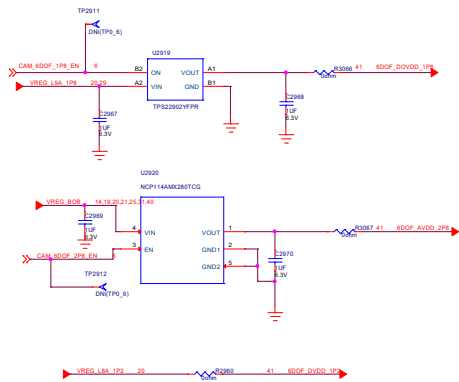
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CAD Note:
Place Test points on the trace, No stub



CAD Note:
Place Test points on the trace, No stub

RIGHT DLP board connector 



Change list

EVT1 change list

[10/16] Page13: Change R5858 from10K to 56K
[10/16] Page36: Fix the library issue on Q3602
[10/16] Page30: Add resistors R3091~R3094 for debug
[10/16] Page38/Page39: Change these two pages for new LCOS display
[10/16] Page6: Change the net name of GPIO31/32/58/59/131/132/133/134 for new LCOS display
[10/16] Page6: Change the net name of I2C bus for new LCOS display
[10/17] Page20: Change the voltage of LDO23 from 3.3V to 1.8V for LCOS display
[10/19] Page29/Page40/Page41: Change these three pages
[10/19] Page28: Change the pull-up power of Smart MIC I2C from VREG_S4A_1P8 to VREG_L6A_1P8
[10/19] Page31: Move ALS/DMIC/Smart mic to FPC
[10/19] Page6: Use GPIO125/126 as Brihtness_up/down button
[10/19] Page6: Use GPIO122 as the backup of MAG_SSC_DRDY
[10/20] Page15: Change the netname of GPIO2/5 of PMI8998
[10/24] Page9/Page11/Page17/Page18/Page20/Page21: Remove SG0901/SG0911/SG1101/SG1102/SG1713/SG1714/SG1715/SG1716/SG1813/SG1814/SG2011/SG2012/SG2113/SG2114
[10/24] Page34: Remove J3403
[10/24] Page29: Change Resistor R2932 from 374K to 210K; Change R2933 from 150K to 47K
[10/24] Page29: Change netname from VREG_VCEL_2P1 to VREG_VCEL_3P3
[11/1] Page14: Remove the connector J1401;Add two test points TP1401,TP1402
[11/1] Page33: Change battery connector
[11/1] Page37: Add brightness control GPIO on J2903, add Resistor R3780,R3781
[11/1] Page27: Move Power on key from USB rigid flex to Audio board
[11/9] Page27: Add net"MIC_PDM_DATA11/CLK01"for another smart DMIC
[12/6] Page33: DNI R3306, R3316
[12/6] Page13: ADD Diode D3403 on CC1 pull up
[01/02] Page29: DEL C4469; Add voice wake second MIC; change CONN pin define
[01/02] Page31: J4016 change to 24pin: 5037722410; remove voice wake second MIC; add flash LED
[01/02] Page40: DEL U3201: Flash LED
[01/02] Page33: change battery conn footprint to SD5040500691
[01/15] Page29: change Depth 1V5 from VREG_L15 to DCDC: R2937 to 330K, R2938 to 220K; change J2904 Pin define
[01/15] Page33: Remove J3302, add solder pad
[01/18] Page39: Change pin define of LCOS-R
[01/19] Page31: Change pin define of ALS conn、
[01/19] Page39: Change pin define of J4012
[01/24] Page39: Vertical mirror U3810, U3809
[01/24] Page1-4: Change content, block diagram and GPIO map

Revision History



Rev		<Title>	
Rev	Document Number		
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Date		Revised	by