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IronGate-EPU

flex

Document Number

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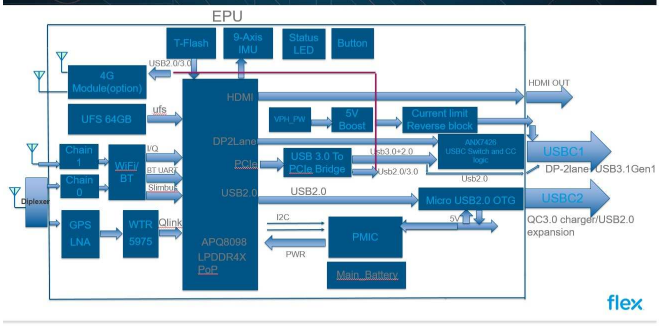
Revision History

REV	DESCRIPTION
A	

Board Change History

SCHEMATIC MCN	HW VERSION	REVISION	DESCRIPTION OF CHANGE

Hardware Architecture Solution – EPU



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C	Mark Magee		V4
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MSM8998 GPIO Configuration For IronGate EPU

GPIO_0	GPIO0_LTE_RF_EN	GPIO_41	NC	GPIO_82	MCU_SPI1_MISO
GPIO_1	GPIO1_LTE_DPR	GPIO_42	NC	GPIO_83	MCU_SPI1_NSS
GPIO_2	NC	GPIO_43	NFC_I2C6_SDA	GPIO_84	MCU_SPI1_SCK
GPIO_3	NC	GPIO_44	NFC_I2C6_SCL	GPIO_85	NC
GPIO_4	UART_MSM_TX	GPIO_45	BT_HCI_UART_RX	GPIO_86	NC
GPIO_5	UART_MSM_RX	GPIO_46	BT_HCI_UART_TX	GPIO_87	NC
GPIO_6	GPIO6_ANX7426_CFG_SDA	GPIO_47	BT_HCI_UART_RFR_N	GPIO_88	NC
GPIO_7	GPIO7_ANX7426_CFG_SCL	GPIO_48	BT_HCI_UART_CTS_N	GPIO_89	SY7076_MODE_Control
GPIO_8	GPIO8_ANX7426_PWR_EN	GPIO_49	NC	GPIO_90	NC
GPIO_9	GPIO9_LTEMODULE_PWR_ON	GPIO_50	NC	GPIO_91	NC
GPIO_10	GPIO10_LTEMODULE_RESET_IN	GPIO_51	NC	GPIO_92	NC
GPIO_11	NC	GPIO_52	NC	GPIO_93	NC
GPIO_12	NC	GPIO_53	NC	GPIO_94	GPIO94_MCU_RESET
GPIO_13	NC	GPIO_54	NC	GPIO_95	SD_CARD_DET_N
GPIO_14	NC	GPIO_55	APPS_I2C7_SDA	GPIO_96	NC
GPIO_15	NC	GPIO_56	APPS_I2C7_SCL	GPIO_97	NC
GPIO_16	NC	GPIO_57	FORCE_USB_BOOT	GPIO_98	NC
GPIO_17	NC	GPIO_58	NC	GPIO_99	NC
GPIO_18	NC	GPIO_59	NC	GPIO_100	NC
GPIO_19	NC	GPIO_60	NC	GPIO_101	GRFC4
GPIO_20	NC	GPIO_61	NC	GPIO_102	GRFC5
GPIO_21	NC	GPIO_62	NC	GPIO_103	GRFC6
GPIO_22	FL_STROBE_TRIG	GPIO_63	NC	GPIO_104	GRFC7
GPIO_23	NC	GPIO_64	NC	GPIO_105	NC
GPIO_24	NC	GPIO_65	NC	GPIO_106	NC
GPIO_25	NC	GPIO_66	NC	GPIO_107	NC
GPIO_26	NC	GPIO_67	NC	GPIO_108	NC
GPIO_27	NC	GPIO_68	NC	GPIO_109	NC
GPIO_28	NC	GPIO_69	NC	GPIO_110	NC
GPIO_29	NC	GPIO_70	NC	GPIO_111	NC
GPIO_30	NC	GPIO_71	NC	GPIO_112	UIM1_DET
GPIO_31	GPIO31_HDMI_CEC	GPIO_72	NC	GPIO_113	UIM_BATT_ALARM
GPIO_32	GPIO32_HDMI_DDC_CLK	GPIO_73	BT_FM_SLIMBUS_DATA	GPIO_114	NC
GPIO_33	GPIO33_HDMI_DDC_DATA	GPIO_74	BT_FM_SLIMBUS_CLK	GPIO_115	CONFIG_PWR_1P8
GPIO_34	GPIO34_HDMI_HPLUG_DET	GPIO_75	HARDWARE_ID_1	GPIO_116	ANX7426_HPD
GPIO_35	PCIE_RESET_N	GPIO_76	HARDWARE_ID_2	GPIO_117	ACCEL_INT
GPIO_36	PCIE_CLKREQ_N	GPIO_77	HARDWARE_ID_3	GPIO_118	NC
GPIO_37	PCIE_WAKE_N	GPIO_78	NC	GPIO_119	NC
GPIO_38	CC_DIR	GPIO_79	NC	GPIO_120	NC
GPIO_39	NC	GPIO_80	SY7076_EN	GPIO_121	MCU_SOC_INT
GPIO_40	NC	GPIO_81	MCU_SPI1_MOSI	GPIO_122	NC

GPIO_123	ANX_RESET_N_FROM_AP
GPIO_124	LTE_WAKEUP_CPU
GPIO_125	ANX7426_INTP_TO_AP
GPIO_126	ANX_CABLE_DET_TO_AP
GPIO_127	GRFC3_MDM
GPIO_128	NC
GPIO_129	NC
GPIO_130	QLINK_REQUEST
GPIO_131	QLINK_ENABLE
GPIO_132	NC
GPIO_133	GPIO133_HDMI_EN
GPIO_134	WMSS_RESET_N
GPIO_135	NC
GPIO_136	NC

GPIO_137	NC
GPIO_138	NC
GPIO_139	NC
GPIO_140	NC
GPIO_141	NC
GPIO_142	NC
GPIO_143	GNSS_EN
GPIO_144	WCI2_LTE_COEX_RXD
GPIO_145	WCI2_LTE_COEX_TXD
GPIO_146	PCIE_PWR_EN
GPIO_147	NC
GPIO_148	RFFE1_DATA
GPIO_149	RFFE1_CLK

PMI8998 GPIO Configuration For IronGate EPU

GPIO_1	NC	GPIO_6	NC	GPIO_11	NC
GPIO_2	NC	GPIO_7	NC	GPIO_12	DIV_CLK3
GPIO_3	NC	GPIO_8	NC	GPIO_13	NC
GPIO_4	NC	GPIO_9	NC	GPIO_14	NC
GPIO_5	NC	GPIO_10	NC		

PM8998 GPIO Configuration For IronGate EPU

GPIO_1	UIM_BATT_ALARM	GPIO_12	NC	GPIO_23	WCSS_PWR_REQ
GPIO_2	NC	GPIO_13	NC	GPIO_24	Option
GPIO_3	WLAN_SW_CTRL	GPIO_14	NC	GPIO_25	Option
GPIO_4	SSC_PWR_EN	GPIO_15	NC	GPIO_26	PM_SLB
GPIO_5	NC	GPIO_16	DIV_CLK3		
GPIO_6	VOL_UP_N	GPIO_17	SMB_SYSOK		
GPIO_7	NC	GPIO_18	SMB_STAT		
GPIO_8	NC	GPIO_19	NC		
GPIO_9	NC	GPIO_20	NC		
GPIO_10	NC	GPIO_21	NC		
GPIO_11	NC	GPIO_22	NC		

WCD9341 GPIO Configuration For IronGate EPU

GPIO_0		GPIO_2		GPIO_4	
GPIO_1		GPIO_3			

GPIO TABLE

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flex

Document Number: GPIO Map

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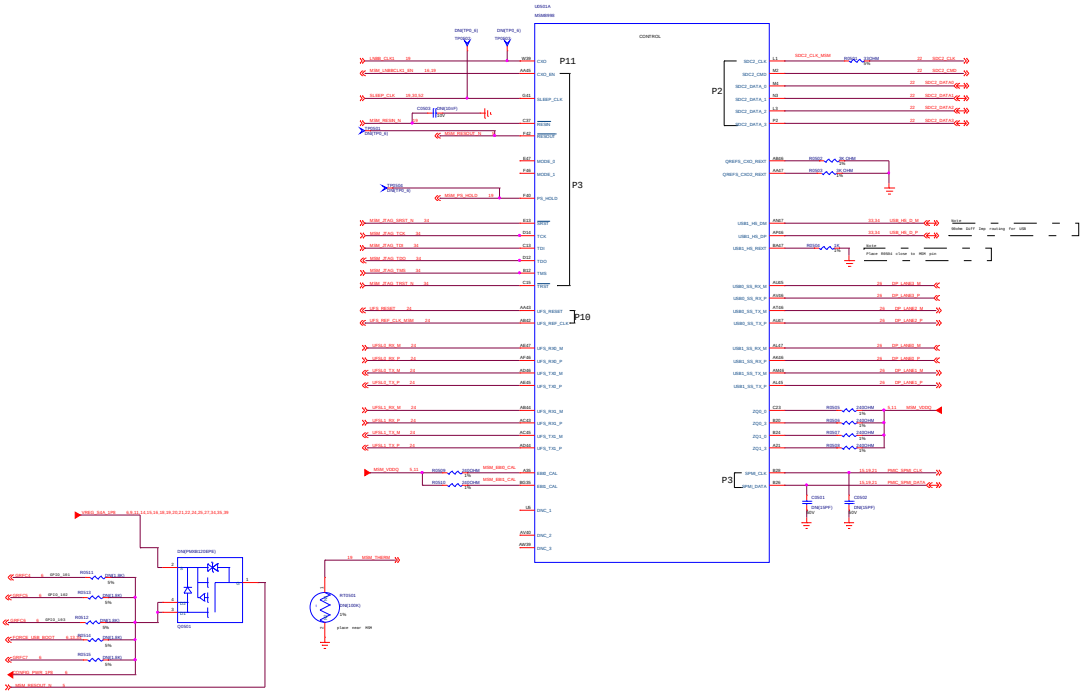
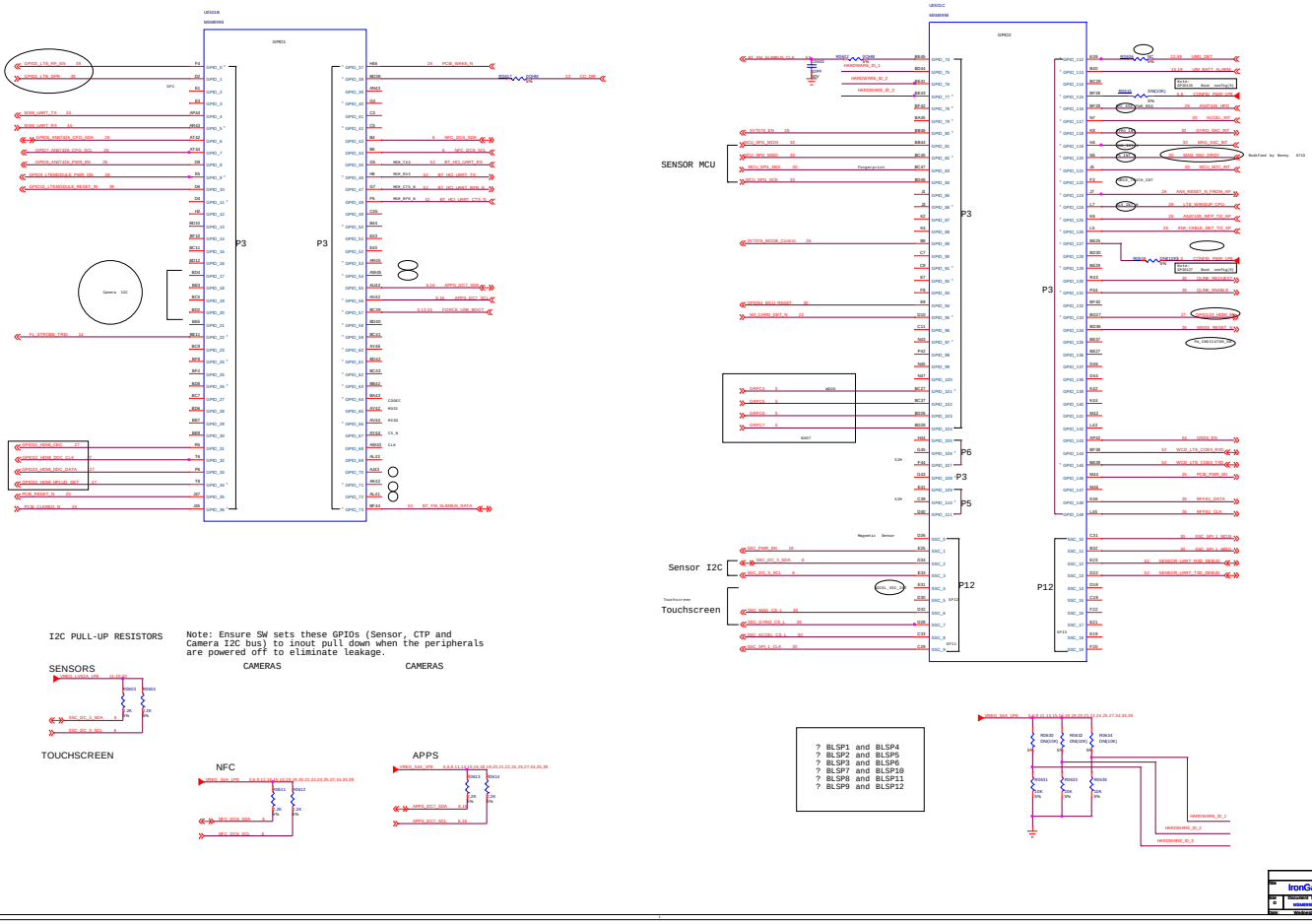


GPIOn	BOOT_CONFIG
GPIO_161	WCD9341 0 = Enable 1 = Disable
GPIO_162	BOOT_CONFIG[1]
GPIO_163	BOOT_CONFIG[2]
GPIO_164	BOOT_CONFIG[3]
GPIO_114	BOOT_CONFIG[4]

BOOT_CONFIG[4:1]	BOOT_CONFIG
0b0000(This design)	UFS -> SD SDC2 -> SD/MLFPE USB on USB3.1
0b0001	SD SDC2 -> UFS
0b0010	SDC2
0b0011	SD/MLFPE USB on USB3.1



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Size	Document Number		Rev
C	MSM8996_GPIO_SOC		V4
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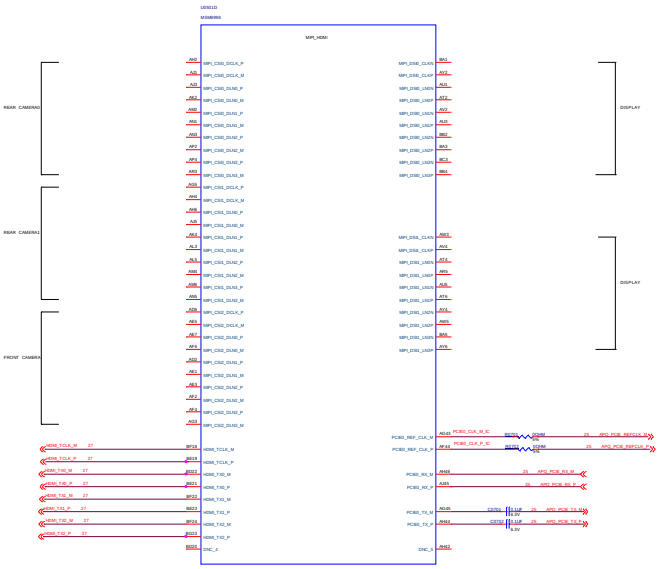

Note: If best EMI practices are followed for MIPI CSI/DSI signals, there is no need for common mode choke filters. You may choose to have placeholders for common mode depending upon your design constraints.
Extreme care must be taken that no stubs are created by doing so.

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Size: D	Document Number: M0A0B1B6_MIPI_CSI_DSI_HDMI	Rev: V4
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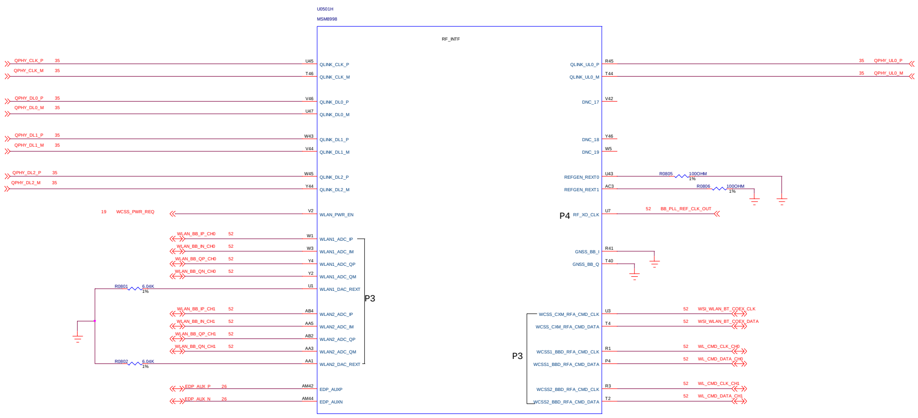

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Size D	Document Number MSM8998_RF_Interface	Rev V1
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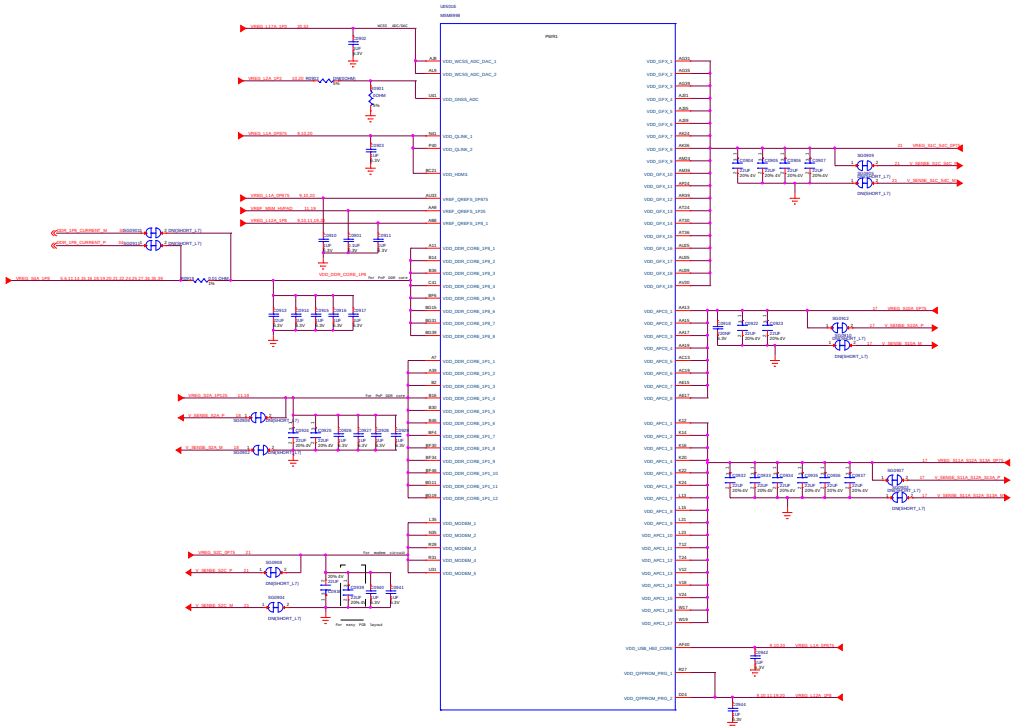

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Size	Document Number		Rev
C	MS8999_PWR1		V4
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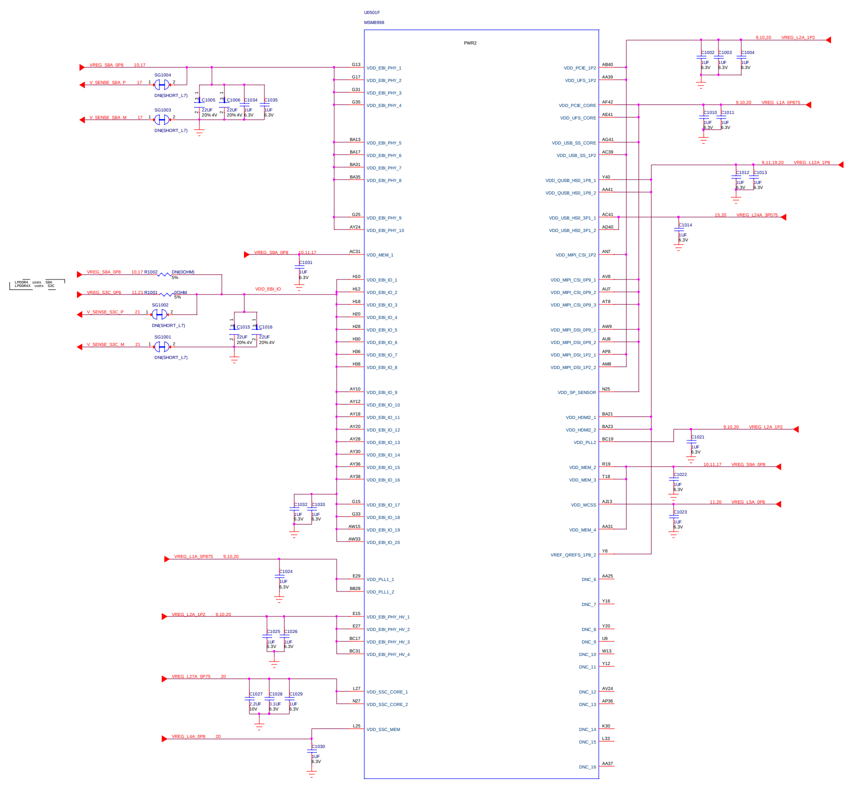
U0501F
MSM8998
PWR2
VDD_EBI_PHY_1
VDD_EBI_PHY_2
VDD_EBI_PHY_3
VDD_EBI_PHY_4
VDD_EBI_PHY_5
VDD_EBI_PHY_6
VDD_EBI_PHY_7
VDD_EBI_PHY_8
VDD_EBI_PHY_9
VDD_EBI_PHY_10
VDD_MEM_1
VDD_EBI_IO_1
VDD_EBI_IO_2
VDD_EBI_IO_3
VDD_EBI_IO_4
VDD_EBI_IO_5
VDD_EBI_IO_6
VDD_EBI_IO_7
VDD_EBI_IO_8
VDD_EBI_IO_9
VDD_EBI_IO_10
VDD_EBI_IO_11
VDD_EBI_IO_12
VDD_EBI_IO_13
VDD_EBI_IO_14
VDD_EBI_IO_15
VDD_EBI_IO_16
VDD_EBI_IO_17
VDD_EBI_IO_18
VDD_EBI_IO_19
VDD_EBI_IO_20
VDD_PLL1_1
VDD_PLL1_2
VDD_EBI_PHY_HV_1
VDD_EBI_PHY_HV_2
VDD_EBI_PHY_HV_3
VDD_EBI_PHY_HV_4
VDD_SSC_CORE_1
VDD_SSC_CORE_2
VDD_SSC_MEM
VDD_PCIE_1P2
VDD_UFS_1P2
VDD_PCIE_CORE
VDD_UFS_CORE
VDD_USB_SS_CORE
VDD_USB_SS_1P2
VDD_QUSB_HS0_1P8_1
VDD_QUSB_HS0_1P8_2
VDD_USB_HS0_3P1_1
VDD_USB_HS0_3P1_2
VDD_MIPI_CSI_1P2
VDD_MIPI_CSI_0P9_1
VDD_MIPI_CSI_0P9_2
VDD_MIPI_CSI_0P9_3
VDD_MIPI_DSI_0P9_1
VDD_MIPI_DSI_0P9_2
VDD_MIPI_DSI_1P2_1
VDD_MIPI_DSI_1P2_2
VDD_SP_SENSOR
VDD_HDMI2_1
VDD_HDMI2_2
VDD_PLL2
VDD_MEM_2
VDD_MEM_3
VDD_MCSS
VDD_MEM_4
VREF_QREFS_1P8_2
VREG_S8A_0P8
V_SENSE_S8A_P
V_SENSE_S8A_M
VREG_S3C_0P6
V_SENSE_S3C_P
V_SENSE_S3C_M
VREG_L1A_1P2
VREG_L2A_1P2
VREG_L11A_0P875
VREG_L12A_1P8
VREG_L24A_3P075
VREG_L5A_0P8
VREG_L27A_0P75
VREG_L4A_0P8
VDD_EBI_IO

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D	MSM8998_PWR2	V1

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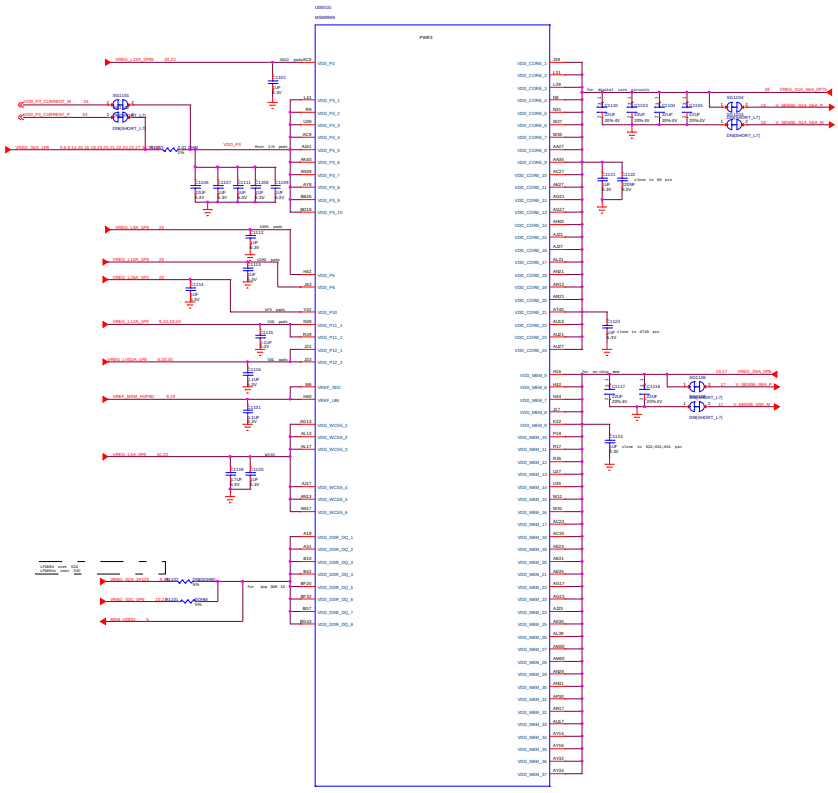

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Size	Document Number		Rev
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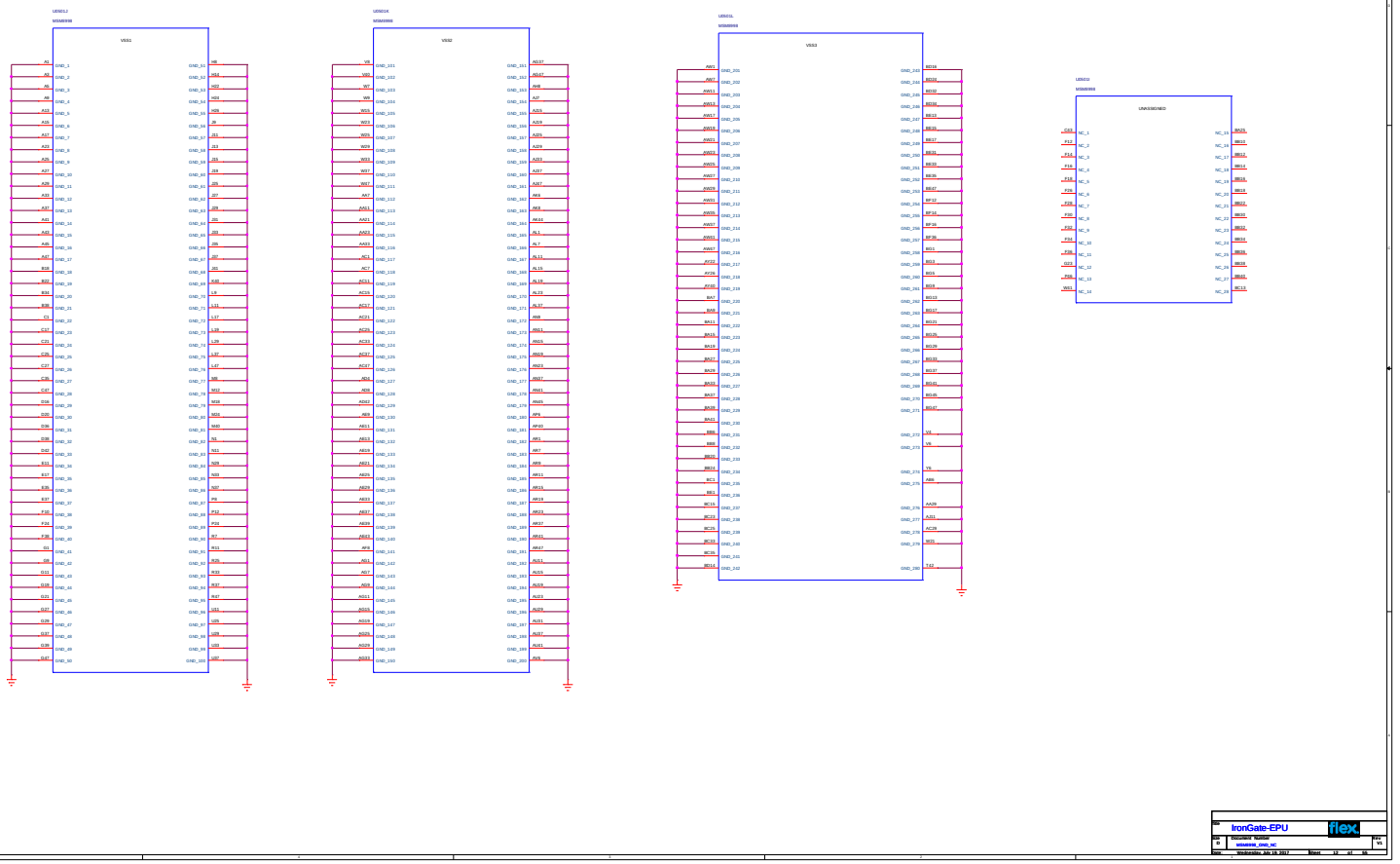

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Size	Document Number		Rev
D	MSM8998_2501_MC		V4
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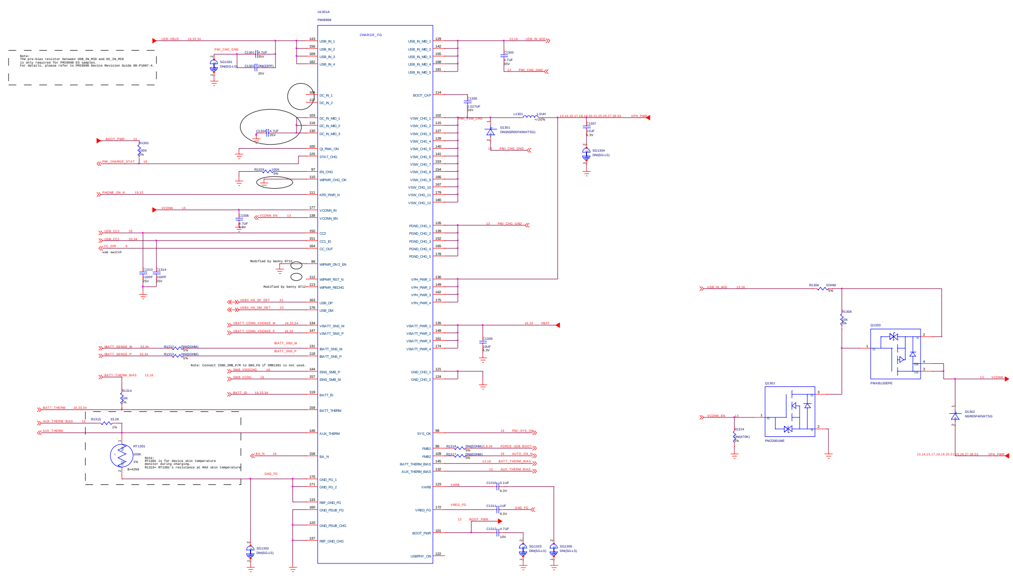

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Size: E	Document Number: PMI8998_Charge_FG		Rev: V1
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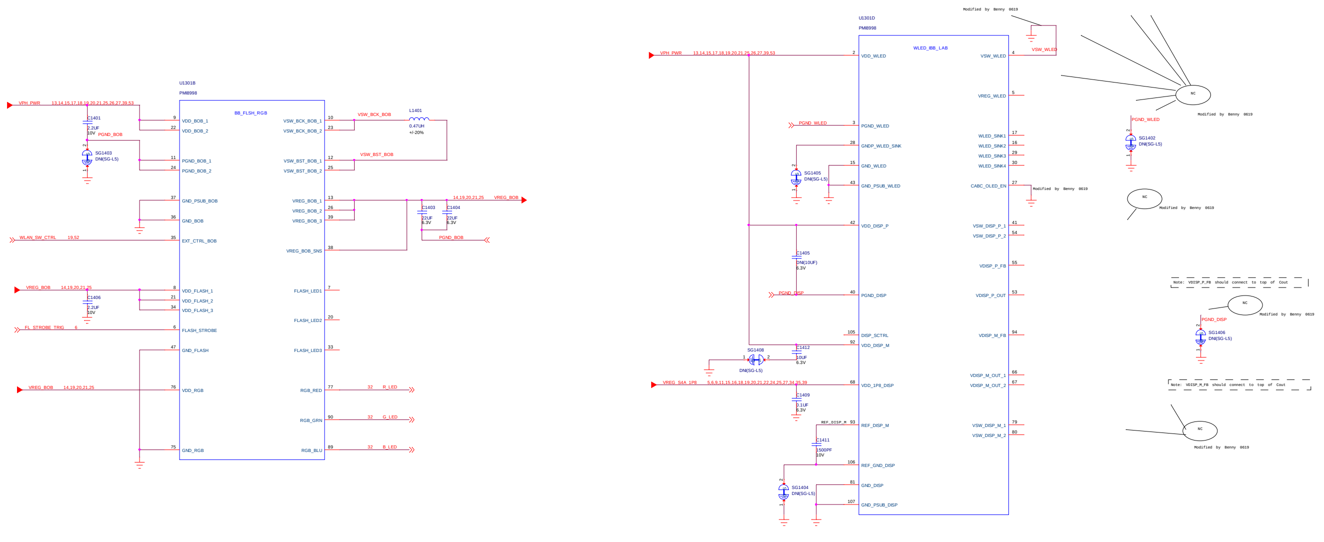

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Size	D
Document Number	PMI8998_Buck_Boost_Flash
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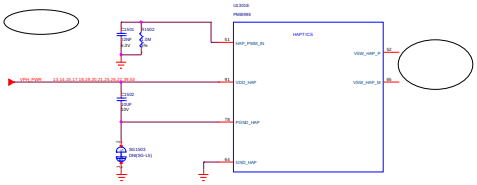
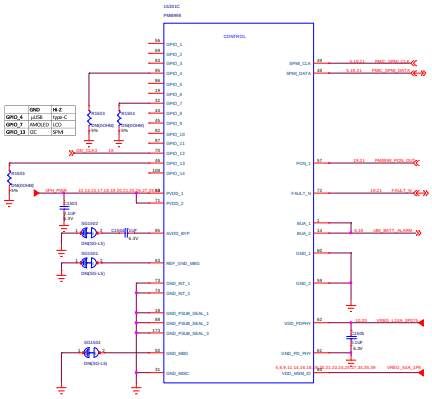
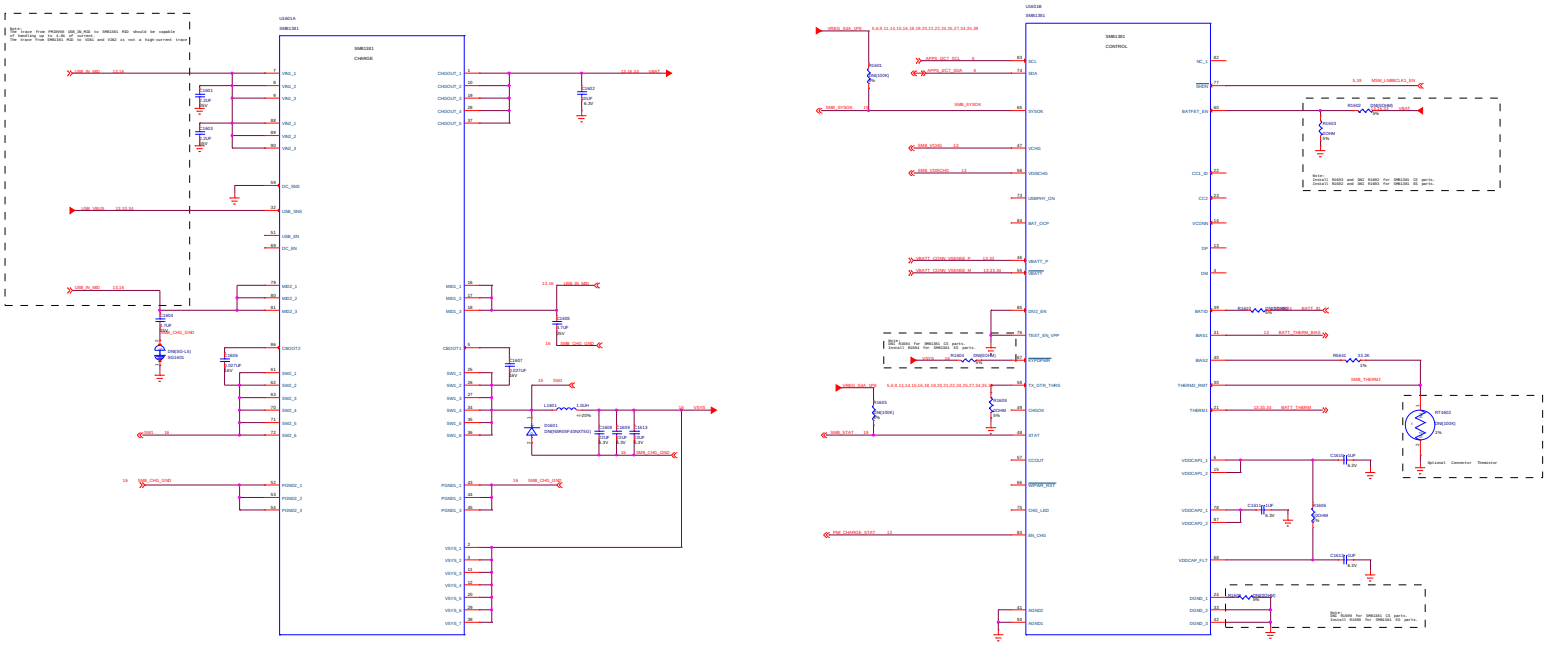




	GND	Hi-Z
GPIO_4	µUSB	type-C
GPIO_7	AMUX10	I/O
GPIO_13	I2C	SPMI



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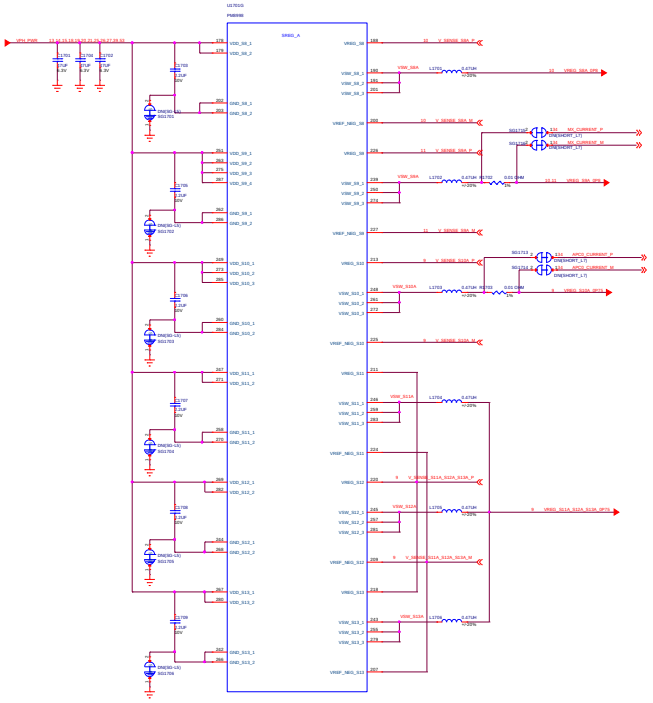
U17010
PM6966
SR6G_A
VDD_SR_1
VDD_SR_2
GND_SR_1
GND_SR_2
VDD_S10_1
VDD_S10_2
VDD_S10_3
GND_S10_1
GND_S10_2
VDD_S11_1
VDD_S11_2
GND_S11_1
GND_S11_2
VDD_S12_1
VDD_S12_2
GND_S12_1
GND_S12_2
VDD_S13_1
VDD_S13_2
GND_S13_1
GND_S13_2
VSW_SR_1
VSW_SR_2
VSW_SR_3
VSW_S10_1
VSW_S10_2
VSW_S10_3
VSW_S11_1
VSW_S11_2
VSW_S11_3
VSW_S12_1
VSW_S12_2
VSW_S12_3
VSW_S13_1
VSW_S13_2
VSW_S13_3
VRSG_SR
VRSG_S10
VRSG_S11
VRSG_S12
VRSG_S13
VRSP_NEG_SR
VRSP_NEG_S10
VRSP_NEG_S11
VRSP_NEG_S12
VRSP_NEG_S13
V_SENSE_SR_P
V_SENSE_SR_M
V_SENSE_S10_P
V_SENSE_S10_M
V_SENSE_S11_P
V_SENSE_S11_M
V_SENSE_S12_S13_S12A_S13A_P
V_SENSE_S12_S13_S12A_S13A_M
VSW_SR_A
VSW_S10_A
VSW_S11_A
VSW_S12_A
VSW_S13_A
L1702
0.47UH
+/-20%
0.001 OHM
1%
SR_CURRENT_P
SR_CURRENT_M
S10_CURRENT_P
S10_CURRENT_M
ONESHORT_17
VRSG_SR_A_SPS
VRSG_S10_A_SPS
VRSG_S12_S13_S12A_S13A_SPS
PM6966_Rails_IOP2
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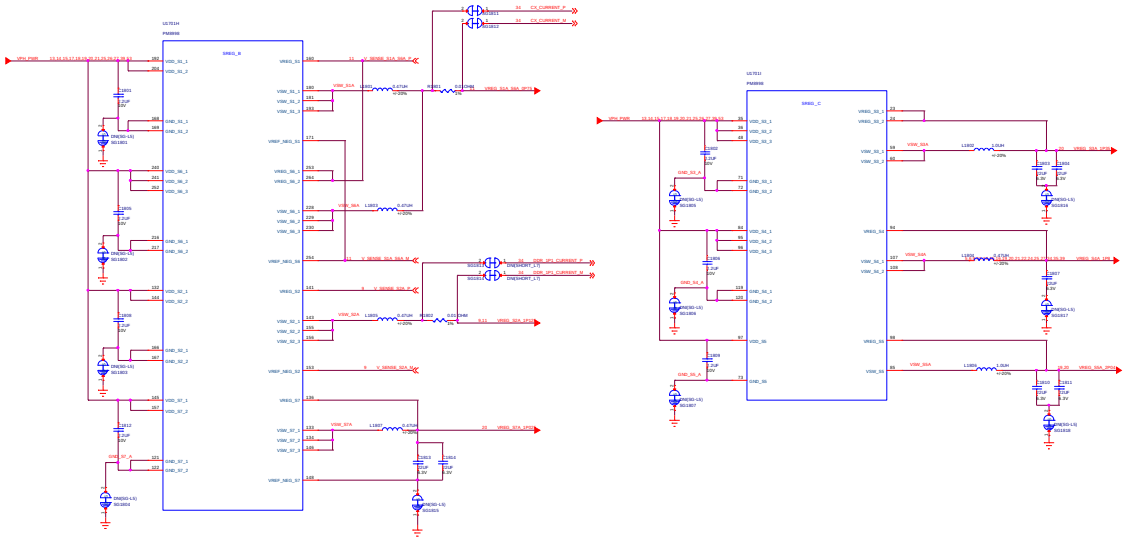

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D	PM8998_Rails_IOP3		V4
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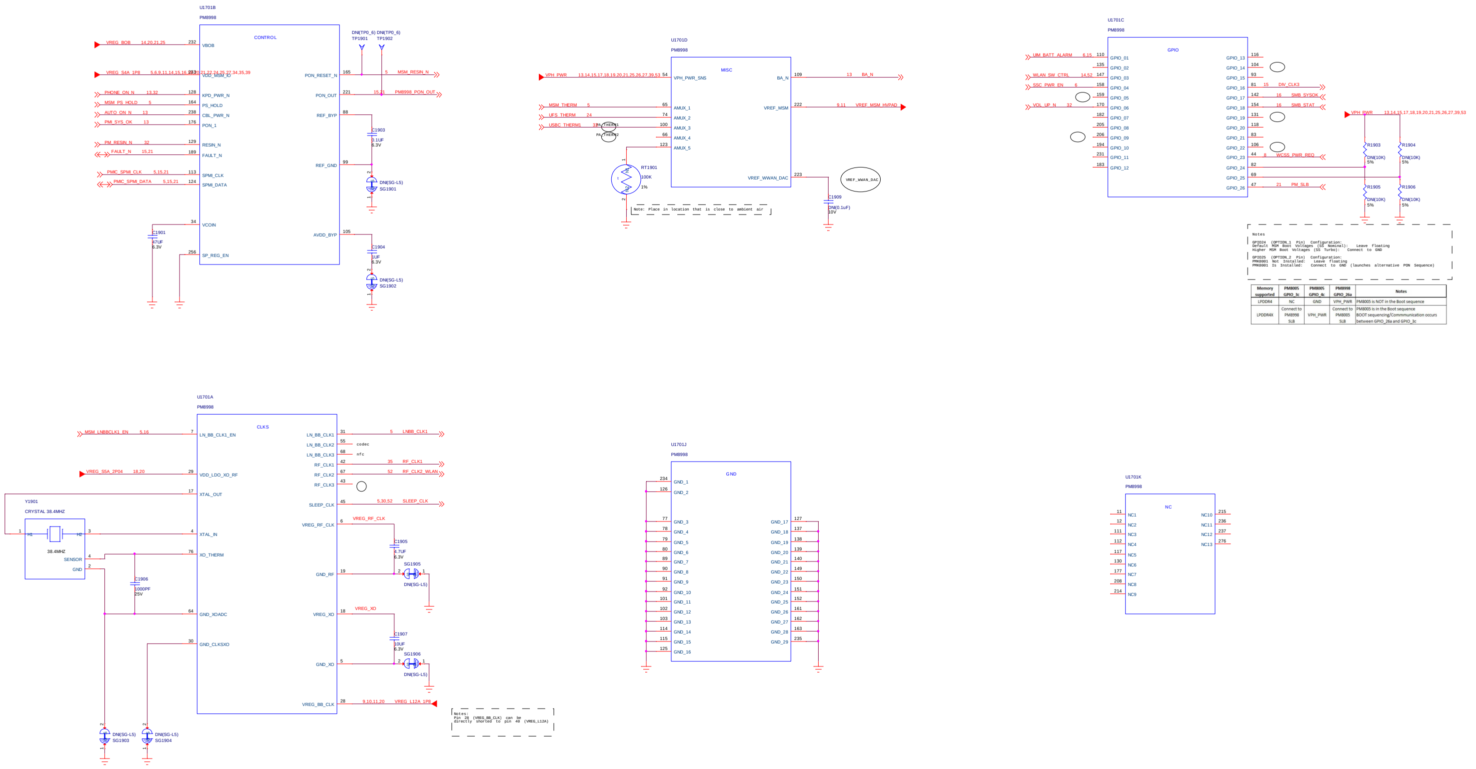

Notes

GPIO24 (OPTION_1 Pin) Configuration:
Default MSM Boot Voltages (SS Nominal): Leave floating
Higher MSM Boot Voltages (SS Turbo): Connect to GND

GPIO25 (OPTION_2 Pin) Configuration:
PMK8001 Not Installed: Leave floating
PMK8001 Is Installed: Connect to GND (launches alternative PON Sequence)

Memory supported	PM8005 GPIO_3c	PM8005 GPIO_4c	PM8998 GPIO_26a	Notes
LPDDR4	NC	GND	VPH_PWR	PM8005 is NOT in the Boot sequence
LPDDR4X	Connect to PM8998 SLB	VPH_PWR	Connect to PM8005 SLB	PM8005 is in the Boot sequence BOOT sequencing/Commmunication occurs between GPIO_26a and GPIO_3c

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Size: D	Document Number: PM8998_CLK_CNTRL_GPIO_AMUX	Rev: V1
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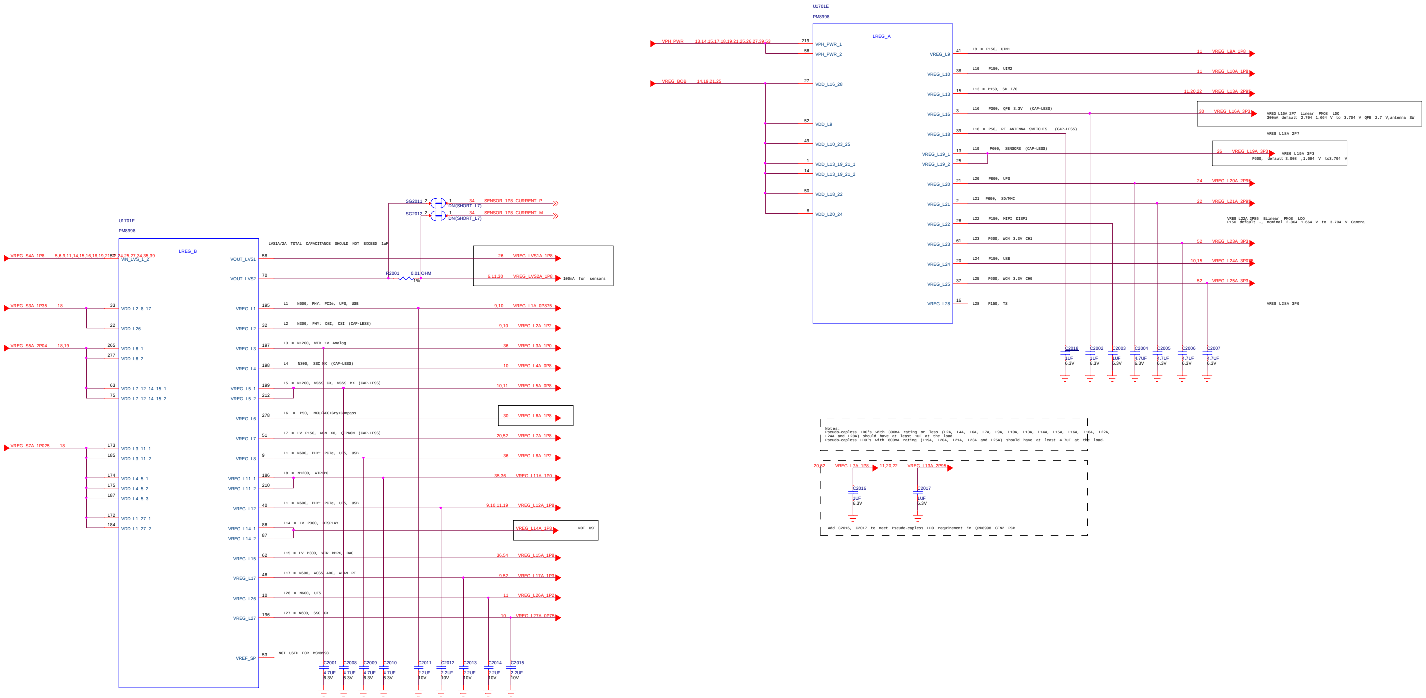

Title	IronGate-EPU		
Size D	Document Number PM8998_LDOs		Rev V1
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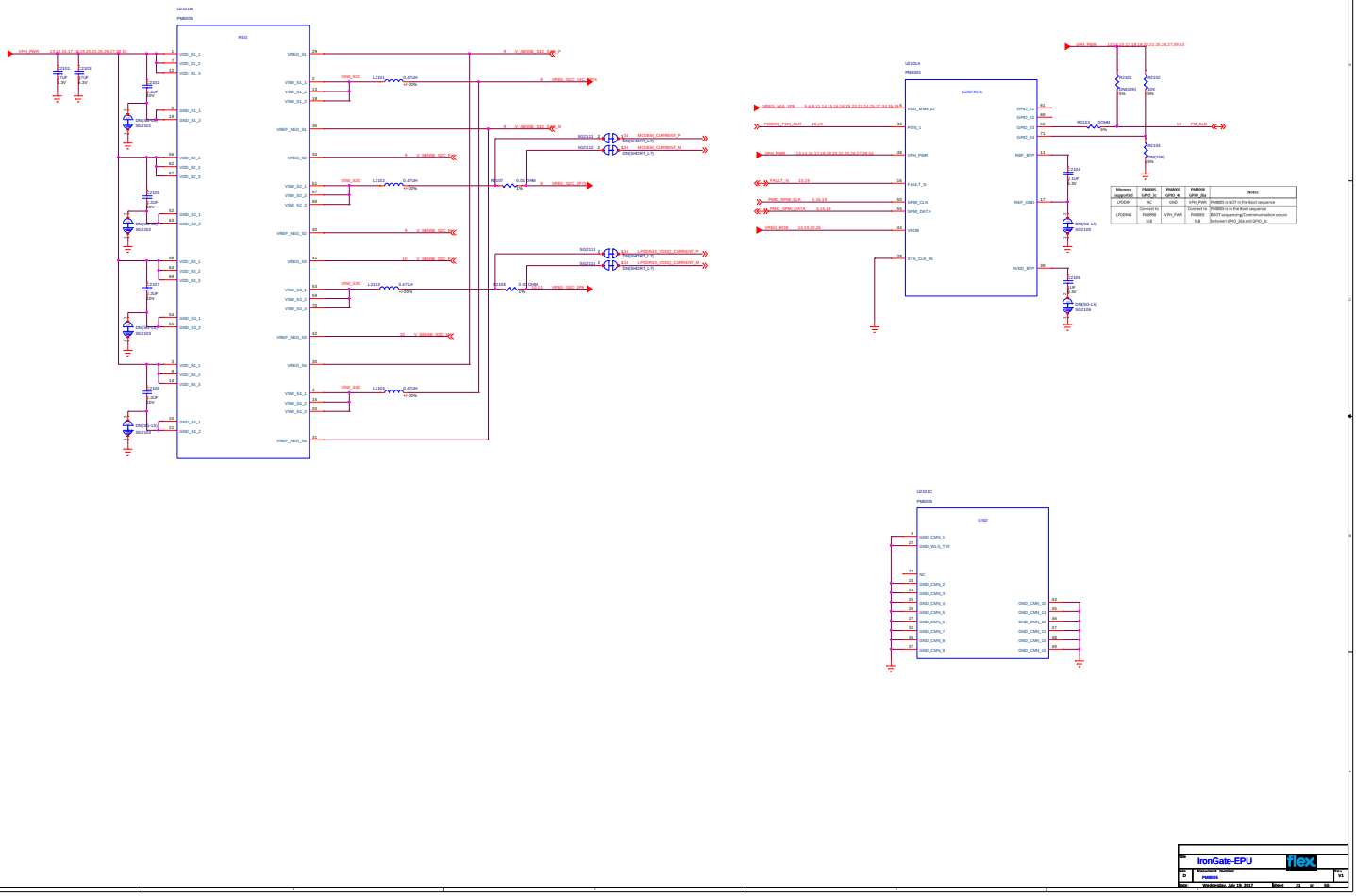
U2101B
PM8005
REG
VPH_PWR
VDD_SI_1
VDD_SI_2
VDD_SI_3
GND_SI_1
GND_SI_2
VREG_S1
VREG_S2
VREG_S3
VREG_S4
VSW_SI_1
VSW_SI_2
VSW_SI_3
VREF_NEG_S1
VREF_NEG_S2
VREF_NEG_S3
VREF_NEG_S4
V_SENSE_SEC_S1P
V_SENSE_SEC_S1N
V_SENSE_SEC_S2P
V_SENSE_SEC_S2N
V_SENSE_SEC_S3P
V_SENSE_SEC_S3N
VREG_SEC_S1
VREG_SEC_S2
VREG_SEC_S3
L2101
L2102
L2103
0.47UH
+/-20%
R2101
R2102
R2103
0.01OHM
1%
MODESN_CURRENT_P
MODESN_CURRENT_M
DRDPRDX_VDDQ_CURRENT_P
DRDPRDX_VDDQ_CURRENT_M
U2101A
PM8005
CONTROL
VDD_MSM_IO
PON_1
VPH_PWR
FAULT_N
SPMI_CLK
SPMI_DATA
VBOB
SYS_CLK_IN
GPIO_01
GPIO_02
GPIO_03
GPIO_04
RSF_BYP
RSF_GND
AVDD_BYP
R2203
200HM
1%
R2201
100K(10K)
5%
R2202
20K
5%
R2204
100K(10K)
5%
Memory supported
PM8005 GPIO_3
PM8005 GPIO_4c
PM8998 GPIO_20d
Notes
LPDDR4
NC
GND
VPH_PWR
PM8998 is NOT in the Boot sequence
LPDDR4X
Connect to PM8998 S1B
Connect to PM8005 S1B
VPH_PWR
Connect to PM8005 BOOT sequencing/Communication occurs between GPIO_3&a and GPIO_3C
U2101C
PM8005
GND
GND_CMN_1
GND_MLS_TST
NC
GND_CMN_2
GND_CMN_3
GND_CMN_4
GND_CMN_5
GND_CMN_6
GND_CMN_7
GND_CMN_8
GND_CMN_9
GND_CMN_10
GND_CMN_11
GND_CMN_12
GND_CMN_13
GND_CMN_14
GND_CMN_15
IronGate-EPU
flex
Document Number
PM8005
Wednesday, July 19, 2017
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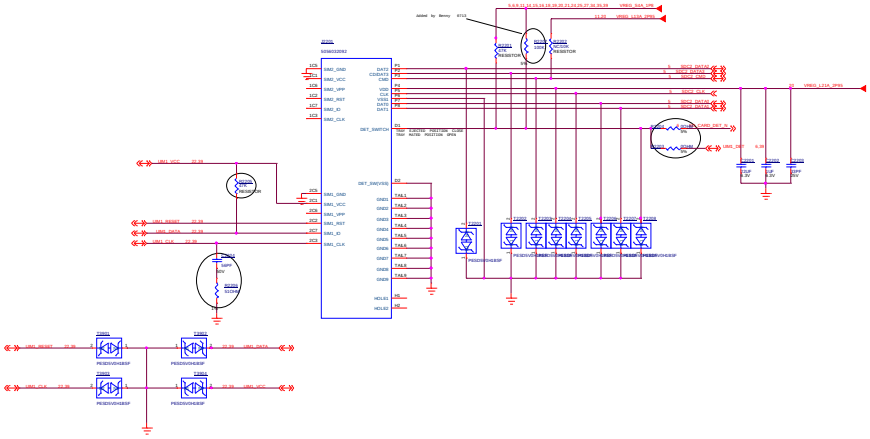
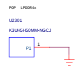
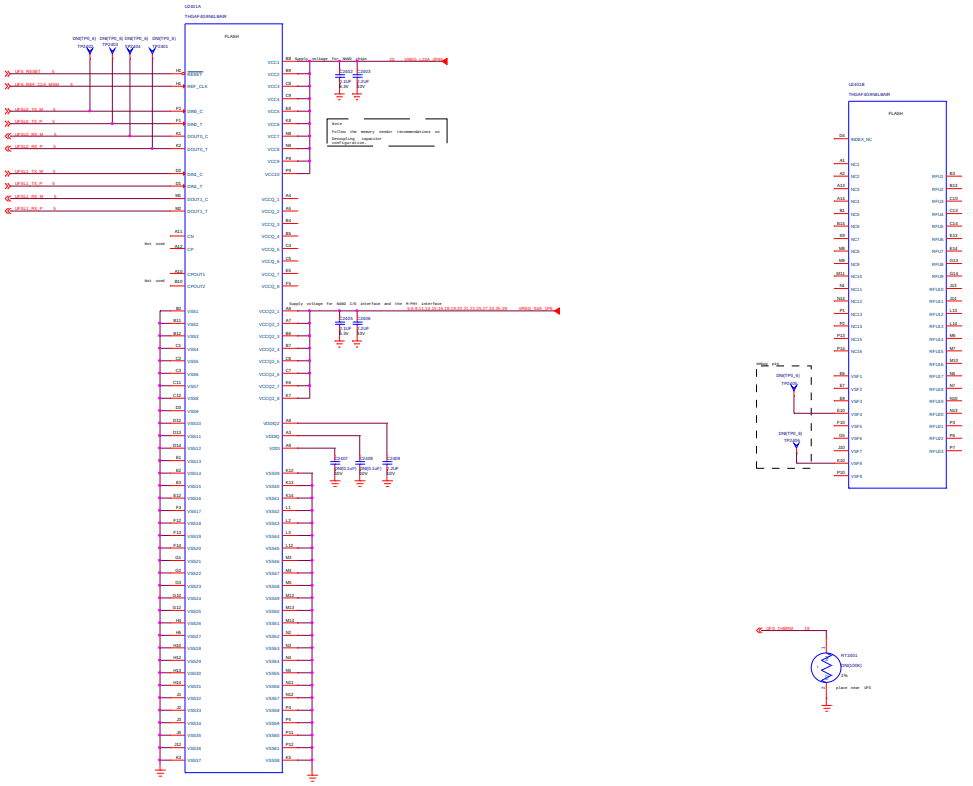
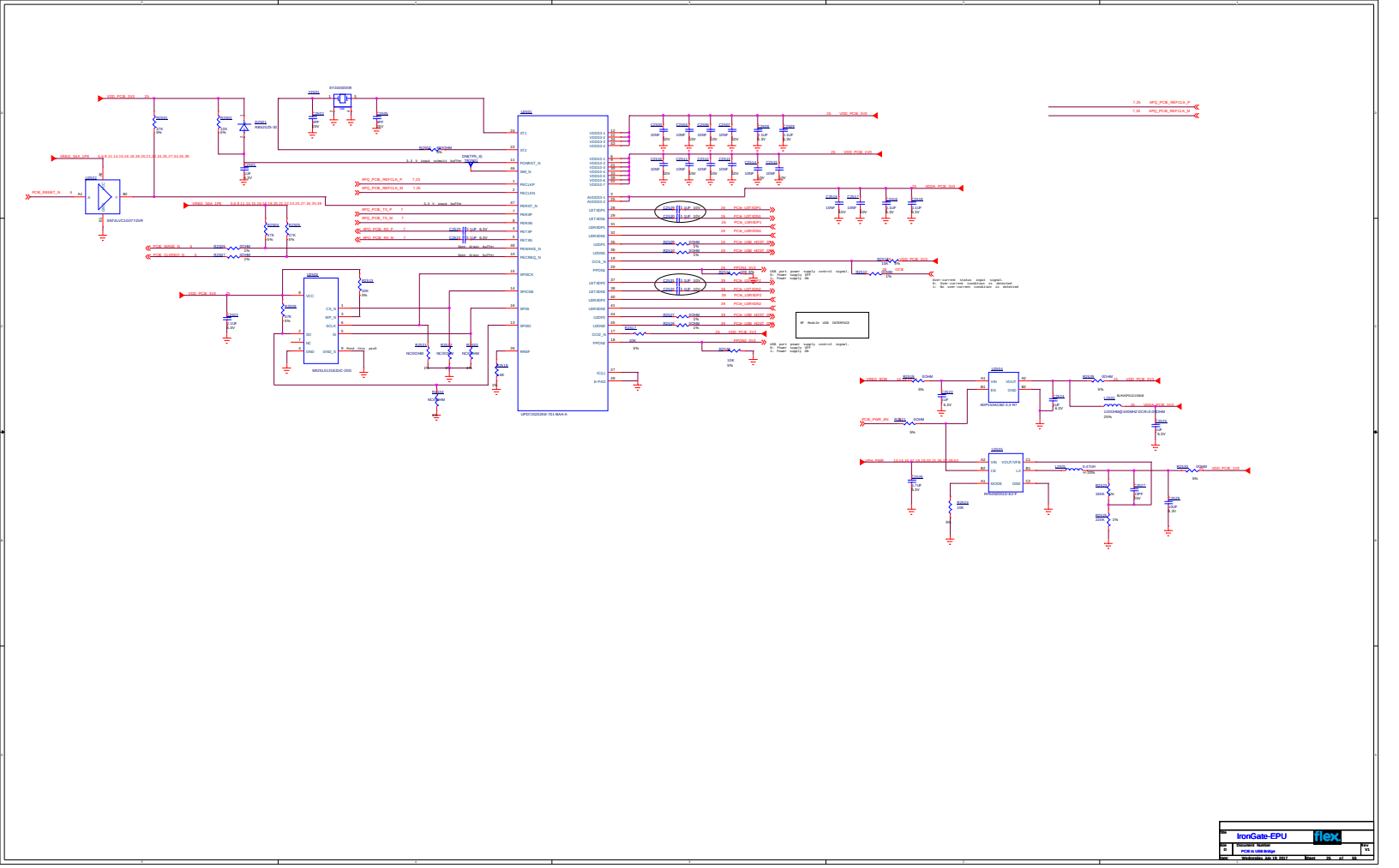

Added by Benny 8713
SD_DATA0
SD_DATA1
SD_DATA2
SD_DATA3
SD_CMD
SD_CLK
SD_CARD_DET_N
SIM1_VCC
SIM1_RESET
SIM1_DATA
SIM1_CLK
SIM1_GND
SIM1_VPP
SIM1_RST
SIM1_ID
DET_SWITCH
DET_SWVSS
PESD5V0H4BSF



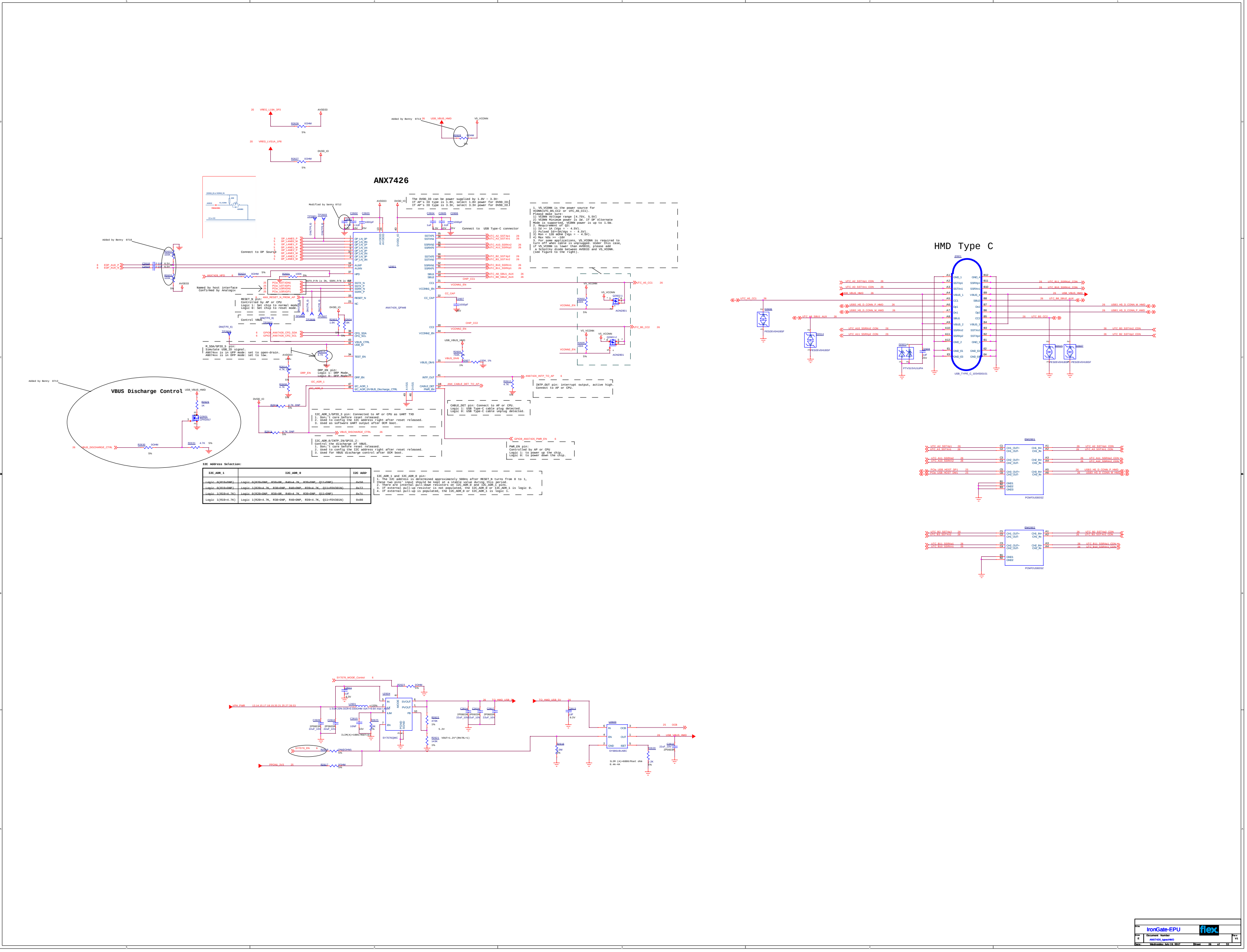
Title	IronGate-EPU		
Size D	Document Number LPDDR4/4x		Rev V1
Date:	Wednesday, July 19, 2017	Sheet 23 of 55	



Title	IronGate-EPU	flex
Size: A	Document Number: UFS	Rev: V1
Date: Wednesday, July 19, 2017	Sheet 24 of 68	



Title	IronGate-EPU
Size	A3
Document Number	PCIE to USB Bridge
Rev	V1
Date	Wednesday, July 19, 2017
Sheet	25 of 65



ANX7426

The DVDD_IO can be power supplied by 1.8V - 3.3V:
If AP's IO type is 1.8V, select 1.8V power for DVDD_IO;
If AP's IO type is 3.3V, select 3.3V power for DVDD_IO.

Connect to USB Type-C connector

1. V5_VCONN is the power source for VCONN(UTC_B5_CC2 or UTC_A5_CC1).
Please make sure:
1) VCONN Voltage range [4.75V, 5.5V]
2) VCONN Minimum power is 1W. If DP Alternate Mode is supported, VCONN power is up to 1.5W.
2. Requirement of Q3:
1) Id >= 1A (Vgs = - 4.5V).
2) Pulsed Id>=3A(Vgs = - 4.5V).
3) Ron < 120 mOhm (Vgs = - 4.5V).
4) Max Vds >= -10V
3. For some applications, V5_VCONN is required to turn off when cable is unplugged. Under this case, if V5_VCONN is lower than AVDD33, please add a Schottky diode between AVDD33 and V5_VCONN. (see figure to the right).

CABLE_DET pin: Connect to AP or CPU.
Logic 1: USB Type-C cable plug detected.
Logic 0: USB Type-C cable unplug detected.

I2C_ADR_1/GPIO_3 pin: Connected to AP or CPU as UART TXD
1. Don¡¯t care before reset released.
2. Used to config the I2C address right after reset released.
3. Used as software UART output after OCM boot.

I2C_ADR_0/INTP_IN/GPIO_2:
Control the discharge of VBUS.
1. Don¡¯t care before reset released.
2. Used to config the I2C address right after reset released.
3. Used for VBUS discharge control after OCM boot.

PWR_EN pin:
Controlled by AP or CPU
Logic 1: to power up the chip.
Logic 0: to power down the chip.

VBUS Discharge Control

HMD Type C

I2C Address Selection:

I2C_ADR_1	I2C_ADR_0	I2C Addr
Logic 0(R19=DNP)	Logic 0(R20=DNP, R38=0R, R40=4.7K, R39=DNP, Q11=DNP)	0x50
Logic 0(R19=DNP)	Logic 1(R20=4.7K, R38=DNP, R40=DNP, R39=4.7K, Q11=FDV301N)	0x72
Logic 1(R19=4.7K)	Logic 0(R20=DNP, R38=0R, R40=4.7K, R39=DNP, Q11=DNP)	0x7c
Logic 1(R19=4.7K)	Logic 1(R20=4.7K, R38=DNP, R40=DNP, R39=4.7K, Q11=FDV301N)	0x80

I2C_ADR_1 and I2C_ADR_0 pin:
1. The I2C address is determined approximately 500ns after RESET_N turns from 0 to 1, these two pins' input should be kept at a stable value during this period.
2. There are internal pull-down resistors on I2C_ADR_0 and I2C_ADR_1 pins.
3. If external pull-up resistor is not populated, the I2C_ADR_0 or I2C_ADR_1 is logic 0.
4. If external pull-up is populated, the I2C_ADR_0 or I2C_ADR_1 is logic 1.

Title: IronGate-EPU
Size: E | Document Number: ANX7426_typecHMD | Rev: V1
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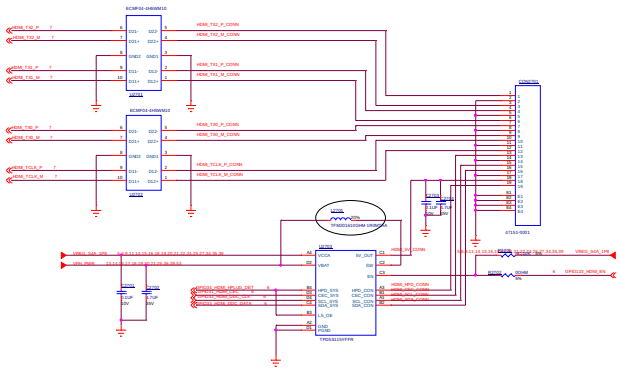
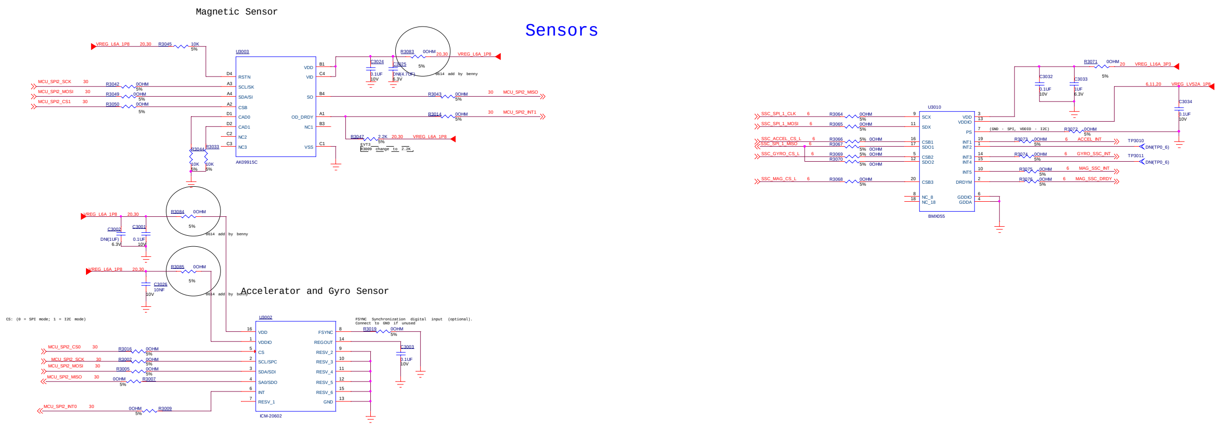
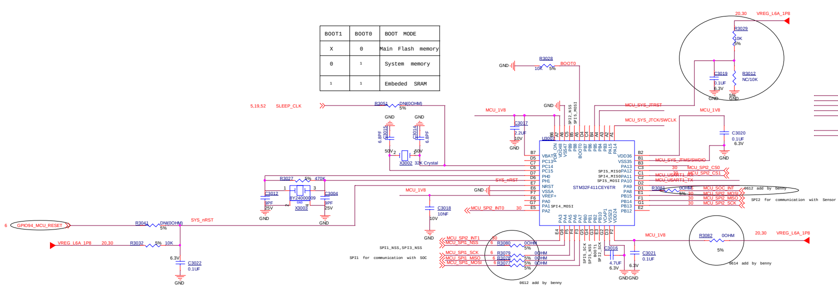


Title	IronGate-EPU	flex
Size: A	Document Number: HDMI	Rev: V4
Date: Wednesday, July 19, 2017	Sheet 27 of 65	

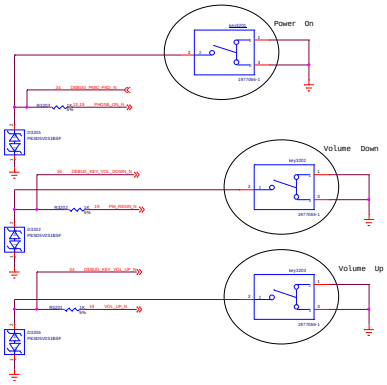
Sensors



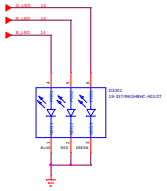
BOOT1	BOOT0	BOOT MODE
X	0	Main Flash memory
0	1	System memory
1	1	Embeded SRAM



Title	IronGate-EPU		
Size D	Document Number: Sensors&MCU		Rev V1
Date: Wednesday, July 19, 2017	Sheet 30 of 55		



Charger indicator



Signal	Description
KPSNS0	Volume Up
PM_RST_N	Volume Down
KYPD_PWR_N	PWER_ON
PM_RST_N + KYPD_PWR_N	Hardware Reset

IronGate-EPU

Document Number

Keypad/Status Indicator

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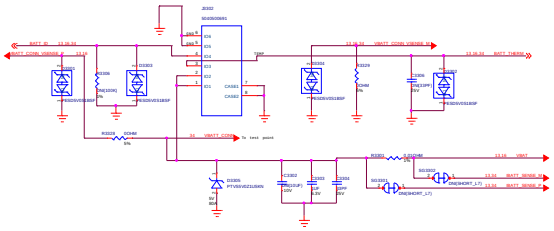
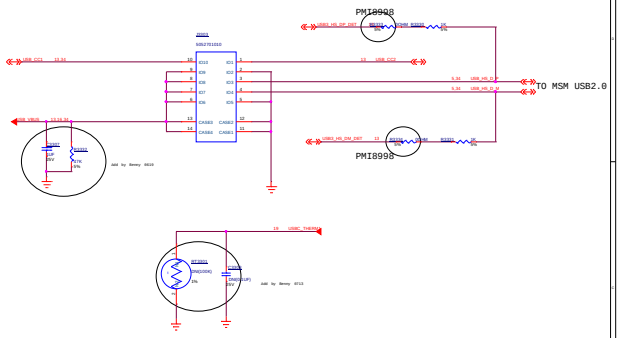
Battery CONN

Battery Connector



Type C(USB2.0 from SD835,Charger)



IronGate-EPU			flex
Size: C	Document Number: Battery_ConnectCharger(TypeC		Rev: V4
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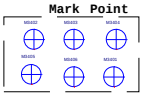
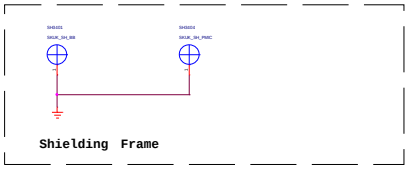
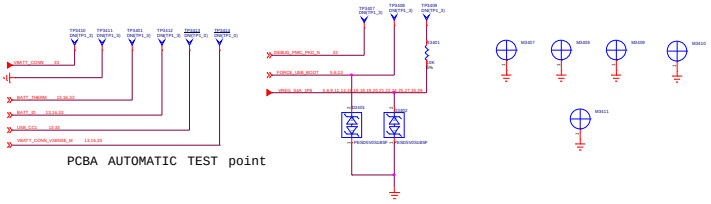
Mark Point





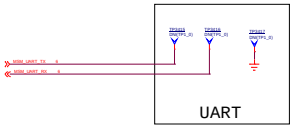
Shielding Frame

Test Point

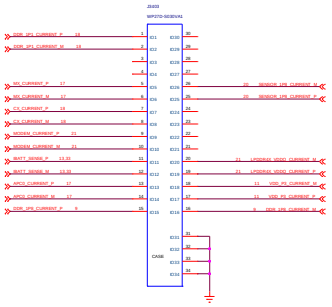


PCBA AUTOMATIC TEST point

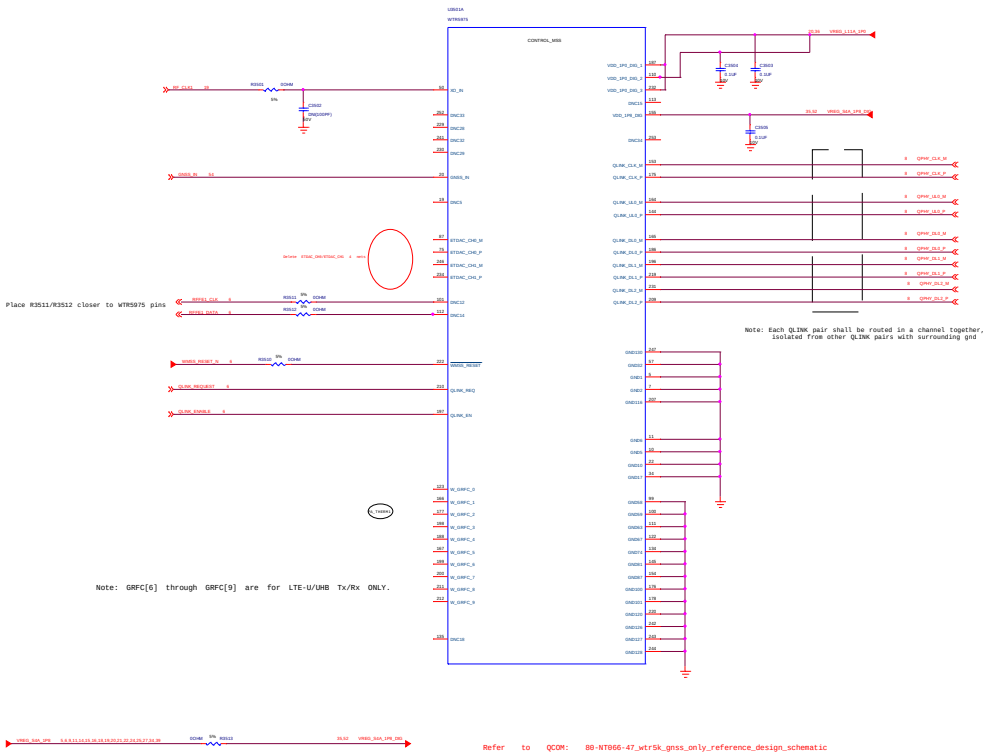
UART



RCM CONNECTOR



WTR5975 MSS



Refer to QCOM: 80-NT066-47_wtr5k_gnss_only_reference_design_schematic

Title: IronGate-EPU			flex
Size: C	Document Number: WTR5975 MSS		Rev: V4
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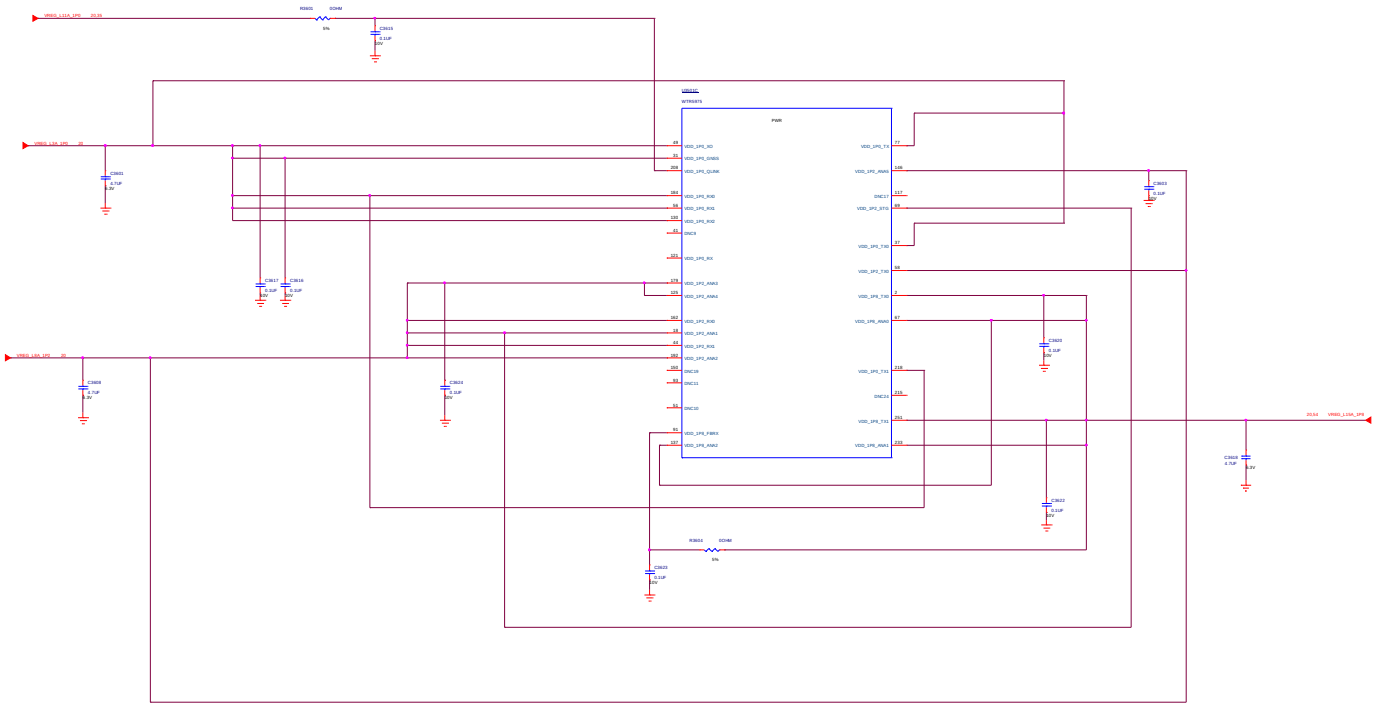
WTR5975 POWER



Delete R3602/R3603/C3613/C3609/C3614/C3612/C3611/C3610/C3606/C3604/C3619/C3621/C3607/C3605/C3602

Title	IronGate-EPU	flex
Size: A	Document Number: WTR5975 POWER	Rev: V4
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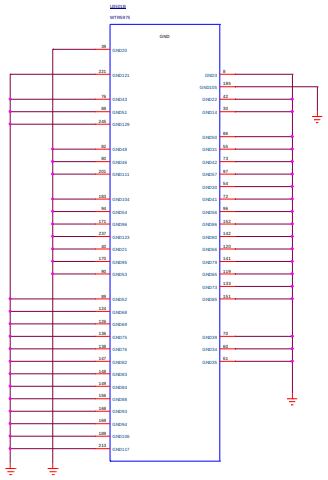
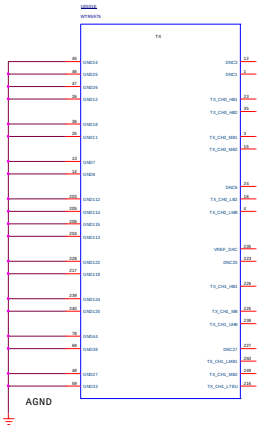
WTR5975 TX & GND





Delete all Tx Line

IronGate-EPU			
Size: A	Document Number: WTR5975 TX_GND		Rev: V1
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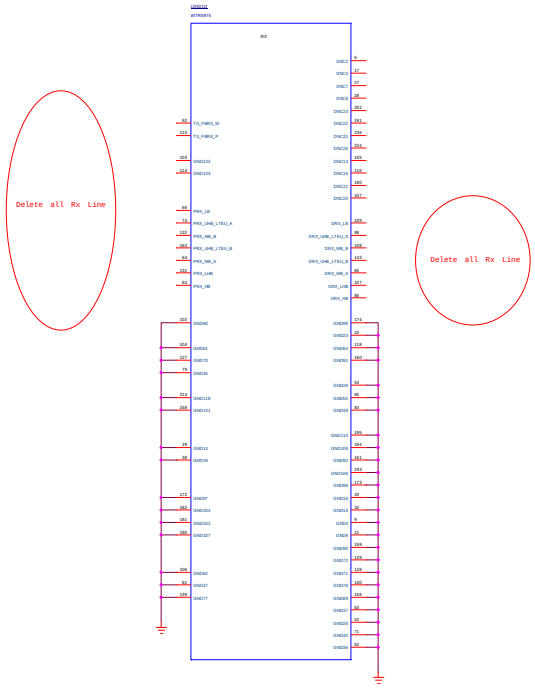
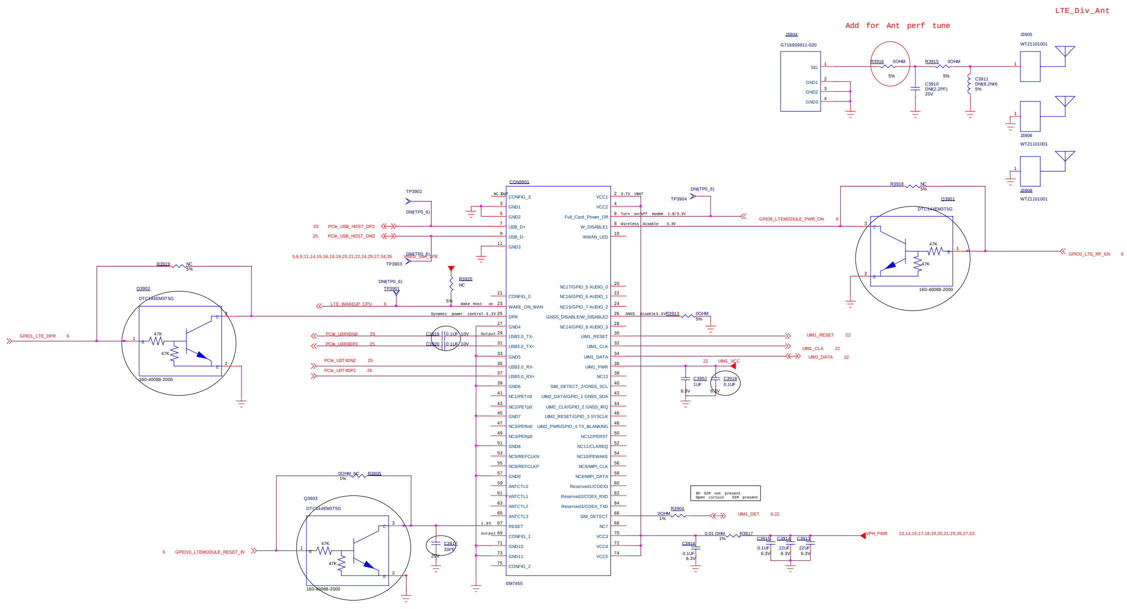
WTR5975 RX

RX inputs are 50ohm and no matching required if connected to 50ohm source.
DC blocks are not required if external devices (i.e. a switch) don't present DC to the eLNA.





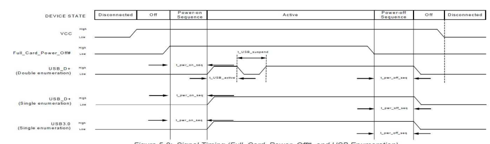


Figure 5-2: Signal Timing (Full_Card_Power_Off#, and USB Enumeration)

Title	IronGate-EPU
Size	D
Document Number	4G_LTE_MODULE&SIM
Rev	V1
Date:	Wednesday, July 19, 2017
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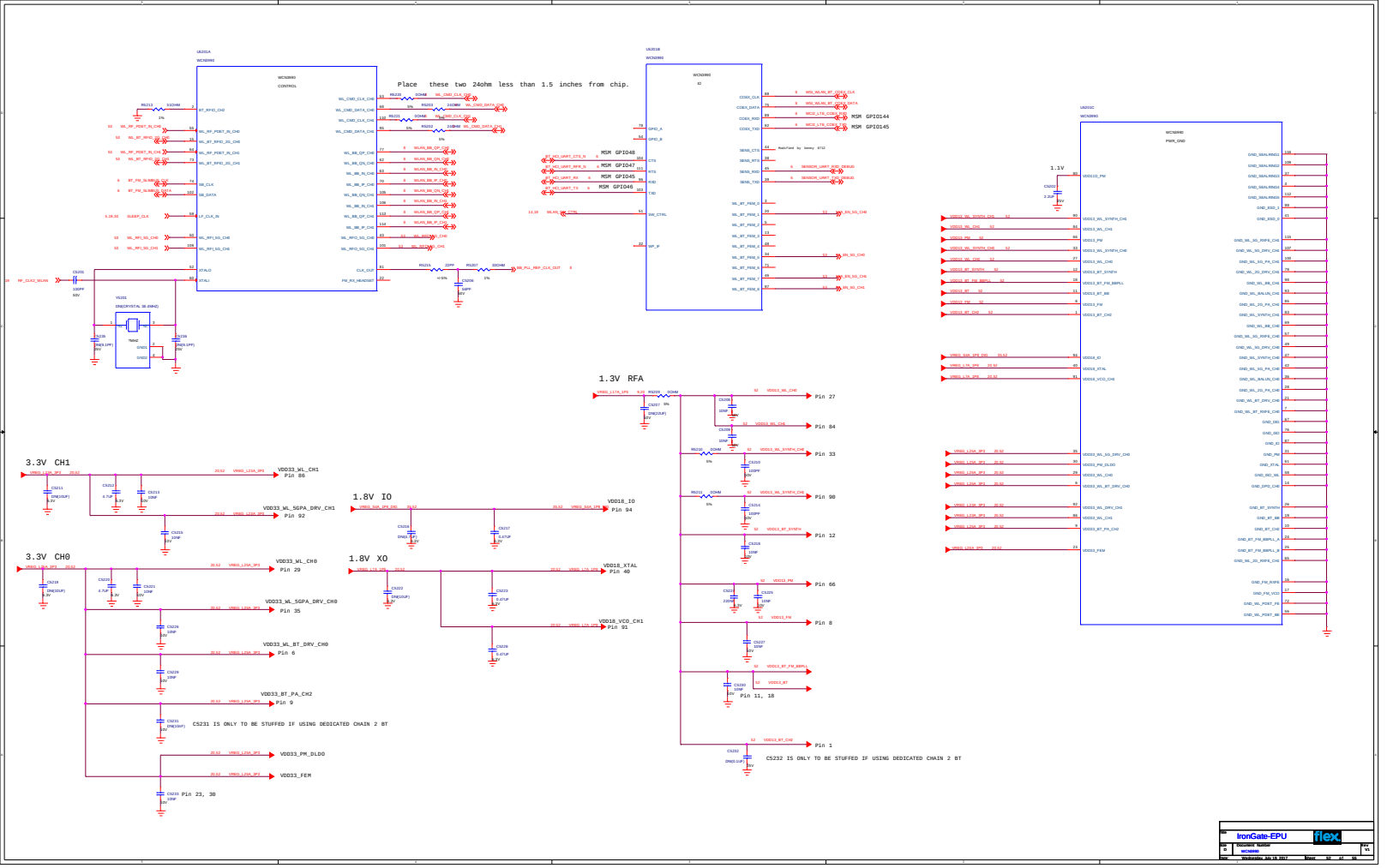
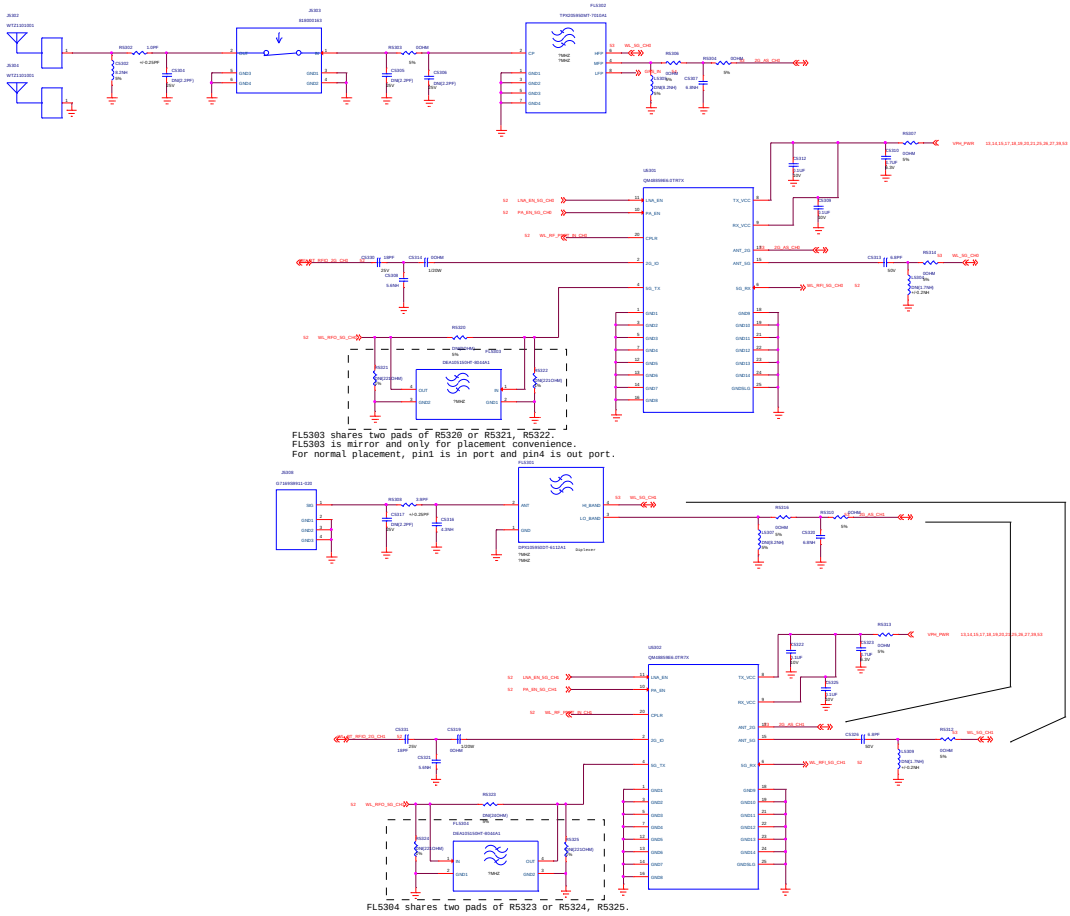


Title: IronGate-EPU			
Size: C	Document Number: WCN3990		Rev: V4
Date: Wednesday, July 19, 2017	Sheet: 92 of 98		

Chain 0



FL5303 shares two pads of R5320 or R5321, R5322.
FL5303 is mirror and only for placement convenience.
For normal placement, pin1 is in port and pin4 is out port.

FL5304 shares two pads of R5323 or R5324, R5325.

IronGate-EPU

flex

Document Number: WLAN_FEM

Rev: V1

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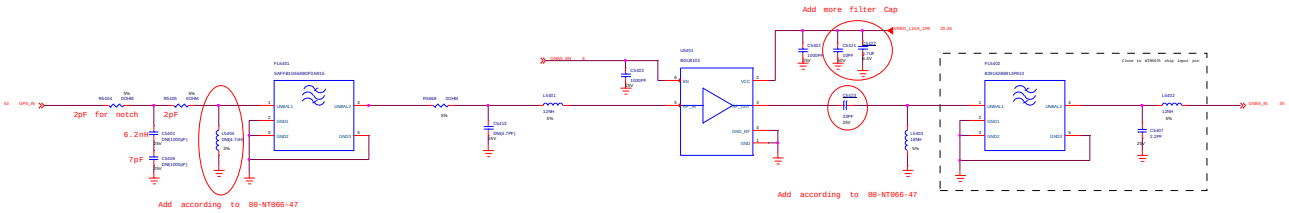

Title	IronGate-EPU		
Size	Document Number		Rev
C	GPS		V4
Date:	Wednesday, Jan 18, 2017	Sheet 64 of 65	

Modified by Benny 0619

1.Add JTAG TEST POINTS

2.Remove L1402(4.7UH),C1413(82PF),C1408(10UF),D1401(NSR05F40NXT5G),C1402(4.7UF),C1414(39PF),L1403(4.7UH),C1407(22UF),C1410(22UF),L1404(4.7UH)

3. Add C3307(1UF),R3332(47K)

Modified by Benny 0630

1.Change Gyro and Mag int from SSC to MSM GPIO118,119

Modified by Benny 0705

1.Correct USB3 connection on J2601

2.Add R3333,R3334

Modified by Benny 0712

1. U1301 pin99 WIPWR_DIV2_EN to GND,
2. U1301pin113,U5201 PIN44 WIPWR_RECHG to NC
3. Change C2601 from 1uF to 4.7uF

Modified by Benny 0713
1. change ESD components to PESD5V0H1BSF in page22
2. add R2207 100k
3. add R2668 0R 0402
3. add RT3301,C3308
4. MAG_SSC_DRDY is changed from ssc to GPIO120
5. Add Q2601,R2629,R2630,R2631

Modified by Benny 0718

1. add R2632,R2633

Title	IronGate-EPU		
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