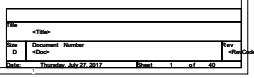
TABLE OF CONTENT



Revision History

REV	DESCRIPTION
0.1	EVT1.0 first release for review

Board Change History

SCHEMATIC MCN	HW VERSION	REVISION	DESCRIPTION OF CHANGE

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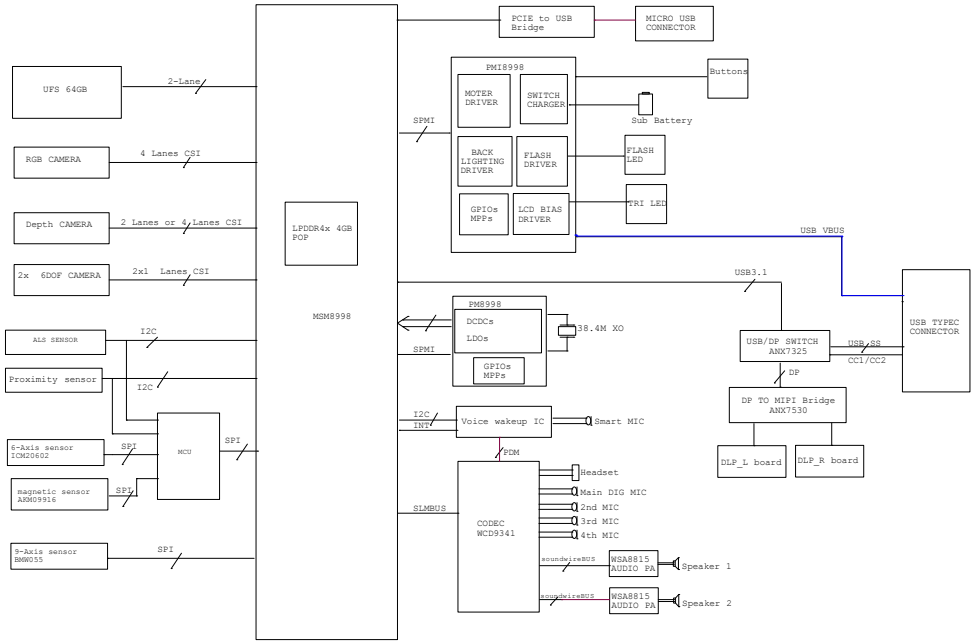
Schematic Block Diagram



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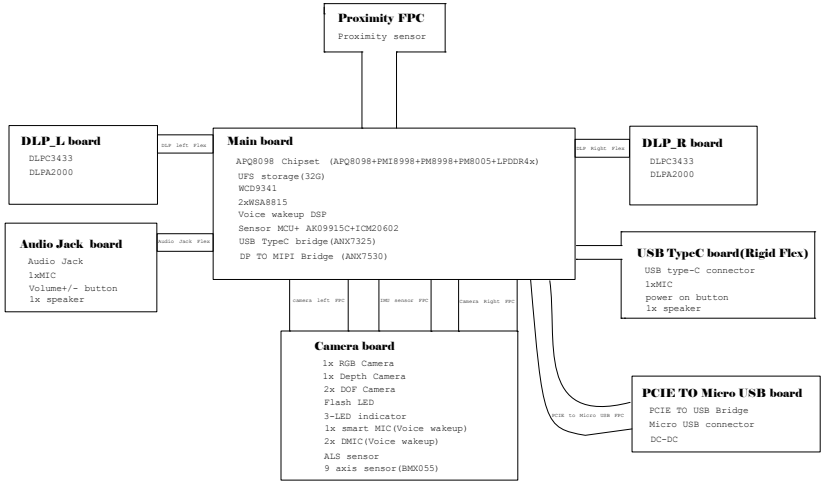

Block Diagram

MSM8998 GPIO Configuration for Irongate HMD

GPIO_0	ANX7401_INTP	GPIO_41	6DOF_FRAME_SYNC	GPIO_82	MCU_SPI1_MISO
GPIO_1	ANX7401_RESET_N	GPIO_42	6DOFL_STROBE	GPIO_83	MCU_SPI1_CS
GPIO_2	BLSP1_I2C_SDA	GPIO_43	VOICE_LCD_I2C6_SDA	GPIO_84	MCU_SPI1_SCK
GPIO_3	BLSP1_I2C_SCL	GPIO_44	VOICE_LCD_I2C6_SCL	GPIO_85	VOICE_SPI_MOSI
GPIO_4	MSM_UART_TX	GPIO_45	NC	GPIO_86	VOICE_SPI_MISO
GPIO_5	MSM_UART_RX	GPIO_46	ANX7325_INTP_TO_AP	GPIO_87	VOICE_SPI_CS_N
GPIO_6	ANX7530_PWR_EN	GPIO_47	MICRO_USB_VBUS_EN	GPIO_88	VOICE_SPI_CLK
GPIO_7	ANX7530_RST_EN	GPIO_48	MICRO_USB_VBUS_OCB_EN	GPIO_89	VOICE_RESET_N
GPIO_8	ANX7401_PWR_EN	GPIO_49	NC	GPIO_90	ANX7401_1P8_EN
GPIO_9	ANX7401_CABLE_DET	GPIO_50	USBC_DET_TO_AP	GPIO_91	VOICE_WAKE_UP_N
GPIO_10	BLSP4_I2C_SDA	GPIO_51	NC	GPIO_92	NC
GPIO_11	BLSP4_I2C_SCL	GPIO_52	CAM_6DOF_2P8_EN	GPIO_93	CAM_6DOF_1P8_EN
GPIO_12	NC	GPIO_53	CODEC_INT2	GPIO_94	ANX7325_PWR_EN
GPIO_13	CAM_MCLK0	GPIO_54	CODEC_INT1	GPIO_95	NC
GPIO_14	CAM_MCLK1	GPIO_55	APPS_I2C7_SDA	GPIO_96	NC
GPIO_15	CAM_MCLK2	GPIO_56	APPS_I2C7_SCL	GPIO_97	NC
GPIO_16	CAM_MCLK3	GPIO_57	FORCE_USB_BOOT	GPIO_98	NC
GPIO_17	CCI_I2C_SDA0	GPIO_58	DLP_L_HOST_IRQ	GPIO_99	NC
GPIO_18	CCI_I2C_SCL0	GPIO_59	DLP_R_HOST_IRQ	GPIO_100	NC
GPIO_19	CCI_I2C_SDA1	GPIO_60	BLSP11_I2C_SDA	GPIO_101	GRFC4
GPIO_20	CCI_I2C_SCL1	GPIO_61	BLSP11_I2C_SCL	GPIO_102	GRFC5
GPIO_21	TOF_START	GPIO_62	MCU_SOC_INT	GPIO_103	GRFC6
GPIO_22	FL_STROBE_TRIG	GPIO_63	ANX7530_INT	GPIO_104	GRFC7
GPIO_23	TOF_EN_ILLUM	GPIO_64	CODEC_RESET_N	GPIO_105	NC
GPIO_24	TOF_VSEL_EN	GPIO_65	CODEC_SPI_S_DIN	GPIO_106	NC
GPIO_25	DEP_3P65_EN	GPIO_66	CODEC_SPI_S_DOUT	GPIO_107	NC
GPIO_26	NC	GPIO_67	CODEC_SPI_S_CSN	GPIO_108	NC
GPIO_27	NC	GPIO_68	CODEC_SPI_S_CLK	GPIO_109	GPIO109_WSA_R_EN
GPIO_28	CAM2_RSTN	GPIO_69	NC	GPIO_110	NC
GPIO_29	CAM1_STBYN	GPIO_70	LPASS_SLIMBUS_CLK	GPIO_111	GPIO111_WSA_L_EN
GPIO_30	CAM1_RSTN	GPIO_71	LPASS_SLIMBUS_DATA0	GPIO_112	NC
GPIO_31	DLP_L_PROJ_ON	GPIO_72	LPASS_SLIMBUS_DATA1	GPIO_113	UIM_BATT_ALARM
GPIO_32	DLP_R_PROJ_ON	GPIO_73	NC	GPIO_114	NC
GPIO_33	MCU_RST_N	GPIO_74	NC	GPIO_115	CONFIG_PWR_1P8
GPIO_34	6DOF_ULPM	GPIO_75	HARDWARE_ID_1	GPIO_116	NC
GPIO_35	PCIE_RESET_N	GPIO_76	HARDWARE_ID_2	GPIO_117	NC
GPIO_36	PCIE_CLKREQ_N	GPIO_77	HARDWARE_ID_3	GPIO_118	NC
GPIO_37	PCIE_WAKE_N	GPIO_78	NC	GPIO_119	NC
GPIO_38	CC_DIR (GND)	GPIO_79	NC	GPIO_120	PS_INT_N
GPIO_39	USB_BRIDGE_RESET_N	GPIO_80	NC	GPIO_121	NC
GPIO_40	6DOFR_STROBE	GPIO_81	MCU_SPI1_MOSI	GPIO_122	NC

GPIO_123	NC
GPIO_124	ALS_INT_N
GPIO_125	NC
GPIO_126	NC
GPIO_127	GRFC3_MDM
GPIO_128	NC
GPIO_129	NC
GPIO_130	NC
GPIO_131	NC
GPIO_132	NC
GPIO_133	NC
GPIO_134	NC
GPIO_135	NC
GPIO_136	NC

GPIO_137	NC
GPIO_138	NC
GPIO_139	NC
GPIO_140	NC
GPIO_141	NC
GPIO_142	NC
GPIO_143	ANX7530_1P0_EN
GPIO_144	NC
GPIO_145	NC
GPIO_146	PCIE_PWR_EN
GPIO_147	NC
GPIO_148	6DOFL_SHUTDOWN_L
GPIO_149	6DOFR_SHUTDOWN_R

PMI8998 GPIO Configuration for Irongate HMD

GPIO_1	NC	GPIO_6	NC	GPIO_11	NC
GPIO_2	NC	GPIO_7	NC	GPIO_12	DIV_CLK3
GPIO_3	NC	GPIO_8	NC	GPIO_13	NC
GPIO_4	NC	GPIO_9	GND	GPIO_14	NC
GPIO_5	NC	GPIO_10	NC		

PM8998 GPIO Configuration for Irongate HMD

GPIO_1	UIM_BATT_ALARM	GPIO_12	NC	GPIO_23	NC
GPIO_2	NC	GPIO_13	NC	GPIO_24	Option
GPIO_3	NC	GPIO_14	DIV_CLK2	GPIO_25	Option
GPIO_4	SSC_PWR_EN	GPIO_15	NC	GPIO_26	PM_SLB
GPIO_5	NC	GPIO_16	DIV_CLK3		
GPIO_6	VOL_UP_N	GPIO_17	NC		
GPIO_7	NC	GPIO_18	NC		
GPIO_8	NC	GPIO_19	NC		
GPIO_9	NC	GPIO_20	CAM_REAR_ON		
GPIO_10	NC	GPIO_21	NC		
GPIO_11	NC	GPIO_22	NC		

WCD9341 GPIO Configuration for Irongate HMD

GPIO_0	GND	GPIO_2	WSA_R_EN	GPIO_4	GND
GPIO_1	WSA_L_EN	GPIO_3	GND		

GPIO TABLE

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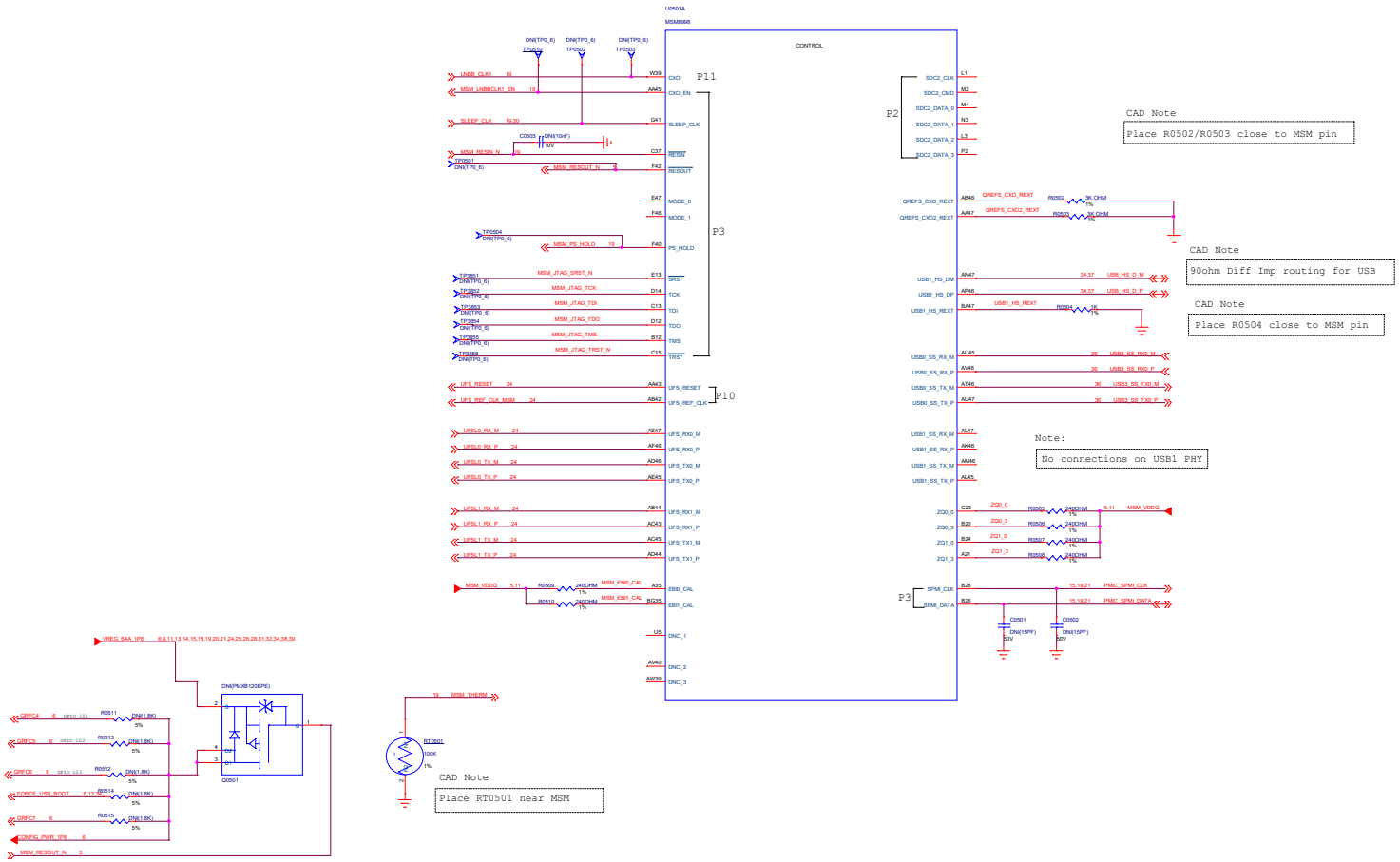

CAD Note

Place RT0501 near MSM

GPIO#	BOOT_CONFIG
GPIO_101	NOOD 0 = Enable 1 = Disable
GPIO_102	BOOT_CONFIG[1]
GPIO_103	BOOT_CONFIG[2]
GPIO_104	BOOT_CONFIG[3]
GPIO_114	BOOT_CONFIG[4]

BOOT_CONFIG[4:1]	BOOT_CONFIG
0b0000(this design)	UFS-> SD SDC2 -> SS/HS/FS USB on USB3.1
0b0001	SD SDC2 -> UFS
0b0010	SDC2
0b0011	SS/HS/FS USB on USB3.1

MSM8998 CONTROL

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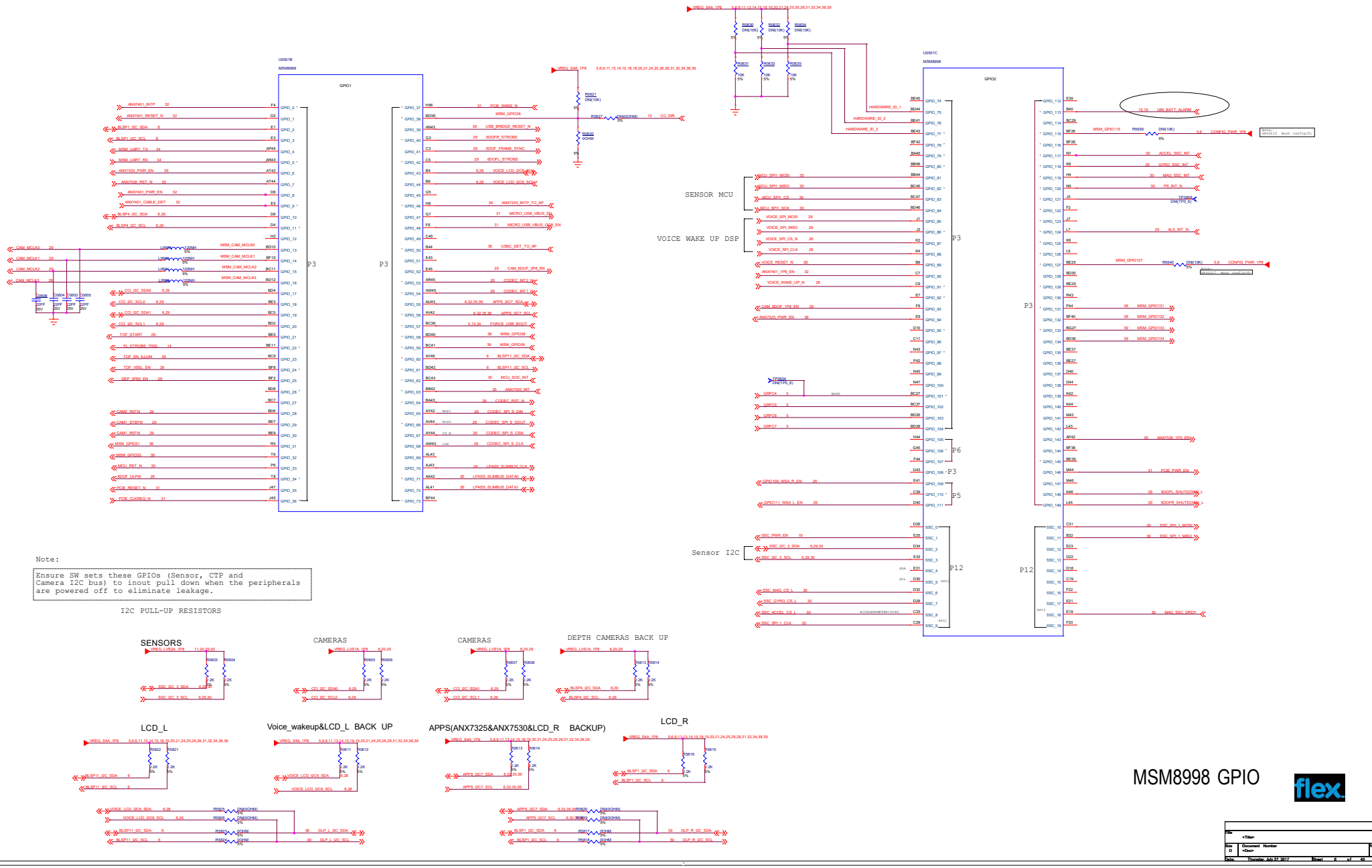
U0501B
MSM8998
GPIO1
P3
U0501C
GPIO2
SENSOR MCU
VOICE WAKE UP DSP
Sensor I2C
Note:
Ensure SW sets these GPIOs (Sensor, CTP and Camera I2C bus) to inout pull down when the peripherals are powered off to eliminate leakage.
I2C PULL-UP RESISTORS
SENSORS
CAMERAS
CAMERAS
DEPTH CAMERAS BACK UP
LCD_L
Voice_wakeup&LCD_L BACK UP
APPS(ANX7325&ANX7530&LCD_R BACKUP)
LCD_R
MSM8998 GPIO
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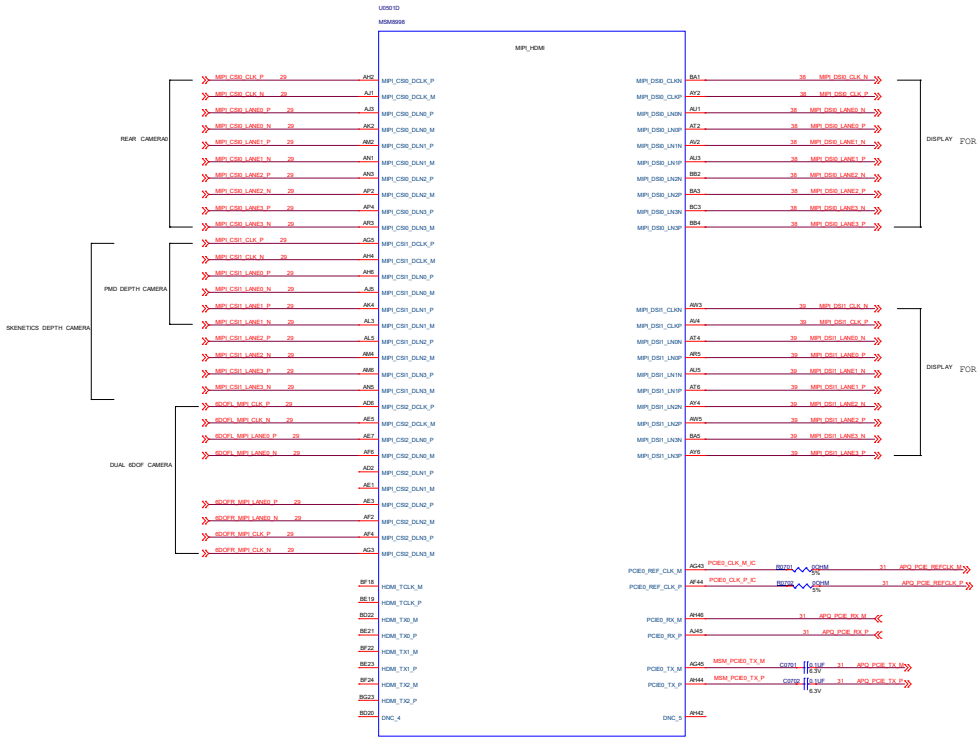

Note:

If best EMI practices are followed for MIPI CSI/DSI signals, there is no need for common mode choke filters. You may choose to have placeholders for common mode depending upon your design constraints.
Extreme care must be taken that no stubs are created by doing so.

MSM8998 MIPI CSI DSI/RF INTERFACE

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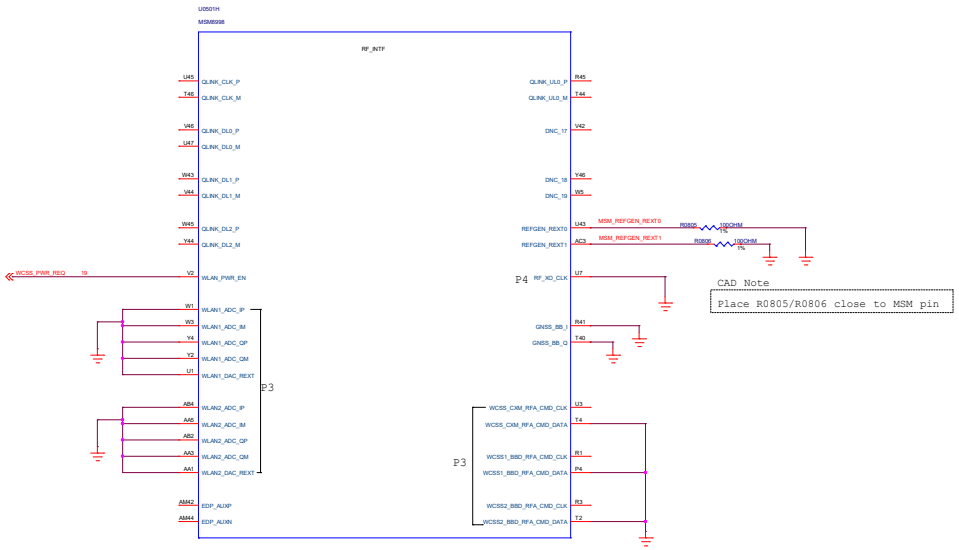

MSM8998 RF

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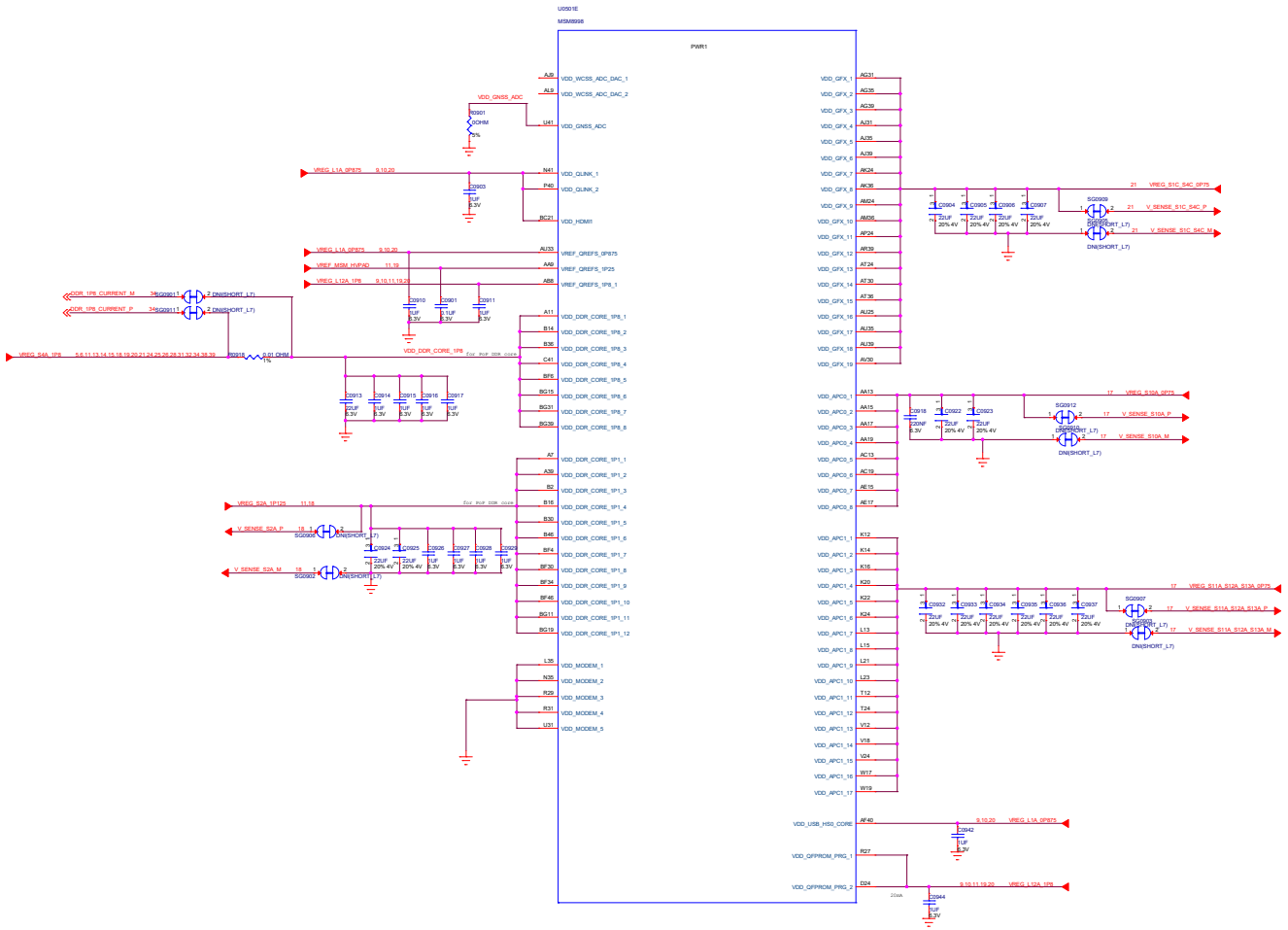

MSM8998 POWER

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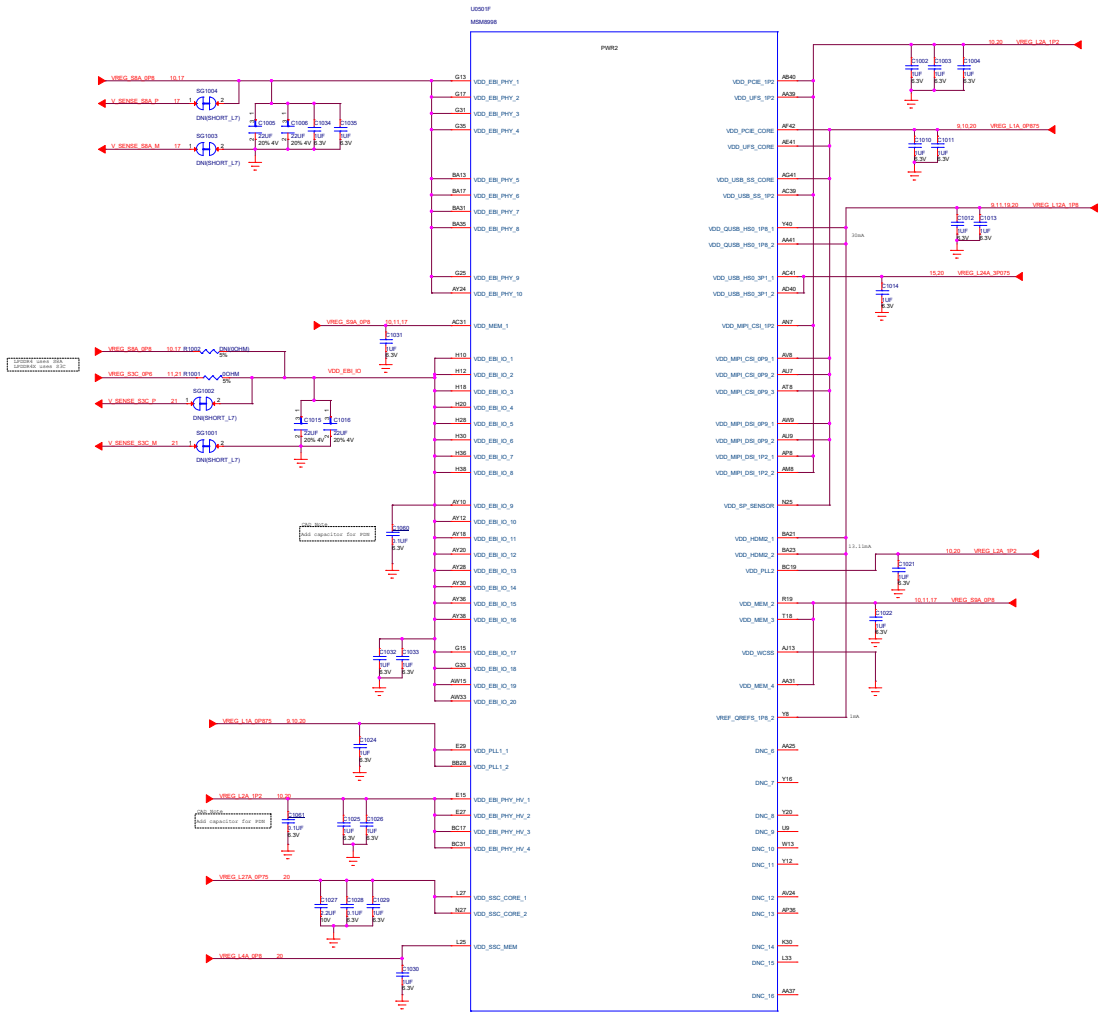

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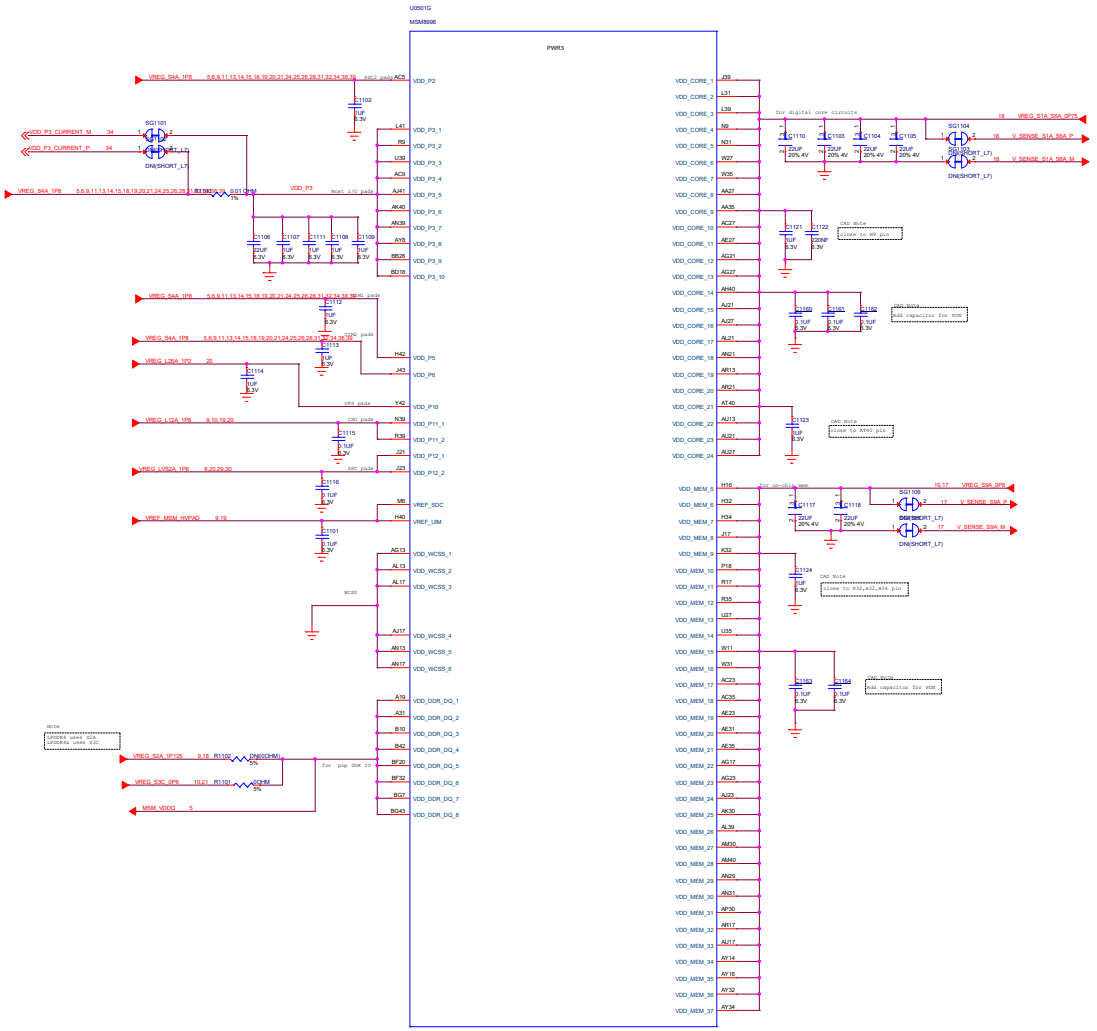

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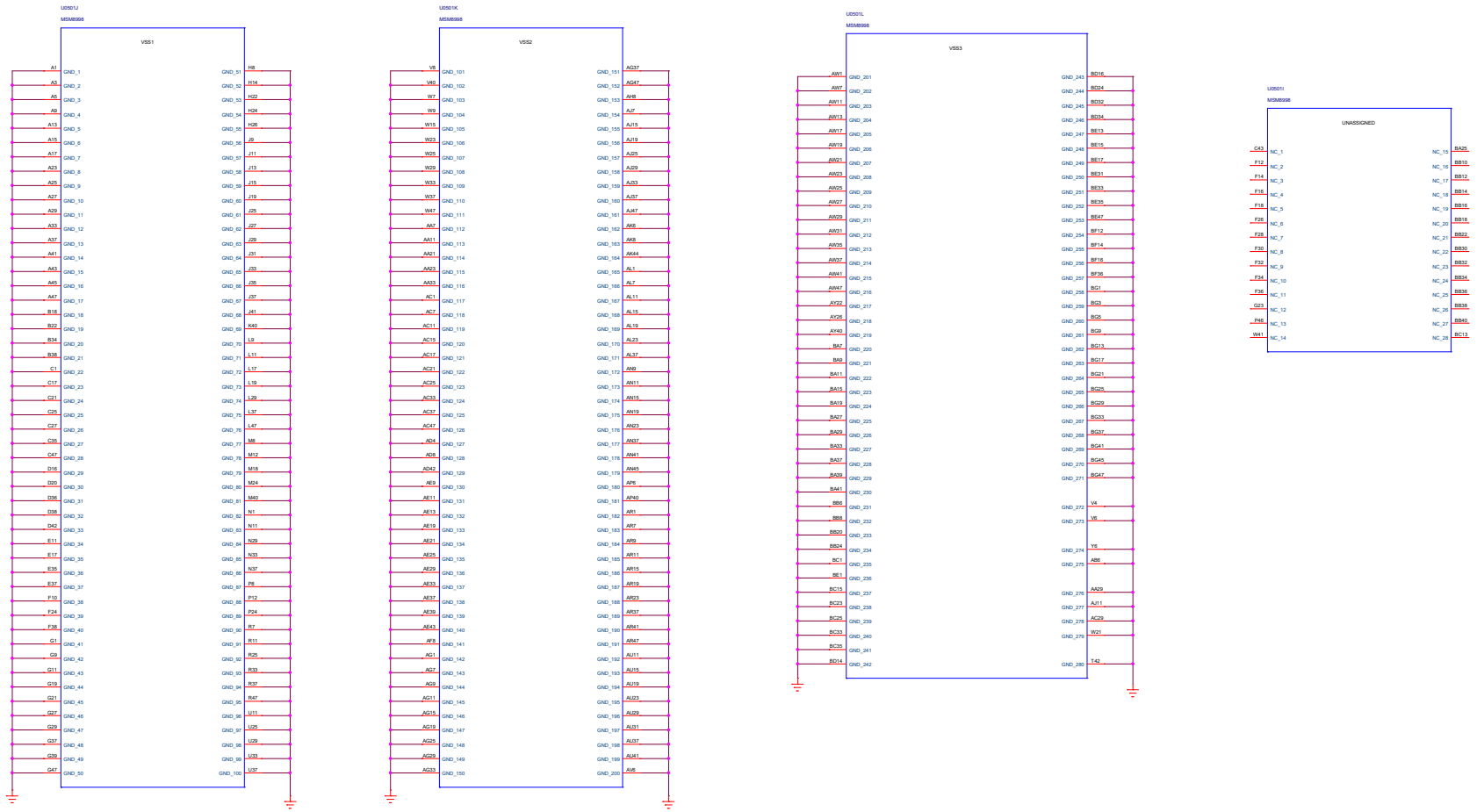

MSM8998 GND

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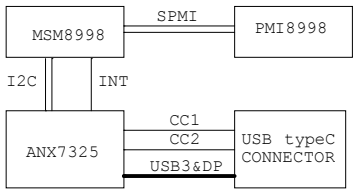
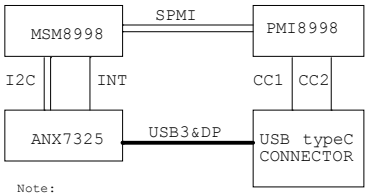
USB TYPEC MAIN SOLUTION



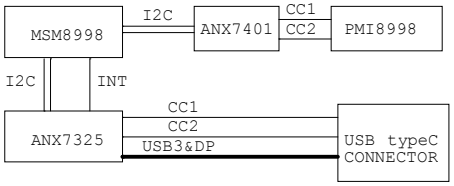
Note:
1.PMI8998 working under uUSB mode
2.Connect GPIO4 of PMI8998 to GND

USB TYPEC BACKUP SOLUTION 1

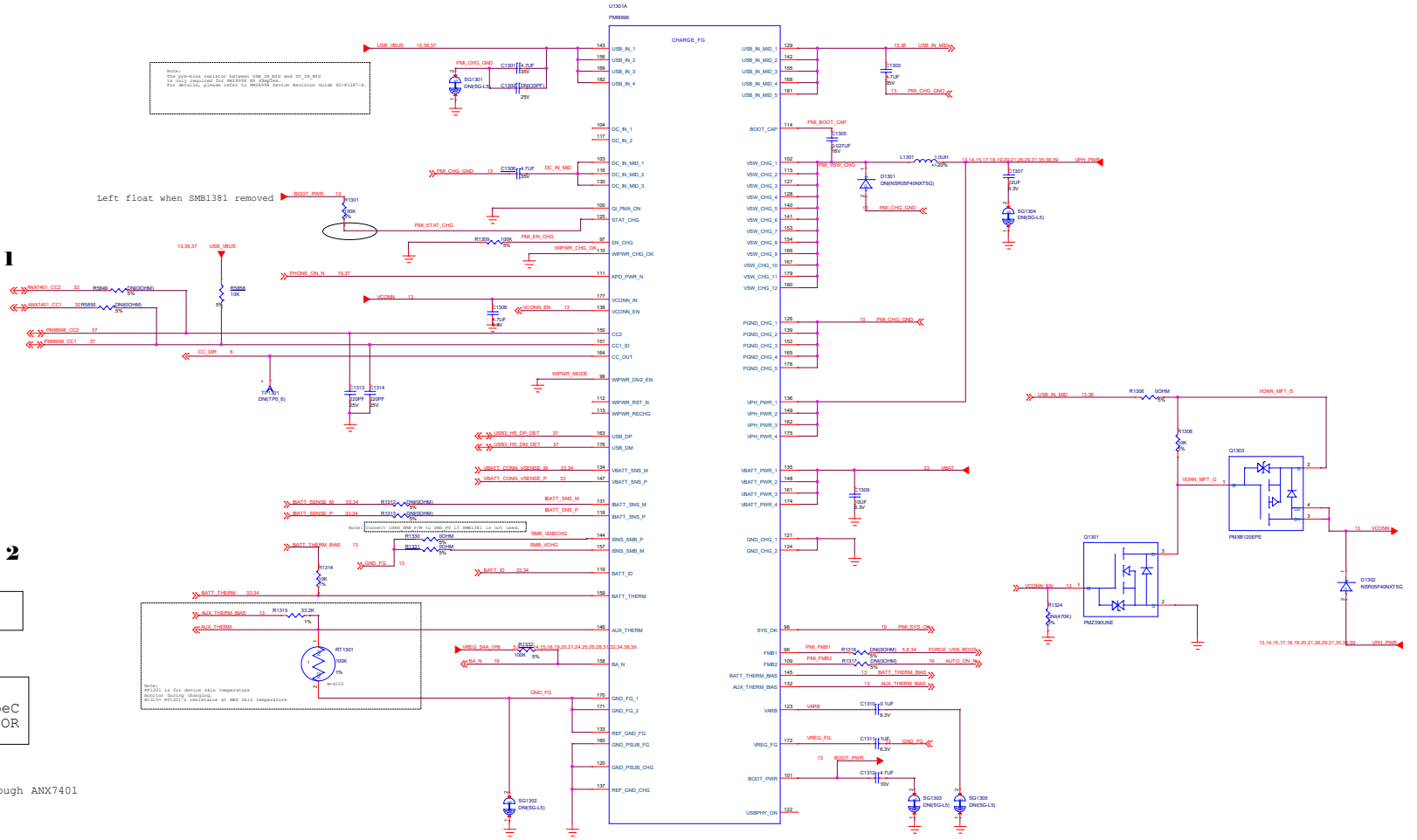


Note:
1.PMI8998 working under TypeC mode
2.Float PMI8998 GPIO4
3.PMI8998 transfer DP ALT infromation to ANX7325 through MSM8998

USB TYPEC BACKUP SOLUTION 2



Note:
1.PMI8998 working under TypeC mode
2.Float PMI8998 GPIO4
3.ANX7325 forward the PD information to PMI8998 through ANX7401



PMI8998_Charge_FG

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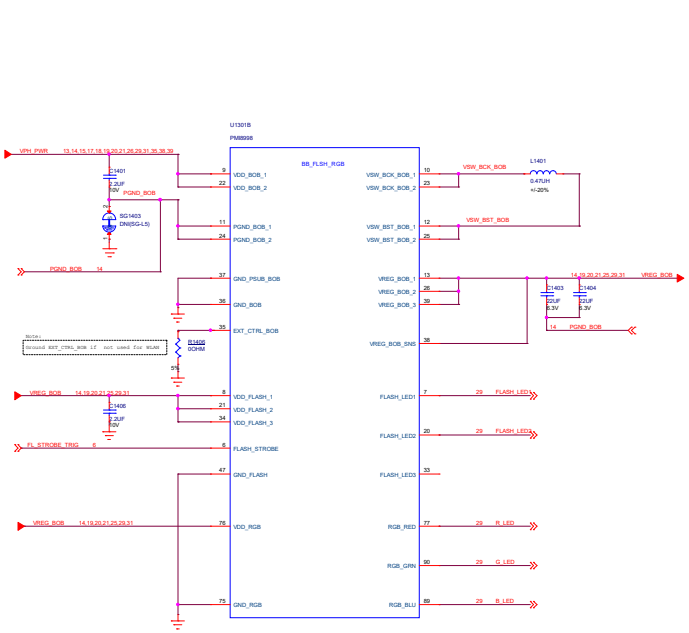

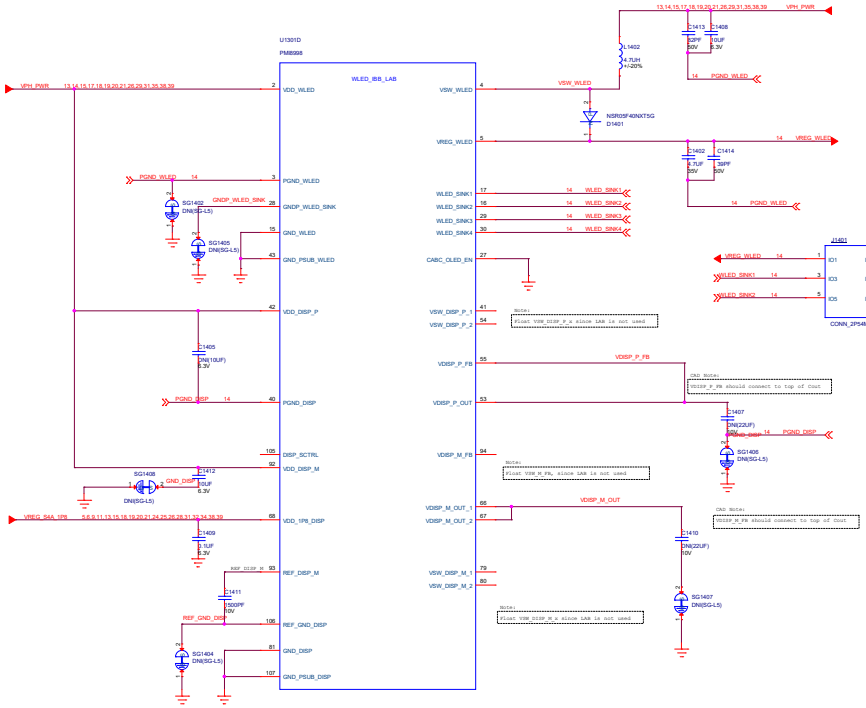

PMI8998_Buck_Boost_Flash

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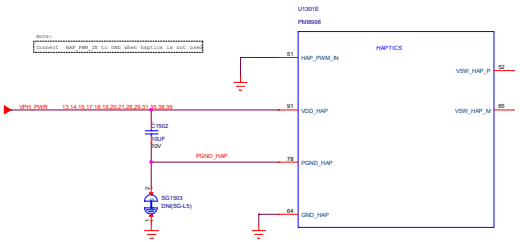

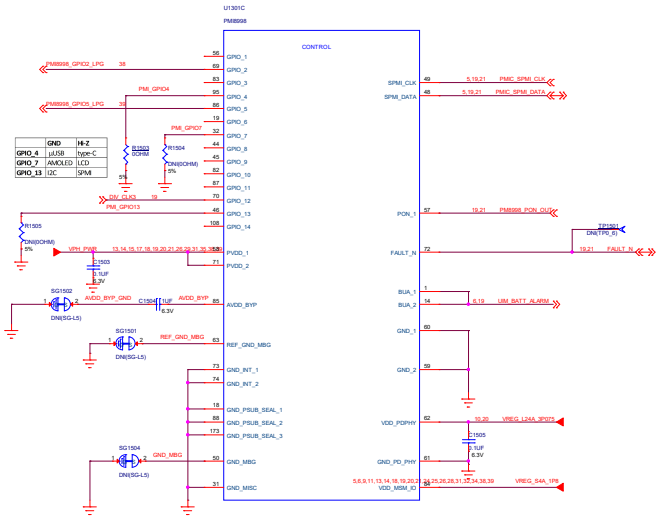

PMi8998 CLKS_GPIO

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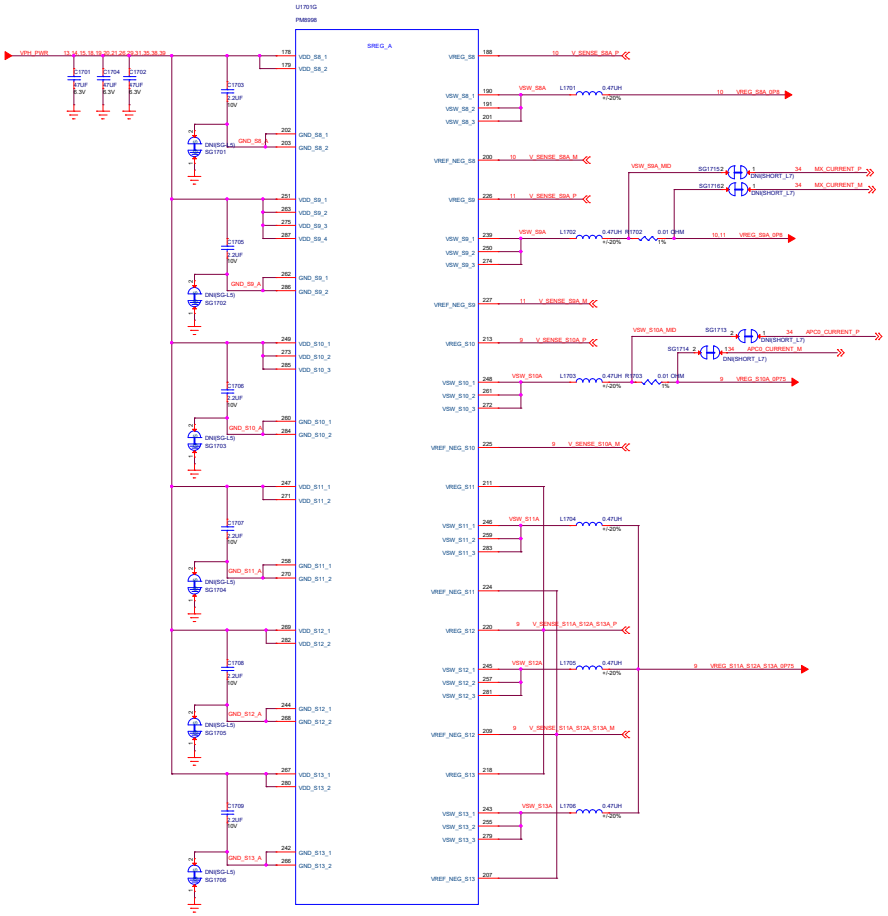

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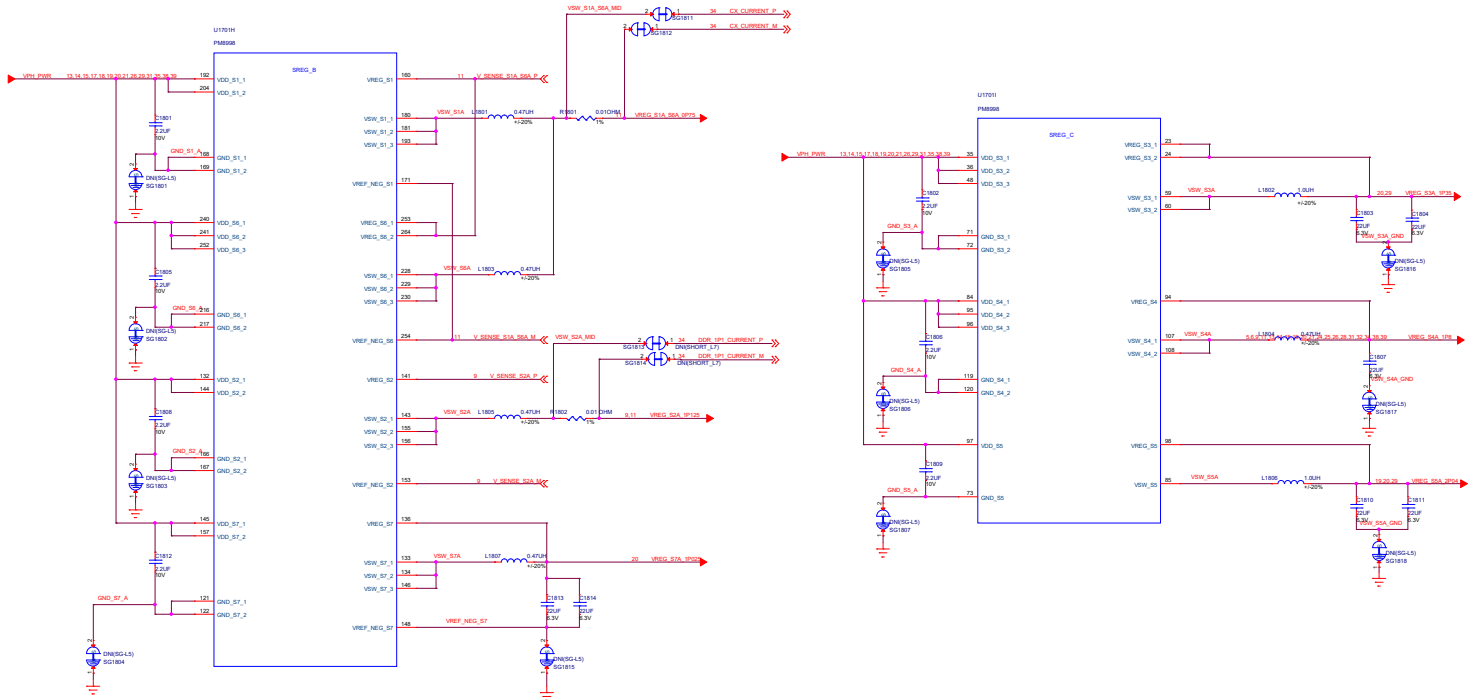

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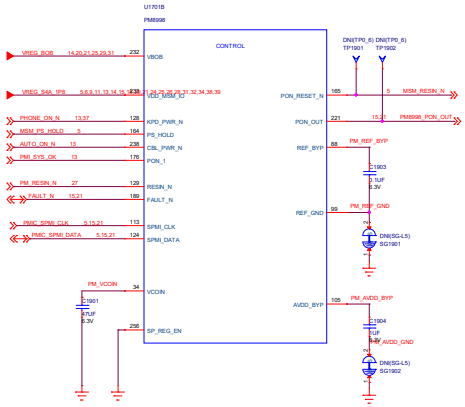
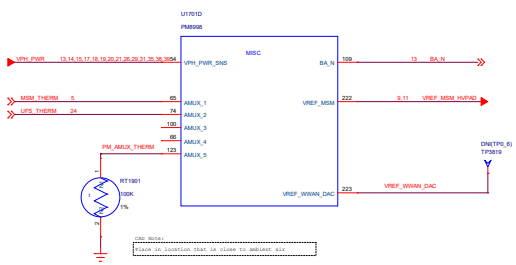
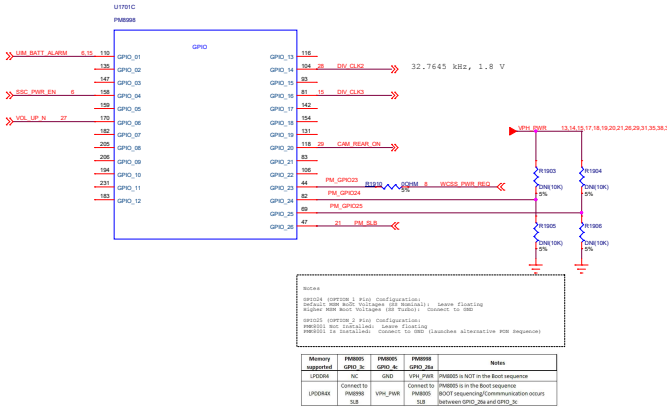
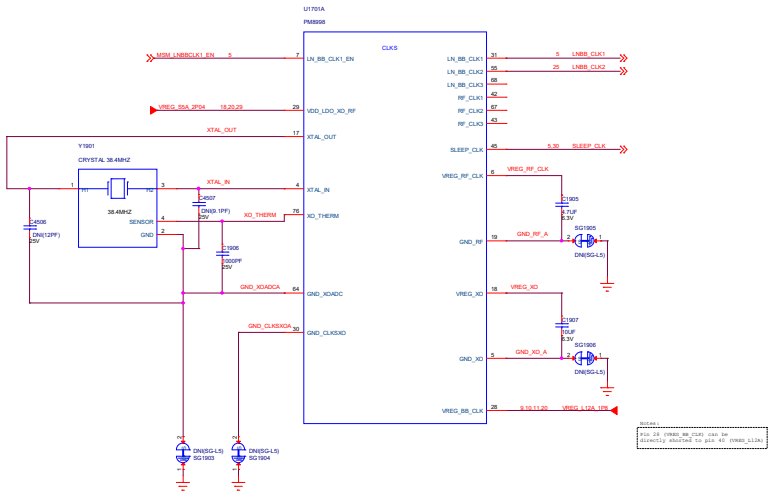
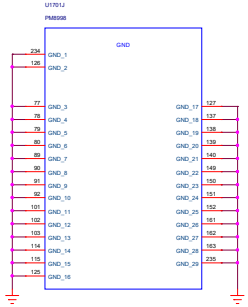


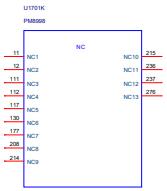




Memory supported	PM8005 GPIO_3c	PM8005 GPIO_4c	PM8998 GPIO_26a	Notes
LPDDR4	NC	GND	VPH_PWR	PM8005 is NOT in the Boot sequence
LPDDR4X	Connect to PM8998 S1B	VPH_PWR	Connect to PM8005 S1B	PM8005 is in the Boot sequence BOOT sequencing/Communication occurs between GPIO_26a and GPIO_3C







PM8998 Control

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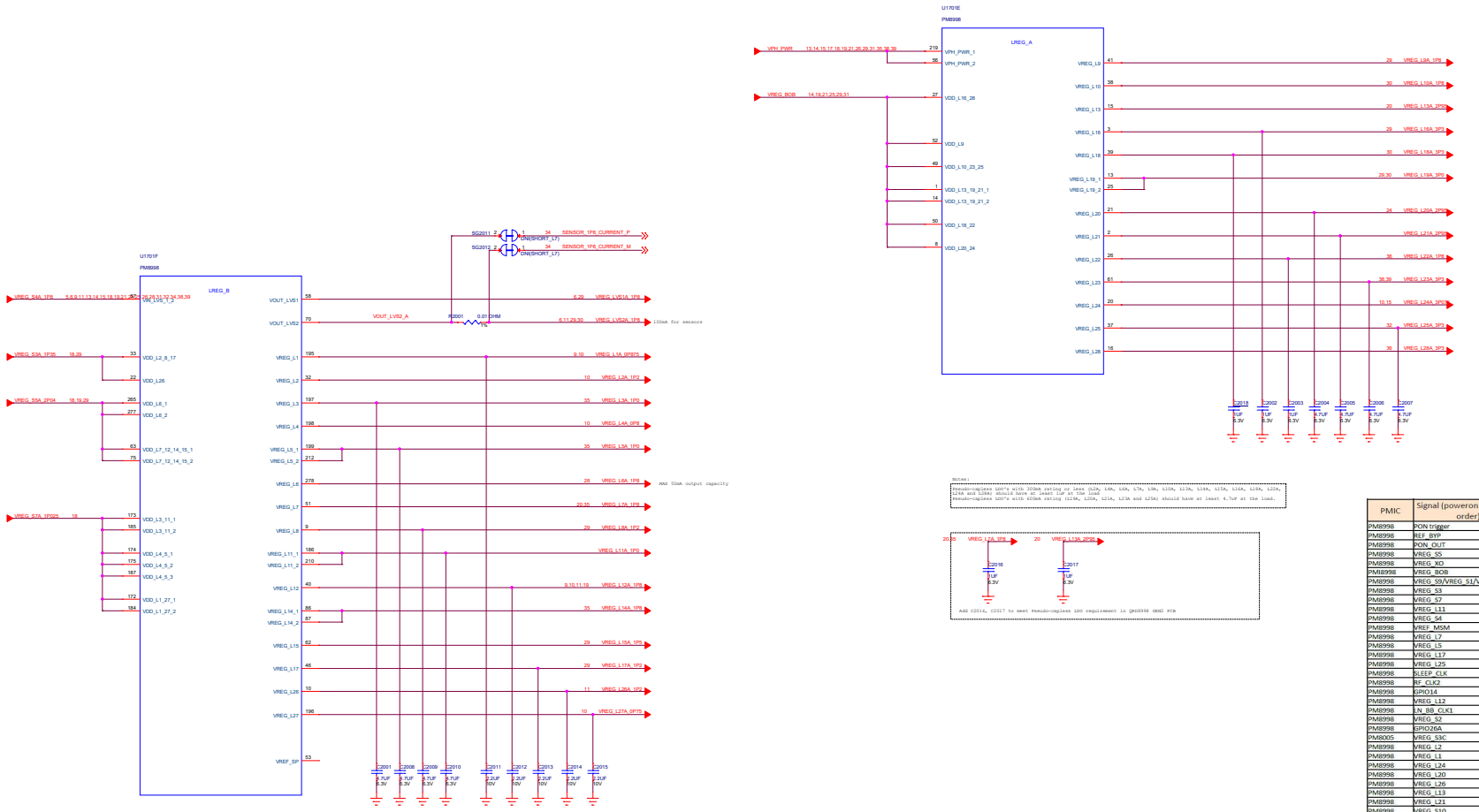

Notes:
Pseudo-capless LDO's with 300mA rating or less (L2A, L4A, L7A, L9A, L10A, L13A, L14A, L15A, L16A, L18A, L20A, L24A and L28A) should have at least 1uF at the load.
Pseudo-capless LDO's with 600mA rating (L19A, L20A, L23A and L25A) should have at least 4.7uF at the load.

PMIC	Signal (poweron sequential order)
PM8998	PON trigger
PM8998	REF_BYP
PM8998	PON_OUT
PM8998	VREG_S5
PM8998	VREG_XO
PM8998	VREG_BOB
PM8998	VREG_S9/VREG_S1/VREG_S8
PM8998	VREG_S3
PM8998	VREG_S7
PM8998	VREG_L11
PM8998	VREG_S4
PM8998	VREF_MSM
PM8998	VREG_L7
PM8998	VREG_L5
PM8998	VREG_L17
PM8998	VREG_L25
PM8998	SLEEP_CLK
PM8998	RF_CLK2
PM8998	GPIO14
PM8998	VREG_L12
PM8998	LN_BB_CLK1
PM8998	VREG_S2
PM8998	GPIO26A
PM8005	VREG_S3C
PM8998	VREG_L2
PM8998	VREG_L1
PM8998	VREG_L24
PM8998	VREG_L20
PM8998	VREG_L26
PM8998	VREG_L13
PM8998	VREG_L21
PM8998	VREG_S10
PM8998	PON_RESET_N

PM8998 LDO

flex

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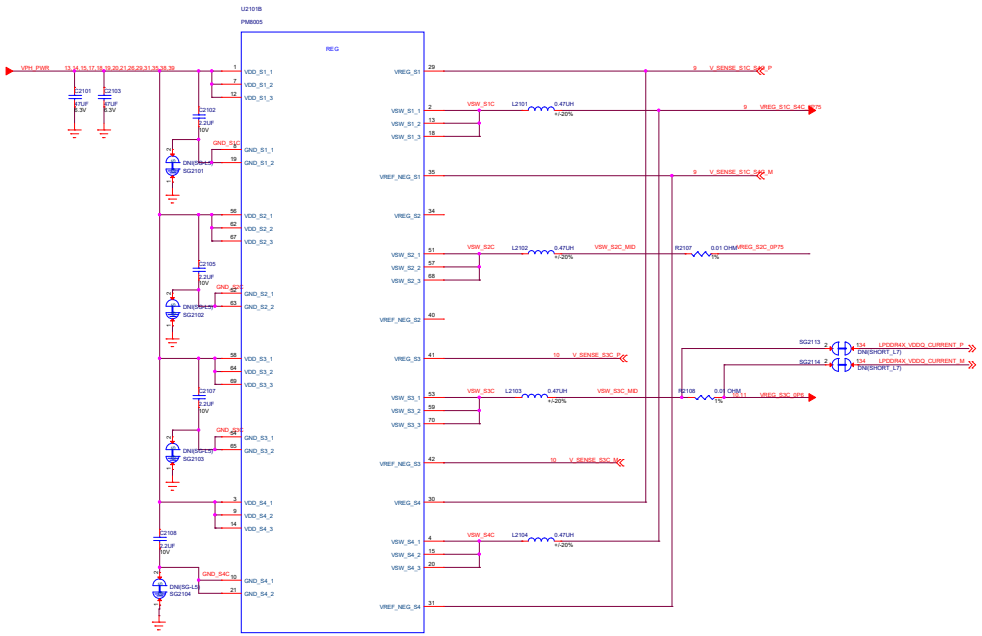
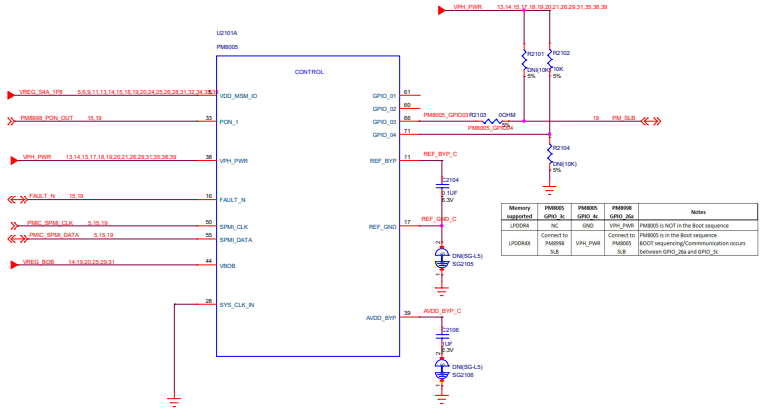
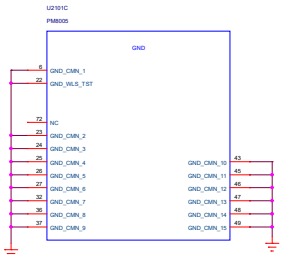




Memory supported	PM8005 GPIO_3c	PM8005 GPIO_4c	PM8998 GPIO_26a	Notes
LPDDR4	NC	GND	VPH_PWR	PM8005 is NOT in the Boot sequence
LPDDR4X	Connect to PM8998 S.8	VPH_PWR	Connect to PM8005 BOOT sequencing/Communication occurs between GPIO_26a and GPIO_3c	PM8005 is in the Boot sequence



PM8005

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Reserved Page

LPDDR4x

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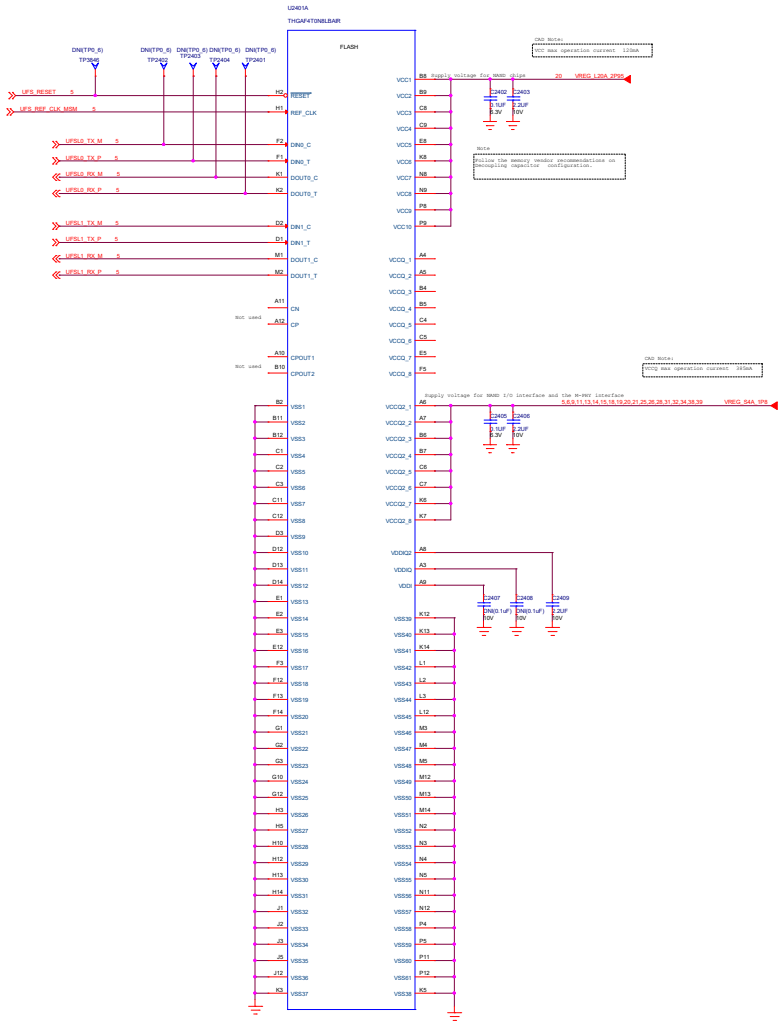

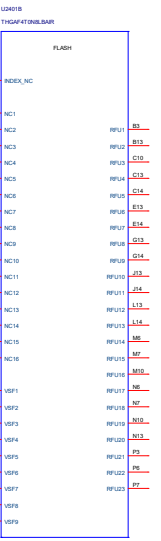

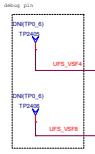

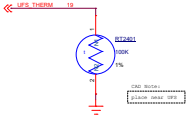

MEMORY UFS

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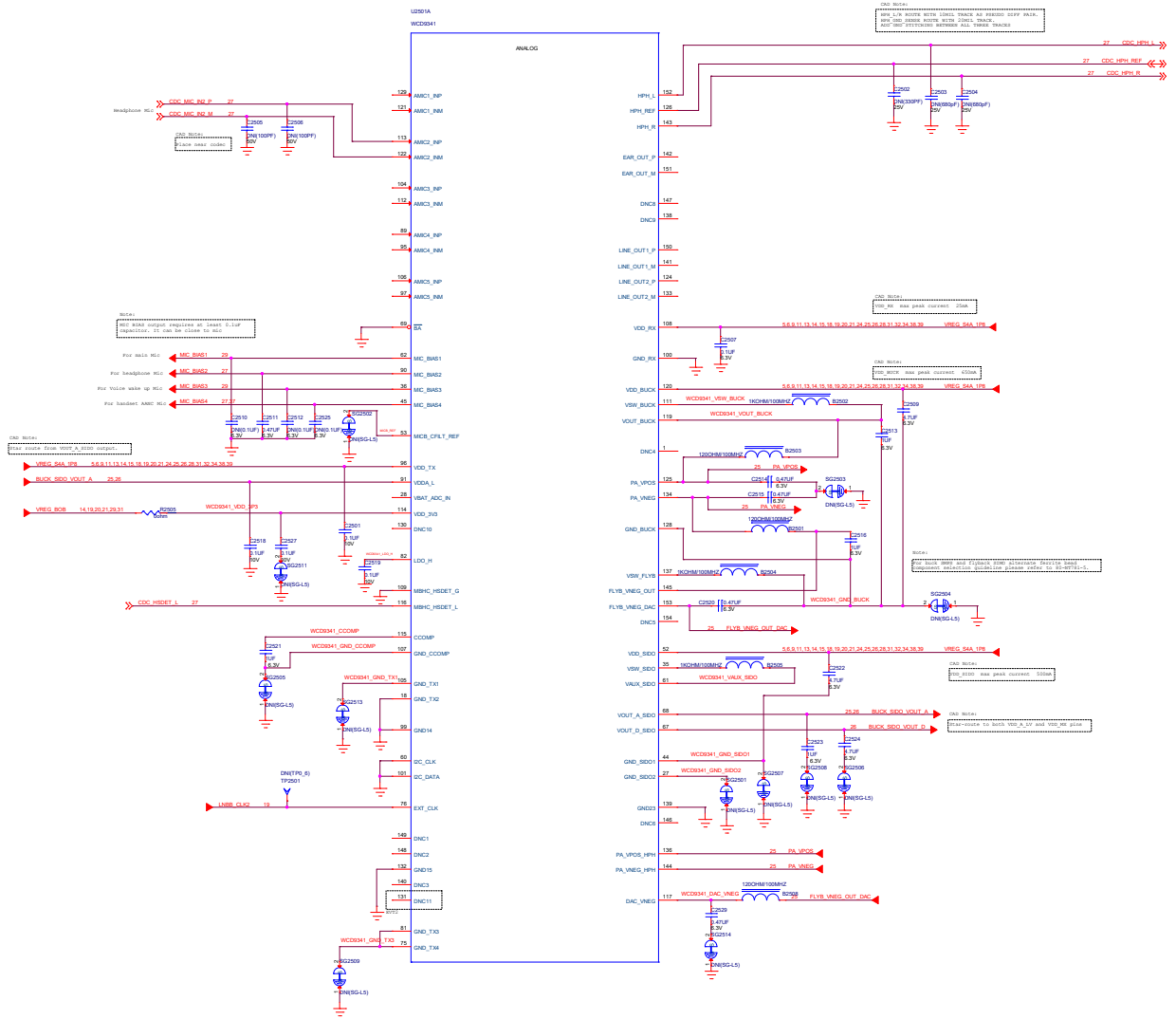

WCD9341 ANALOG

flex

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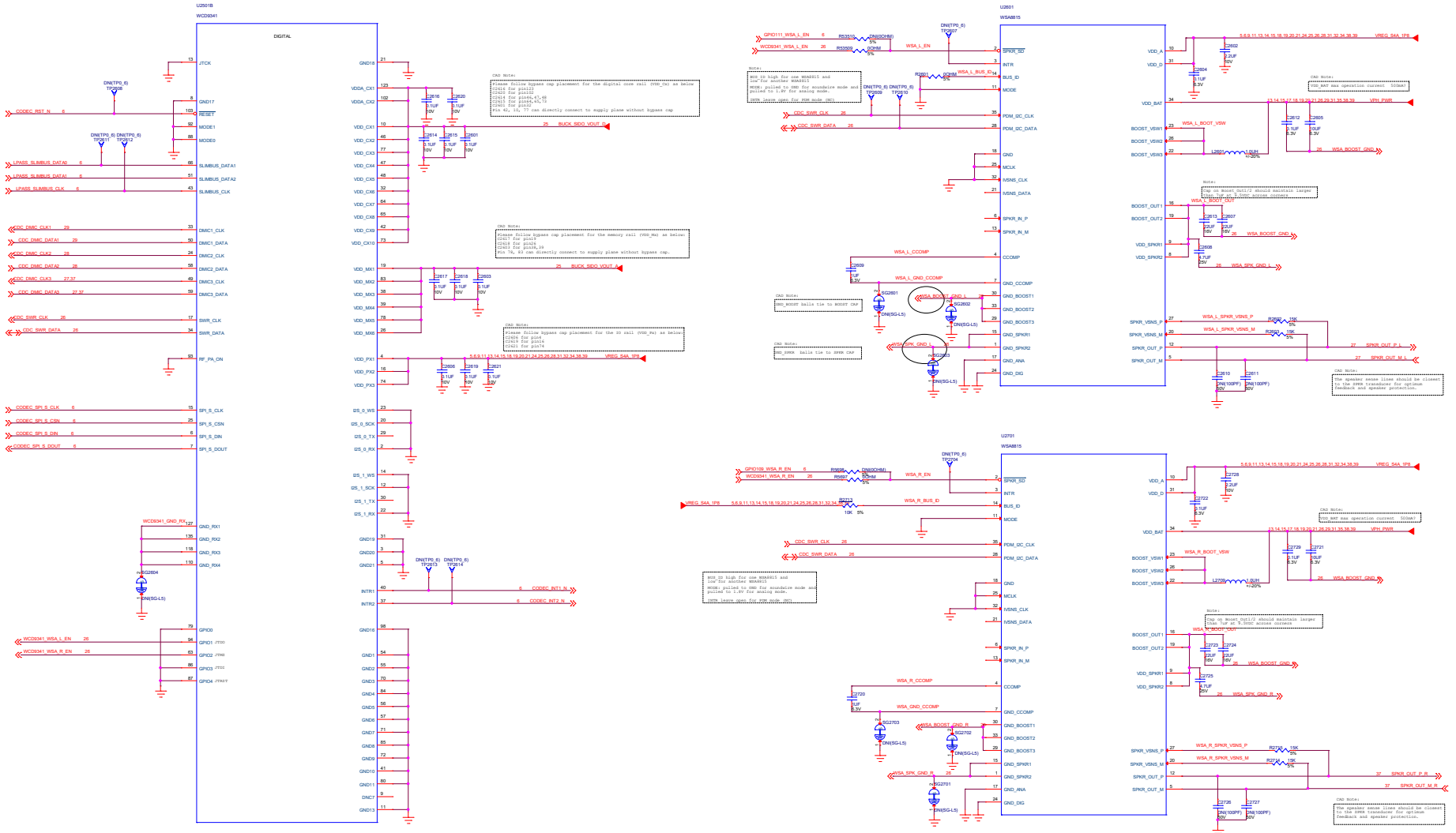
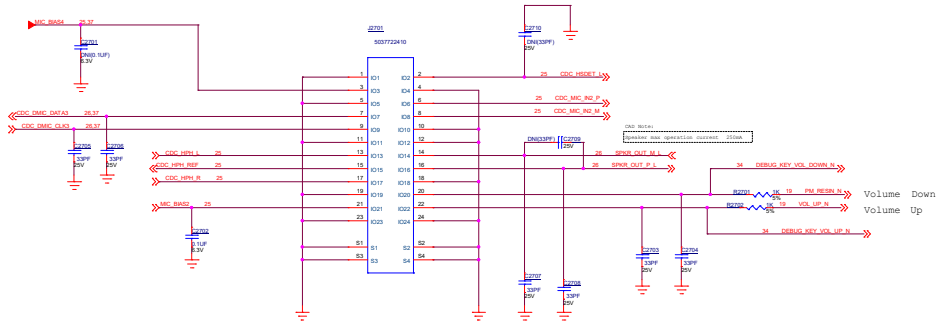

U2501B
WCD9341
DIGITAL
JTCK
RESET
MODE1
MODE0
SLIMBUS_DATA1
SLIMBUS_DATA2
SLIMBUS_CLK
DMIC1_CLK
DMIC1_DATA
DMIC2_CLK
DMIC2_DATA
DMIC3_CLK
DMIC3_DATA
SWR_CLK
SWR_DATA
RF_PA_ON
SPI_S_CLK
SPI_S_CSN
SPI_S_DIN
SPI_S_DOUT
GND_RX1
GND_RX2
GND_RX3
GND_RX4
GPIO0
GPIO1 JTDO
GPIO2 JTMS
GPIO3 JTDI
GPIO4 JTRST
I2S_0_WS
I2S_0_SCK
I2S_0_TX
I2S_0_RX
I2S_1_WS
I2S_1_SCK
I2S_1_TX
I2S_1_RX
INTR1
INTR2
U2601
WSA8815
U2701
WSA8815
WCD9341 DIGITAL/WSA



Headphone board connector

flex

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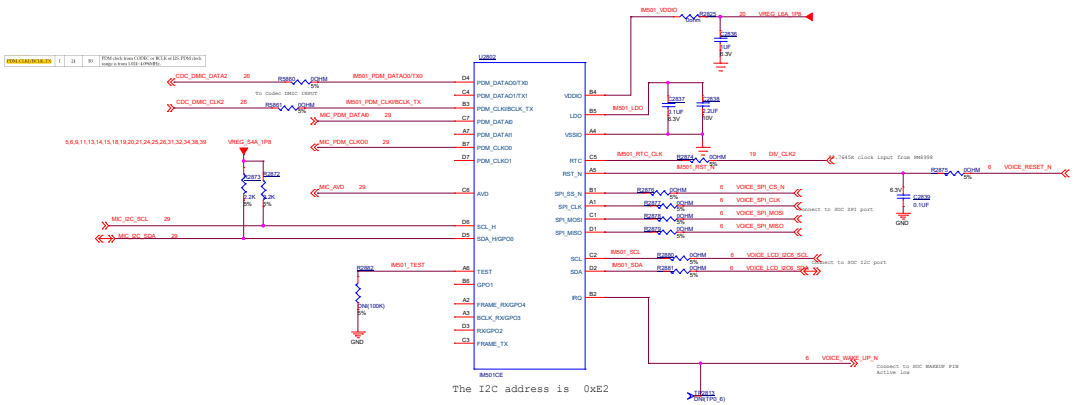

Voice wake up DSP

flex

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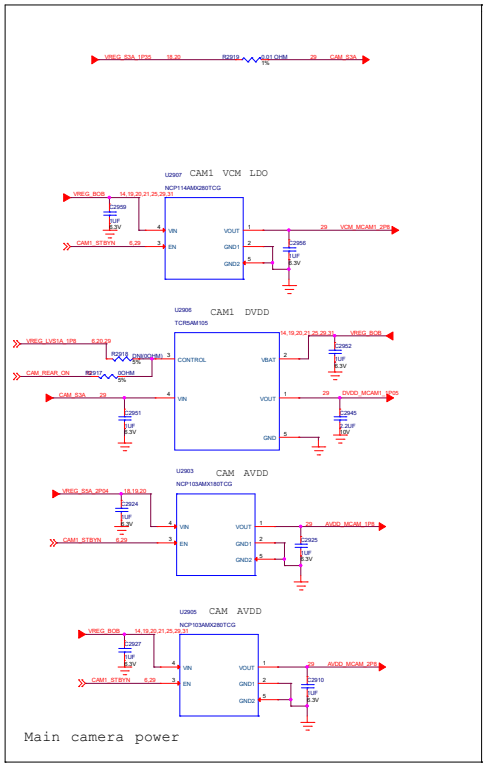
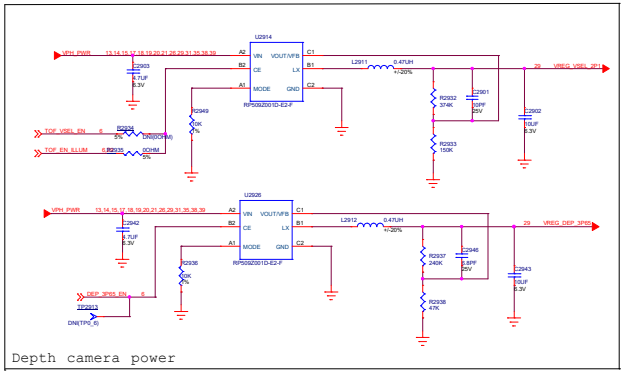
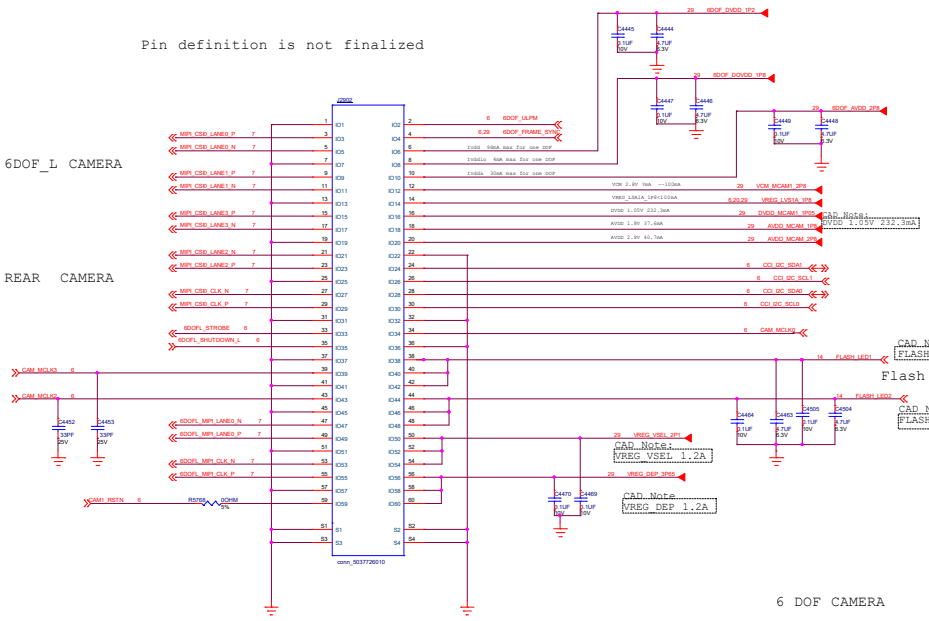




Pin definition is not finalized

6DOF_L CAMERA

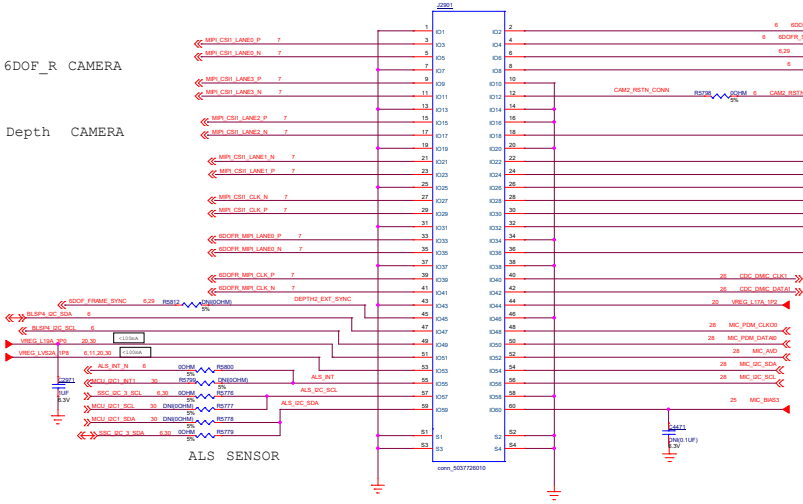
REAR CAMERA

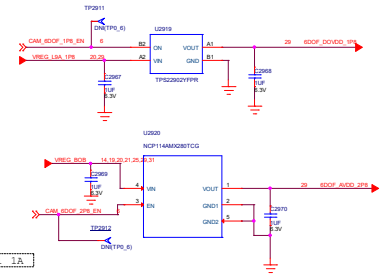


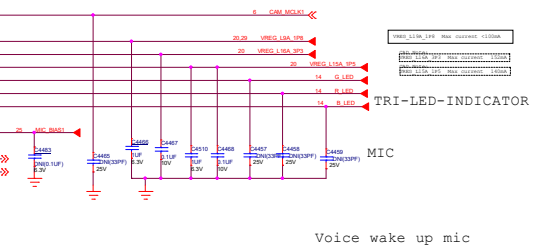
Pin definition is not finalized

6DOF_R CAMERA

Depth CAMERA







CAMERA BOARD CONNECTOR

flex

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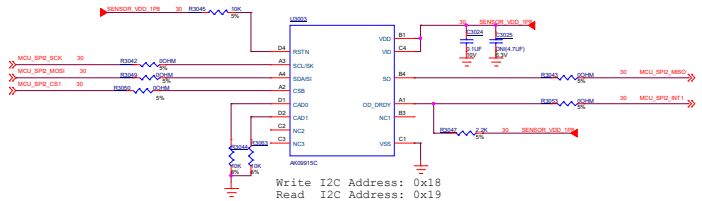
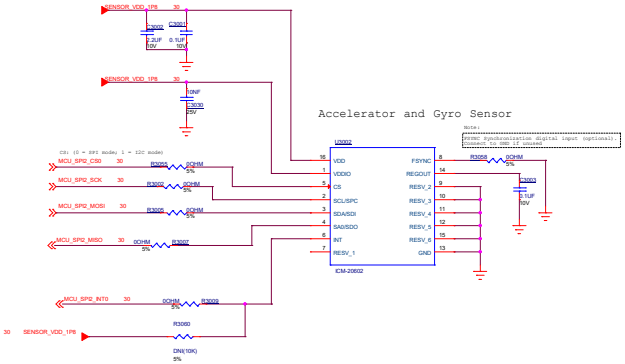
Sensors

Magnetic Sensor

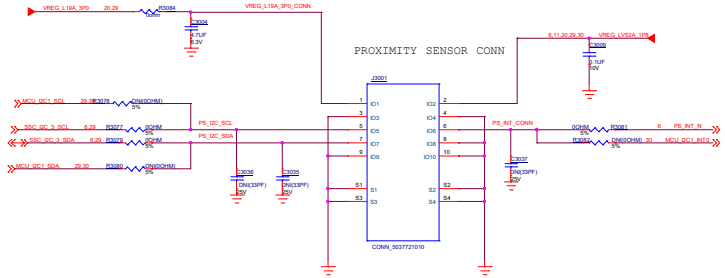


Write I2C Address: 0x18
Read I2C Address: 0x19

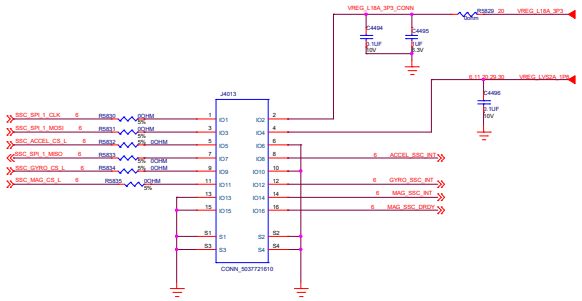
Accelerator and Gyro Sensor



ALS sensor on camera board



9axis sensor BMX055 on camera board

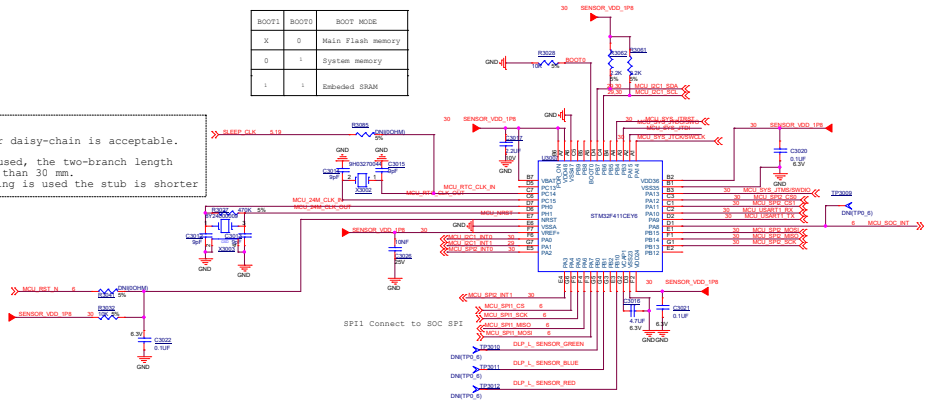


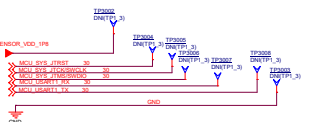
BOOT1	BOOT0	BOOT MODE
X	0	Main Flash memory
0	1	System memory
1	1	Embeded SRAM

CAD Note

SLEEP_CLK .
Either star routing or daisy-chain is acceptable.

- If star routing is used, the two-branch length difference is shorter than 30 mm.
- If daisy-chain routing is used the stub is shorter than 7 mm.





SENSORS&MCU

flex

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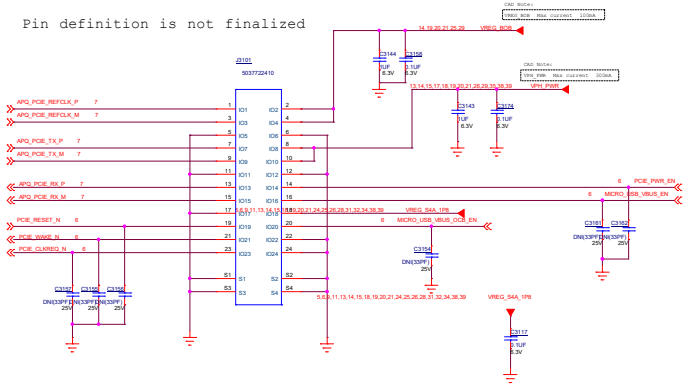

PCIE to USB Bridge Conn

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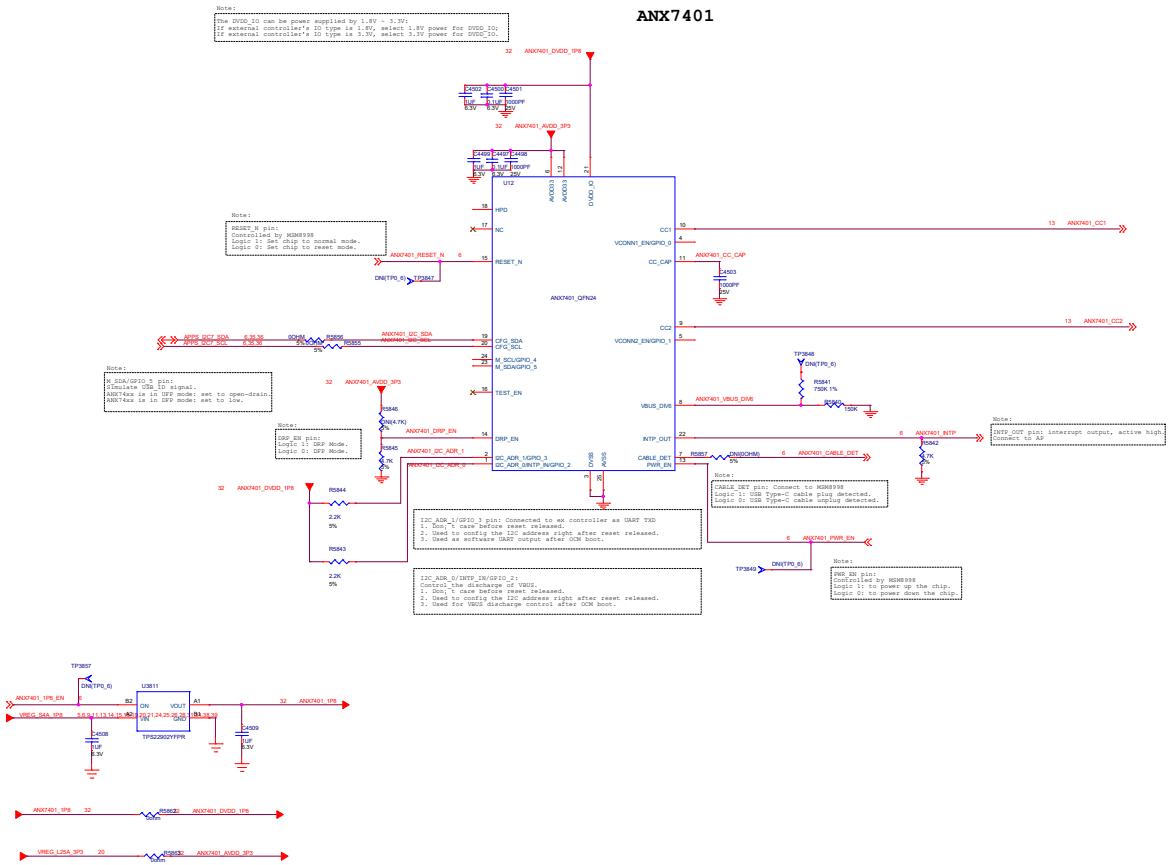

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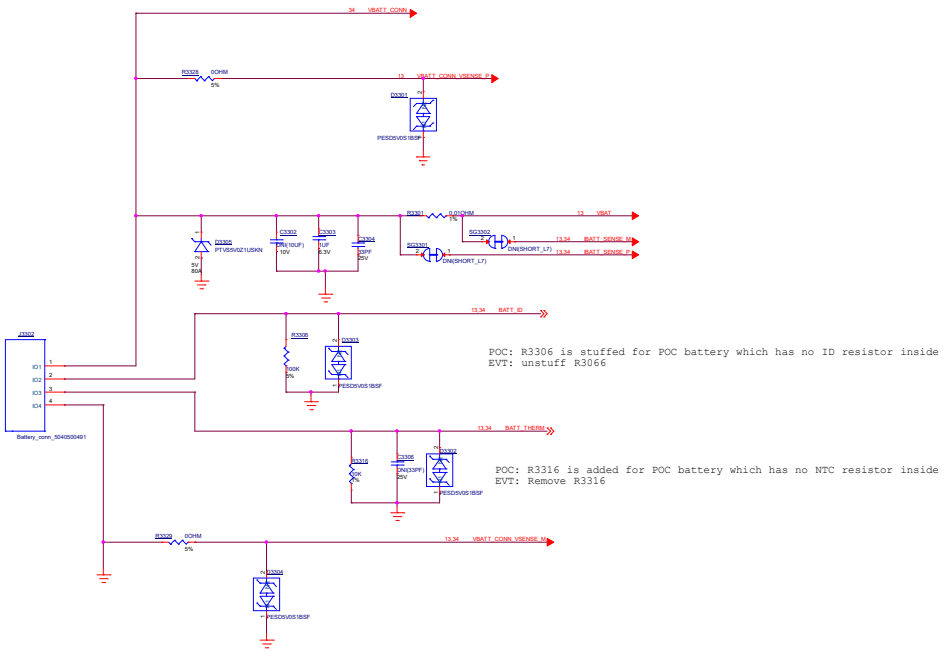
Sub Battery CONN

The battery connector pin definition is not finalized



POC: R3306 is stuffed for POC battery which has no ID resistor inside
EVT: unstuff R3066

POC: R3316 is added for POC battery which has no NTC resistor inside
EVT: Remove R3316

Sub Battery CONN

flex

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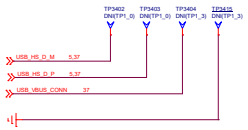
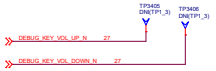
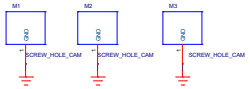
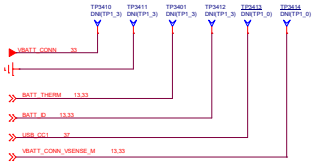
Test Point

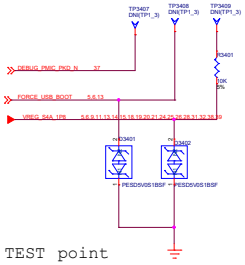




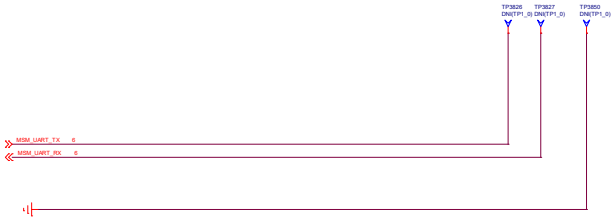


Screw hole



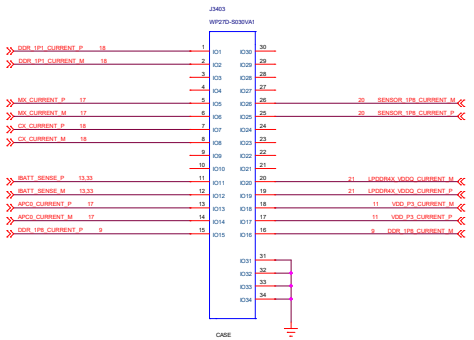


PCBA AUTOMATIC TEST point



UART TP

RCM CONNECTOR



Test point/GND/Shields

flex

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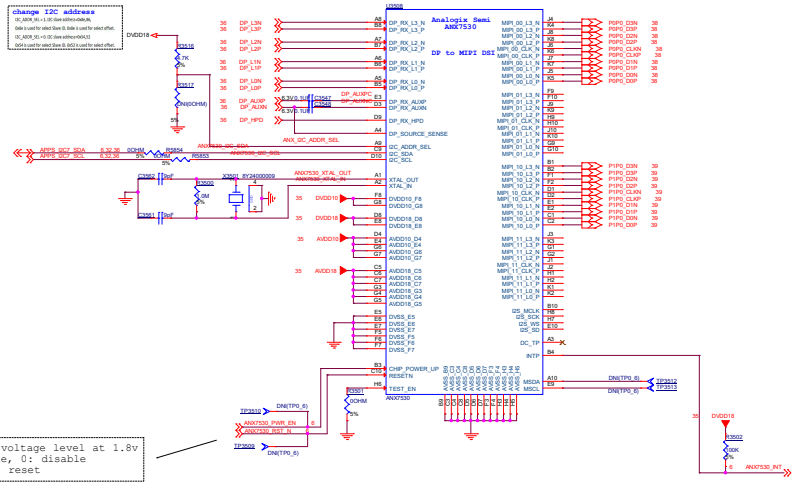
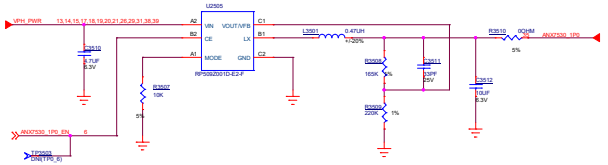
ANX7530



Note

From MSM8998, input voltage level at 1.8v
Pwr_Enable: 1: enable, 0: disable
Rst_N: 1: Normal, 0: reset



CAD Note

Decouping capacitors close to ANX7530 PIN

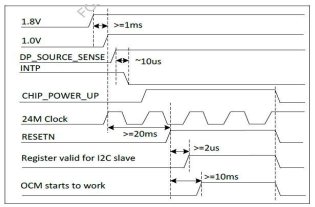
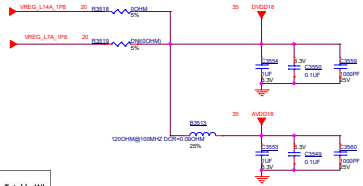


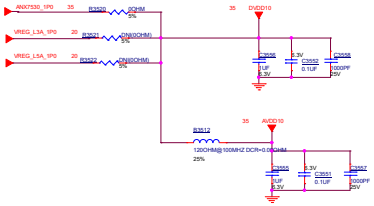
Table 6-6 Power Consumption in Active Mode

Input Video Clock	Current (mA)				Total (mW)
	AVDD10	AVDD18	DVDD18	DVDD10	
390MHz	178.00	77.00	1.00	88.00	406.40
524MHz	175.00	78.00	1.00	94.00	411.20
619MHz	175.00	78.00	1.00	101.00	418.20



CAD Note

DVDD10 &AVDD10 276mA



DP to MIPI Bridge ANX7530

flex

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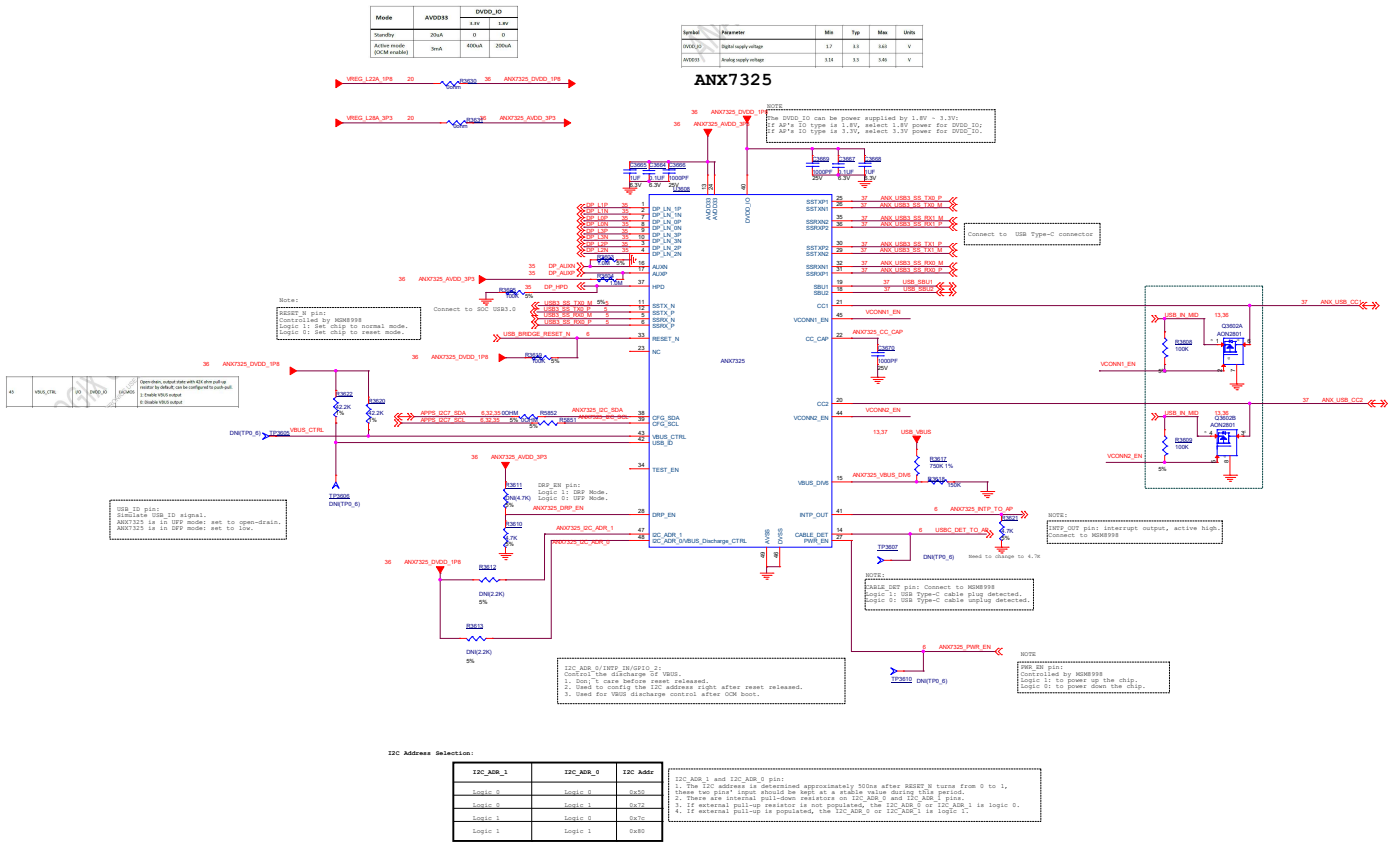

USB TYPEC BRIDGE ANX7325

flex

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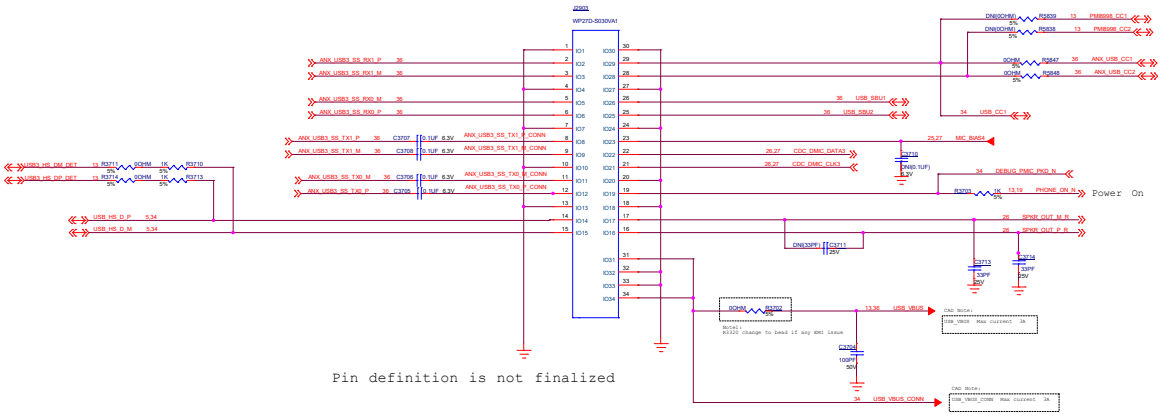
CAD Note:
Ensure R3710 and R3713 isolation resistor placed close to the Sub board connector.

Note:
To reduce the capacitive loading of DP/DM lines if required
change R3711 and R3714 to ferrite beads



Pin definition is not finalized

USB typeC board connector

flex

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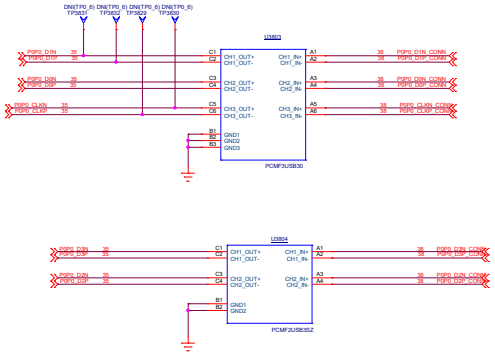
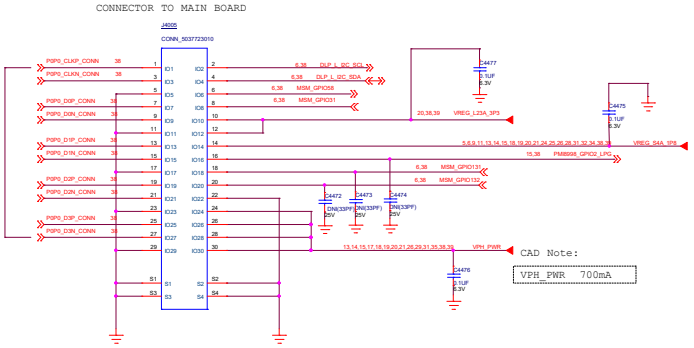
CAD Note:
Place Test points on the trace, No stub



Pin definition is not finalized

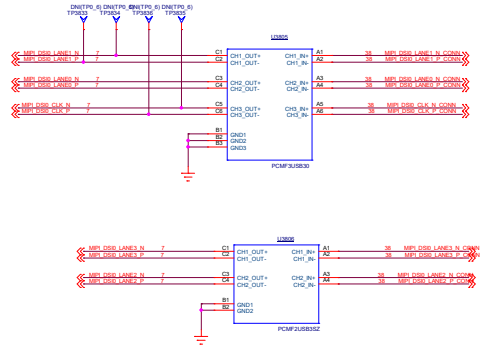
CONNECTOR TO MAIN BOARD

MIPI from DP Bridge



CAD Note:
VPH_PWR 700mA

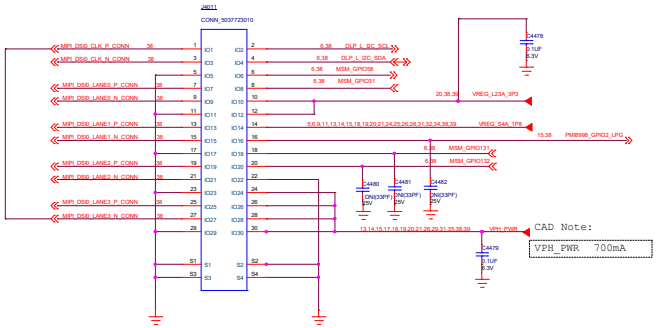
CAD Note:
Place Test points on the trace, No stub



Pin definition is not finalized

CONNECTOR TO MAIN BOARD

MIPI from HMD SD835



CAD Note:
VPH_PWR 700mA

Left DLP board connector

flex

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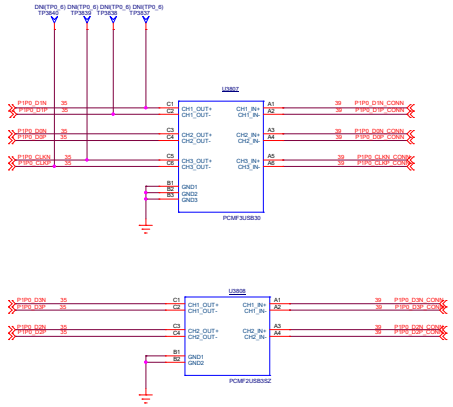
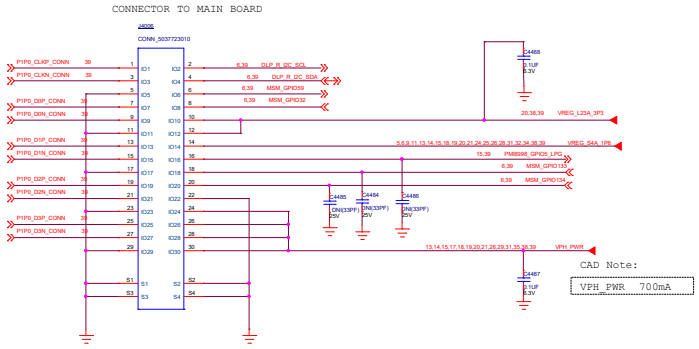
CAD Note:
Place Test points on the trace, No stub



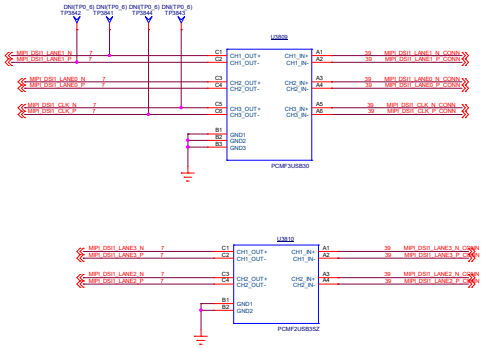
Pin definition is not finalized

CONNECTOR TO MAIN BOARD



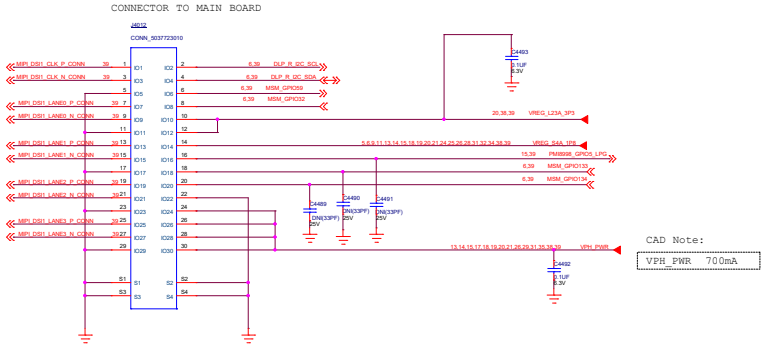
CAD Note:
VPH_PWR 700mA

CAD Note:
Place Test points on the trace, No stub



Pin definition is not finalized

CONNECTOR TO MAIN BOARD



CAD Note:
VPH_PWR 700mA

RIGHT DLP board connector

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Change list

EVT1 change list

[6/30] Page28: Change C2836 from 0201 0.1uf to 0201 1uf
[6/30] Page29: Add 0201 1uf capacitor C4510
[7/3] Page29: Change C4466 from 0.1uf to 1uf
[7/5] Page6: add a test point TP3858
[7/5] Page30: add a 10K pull-up resistor R3060 for ICM20602 int, DNI
[7/6] Page11: add capacitor C1160/C1161/C1162/C1163/C1164 for better PDN performance
[7/10] Page33: stuff R3306/add R3316 for POC battery
[7/10] Page29: add a 1.0uf capacitor C2970
[7/10] Page15: add a TP TP1501 for FAULT_N
[7/10] Page05: add a TP TP0510 for LN_BB_CLK1_EN
[7/11] Page26: Remove TP2701/TP2702
[7/11] Page29: unstuff C4483/C4471
[7/11] Page27: unstuff C2701
[7/11] Page37: unstuff C3710
[7/12] Page29: Change R2932 from 300k to 374k
[7/14] Page29: Remove SG2901 SG2902 for better routing
[7/24] Page30: Change R3085 to DNI
[7/24] Page38/Page39: Change the pin definition of EMI filters
[7/24] Page29: Change R2934 to unstuffed, Change R2935 to stuffed
[7/24] Page29: Add testpoint TP2912/TP2913
[7/24] Page32: Change Resistor R5843/R5844 from unstuffed to stuffed
[7/28] Page13: Change Resistor R5858 from unstuffed to stuffed

Revision History

flex

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