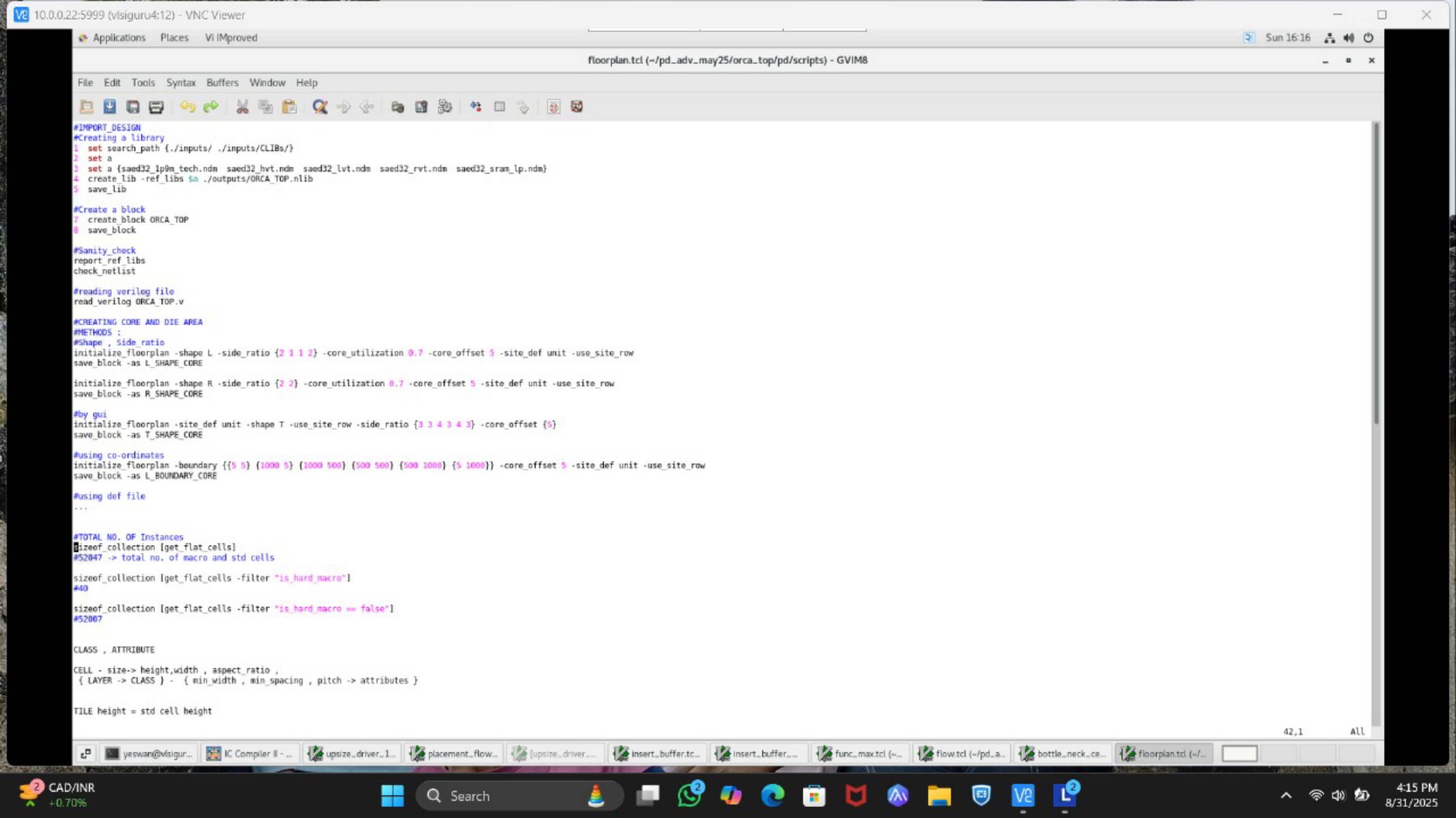
10.0.0.22:5999 (vlsiguru4:12) - VNC Viewer
Applications Places Vi IMproved
Sun 16:16
floorplan.tcl (~/pd_adv_may25/orca_top/pd/scripts) - GVIM8
File Edit Tools Syntax Buffers Window Help
#IMPORT_DESIGN
#Creating a library
set search_path {./inputs/ ./inputs/CLIBs/}
set a
set a {saed32_1p9m_tech.ndm saed32_hvt.ndm saed32_lvt.ndm saed32_rvt.ndm saed32_sram_lp.ndm}
create_lib -ref_libs $a ./outputs/ORCA_TOP.nlib
save_lib
#Create a block
create_block ORCA_TOP
save_block
#Sanity_check
report_ref_libs
check_netlist
#reading verilog file
read_verilog ORCA_TOP.v
#CREATING CORE AND DIE AREA
#METHODS :
#Shape , Side_ratio
initialize_floorplan -shape L -side_ratio {2 1 1 2} -core_utilization 0.7 -core_offset 5 -site_def unit -use_site_row
save_block -as L_SHAPE_CORE
initialize_floorplan -shape R -side_ratio {2 2} -core_utilization 0.7 -core_offset 5 -site_def unit -use_site_row
save_block -as R_SHAPE_CORE
#by gui
initialize_floorplan -site_def unit -shape T -use_site_row -side_ratio {3 3 4 3 4 3} -core_offset {5}
save_block -as T_SHAPE_CORE
#using co-ordinates
initialize_floorplan -boundary {{5 5} {1000 5} {1000 500} {500 500} {500 1000} {5 1000}} -core_offset 5 -site_def unit -use_site_row
save_block -as L_BOUNDARY_CORE
#using def file
...
#TOTAL NO. OF Instances
sizeof_collection [get_flat_cells]
#52047 -> total no. of macro and std cells
sizeof_collection [get_flat_cells -filter "is_hard_macro"]
#40
sizeof_collection [get_flat_cells -filter "is_hard_macro == false"]
#52007
CLASS , ATTRIBUTE
CELL - size-> height,width , aspect_ratio ,
{ LAYER -> CLASS } - { min_width , min_spacing , pitch -> attributes }
TILE height = std cell height
42,1 All
yeswan@vlsigur...
IC Compiler II - ...
upsize_driver_1...
placement_flow...
[upsize_driver_...
insert_buffer.tc...
insert_buffer_...
func_max.tcl (~...
flow.tcl (~/pd_a...
bottle_neck_ce...
floorplan.tcl (~/...
CAD/INR
+0.70%
Search
4:15 PM
8/31/2025