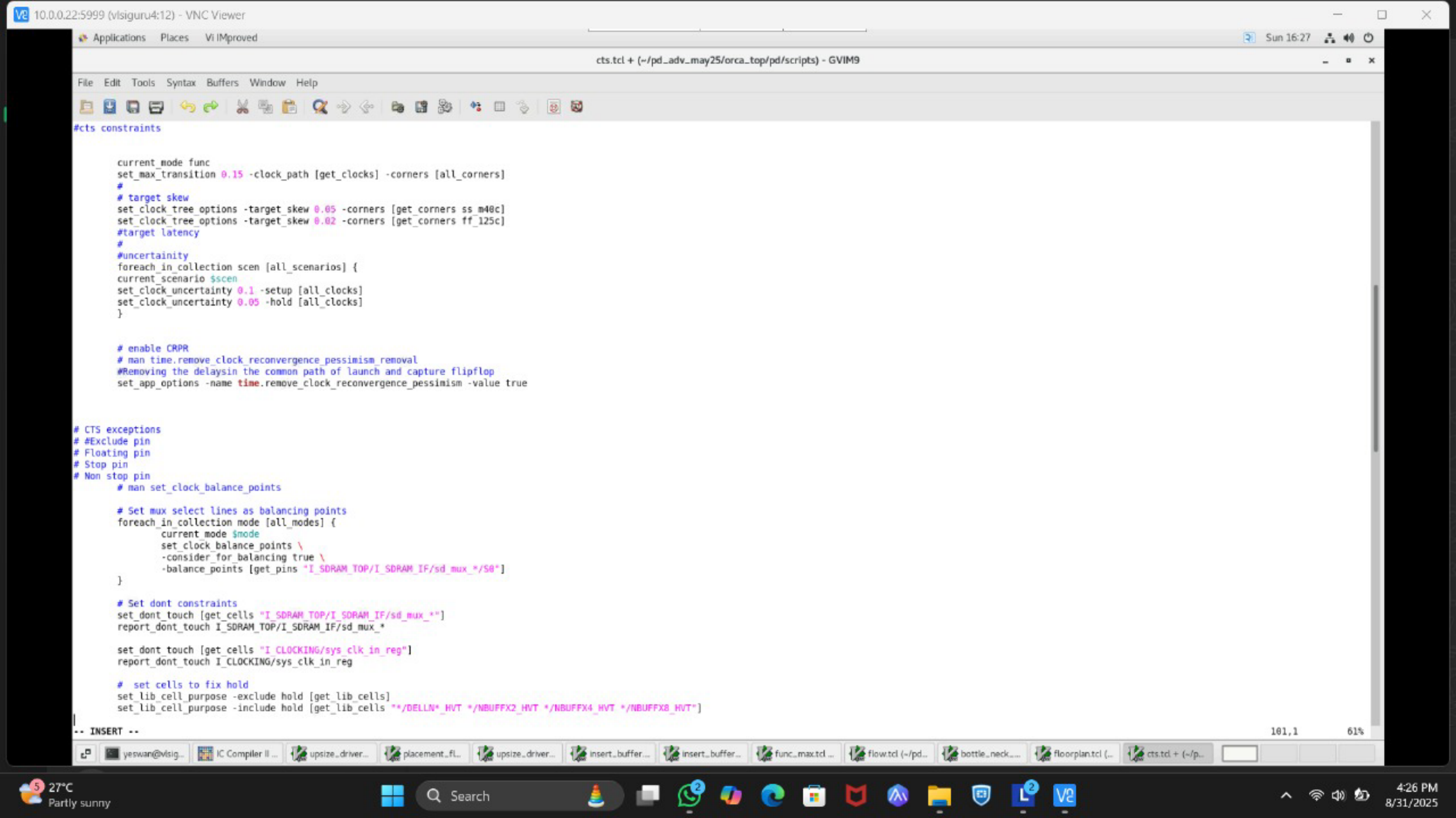
cts.tcl + (~/pd_adv_may25/orca_top/pd/scripts) - GVIM9

File Edit Tools Syntax Buffers Window Help

```
##################     cts spec file ######################
# read man on check_design , check_clock_trees
       #check_design -checks names_of_checks
check_design -checks pre_clock_tree_stage

check_clock_trees

#CELLS IN THE CLOCK PATH BEFORE CTS STAGE : MUX , ANDOR , BUFF
#FEEDTHROUGH CLOCKS : INPUT TO OUTPUT - SD_DDR_CLK , SD_DDR_CLKn
#test mode and occbypass controller -
#DFT - shift mode , capture mode[test clk] , capture at speed mode [func clk]
#ICG CELLS



# already cells are  existingin clk path .but  why the cells to be added ?
       # to balance the skew
#
#derive_clock_cell_reference
       #alternate cells for the cells already existing in cts path
       # go to scripts folder and do copy
              #cp /home/pd_sept/PD/scripts/cts_include_refs.tcl .
              # edit the file  to have LVT/RVT cells
#EXCLUDING ALL THE CELLS WHICH ARE PRESENT IN THE LIBRARY
set_lib_cell_purpose -exclude cts [get_lib_cells]

source ./scripts/cts_include_refs.tcl
set_lib_cell_purpose -include cts [get_lib_cells "*/NBUFF*LVT */NBUFF*RVT */INVX*_LVT */INVX*_RVT */*DFF**"]



# NDR
#cts constraints
#

#

#NDR[Non default rules] :- double width and double spacing
#Min metal , max metal layer to be used
#double spacing between them
#taper distance - 0.4
remove_routing_rules -all
create_routing_rule iccrm_clock_double_spacing -default_reference_rule -multiplier_spacing 2 -taper_distance 0.4 -driver_taper_distance 0.4
set_clock_routing_rules -net_type sink -rules iccrm_clock_double_spacing -min_routing_layer M4 -max_routing_layer M5


#
#
#cts constraints

-- INSERT --                                                                    52,1          Top
```


10.0.0.22:5999 (vlsiguru4:12) - VNC Viewer
Applications Places Vi IMproved
Sun 16:27
cts.tcl + (~/pd_adv_may25/orca_top/pd/scripts) - GVIM9
File Edit Tools Syntax Buffers Window Help
#cts constraints
current_mode func
set_max_transition 0.15 -clock_path [get_clocks] -corners [all_corners]
#
target skew
set_clock_tree_options -target_skew 0.05 -corners [get_corners ss_m40c]
set_clock_tree_options -target_skew 0.02 -corners [get_corners ff_125c]
#target latency
#
#uncertainity
foreach_in_collection scen [all_scenarios] {
current_scenario $scen
set_clock_uncertainty 0.1 -setup [all_clocks]
set_clock_uncertainty 0.05 -hold [all_clocks]
}
# enable CRPR
# man time.remove_clock_reconvergence_pessimism_removal
#Removing the delaysin the common path of launch and capture flipflop
set_app_options -name time.remove_clock_reconvergence_pessimism -value true
# CTS exceptions
# #Exclude pin
# Floating pin
# Stop pin
# Non stop pin
# man set_clock_balance_points
# Set mux select lines as balancing points
foreach_in_collection mode [all_modes] {
current_mode $mode
set_clock_balance_points \
-consider_for_balancing true \
-balance_points [get_pins "I_SDRAM_TOP/I_SDRAM_IF/sd_mux_*/S0"]
}
# Set dont constraints
set_dont_touch [get_cells "I_SDRAM_TOP/I_SDRAM_IF/sd_mux_*"]
report_dont_touch I_SDRAM_TOP/I_SDRAM_IF/sd_mux_*
set_dont_touch [get_cells "I_CLOCKING/sys_clk_in_reg"]
report_dont_touch I_CLOCKING/sys_clk_in_reg
set cells to fix hold
set_lib_cell_purpose -exclude hold [get_lib_cells]
set_lib_cell_purpose -include hold [get_lib_cells "*/DELLN*_HVT */NBUFFX2_HVT */NBUFFX4_HVT */NBUFFX8_HVT"]
-- INSERT --
101,1 61%
yeswan@vlsig... IC Compiler II ... upsize_driver... placement_fl... upsize_driver... insert_buffer... insert_buffer... func_max.tcl ... flow.tcl (~/pd... bottle_neck.... floorplan.tcl (... cts.tcl + (~/p...
27°C Partly sunny
Search
4:26 PM 8/31/2025

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File Edit Tools Syntax Buffers Window Help

```
        # Set mux select lines as balancing points
        foreach_in_collection mode [all_modes] {
                current_mode $mode
                set_clock_balance_points \
                -consider_for_balancing true \
                -balance_points [get_pins "I_SDRAM_TOP/I_SDRAM_IF/sd_mux_*/S0"]
        }

        # Set dont constraints
        set_dont_touch [get_cells "I_SDRAM_TOP/I_SDRAM_IF/sd_mux_*"]
        report_dont_touch I_SDRAM_TOP/I_SDRAM_IF/sd_mux_*

        set_dont_touch [get_cells "I_CLOCKING/sys_clk_in_reg"]
        report_dont_touch I_CLOCKING/sys_clk_in_reg

        #  set cells to fix hold
        set_lib_cell_purpose -exclude hold [get_lib_cells]
        set_lib_cell_purpose -include hold [get_lib_cells "*/DELLN* HVT */NBUFFX2_HVT */NBUFFX4_HVT */NBUFFX8_HVT"]

        # Give prefix to cells added in cts path
        set_app_option -name cts.common.user_instance_name_prefix -value clock_opt_clock_

        # Give prefix to cells added in data path
        set_app_option -name opt.common.user_instance_name_prefix -value clock_opt_opt_

#Build CTS
        # Remove route global
        remove_routes -global_route

# run clock opt
        #clock_opt -list_only
clock_opt -to build_clock
save_block -as build_clock_done

clock_opt -to route_clock

save_block -as cts_done


# open the block
#open_block cts_done
report_global_timing
set_app_options -name clock_opt.hold.effort -value high
set_app_options -name ccd.hold_control_effort -value high
set_app_options -name opt.dft.clock_aware_scan_reorder -value true

clock_opt -from final_opto
save_block -as clock_opt_done
```

-- INSERT -- 133,1 Bot