6. If required by the application, reconfigure the sample sequencer priorities in the **ADCSSPRI** register. The default configuration has Sample Sequencer 0 with the highest priority and Sample Sequencer 3 as the lowest priority.

13.4.2 Sample Sequencer Configuration

Configuration of the sample sequencers is slightly more complex than the module initialization because each sample sequencer is completely programmable.

The configuration for each sample sequencer should be as follows:

1. Ensure that the sample sequencer is disabled by clearing the corresponding ASENn bit in the **ADCACTSS** register. Programming of the sample sequencers is allowed without having them enabled. Disabling the sequencer during programming prevents erroneous execution if a trigger event were to occur during the configuration process.
2. Configure the trigger event for the sample sequencer in the **ADCEMUX** register.
3. For each sample in the sample sequence, configure the corresponding input source in the **ADCSSMUXn** register.
4. For each sample in the sample sequence, configure the sample control bits in the corresponding nibble in the **ADCSSCTLn** register. When programming the last nibble, ensure that the END bit is set. Failure to set the END bit causes unpredictable behavior.
5. If interrupts are to be used, set the corresponding MASK bit in the **ADCIM** register.
6. Enable the sample sequencer logic by setting the corresponding ASENn bit in the **ADCACTSS** register.

13.5 Register Map

Table 13-4 on page 779 lists the ADC registers. The offset listed is a hexadecimal increment to the register's address, relative to that ADC module's base address of:

- ADC0: 0x4003.8000
- ADC1: 0x4003.9000

Note that the ADC module clock must be enabled before the registers can be programmed (see page 327). There must be a delay of 3 system clocks after the ADC module clock is enabled before any ADC module registers are accessed.

Table 13-4. ADC Register Map

Offset	Name	Type	Reset	Description	See page
0x000	ADCACTSS	R/W	0x0000.0000	ADC Active Sample Sequencer	782
0x004	ADCRIS	RO	0x0000.0000	ADC Raw Interrupt Status	784
0x008	ADCIM	R/W	0x0000.0000	ADC Interrupt Mask	786
0x00C	ADCISC	R/W1C	0x0000.0000	ADC Interrupt Status and Clear	789
0x010	ADCOSTAT	R/W1C	0x0000.0000	ADC Overflow Status	792
0x014	ADCEMUX	R/W	0x0000.0000	ADC Event Multiplexer Select	794

Table 13-4. ADC Register Map *(continued)*

Offset	Name	Type	Reset	Description	See page
0x018	ADCUSTAT	R/W1C	0x0000.0000	ADC Underflow Status	799
0x020	ADCSSPRI	R/W	0x0000.3210	ADC Sample Sequencer Priority	800
0x024	ADCSPC	R/W	0x0000.0000	ADC Sample Phase Control	802
0x028	ADCPSSI	R/W	-	ADC Processor Sample Sequence Initiate	804
0x030	ADCSAC	R/W	0x0000.0000	ADC Sample Averaging Control	806
0x034	ADCDCISC	R/W1C	0x0000.0000	ADC Digital Comparator Interrupt Status and Clear	807
0x038	ADCCTL	R/W	0x0000.0000	ADC Control	809
0x040	ADCSSMUX0	R/W	0x0000.0000	ADC Sample Sequence Input Multiplexer Select 0	810
0x044	ADCSSCTL0	R/W	0x0000.0000	ADC Sample Sequence Control 0	812
0x048	ADCSSFIFO0	RO	-	ADC Sample Sequence Result FIFO 0	819
0x04C	ADCSSFSTAT0	RO	0x0000.0100	ADC Sample Sequence FIFO 0 Status	820
0x050	ADCSSOP0	R/W	0x0000.0000	ADC Sample Sequence 0 Operation	822
0x054	ADCSSDC0	R/W	0x0000.0000	ADC Sample Sequence 0 Digital Comparator Select	824
0x060	ADCSSMUX1	R/W	0x0000.0000	ADC Sample Sequence Input Multiplexer Select 1	826
0x064	ADCSSCTL1	R/W	0x0000.0000	ADC Sample Sequence Control 1	827
0x068	ADCSSFIFO1	RO	-	ADC Sample Sequence Result FIFO 1	819
0x06C	ADCSSFSTAT1	RO	0x0000.0100	ADC Sample Sequence FIFO 1 Status	820
0x070	ADCSSOP1	R/W	0x0000.0000	ADC Sample Sequence 1 Operation	831
0x074	ADCSSDC1	R/W	0x0000.0000	ADC Sample Sequence 1 Digital Comparator Select	832
0x080	ADCSSMUX2	R/W	0x0000.0000	ADC Sample Sequence Input Multiplexer Select 2	826
0x084	ADCSSCTL2	R/W	0x0000.0000	ADC Sample Sequence Control 2	827
0x088	ADCSSFIFO2	RO	-	ADC Sample Sequence Result FIFO 2	819
0x08C	ADCSSFSTAT2	RO	0x0000.0100	ADC Sample Sequence FIFO 2 Status	820
0x090	ADCSSOP2	R/W	0x0000.0000	ADC Sample Sequence 2 Operation	831
0x094	ADCSSDC2	R/W	0x0000.0000	ADC Sample Sequence 2 Digital Comparator Select	832
0x0A0	ADCSSMUX3	R/W	0x0000.0000	ADC Sample Sequence Input Multiplexer Select 3	834
0x0A4	ADCSSCTL3	R/W	0x0000.0000	ADC Sample Sequence Control 3	835
0x0A8	ADCSSFIFO3	RO	-	ADC Sample Sequence Result FIFO 3	819
0x0AC	ADCSSFSTAT3	RO	0x0000.0100	ADC Sample Sequence FIFO 3 Status	820
0x0B0	ADCSSOP3	R/W	0x0000.0000	ADC Sample Sequence 3 Operation	837
0x0B4	ADCSSDC3	R/W	0x0000.0000	ADC Sample Sequence 3 Digital Comparator Select	838
0xD00	ADCDCRIC	WO	0x0000.0000	ADC Digital Comparator Reset Initial Conditions	839

Table 13-4. ADC Register Map *(continued)*

Offset	Name	Type	Reset	Description	See page
0xE00	ADCDCCTL0	R/W	0x0000.0000	ADC Digital Comparator Control 0	844
0xE04	ADCDCCTL1	R/W	0x0000.0000	ADC Digital Comparator Control 1	844
0xE08	ADCDCCTL2	R/W	0x0000.0000	ADC Digital Comparator Control 2	844
0xE0C	ADCDCCTL3	R/W	0x0000.0000	ADC Digital Comparator Control 3	844
0xE10	ADCDCCTL4	R/W	0x0000.0000	ADC Digital Comparator Control 4	844
0xE14	ADCDCCTL5	R/W	0x0000.0000	ADC Digital Comparator Control 5	844
0xE18	ADCDCCTL6	R/W	0x0000.0000	ADC Digital Comparator Control 6	844
0xE1C	ADCDCCTL7	R/W	0x0000.0000	ADC Digital Comparator Control 7	844
0xE40	ADCDCCMP0	R/W	0x0000.0000	ADC Digital Comparator Range 0	846
0xE44	ADCDCCMP1	R/W	0x0000.0000	ADC Digital Comparator Range 1	846
0xE48	ADCDCCMP2	R/W	0x0000.0000	ADC Digital Comparator Range 2	846
0xE4C	ADCDCCMP3	R/W	0x0000.0000	ADC Digital Comparator Range 3	846
0xE50	ADCDCCMP4	R/W	0x0000.0000	ADC Digital Comparator Range 4	846
0xE54	ADCDCCMP5	R/W	0x0000.0000	ADC Digital Comparator Range 5	846
0xE58	ADCDCCMP6	R/W	0x0000.0000	ADC Digital Comparator Range 6	846
0xE5C	ADCDCCMP7	R/W	0x0000.0000	ADC Digital Comparator Range 7	846
0xFC0	ADCPP	RO	0x00B0.20C7	ADC Peripheral Properties	847
0xFC4	ADCPC	R/W	0x0000.0007	ADC Peripheral Configuration	849
0xFC8	ADCCC	R/W	0x0000.0000	ADC Clock Configuration	850

13.6 Register Descriptions

The remainder of this section lists and describes the ADC registers, in numerical order by address offset.