This problem set has 6 questions, for a total of 100 points. Answer the questions below and mark your answers in the spaces provided. Please provide details on how your answer was calculated.

Your Name: Yeury Czalva

- 1. Assume a color display using 8 bits for each of the primary colors (red, green, blue) per pixel and a frame size of 1280×1024 .
 - (a) [5 points] What is the minimum size in bytes of the frame buffer to store a frame?

(b) [5 points] How long would it take, at a minimum, for the frame to be sent over a 100 Mbit/s network?

Looking back at the table from slides -> 1 mbit/s = 10 bit/s So Answering the question low Mbit/s = 100 × 10 bit/s = 108 bit/e Size of frame = 3,932, 160 XY = 31,457, 2800 bit After looking of equation for time => time = size = 31,457,280 bits 10 511/5 = (0.3145728,

- Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3GHz clock rate and a CPI of 1.5. P2 has a 2.5GHz clock rate and a CPI of 1.0. P3 has a 4.0GHz clock rate and has a CPI of 2.2.
 - (a) [6 points] Which processor has the highest performance expressed in instructions per second? = IPS

clock rate. CPU une IC Ry has the highest IPS,	= instruction cant	X CPI . clack rate	1 GHz = 10	9 HZ
clock rate. CPU Line IC Ry Line CPI IPS; CPI Line CPI IPS;	CIOCH TO	external W (PI	IPS, = 361	He = 2×10
clock rate. CPV Line IC P2 has the highest IPS,	x rate. CPU: instru	PI lock rate	IB = 2.5 G	1Hz = 2.51
CPI Las the highest	CPI	1105900	IPS, = 4 CT#	= 1.82
	Krate · CPU Line IC	To has the highest	2.2	- X 10
clock rate - Chu time = IC Performance Per	CFI - I	C Performance		

(b) [6 points] If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

Chot time: 103, I Gitte: 10° Hz

From Problem A = Know that instructions = JPS x CPU time

clock cycles = CPU time x clock rate

Processor I : instructions, = 2 x 10° x 10 = 2 x 10°

clock cycles, = 10 x 3 chtz = 10x3x 10°

= 3 x 10°

Processor 2: instructions = 2.5 x 10° x 10 = 2.5 x 10°

clock cycles = 10x 2.5 chtz = 10 x 2.5 x 10°

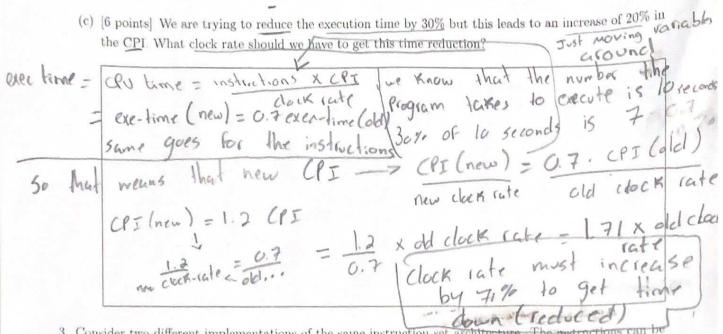
clock cycles = 1.82 x 10° x 10 = 1.82 x 10°

Processor 3: instructions = 1.82 x 10° x 10 = 1.82 x 10°

clock cycles = 10x 4 chtz = 10x4x 10°

clock cycles = 10x 4 chtz = 10x4x 10°

= 4 x 10°



3. Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3GHz and CPIs of 2, 2, 2, and 2. Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D.

(a) [6 points] What is the global CPL for each implementation?

Come to find out that 1.0E6 = 10 = 1,000,000 = 2° ((Pix instruction count)

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(IXIOS) + (2) × 2 × 18) + (3+5 + 105) + (3×2×105)

= 2.6 × 106 Pa clock cylle: (2x105) + (2x2x105) + (2x2x105) + (2x2x105) 10x10% (PI = clock cycles

of instructions

$$P_3 \rightarrow CPI = \frac{3.6 \times 10^6}{10^6} = 2.6$$

$$P_3 \rightarrow CPI = \frac{3 \times 10^6}{10^6} = 2$$

(b) [6 points] Find the clock cycles required in both cases.

- 4. Compilers can have a profound impact on the performance of an application. Assume that for a program, compiler A results in a dynamic instruction count of 1.0E9 and has an execution time of 1.1s, while compiler B results in a dynamic instruction count of 1.2E9 and an execution time of 1.5s.
 - (a) [6 points] Find the average CPI for each program given that the processor has a clock cycle time of 1ns.

CPU = IC X CPI X Cycle time

$$time = \frac{1}{12}$$

CPI = CPU time

 $A \rightarrow CPI = \frac{1.1s}{10^9 \times 10^9} = 1.1$

B -> CPI = $\frac{1.5s}{1.2 \times 10^9 \times 10^9} = 1.25$

(b) [6 points] Assume the compiled programs run on two different processors, If the execution times on the two processors are the same, how much faster is the clock of the processor running compiler A's code versus the clock of the processor running compiler B's code?

A sclock rate = IC, x CPIA x Clock rate B

I clock rate = IC, x CPIA x Clock rate B

I clock rate = O.73 Clock rate B

P. is about 27%

Flower than Po

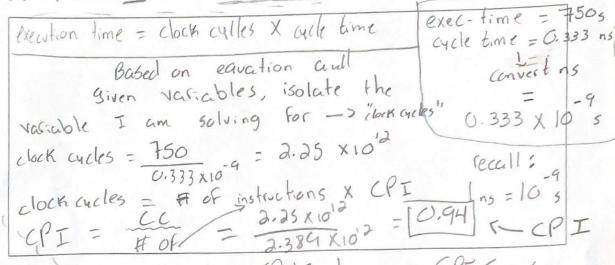
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(c) [6 points] A new compiler is developed that uses only 6.0E8 instructions and has an average CPI of 1.1. What is the speedup of using the new compiler versus using compiler A or B on the original processor?

or $CPV = IC \times CPI \times cycle time = 6 \times 10^3 \times 1.1 \times 10^5 = 0.66s$ $CPV = IC \times CPI \times cycle time = 6 \times 10^3 \times 1.1 \times 10^5 = 0.66s$ $CPV = IC \times CPI \times cycle time = 6 \times 10^3 \times 1.1 \times 10^5 = 0.66s$ $CPV = IC \times CPI \times cycle time = 6 \times 10^3 \times 1.1 \times 10^5 = 0.66s$ $CPV = IC \times CPI \times cycle time = 6 \times 10^3 \times 1.1 \times 10^5 = 0.66s$ $CPV = IC \times CPI \times cycle time = 6 \times 10^3 \times 1.1 \times 10^5 = 0.66s$ $CPV = IC \times CPI \times cycle time = 6 \times 10^3 \times 1.1 \times 10^5 = 0.66s$ $CPV = IC \times CPI \times cycle time = 6 \times 10^3 \times 1.1 \times 10^5 = 0.66s$ $CPV = IC \times CPI \times cycle time = 6 \times 10^3 \times 1.1 \times 10^5 = 0.66s$ $CPV = IC \times CPI \times cycle time = 6 \times 10^3 \times 1.1 \times 10^5 = 0.66s$ $CPV = IC \times CPI \times cycle time = 6 \times 10^3 \times 1.1 \times 10^5 = 0.66s$ $CPV = IC \times CPI \times cycle time = 6 \times 10^3 \times 1.1 \times 10^5 = 0.66s$ $CPV = IC \times CPI \times cycle time = 6 \times 10^3 \times 1.1 \times 10^5 = 0.66s$ $CPV = IC \times CPI \times cycle time = 6 \times 10^3 \times 1.1 \times 10^5 = 0.66s$ $CPV = IC \times CPI \times cycle time = 6 \times 10^3 \times 1.1 \times 10^5 = 0.66s$ $CPV = IC \times CPI \times cycle time = 6 \times 10^3 \times 1.1 \times 10^5 = 0.66s$ $CPV = IC \times CPI \times cycle time = 6 \times 10^3 \times 1.1 \times 10^5 = 0.66s$ $CPV = IC \times CPI \times cycle time = 6 \times 10^3 \times 1.1 \times 10^5 = 0.66s$ $CPV = IC \times CPI \times cycle time = 6 \times 10^3 \times 1.1 \times 10^5 = 0.66s$ $CPV = IC \times CPI \times cycle time = 6 \times 10^3 \times 1.1 \times 10^5 = 0.66s$ $CPV = IC \times CPI \times cycle time = 6 \times 10^3 \times 1.1 \times 10^5 = 0.66s$ $CPV = IC \times CPI \times cycle time = 6 \times 10^3 \times 1.1 \times 10^5 = 0.66s$ $CPV = IC \times CPI \times cycle time = 6 \times 10^3 \times 10^3$

- 5. The results of the SPEC CPU2006 bzip2 benchmark running on an AMD Barcelona has an instruction count of 2 389E12, an execution time of 750s, and a reference time of 9650s.
 - (a) [6 points] Find the CPI if the clock cycle time is 0.333ns.



(c) [6 points] Suppose that we are developing a new version of the AMD Barcelona processor with a 4GHz clock rate. We have added some additional instructions to the instruction set in such a way that the number of instructions has been reduced by 15%. The execution time is reduced to 700s and the new SPECratio is 13.7. Find the new CPL.

cucle time = \frac{1}{4\text{GHz}} = 0.25 \text{ X 10 s} \\

\text{exectime} = \text{clock cycles X cycle time} \\
\text{clock cycles} = \text{exectime} \\
\text{cycle time} = \frac{100}{0.35 \text{ K 10}} = \frac{2.8 \text{ X 10}^{12}}{0.25 \text{ K 10}} \\
\text{row} \text{I cun find CPI, Since I have clock cycles} \\
\text{cycles} \\
\text{c

(d) [6 points] For a second benchmark, libquantum, assume an execution time of 960ns, CPI of 1.61, and clock rate of 3GHz. If the execution time is reduced by an additional 10% without affecting to the CPI and with a clock rate of 4GHz, determine the number of instructions.

CPI = exective x clock(ate solve for exections

of instructions = exection x clock (ate constructions)

CPI = 864 x 10 - 9 x 9 x 10 - 9

6. Section 1.11 (textbook) cites as a pitfall the utilization of a subset of the performance equation as a performance metric. To illustrate this, consider two processors. P1 has a clock rate of 4GHz, average CPI of 0.9, and requires the execution of 5.0E9 instructions. P2 has a clock rate of 3GHz, an average of CPI of 0.75, and requires the execution of 1.0E9 instructions.

(a) [6 points] One usual fallacy is to consider the computer with the largest clock rate as having the largest performance. Check if this is true for P1 and P2.

largest performance. Check if this is true for PI and P2.)

$$P_{1-2} = \frac{I \subset X \subset PI}{Clack \text{ rate}}$$

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$$P$$

(b) [6 points] Another fallacy is to consider that the processor executing with the largest number of instructions will need a larger CPU time. Consider that processor P1 is executing a sequence of 1.0E9 instructions and that the CPI of processors P1 and P2 do not change, determine the number of instructions that P2 can execute in the same time that P1 needs to execute 1.0E9 instructions.

Problem =
$$\frac{10^9 \times 6.9}{4 \text{ GHz}} = \frac{0.9 \times 10^9}{4 \times 10^9 \text{Hz}} = 0.225$$

Problem = $\frac{10^9 \times 6.9}{4 \times 10^9 \text{Hz}} = 0.225$
 $\frac{3 \text{ GHz}}{3 \text{ GHz}}$
Hof instructions = $\frac{0.225 \times 3 \times 10^9}{0.75} = 9 \times 10^8$

It is clearly that P, Con Process more instructions than Pa and most importantly at the same ferral time (c) [6 points] A common fallacy is to use MIPS (millions of instructions per second) to compare the performance of two different processors, and consider that the processor with the largest MIPS has the largest performance. Check if this is true for P1 and P2.

the largest performance. Check if this is true for P1 and P2.

MIPS =
$$\frac{\text{Clock Gate}}{\text{CPI x 10}^6}$$
 $P_1 = \frac{\text{4 GHz}}{0.9 \times 10^6} = \frac{\text{4 x 10}^6 \text{Hz}}{0.9 \times 10^6} = \frac{\text{4 u u u}}{0.9 \times 10^6}$
 $P_2 = \frac{3 \text{ tr Hz}}{0.75 \times 10^6} = \frac{3 \times 10^6 \text{ Hz}}{0.75 \times 10^6} = \frac{\text{4 u u u}}{0.9 \times 10^6}$
 $\frac{\text{Results of the processors with the largest MITS into the processor with the largest MITS into the processor with the largest MITS into the processor with the largest MITS into th$