

VE370 Homework 7 Wang Lan 519370910084

1. (20 points) For a 2-way set associative cache with a 32-bit address and write back mechanism, the partition of the 32 bits are as follows:

- Offset: bit 6 to 0
- Index: bit 11-7

(1) What is the size of the cache? (5 points)

Starting from power on, the following byte addresses were used to access the cache memory: 0, 4, 20, 136, 232, 164, 1024, 30, 140, 3100, 176, 2180

(2) What is the hit ratio? (5 points)

(3) Show the final state of the cache, with each valid line represented as <index, tag, data>.

(10 points)

(1) 5-bit index $\Rightarrow 2^5 = 32$ sets

2 blocks per set $\Rightarrow 64$ blocks

7-bit offset \Rightarrow 5-bit word offset + 2-bit byte offset $\Rightarrow 2^5 = 32$ words

$$32 \times 64 \times 32 + (20+1+1) \times 64 = 8368 \text{ Byte} = 8.172 \text{ KB}$$

	tag	index	H/M
0000 0000 0000	0	0	M
0000 0000 0100	0	0	H
0000 0001 0100	0	0	H
0000 1000 1000	0	1	M
0000 1110 1000	0	1	H
0000 1010 0100	0	1	H
0100 0000 0000	0	8	M
0000 0001 1110	0	0	H
0000 1000 1100	0	1	H
1100 0001 1100	0	24	M
0000 1011 0000	0	1	H
1000 1000 0100	0	17	M

$$\frac{7}{12} = 58.33\%$$

(3) $\langle 0, 0, \text{MEM}[0] \sim \text{MEM}[31] \rangle$

$\langle 1, 0, \text{MEM}[32] \sim \text{MEM}[63] \rangle$

$\langle 8, 0, \text{MEM}[256] \sim \text{MEM}[287] \rangle$

$\langle 17, 0, \text{MEM}[544] \sim \text{MEM}[575] \rangle$

$\langle 24, 0, \text{MEM}[768] \sim \text{MEM}[799] \rangle$

2. (20 points) In general, cache access time is proportional to its capacity. Assume that main memory accesses take 70 ns and that memory accesses are 36% of all instructions. The following table shows data for caches attached to each of two processors, P1 and P2.

	Size	Miss Rate	Hit Time
P1	16KB	4.3%	1.18 ns
P2	32KB	2.7%	2.22 ns

- (1) Assuming that the cache hit time determines the cycle times for P1 and P2, what are their respective clock rates? (5 points)
- (2) What is the AMAT for P1 and P2? AMAT (Average Memory Access Time) is defined as follows: $\text{AMAT} = \text{Hit time} + \text{Miss rate} \times \text{Miss penalty}$ (5 points).
- (3) Assuming a base CPI of 1.0 without any memory stalls, what is the actual CPI for P1 and P2? Which processor is faster? (10 points)

$$(1) \frac{1}{1.18} = 0.847 \text{ GHz}$$

$$\frac{1}{2.22} = 0.450 \text{ GHz}$$

$$(2) P1: \text{AMAT} = 1.18 + 4.3\% \times 70 = 4.19 \text{ ns}$$

$$P2: \text{AMAT} = 2.22 + 2.7\% \times 70 = 4.11 \text{ ns}$$

$$(3) P1: \frac{70}{1.18} \times 4.3\% + 1 = 3.551 \Rightarrow P2$$

$$P2: \frac{70}{2.22} \times 2.7\% + 1 = 1.851$$

3, 180, 43, 3, 191, 89, 190, 14, 181, 44, 186, 252

- (1) Show the final cache contents for a 3-way set associative cache with two-word blocks and a total size of 24 words. Use LRU replacement. For each reference identify the index bits, the tag bits, the offset bits, and if it is a hit or a miss. (20 points)
- (2) Show the final cache contents for a fully associative cache with one-word blocks and a total size of 8 words. Use LRU replacement. For each reference identify the index bits, the tag bits, and if it is a hit or a miss. (20 points)
- (3) What is the miss rate for a fully associative cache with two-word blocks and a total size of 8 words, using LRU replacement? What is the miss rate using MRU (most recently used) replacement? Finally what is the best possible miss rate for this cache, given any replacement policy? (20 points)

	tag	index	offset (word)	offset (byte)	H/M
00000 0011	050	00	0	11	M
10110 0100	101	10	1	00	M
00100 1011	001	01	0	11	M
00000 0011	000	00	0	11	H
10111 1111	101	11	1	11	M
01011 1001	010	11	0	01	M
10111 1110	101	11	1	10	H
00000 1110	000	01	1	10	M
10111 0101	101	10	1	01	H
00100 1100	001	01	1	00	H
10111 0100	101	11	0	10	H
11111 1100	111	11	1	00	M

00	Y 0 000 MEM[0]	MEM[1]
N		
N		

01	Y 0 001 MEM[0]	MEM[1]
Y 0 000 MEM[2]	MEM[3]	
N		

10	Y 0 101 MEM[44]	MEM[45]
N		
N		

11	Y 0 101 MEM[46]	MEM[47]
Y 0 010 MEM[22]	MEM[23]	
Y 0 111 MEM[62]	MEM[63]	

	tag	index	offset (byte)	H/M
00000 0011	000000	0	11	M
1011 0100	10110	1	00	M
0010 1011	00101	0	11	M
00000 0011	000000	0	11	H
1011 1111	10111	1	11	M
0101 1001	01011	0	01	M
1011 1110	10111	1	10	H
00000 1110	000001	1	10	M
1011 0101	10110	1	01	M
0010 1100	00101	1	00	M
1011 1010	10111	0	10	M
1111 1100	11111	1	00	M

0	Y	0	00000	MEM[0]
	Y	0	00101	MEM[10]
	Y	0	01011	MEM[22]
	Y	0	10111	MEM[46]

1	Y	0	11111	MEM[63]
	Y	0	10111	MEM[47]
	Y	0	00001	MEM[3]
	Y	0	00101	MEM[11]

	tag	offset (word)	offset (byte)	H/M (LRU)	H/M (MRU)
00000 0011	000000	0	11	M	M
1011 0100	10110	1	00	M	M
0010 1011	00101	0	11	M	M
00000 0011	000000	0	11	H	H
1011 1111	10111	1	11	M	M
0101 1001	01011	0	01	M	M
1011 1110	10111	1	10	H	M
00000 1110	000001	1	10	M	M
1011 0101	10110	1	01	M	M
0010 1100	00101	1	00	M	H
1011 1010	10111	0	10	M	H
1111 1100	11111	1	00	M	M

$$\frac{10}{12} = 83.33\% \quad \frac{9}{12} = 75\%$$

⇒ MRU