Behavioral Model of SiC MOSFET on Hard-Switching Condition

Zhechi Ye
Dept. of Electrical Engineering
Tsinghua University
Beijing, P.R.C
yezc15@mails.tsinghua.edu.cn

Xudong Wang
Dept. of Electrical Engineering
Tsinghua University
Beijing, P.R.C

***Abstract*—A behavioral model of SiC MOSFET on hard-switching condition is proposed. The model is based on double pulse test (DPT), in which the SiC MOSFET is combined with a SiC Schottky Barrier Diode (SBD). The nonlinearity of the junction capacitance and parasitic elements in the circuit are considered. To reduce the complexity of commonly proposed models, the model develops average value equations rather than differential equations to describe the circuit and estimate the switching time. The results of calculation and experiments are compared with previously proposed model, which shows that the model can provide a simple prediction of SiC MOSFET hard-switching characteristics.**

Keywords—SiC MOSFET, Modelling

I. INTRODUCTION

In recent years, power devices with wide-bandgap semiconductor materials, especially silicon carbide (SiC) and gallium nitride (GaN), have been regarded as a promising alternative to Si-based devices because of their superior properties. In most situations, power devices are used as controlled switches in circuit topologies. However, due to their nonideal characteristics, the performances are limited. For many applications that are not suitable for Si-based devices, the requirements (high voltage, high frequency) could be best achieved by SiC MOSFETs due to their low on-state resistances, small parasitic capacitances and high thermal limits. Also, the power density of power converters could be increased greatly by using SiC MOSFETs [1]-[3].

In most applications, models of semiconductor devices are especially important for designing power converters, as they could affect the accuracy of simulations and the system performance.

Recent studies have proposed different models to describe the characteristic of SiC MOSFETs [4]-[6]. Many of them could get accurate calculation of the voltage and current transient process on SiC MOSFET switching conditions. But there are two common problems of these models that restrict their application. Firstly, these models mainly adopt large amount of differential equations to describe the circuit, which though add to the accuracy, will also increase the complexity of calculation. As a result, in terms of large scale simulations, this kind of model will lead to a much longer simulation time and make it not practical. Second, these models depend greatly on the parasitic parameters of the circuits. The accuracy can not be guaranteed when different type of device or PCB layout is applied.

To reduce the complexity and increase the practicability of SiC MOSFET models, this paper proposed a new behavioral SiC MOSFET model to describe the hard-switching process and estimate transient time. With simple calculation, this model could get acceptable result of estimation compared with experiment results, which allows it to be applied into large scale simulations easily.

II. PROPOSED MODEL

The proposed model is based on double pulse test (DPT), which is a typical hard switching test for SiC MOSFET and SiC Schottky Barrier Diode (SBD) (the equivalent circuit is shown in Fig. 1). As transient characteristics of the power devices are best represented by voltage and current waveforms, it is common to exam the whole switching process by different stages of waveforms. The aim of this proposed model is to estimate the time of different stages by calculation and get a complete behavioral model of SiC MOSFET on hard-switching condition.

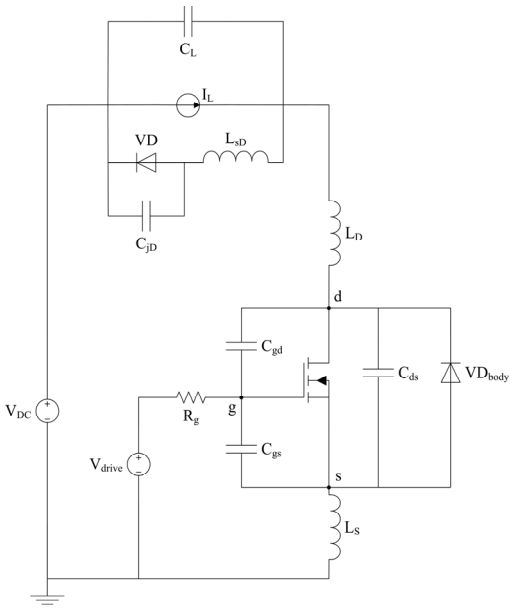

Fig. 1. DPT equivalent circuit

The switching transition (including turning-on and turning-off) is divided into several different stages, as shown in Fig. 2 and Fig. 3. As shown in Fig. 1, the in put of the DPT circuit is a DC voltage source V_{DC}, the inductive load is represented as a DC current source I_L during switching transition, and the MOSFET and the SBD are shown in their equivalent circuits. For the SiC MOSFET, C_{gd}, C_{gs} and C_{ds} are represented for parasitic capacitors, and the gate-drive voltage is v_{drive} with gate resistance R_g. For the SBD, it is considered as an ideal diode VD with parasitic capacitance C_{jD} and inductance L_{sD}. Components C_L, L_D and L_S are represented for parasitic parameters of traces and device packages.

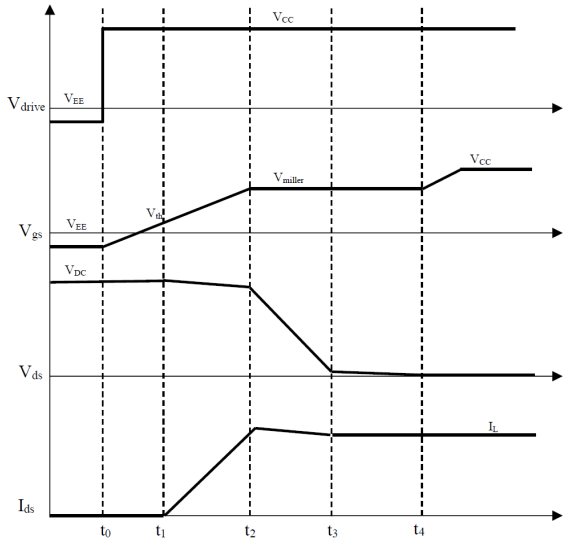

Fig. 2. Switching waveform of turning-on

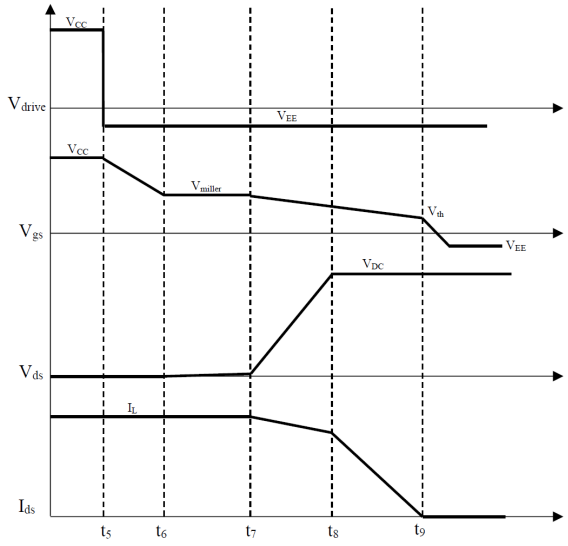

Fig. 3. Switching waveform of turning-off

For calculation, some important parameters should be extracted from the datasheet, including parasitic capacitances, tans-conductance of the SiC MOSFET (g_{fs}), threshold voltage (V_{th}) and miller voltage (V_{miller}). Fig. 4 shows typical capacitance curve of the SiC MOSFET. The nonlinearity is obvious. Fig. 5 shows typical transfer characteristics of SiC MOSFET. Both curves are from datasheet of CMF20120D [7].

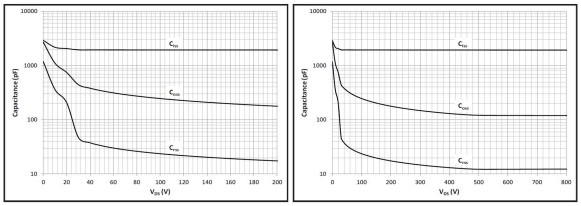

Fig. 4. Typical Capacitance Curve (CMF20120D)

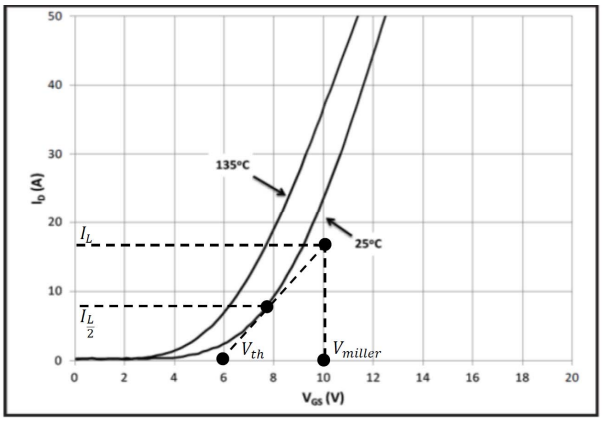

Fig. 5. Typical Transfer Characteristics (CMF20120D)

To get the capacitance value for calculation, two different typical values for relatively low voltage and high voltage are selected. For example, C_{ds} could be expressed as:

$$C_{ds} = C_{oss} - C_{rss} \tag{1}$$

And the value for calculation could be derived as:

$$C_{ds1} = C_{ds}\,|_{V_{ds}=\frac{V_{DC}}{2}} = (C_{oss} - C_{rss})\,|_{V_{ds}=\frac{V_{DC}}{2}} \tag{2}$$

$$C_{ds2} = C_{ds}\,|_{V_{ds}=V_{DC}} = (C_{oss} - C_{rss})\,|_{V_{ds}=V_{DC}} \tag{3}$$

C_{gd1} and C_{gd2} could be derived similarly. Besides, the junction capacitance C_{jD} of SBD could also be obtained by this method.

To get the value of g_{fs}, V_{th} and V_{miller}, a tangent line is drawn in the transfer characteristics at half of the load current,

and use its slope for g_{fs}, intercept for V_{th} and the voltage at load current I_L for V_{miller}, as shown in Fig. 5.

In the following, the model is presented with parameters in the circuit and extracted from the datasheet.

A. Turn-on Transition (Fig. 2)

Stage 1 [t_0, t_1] turn-on delay time: In this stage, input capacitance C_{iss} is charged as v_{drive} rise to V_{CC} at t_0. The MOSFET channel will not turn-on until v_{gs} reaches V_{th}. Thus the delay time could be derived as:

$$V_{th} = V_{CC}(1-\exp(-\frac{t_1-t_0}{\tau_{iss1}})) \tag{4}$$

where $\tau_{iss1} = R_g(C_{gs}+C_{gd1})$. By replacing $1-\exp(-\frac{t_1-t_0}{\tau_{iss1}})$ as $\frac{t_1-t_0}{\tau_{iss1}}$, (4) could be further simplified as:

$$t_1 - t_0 = \frac{V_{th}}{V_{CC}}\tau_{iss1} \tag{5}$$

Stage 2 [t_1, t_2] current rise time: In this stage, i_d starts to rise from zero to reach I_L as v_{gs} keeps rising to V_{miller}, and the SBD current starts to decrease. Besides, v_{ds} starts to drop as i_d flow across the parasitic inductance. The input capacitance continues to be charged as:

$$I_{g2} = C_{iss1}\frac{V_{miller}-V_{th}}{t_2-t_1} \tag{6}$$

where I_{g2} is the average charging current through gate, $C_{iss1} = C_{gs}+C_{gd1}$. And for the drive loop:

$$I_{g2}R_g = V_{CC} - \frac{V_{miller}+V_{th}}{2} - L_S\frac{I_L}{t_2-t_1} \tag{7}$$

Thus, the current rise time could be derived as:

$$t_2 - t_1 = \frac{\tau_{iss1}(V_{miller}-V_{th}) + L_S I_L}{V_{CC} - \frac{V_{miller}+V_{th}}{2}} \tag{8}$$

As the existence of parasitic inductance, v_{ds} will slightly drop from V_{DC} to V_{ds2}, which could be described as:

$$V_{ds2} = V_{DC} - (L_S+L_D)\frac{I_L}{t_2-t_1} \tag{9}$$

Stage 3 [t_2, t_3] voltage falling time I: In this stage, v_{ds} begins to drop from V_{ds2} to the boundary voltage of MOSFET as $V_{miller}-V_{th}$, and v_{gs} remains at V_{miller}. C_{oss} is discharged at this stage and the impact of SBD cannot be dismissed as it will cause a slight peak current.

J. Wang etc. have built a detailed model of this stage in [4], which takes the reverse recovery process of SBD into calculation. However, it is not easy to obtain those recovery parameters such as snappiness factor and reverse recovery charge. In fact, the major impact is caused by the SBD junction diode and it could be derived much easier. Therefore, equations in [4] could be simplified by neglecting parameters except C_{jD} as:

$$\frac{V_{ds2}-V_{miller}+V_{th}}{t_3-t_2} = \frac{V_{CC}-V_{miller}}{R_g C_{gd1} + \frac{C_{oss1}+C_{jD}+C_L}{g_{fs}}} \tag{10}$$

where $C_{oss1} = C_{ds1}+C_{gd1}$. And the stage time could be derived as:

$$t_3 - t_2 = \frac{V_{ds2}-V_{miller}+V_{th}}{V_{CC}-V_{miller}}(R_g C_{gd1} + \frac{C_{oss1}+C_{jD}+C_L}{g_{fs}}) \tag{11}$$

Stage 4 [t_3, t_4] voltage falling time II: In this stage, the SiC MOSFET goes into ohmic region and v_{gs} continues to remain at V_{miller}. C_{gd} is being discharged as:

$$I_{g4} = C_{gd2}\frac{V_{miller}-V_{th}}{t_4-t_3} \tag{12}$$

where I_{g4} is the average gate current, and could be expressed as:

$$I_{g4} = \frac{V_{CC}-V_{miller}}{R_g} \tag{13}$$

The stage time could be derived as:

$$t_4 - t_3 = \frac{V_{miller}-V_{th}}{V_{CC}-V_{miller}}R_g C_{gd2} \tag{14}$$

Stage 5 [t_4, t_5] on-state operation: In this stage, v_{ds} and i_d will no longer be controlled by v_{gs}. Then the drain current will vibrate for a short time. Because this vibration only causes

smaller conduction loss compared with former stages, and it is difficult to calculate due to the loss of gate control, this process is not considered in the model. After vibrating, i_d keeps at I_L and only conduction loss exists.

B. Turn-off Transition (Fig. 3)

Stage 6 [t_5, t_6] turn-off delay time: In this stage, v_{drive} drops to V_{EE} and v_{ds} will not increase until v_{gs} drops to V_{miller}. C_{iss} is being discharged in this stage, and the delay time could be derived as:

$$V_{miller} = V_{EE}(1-\exp(-\frac{t_6-t_5}{\tau_{iss2}})) + V_{CC}\exp(-\frac{t_6-t_5}{\tau_{iss2}}) \quad (15)$$

where $\tau_{iss2} = R_g(C_{gs}+C_{gd2})$. Similarly as (4), this could be simplified as:

$$t_6 - t_5 = \frac{V_{CC}-V_{miller}}{V_{CC}-V_{EE}}\tau_{iss2} \quad (16)$$

Stage 7 [t_6, t_7] voltage rise time I: In this stage, the SiC MOSFET is still working at ohmic region. i_d stays at I_L until v_{ds} rises to $V_{miller}-V_{th}$ at t_7. v_{gs} remains at V_{miller} and impact of L_S is neglectable. Similarly as stage 4, this process could be represented as:

$$I_{g7} = C_{gd2}\frac{V_{miller}-V_{th}}{t_7-t_6} = \frac{V_{miller}-V_{EE}}{R_g} \quad (17)$$

And the stage time could be solved as:

$$t_7 - t_6 = \frac{V_{miller}-V_{th}}{V_{miller}-V_{EE}}R_g C_{gd2} \quad (18)$$

Stage 8 [t_7, t_8] voltage rise time II: In this stage, the SiC MOSFET reaches saturation region, and v_{ds} will rise rapidly to V_{DC} at t_8. i_d and v_{gs} start to fall, which will reach I_{d8} and V_{gs8} at t_8. C_{oss} and C_{jD} are charged at this stage, which should be taken into consideration. According to [5], C_{gs} is neglected when considering the gate current. The process could be expressed as:

$$I_L - I_{d8} = (C_{jD}+C_L)\frac{dV_{ds}}{dt} \quad (19)$$

$$I_L - I_{ch8} = (C_{jD}+C_L+C_{oss})\frac{dV_{ds}}{dt} \quad (20)$$

$$I_{g8} = C_{gd1}\frac{dV_{ds}}{dt} \quad (21)$$

where I_{ch8} is the channel current, which is represented as:

$$I_{ch8} = g_{fs}(V_{gs8}-V_{th}) \quad (22)$$

In this stage, the voltage drop across the parasitic inductance is neglectable as the discussion in [4]. The gate current could also be calculated as:

$$I_{g8}R_g = V_{gs8} - V_{EE} \quad (23)$$

By solving (19) ~ (23), I_{d8} could be expressed as:

$$I_{d8} = I_L - \frac{(C_{jD}+C_L)(I_L+(V_{th}-V_{EE})g_{fs})}{g_{fs}R_g C_{gd1}+C_{jD}+C_L+C_{oss}} \quad (24)$$

and the channel current:

$$I_{ch8} = I_L - \frac{(C_{jD}+C_L+C_{oss})(I_L+(V_{th}-V_{EE})g_{fs})}{g_{fs}R_g C_{gd1}+C_{jD}+C_L+C_{oss}} \quad (24)$$

Rewriting (19) with average current and voltage as:

$$\frac{I_L-I_{d8}}{2} = (C_{jD}+C_L)\frac{V_{DC}-V_{miller}+V_{th}}{t_8-t_7} \quad (25)$$

Meanwhile, V_{gs8} could also be derived using (22) and (25). The stage time could be calculated as:

$$t_8 - t_7 = \frac{2(g_{fs}R_g C_{gd1}+C_{jD}+C_L+C_{oss})(V_{DC}-V_{miller}+V_{th})}{I_L+(V_{th}-V_{EE})g_{fs}} \quad (26)$$

Stage 9 [t_8, t_9] current falling time: In this stage, v_{gs} and i_d continues to fall and the load current begins to divert from SiC MOSFET to SBD. When v_{gs} reaches V_{th} at t_9, i_d reduces to zero. Similarly as stage 2, C_{iss} is discharged as:

$$I_{g9} = C_{iss1}\frac{V_{gs8}-V_{th}}{t_9-t_8} = C_{iss1}\frac{I_{ch8}}{g_{fs}(t_9-t_8)} \quad (27)$$

The decreasing current will induce a voltage across the parasitic inductance, and for the drive loop it could be expressed as:

$$I_{g9}R_g = \frac{V_{miller}+V_{th}}{2} - V_{EE} - L_S\frac{I_{ds8}}{t_9 - t_8} \tag{28}$$

By substituting (28) into (27), the stage time could be derived as:

$$t_9 - t_8 = \frac{\tau_{iss1}I_{ch8} + g_{fs}L_S I_{ds8}}{g_{fs}\left(\frac{V_{miller}+V_{th}}{2} - V_{EE}\right)} \tag{29}$$

Stage 10 [t_9,∞] off-state operation: In this stage, v_{gs} falls to V_{EE} gradually, and the channel current of SiC MOSFET will be zero. v_{ds} will have ringing phenomena due to parasitic parameters in the circuit and causing drain-source current ripples. Similarly as stage 5, this ringing phenomena is not considered in the model. After that, the load current will totally flow though SBD, and only conduction loss exists.

III. Comparison of Experimental Result and Calculation

A test-bench of DPT is built to verify the proposed model. The SiC MOSFET under test is CMF20120D and the SBD is C4D30120D, both from Cree Inc.

The V_{DC} is set at 500V, and v_{drive} is set at 20V for turn-on transient and -5V for turn-of transient. The load current is kept at 18.3A and gate resistance R_g is changed from 5ohm to 20ohm to change the working condition of the SiC MOSFET. The experimental results are compared with calculations using both the model in this article and the model in [5].

Fig. 6 shows the turn-on time with different gate resistances. Two models get similar calculation results, and total turn-on time have about 60 ns error compared with experimental data. Fig. 7 shows the current rise time of turn-on transition, and the calculated time have about 5~20 ns error compared with experiment, which indicates that the error in total turn-on time calculation is mainly caused in voltage falling stages. For further improvement, more detailed discussion on voltage falling time is supposed to be done.

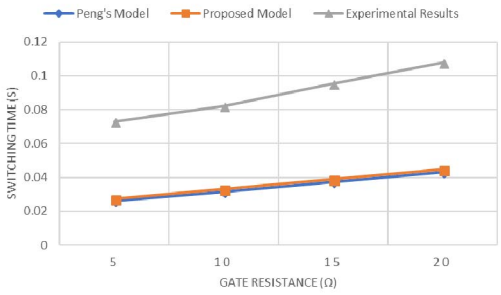

Fig. 6. Turn-on Time with Different Gate Resistances

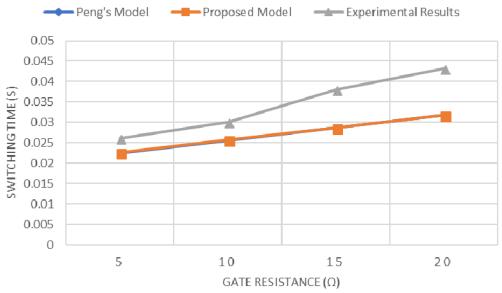

Fig. 7. Current Rise Time with Different Gate Resistances

Fig. 8 shows the turn-off time with different gate resistances and Fig. 9 shows the voltage rise time. Unlike turn-on transition, calculation results by two models have great difference in turn-off transition, and the model proposed in this article is more accurate than Peng's model in [4].

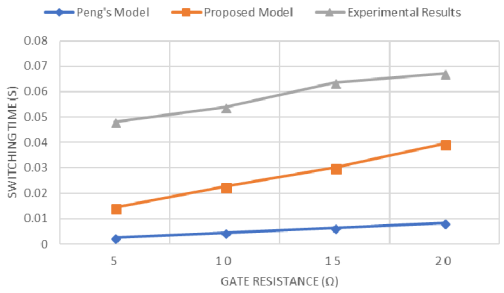

Fig. 8. Turn-Off Time with Different Gate Resistances

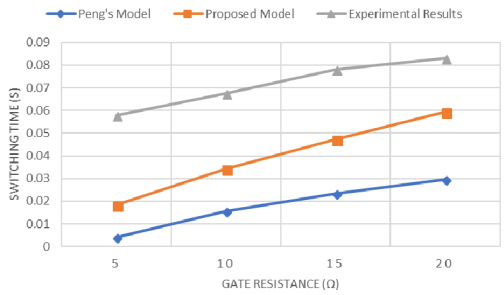

Fig. 9. Voltage Rise Time with Different Gate Resistances

Compared with models in [4] and [6], which use differential equations to calculate the MOSFET switching transitions, the model proposed in this paper only uses average value equations. Although the former could describe some details like ringing phenomena, solving those differential equations always takes longer time than algebraic equations. Besides, as switching time is important for designing and sometimes those details are neglectable, the model in this paper may have advantage over the former ones.

For future researches, the accuracy of the proposed model could be furtherly improved, especially for the turn-on transition. To obtain a better hard-switching turn-on transition model, detailed studies should be focused on SBD, which has a great impact on voltage falling times and is not thoroughly considered in this MOSFET model.

IV. Conclusion

A behavioral model of SiC MOSFET on hard-switching condition is proposed. Nonlinearity in the junction capacitance of SiC MOSFET, diode junction capacitance and parasitic elements in the circuit are considered in the model. The comparison with the experimental results shows that the model can provide a simple prediction of SiC MOSFET switching time on hard-switching condition, which allows it to be applied on large scale simulations or other circuit design applications.

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