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SESSION 12
High Performance Optical Receivers

A 0.96pJ/b 7×50Gb/s-per-Fiber WDM Receiver with Stacked 7nm CMOS and 45nm Silicon Photonic Dies

Mayank Raj[1], Chuan Xie[1], Ade Bekele[1], Adam Chou[1], Wenfeng Zhang[1], Ying Cao[1], Jae Wook Kim[1], Nakul Narang[2], Hongyuan Zhao[2], Yipeng Wang[2], Kee Hian Tan[2], Winson Lin[1], Jay Im[1], David Mahashin[1], Santiago Asuncion[1], Parag Upadhyaya[1], and Yohan Frans[1]

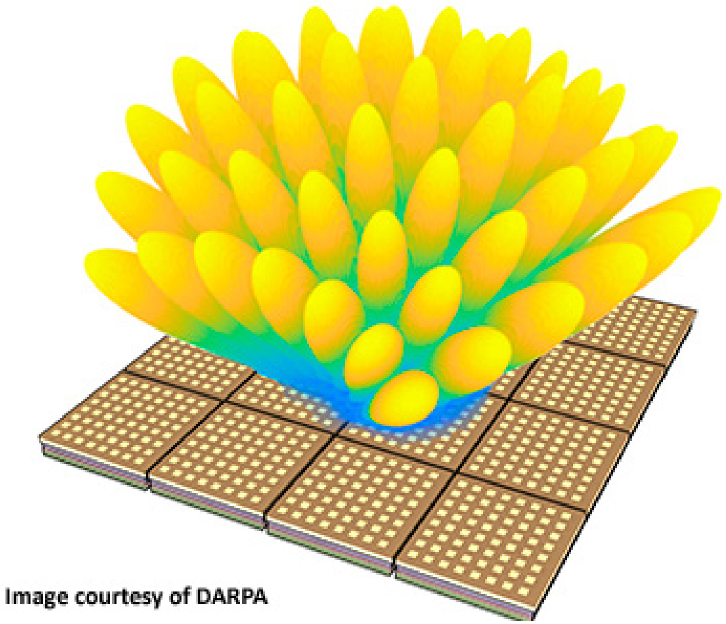
[1]AMD, San Jose, CA

[2]AMD, Singapore, Singapore

Outline

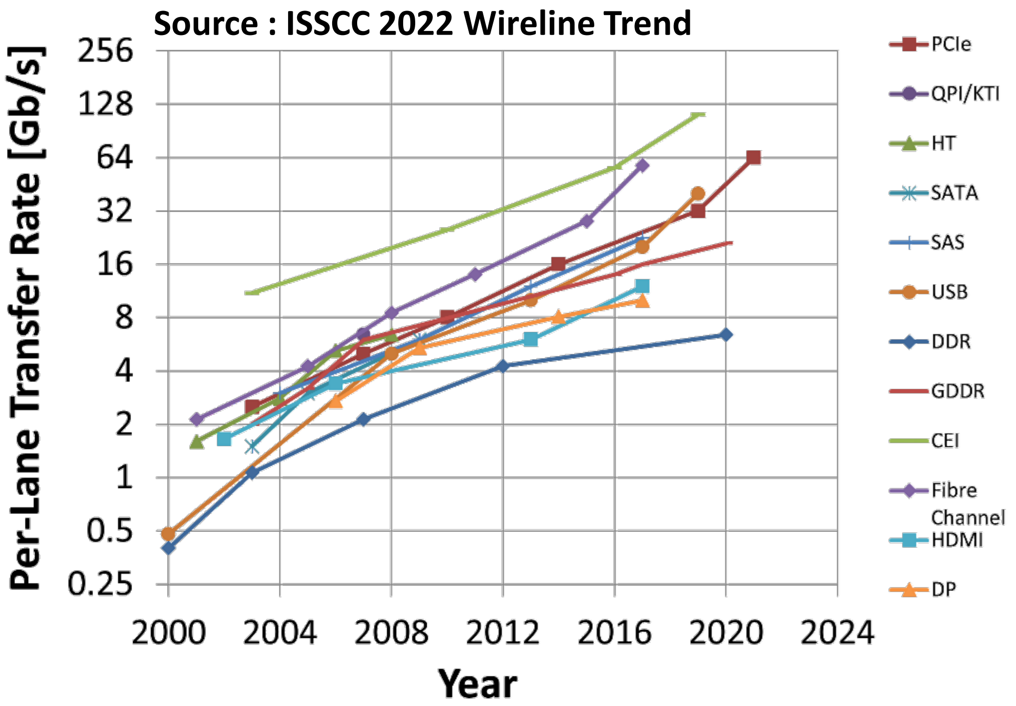
- Motivation
- Hybrid Integration
- Optical Filter (PIC)
- Proposed RX (EIC)
- Measurement Results
- Conclusions

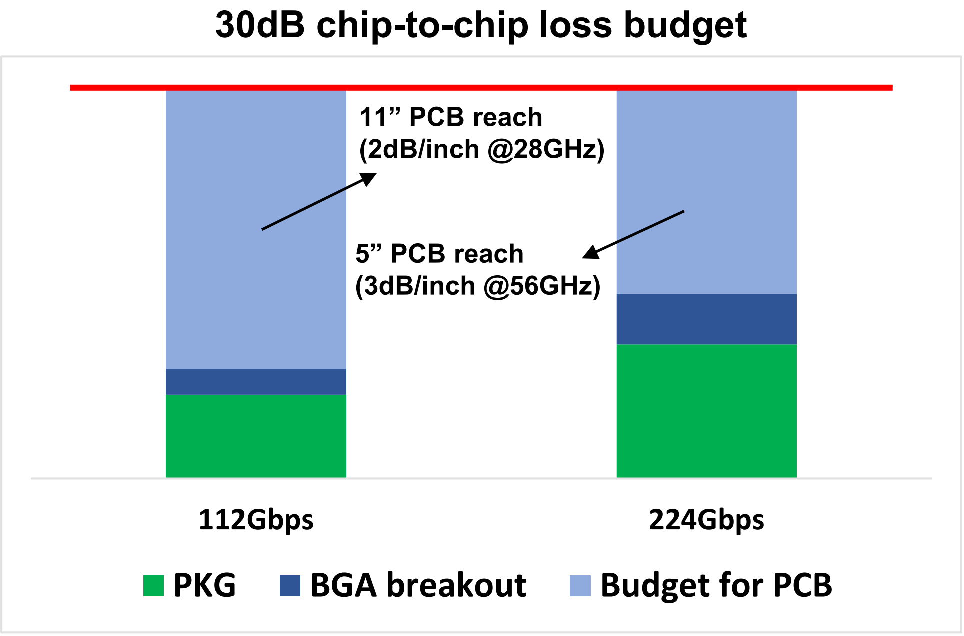
Computing Trend: Distributed/Disaggregated



- Trend: distributed/disaggregated compute nodes over long distance (e.g., Phased Array Digital Beamforming, High-Performance Computing)
- Need: high BW, low-power, low-latency, long-reach interconnect

Electrical Link Will Have Reach Issue

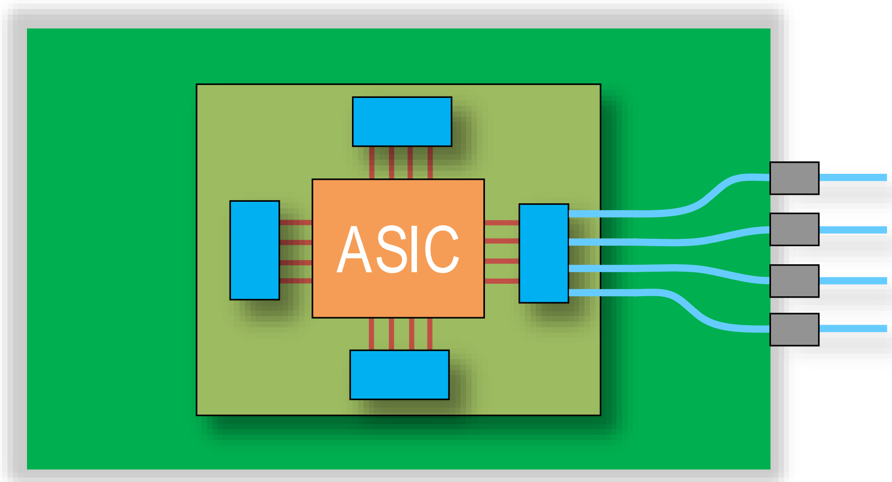




Source : OIF/IEEE conferences

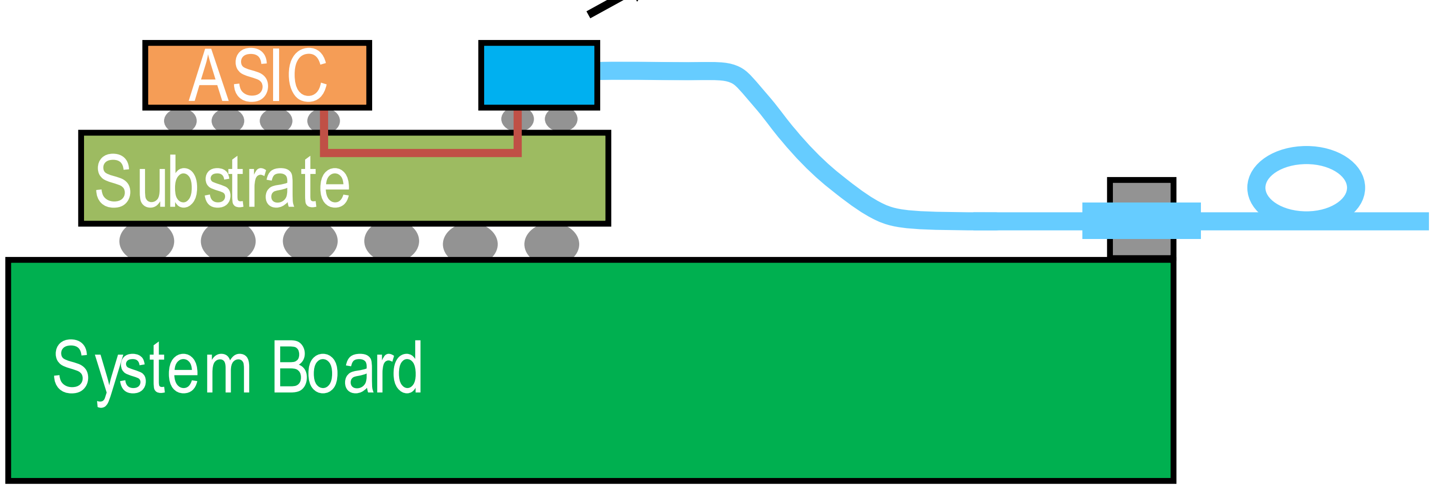
- Data-rate is growing ~2x every 3-4 years
- Running into reach/distance issue at 100Gbps+, need higher cost (e.g., cables and retimers to extend reach)
- In-package Si-Photonics Transceiver is a potential solution

Optical Link Application



Top View

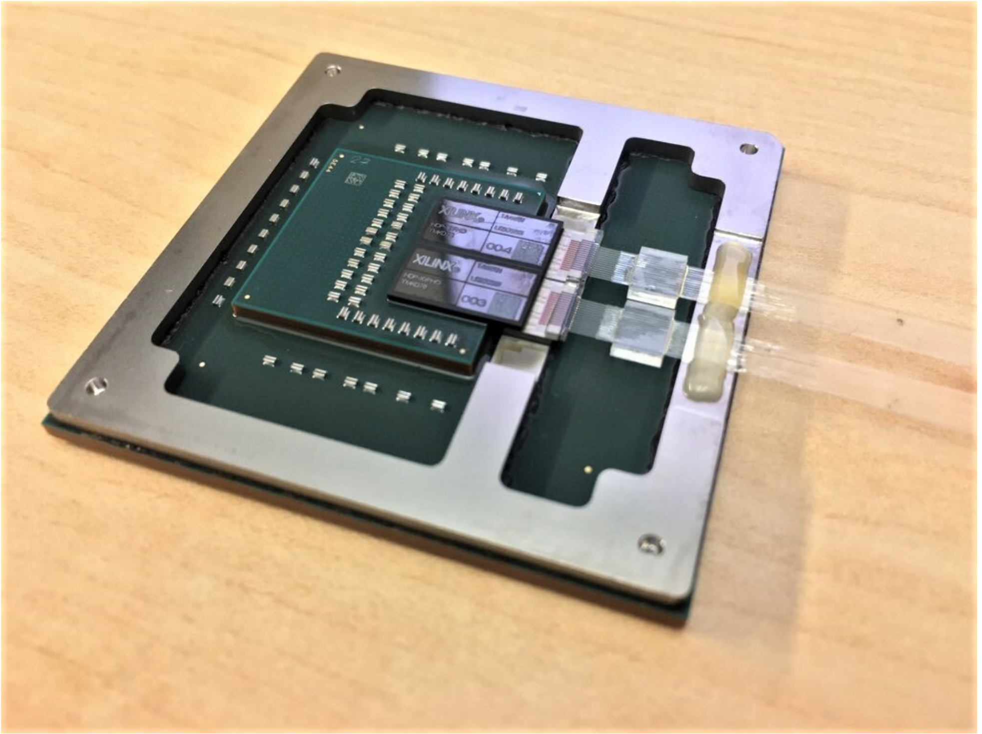
This work is focused on RX O-E

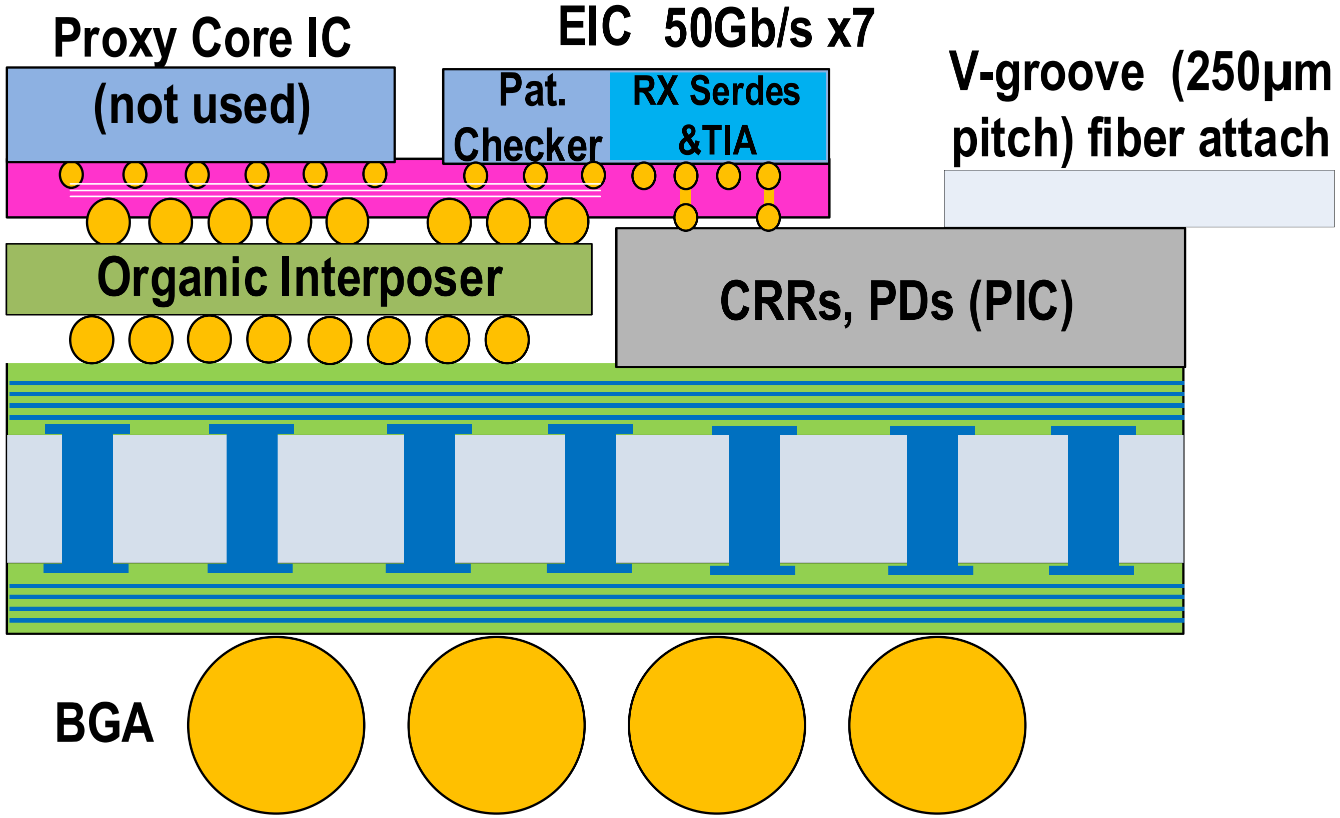


Side View

- Optical error free w/o FEC – important for compute applications
- External laser to alleviate heating issues
- Single mode – (10m-2km)
- Energy efficient

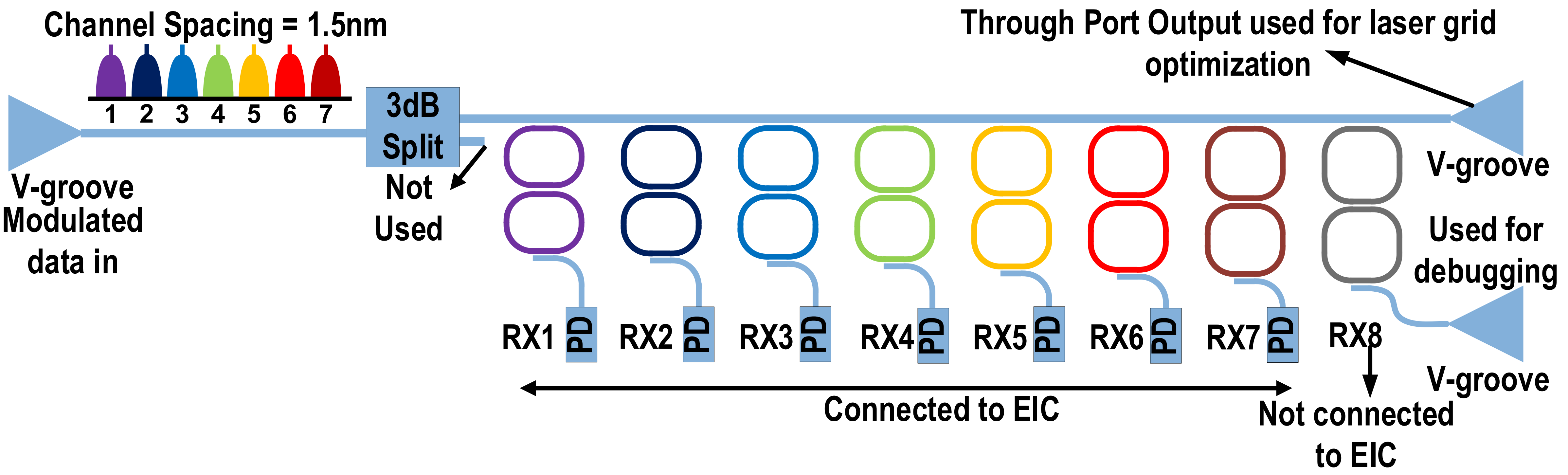
MCM Prototype





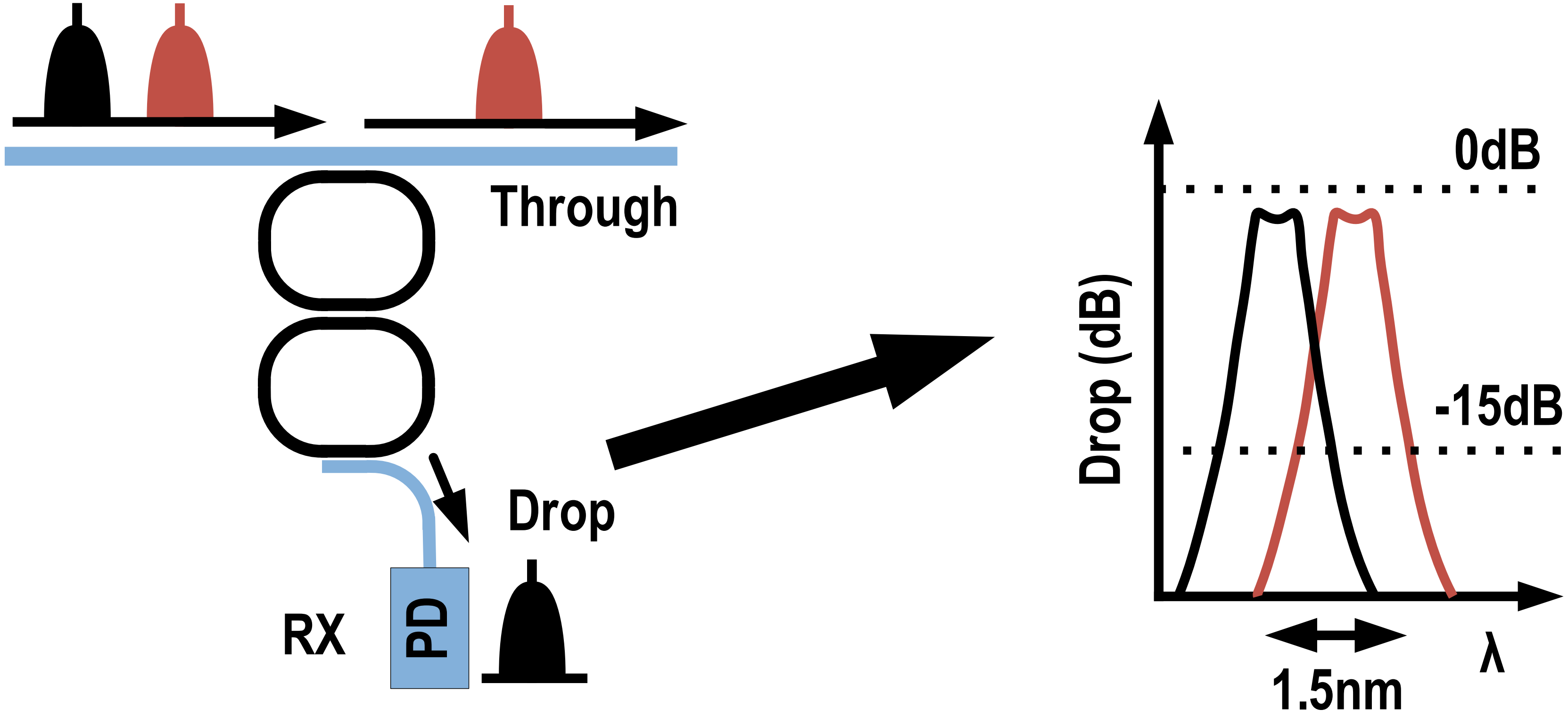
- EIC RX input directly on top of the PIC using Cu-pillar bumps
- 15-fiber array with a 250µm pitch via V-grooves

PIC Architecture



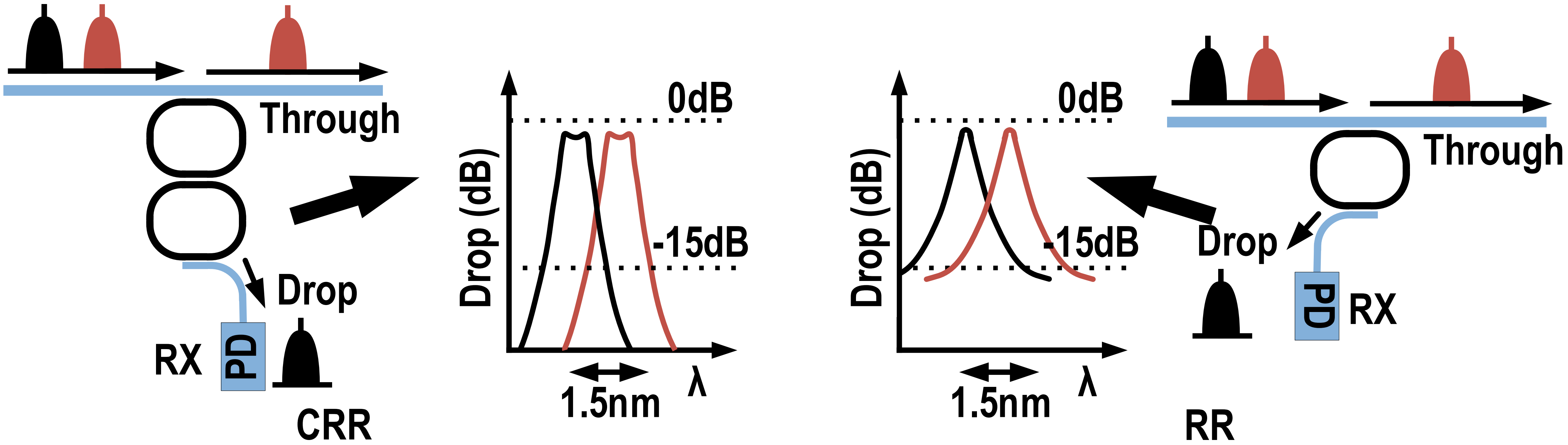
- 7λ WDM with 1.5nm channel spacing: 50Gb/s NRZ per lambda
- Cascaded Ring Resonator (CRR) based WDM filter

CRR WDM Filter



- <1.5dB insertion loss (IL)
- Crosstalk of <15dB
- 1.5nm channel separation

WDM Filter – advantages of CRR over RR

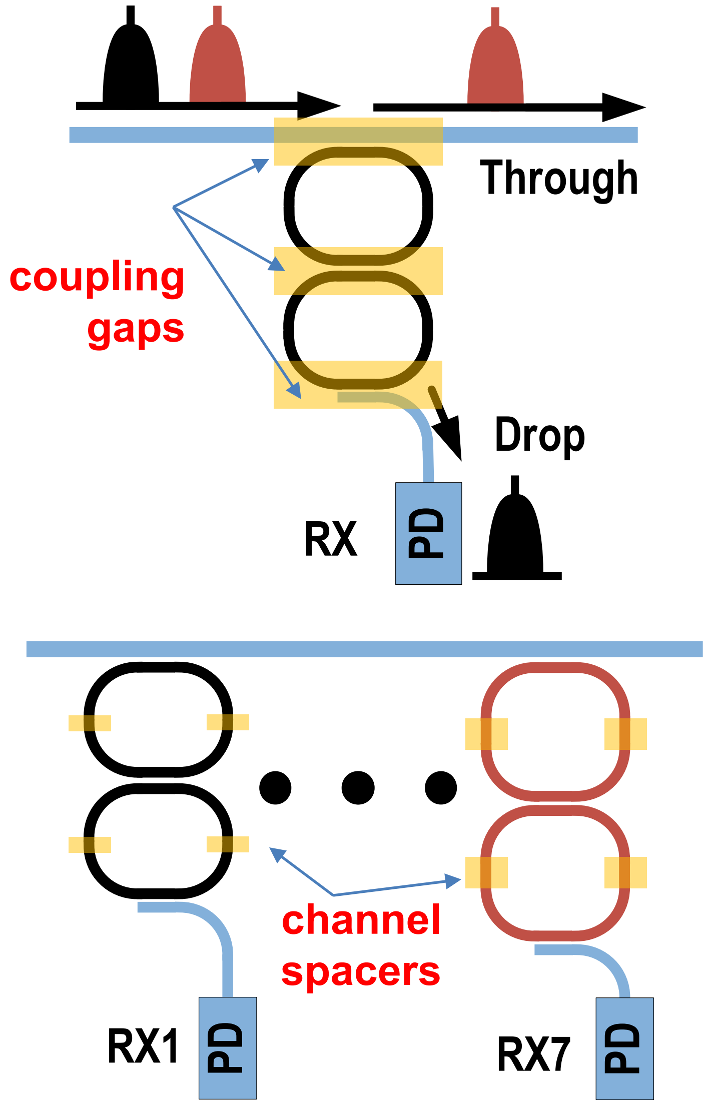


- 40dB/dec roll off → better channel isolation
- Flat top → better bandwidth
- Flat top → kinder to channel misalignment

CRR design: Improving process variation

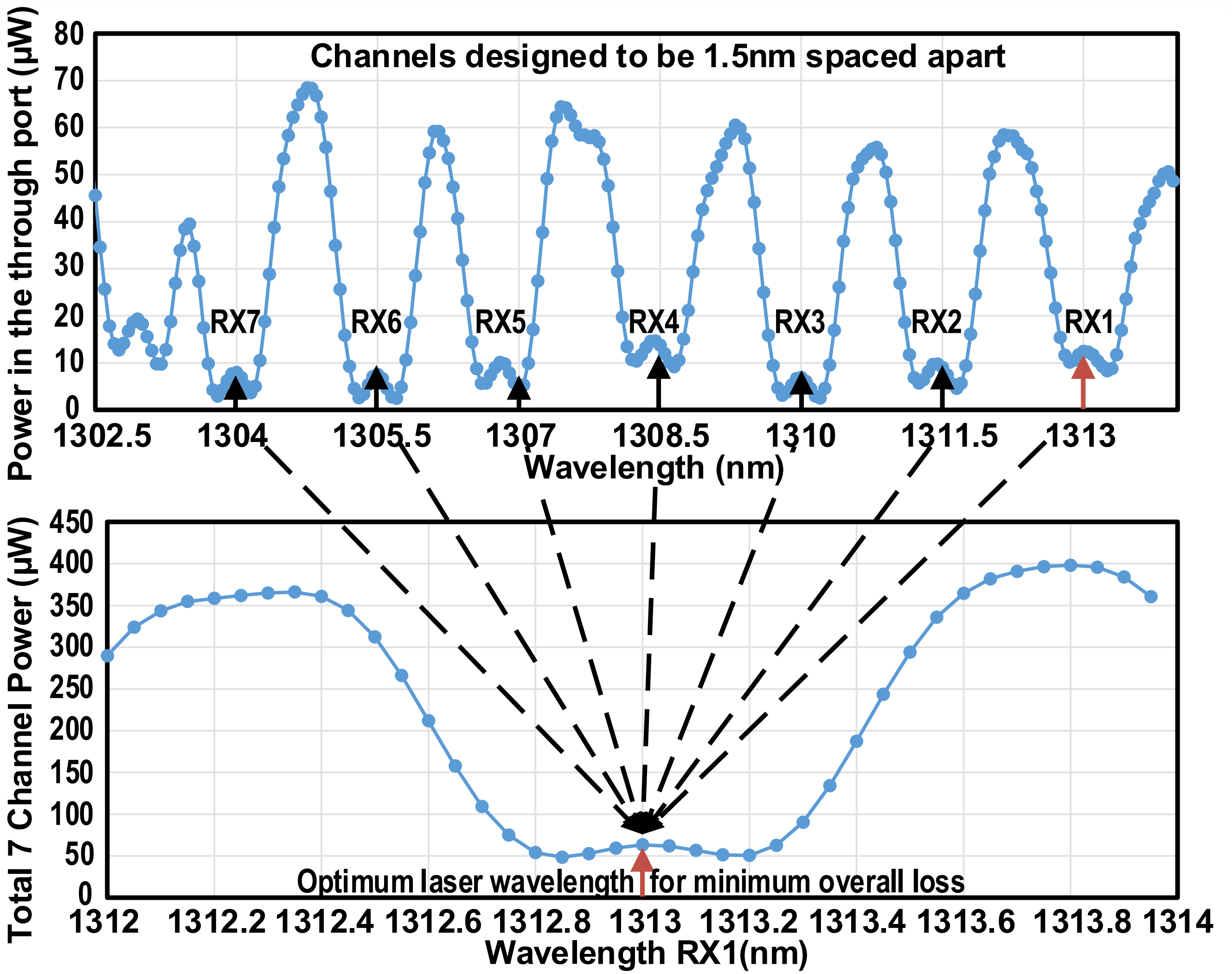
- Racetrack design → longer coupling section
- Coupling gap can be wider

- Channel spacing implemented by vertical spacers
- Same coupler design used in all 8 filters



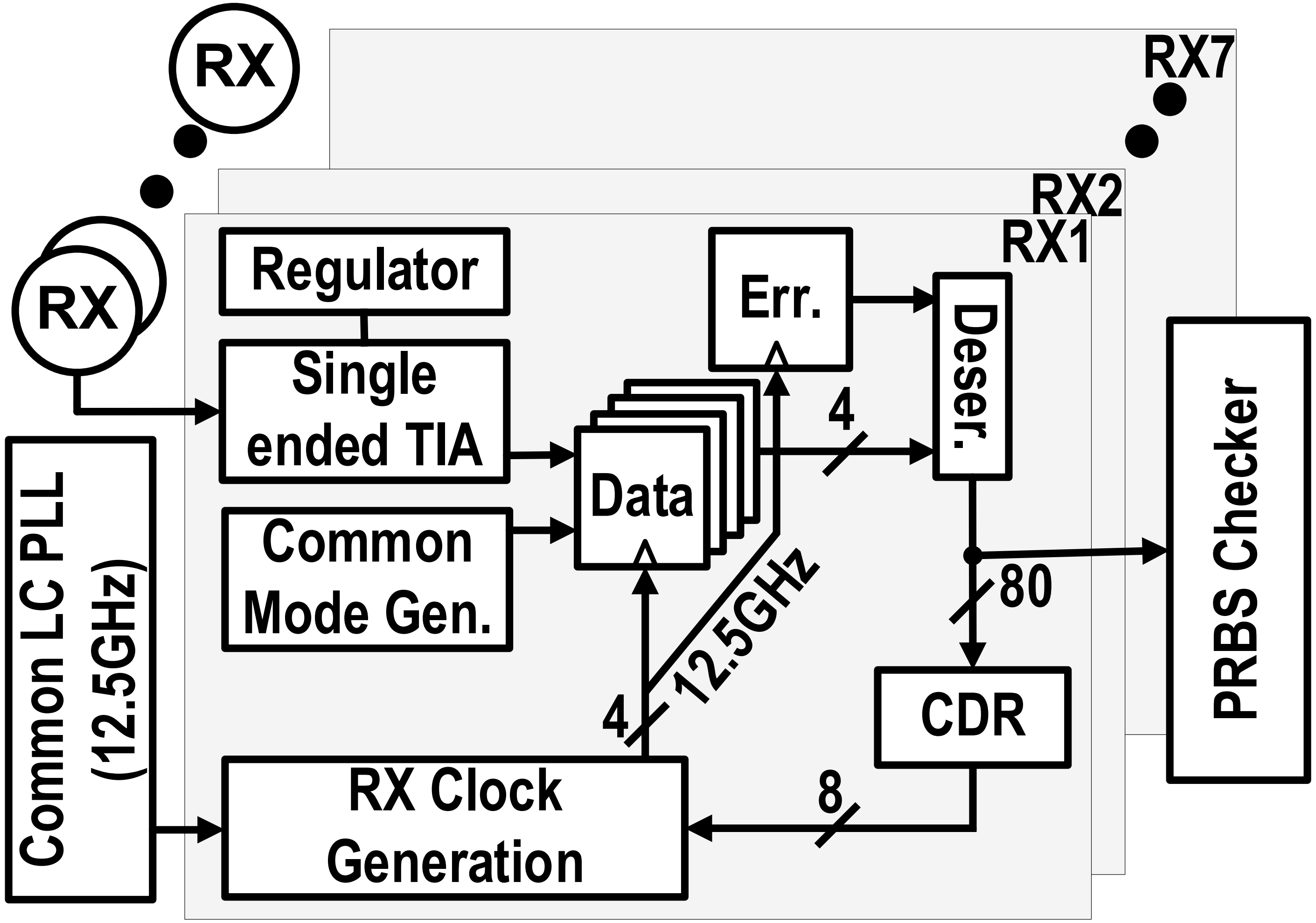
Matching CRRs with laser grid

- Single through port to measure overall RX response
- Sum the power for RX1-RX7
- Sweep RX1's lambda
- RX2-RX7 lambda is fixed due to 1.5nm grid
- Find RX1 lambda with lowest overall power (1313nm)

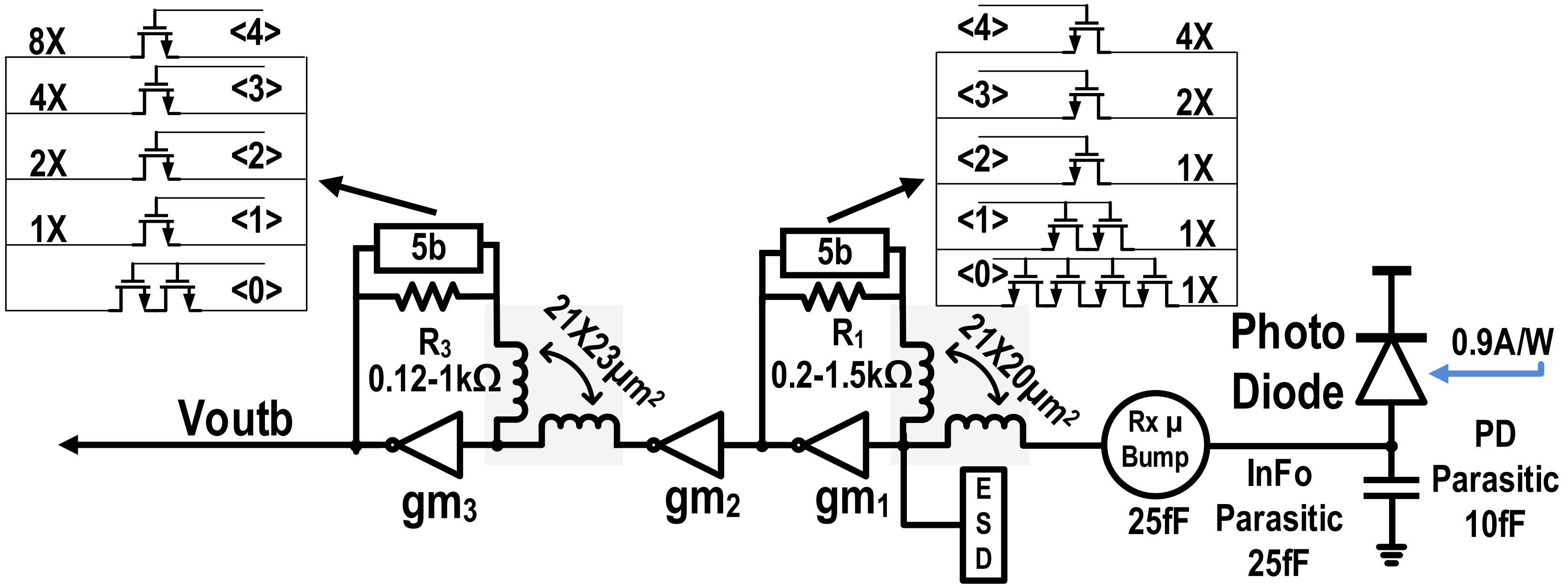


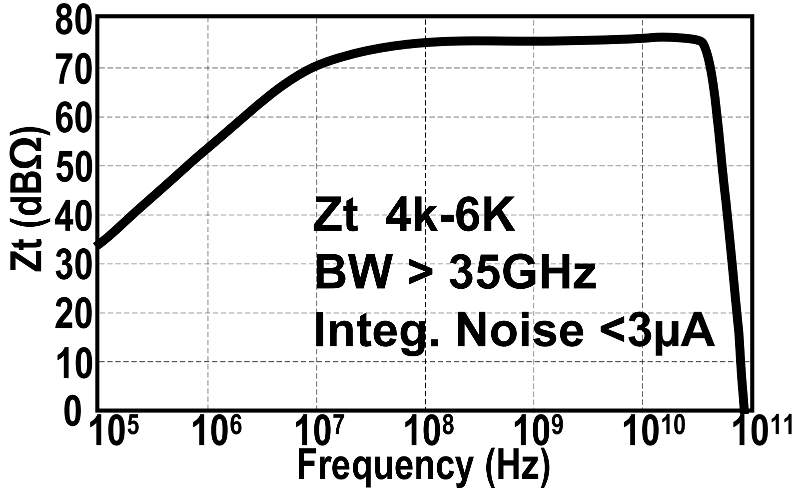
EIC: Architecture

- 50Gb/s 7 channels
- Quarter rate RX clocking
- Common LC PLL
- On-chip PRBS checkers
- Design focus on power and area reduction



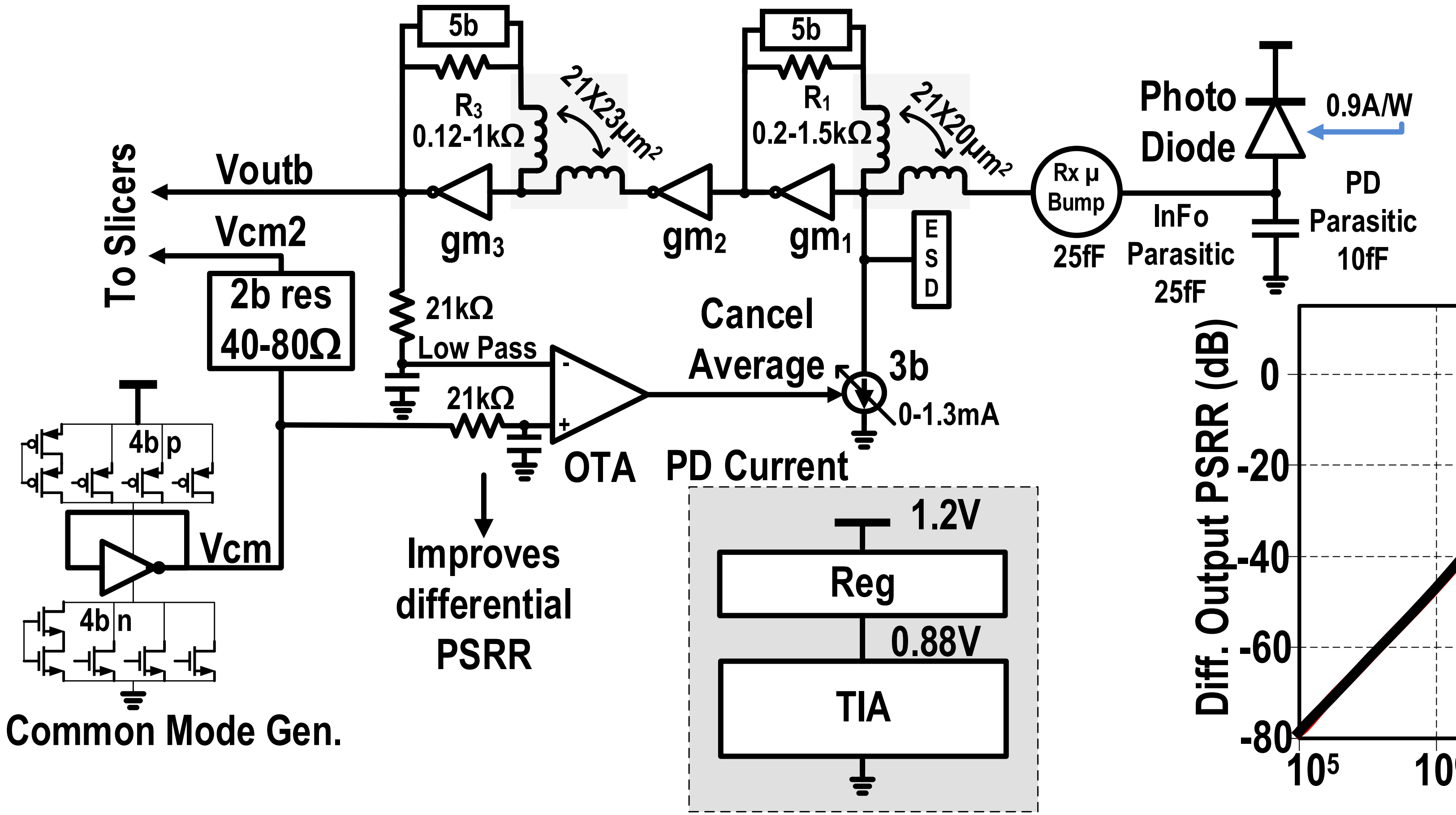
TIA Architecture

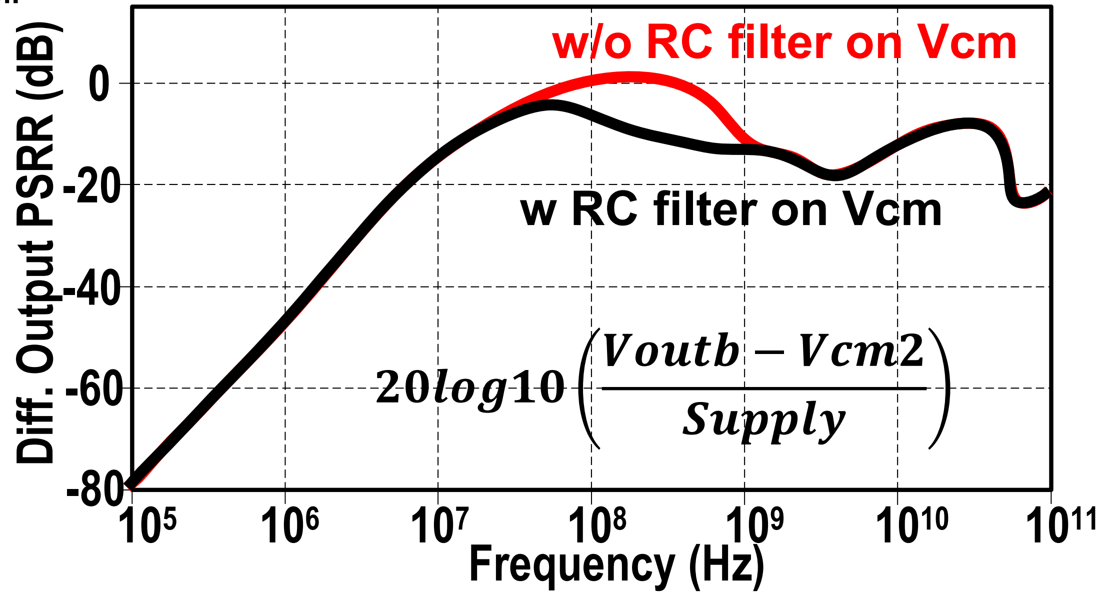




- Single ended inverter-based TIA to utilize gm/C scaling
- T-coil peaking to reduce number of stages and save power
- Programmable NMOS based resistor to control gain/BW

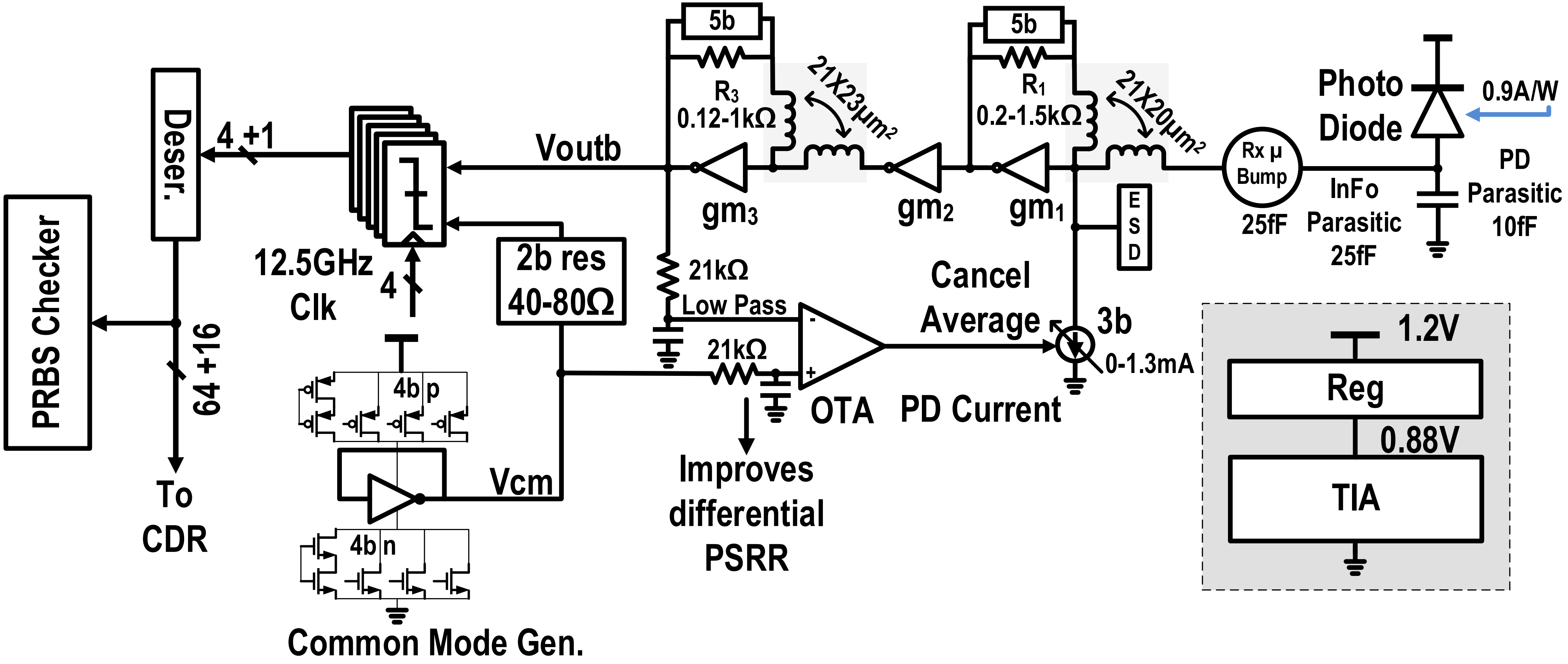
TIA DC loop and PSRR





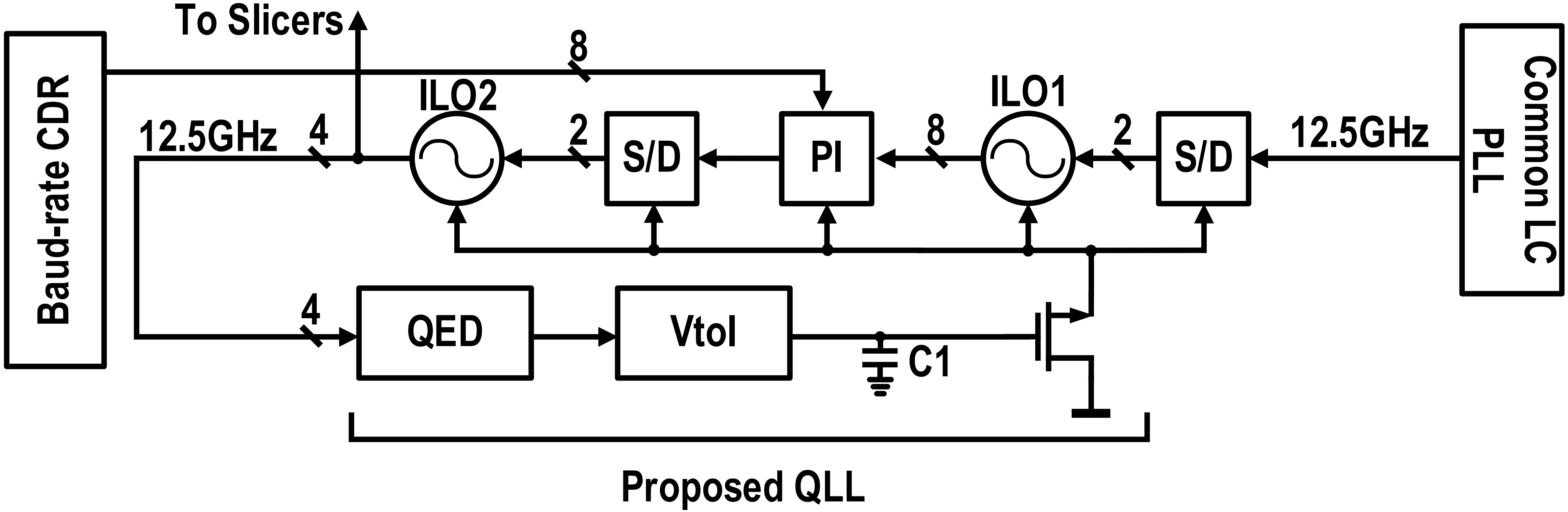
- Regulated supply with DC loop and common mode gen

Overall RX architecture



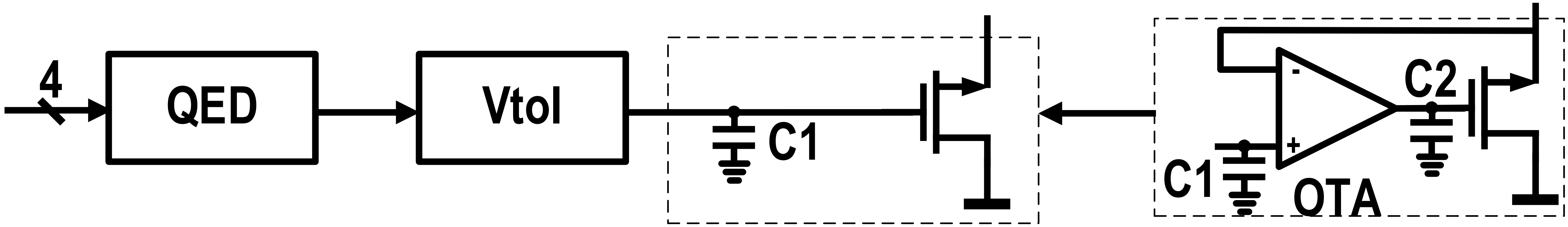
- Voutb is directly fed to the 4 data and 1 error slicers
- Kickback matched on the Vcm and Voutb node

Clock Generation for CDR



- Baud-rate CDR with ILO-PI-ILO architecture
- QLL corrects I/Q mismatches and generates supply voltage
- Reference 12.5GHz is generated by a common LC PLL

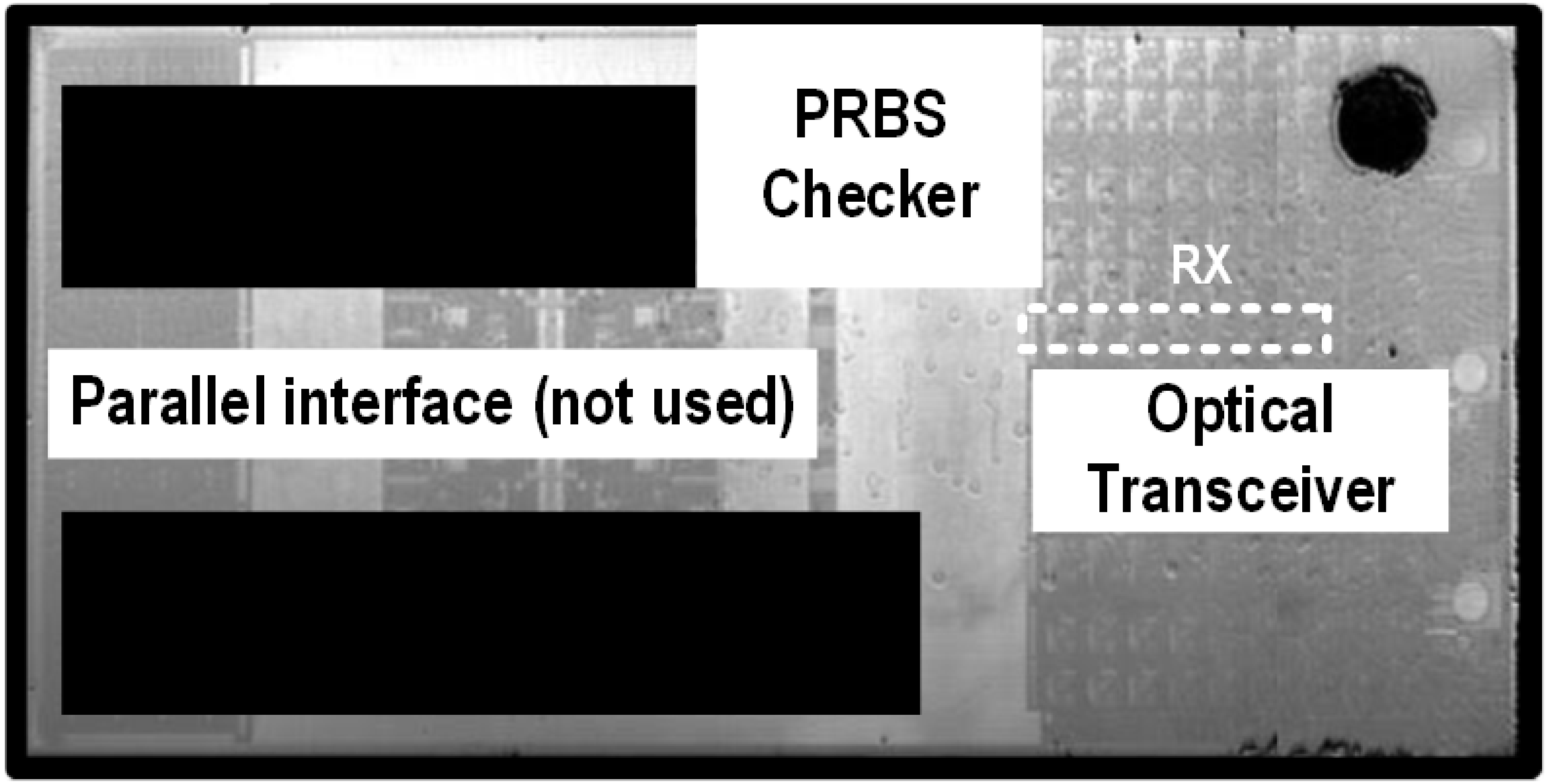
QLL Area Savings



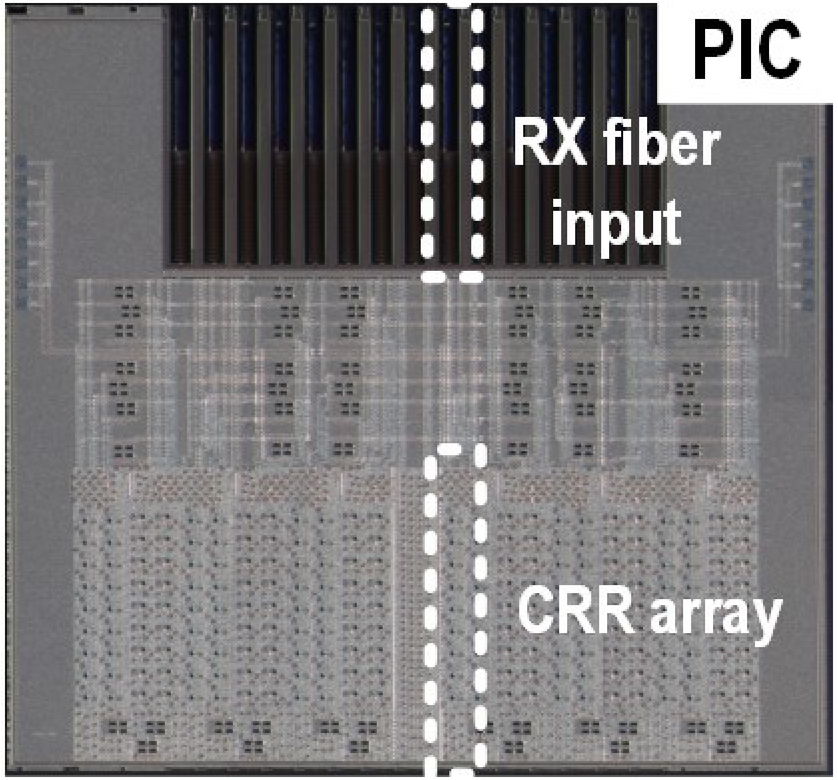
C. F. Poon *et al.*, *JSSC,* 2022

- QED driven Voltage to Current (V-to-I) circuit directly drives the NMOS source follower of the regulator
- Remove the OTA, the filter capacitor C2, and reduce C1
- Total of 50% area reduction compared to prior art

Chip Micrographs



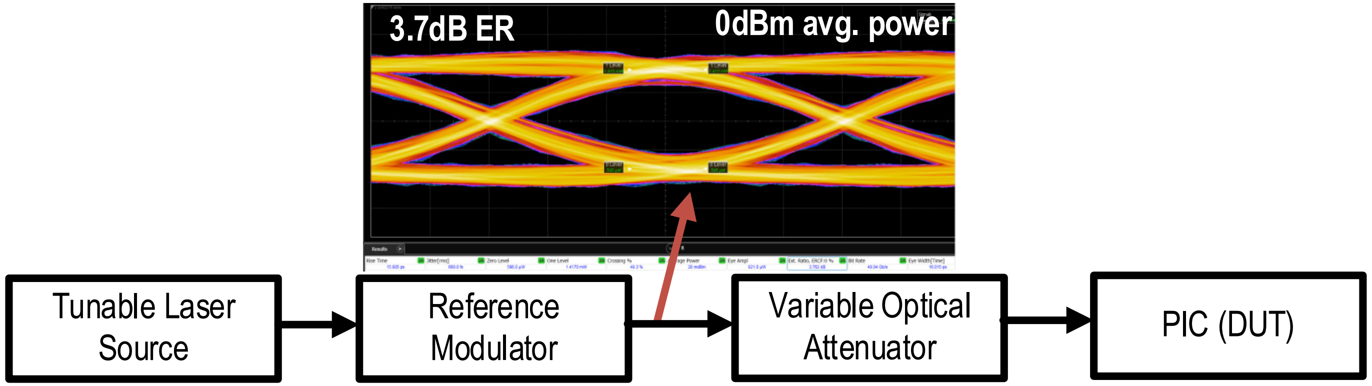
EIC: 7nm FinFET

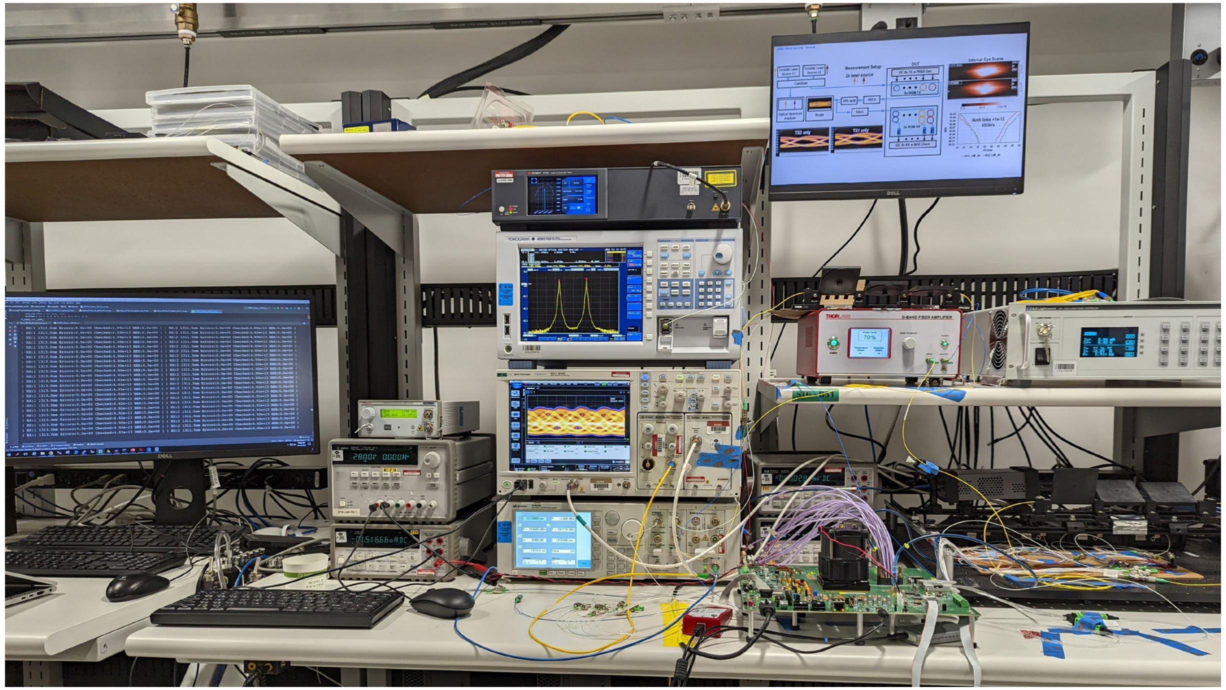


PIC: 45nm SOI

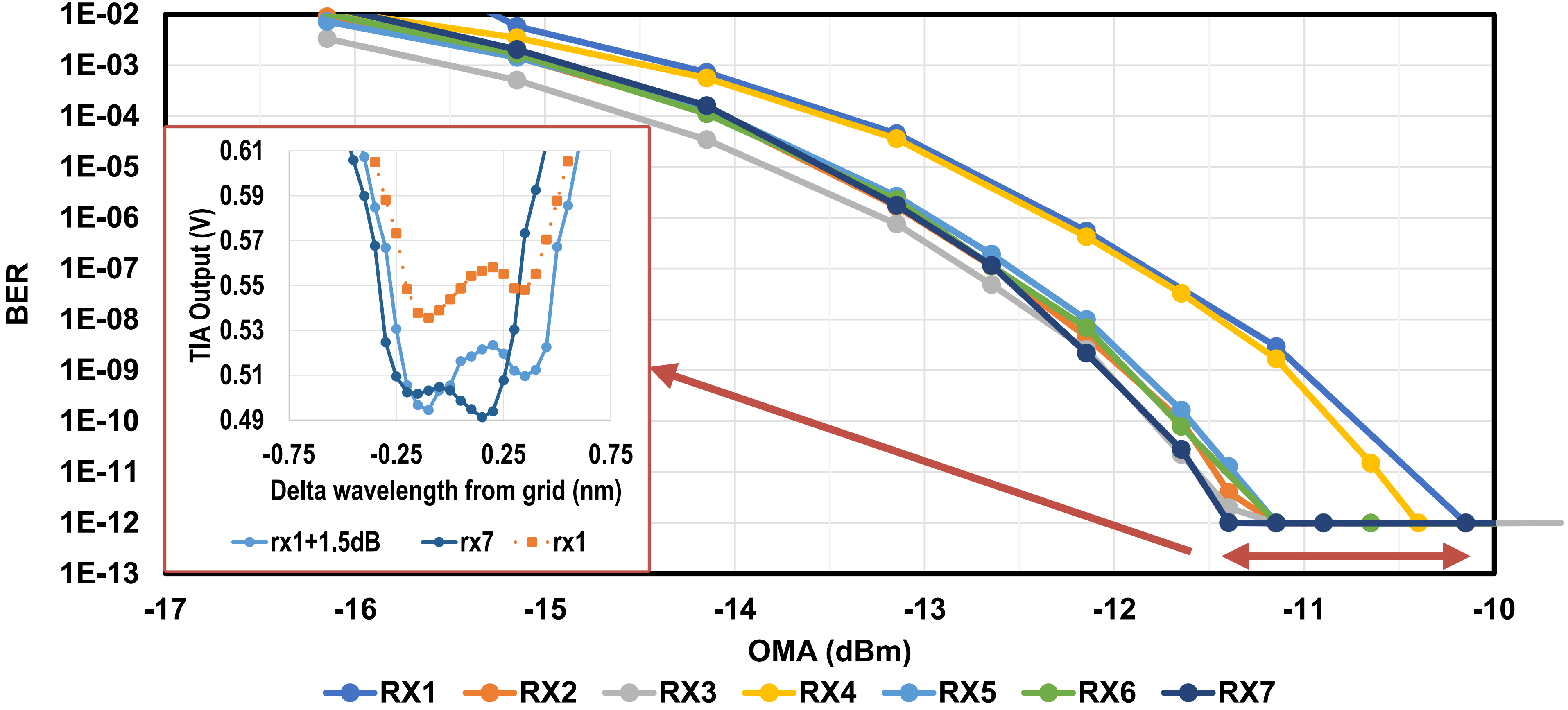
Measurement Setup

- Tunable laser source for wavelength sweep
- Reference modulator to generate optical data input
- Variable optical attenuator for sensitivity measurements



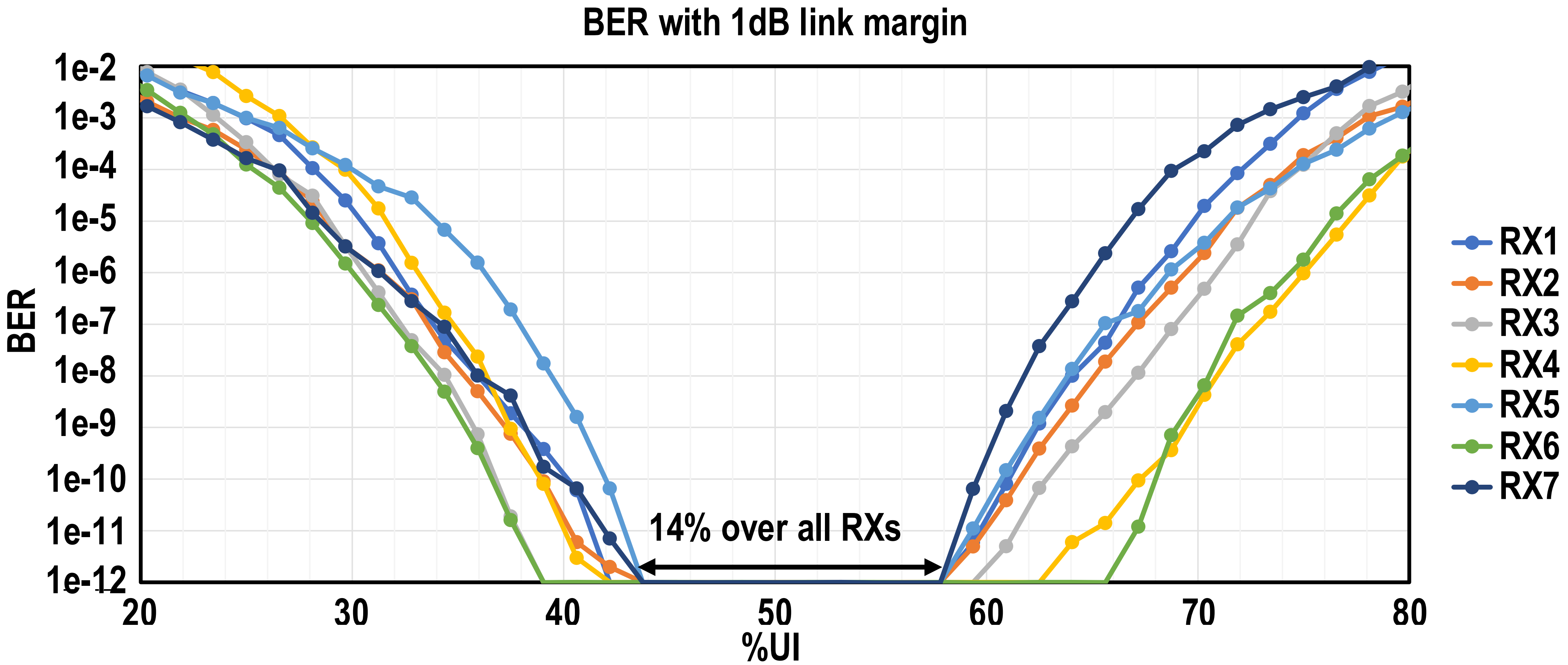


RX OMA Sensitivity (BER 1e-12)



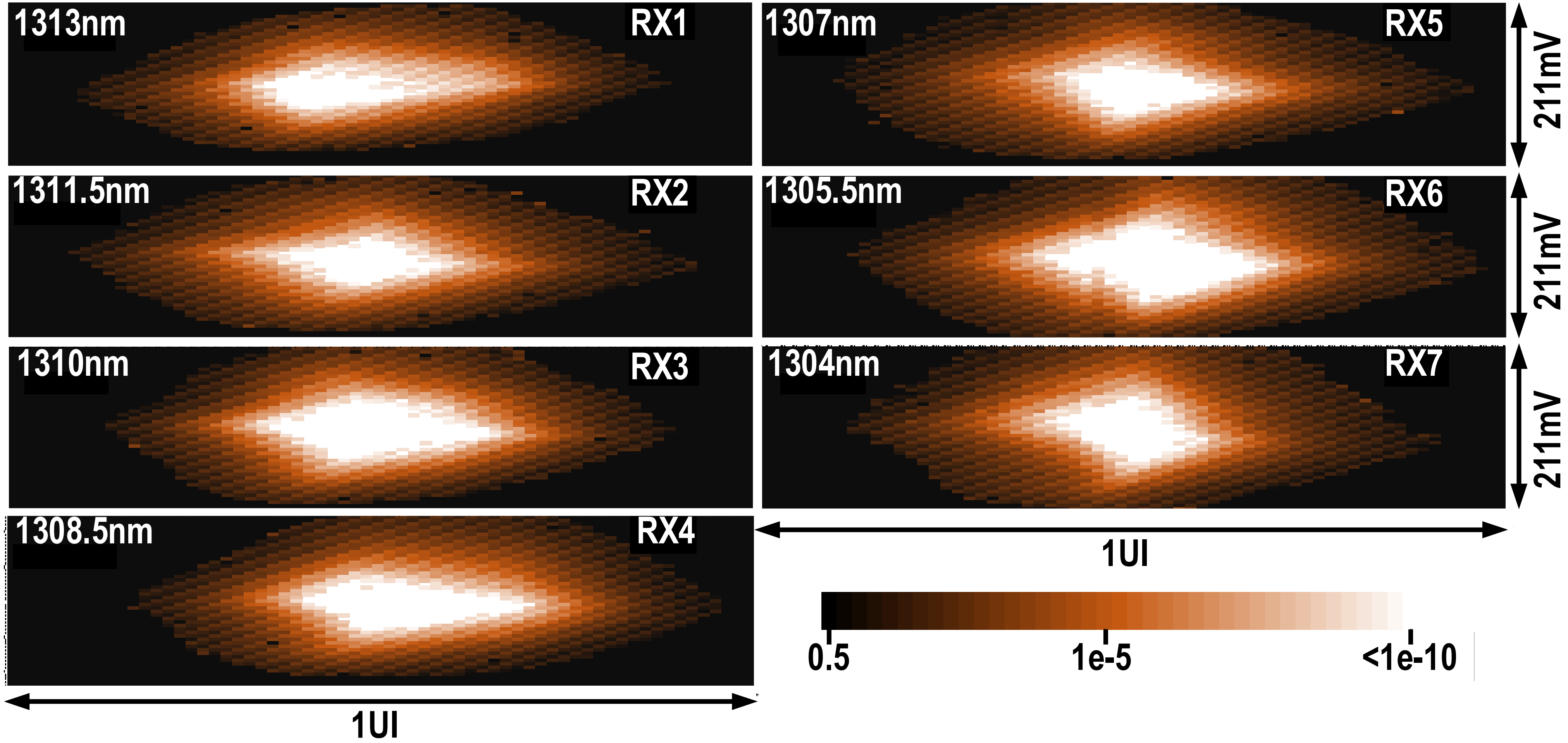
- RX1-RX7 show median sensitivity of -11.1dBm OMA
- Sensitivity reduction in RX4 and RX1 → CRR insertion loss (from process variation)

RX BER Bathtub Measurements



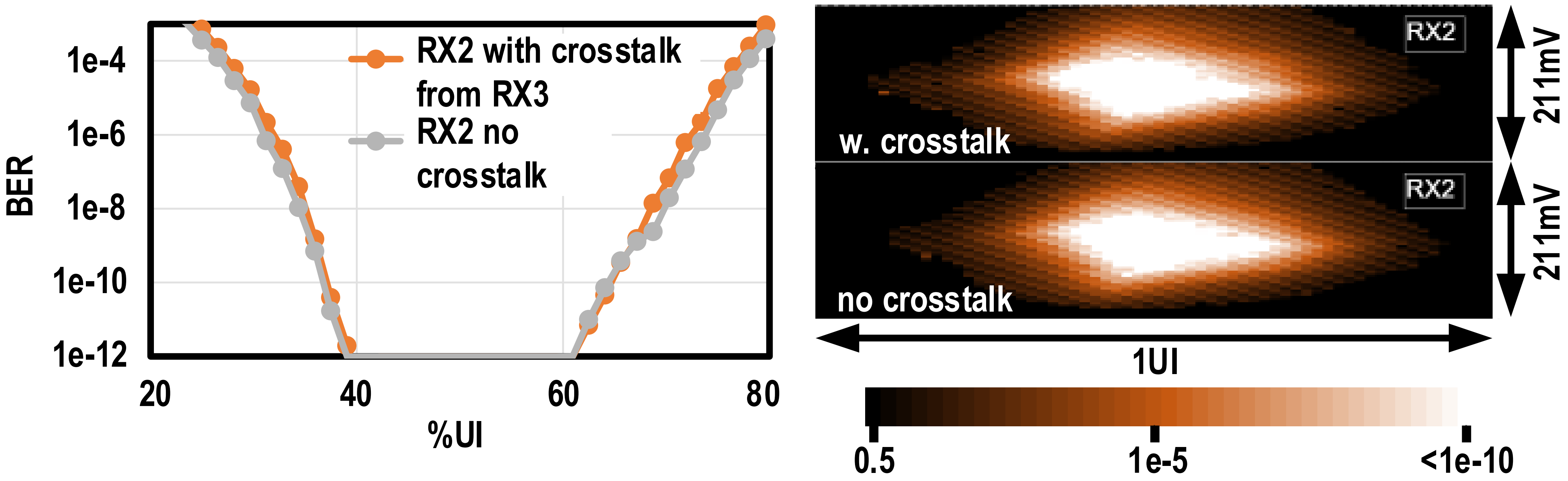
- RX1-RX7 1e-12 error free without FEC
  - This is despite RX5's laser wavelength being off from the filter center by 200pm (due to process variation)

RX Internal 2D Eye Scans



- RX1-RX7 show healthy vertical and horizontal eye openings

RX2–RX3 crosstalk



- RX2-RX3 enabled at the same time using a 2-λ laser source
- Minimal crosstalk impact on vertical and horizontal eye margins

Performance Comparison

	ISSCC 15	JSSC 20	ISSCC 21	JSSC 17	**This Work**
Technology	40nm CMOS	16nm FinFET	28nm CMOS	14nm FinFET	**7nm FinFET**
Integration	Hybrid	Hybrid	Hybrid	Hybrid	**Hybrid**
Data Rate	4x20Gb/s	50 Gb/s	100 Gb/s	64 Gb/s	**7x50 Gb/s**
WDM	Yes	No	No	No	**Yes**
Channel Grid	2.4 nm	NA	NA	NA	**1.5 nm**
Wavelength	1540-1550 nm	1570 nm	1310 nm	850 nm	**1304nm - 1313nm**
Modulation	NRZ	NRZ	4-PAM	NRZ	**NRZ**
Input Cap	80 fF	90 fF	70 fF	69 fF	**60 fF**
PD Resp.	-	1 A/W	1 A/W	0.52 A/W	**0.9 A/W**
Sens. (OMA)	-7.2 dBm	-10.9 dBm	-11.1 dBm for 56 Gb/s NRZ	-9dBm at 56Gb/s	**-11.4 dBm***
RX Area	-	0.27mm^2	0.45 mm^2	0.028 mm^2	**0.031 mm^2**
RX Efficiency	0.73 pJ/bit**	1.66 pJ/bit	1.17 pJ/bit	1.4 pJ/bit	**0.96 pJ/bit**

*Best across 7 channels **No SerDes

Conclusions

- 7x50Gb/s WDM receiver
- Error free (BER<1e-12) performance w/o FEC
- Hybrid integration with EIC in 7nm and PIC in 45nm SOI process
- RX occupies 0.031mm^2 while consuming 0.96pJ/bit
- Median sensitivity of -11.1dBm (OMA) across 7 RX channels

Acknowledgements

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- The authors thank the AMD design, layout, and verification teams

Disclaimer

A 7 pA/√Hz Asymmetric Differential TIA for 100 Gb/s PAM-4 links with -14 dBm Optical Sensitivity in 16 nm CMOS

Kadaba R. Lakshmikumar[*1], Alexander Kurylak[*1], Romesh Kumar Nandwana[*1], Bibhu Das[1], Joe Pampanin[1], Mike Brubaker[1], Pavan Kumar Hanumolu[2]

[1]Cisco Systems Inc., Allentown, PA, USA
[2]University of Illinois at Urbana-Champaign, IL, USA
*Equally Credited Authors (ECAs)

Outline

- Motivation
- Single-ended TIA
- Conventional differential TIA
- Proposed asymmetric differential TIA
- Experimental validation
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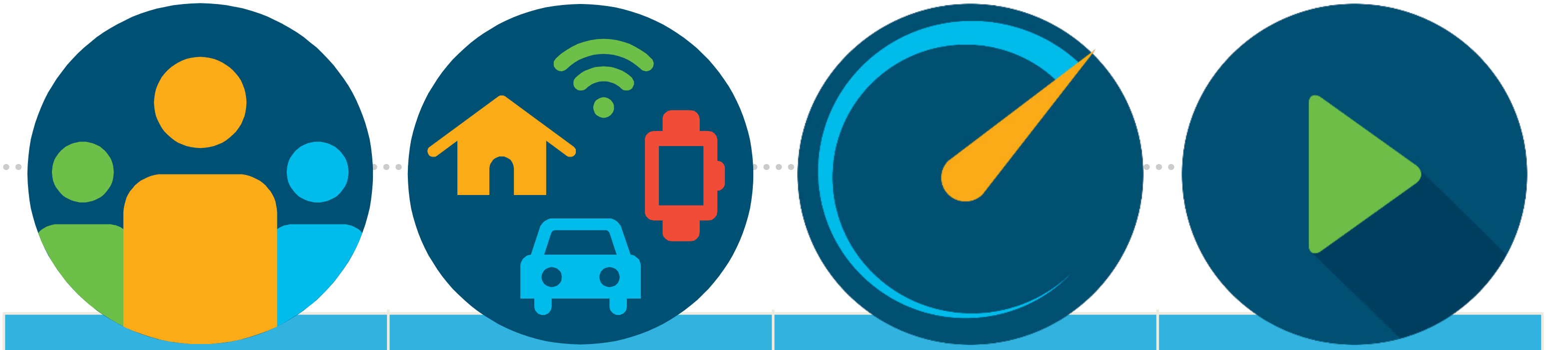
Global Internet Growth and Trends

Key Digital Transformers



	More Internet Users	More Devices & Connections	Faster Broadband Speeds	More Video Viewing
2018	3.9 Billion	18.4 Billion	45.9 Mbps	73% of Traffic
2023	5.3 Billion	29.3 Billion	110.4 Mbps	82% of Traffic

Source: Cisco Annual Internet Report, 2018–2023

Data Center Traffic and Energy Consumption

A Within Data Center (71.5%)

Storage, production and development data, authentication

B Data Center to Data Center (13.6%)

Replication, CDN, intercloud links

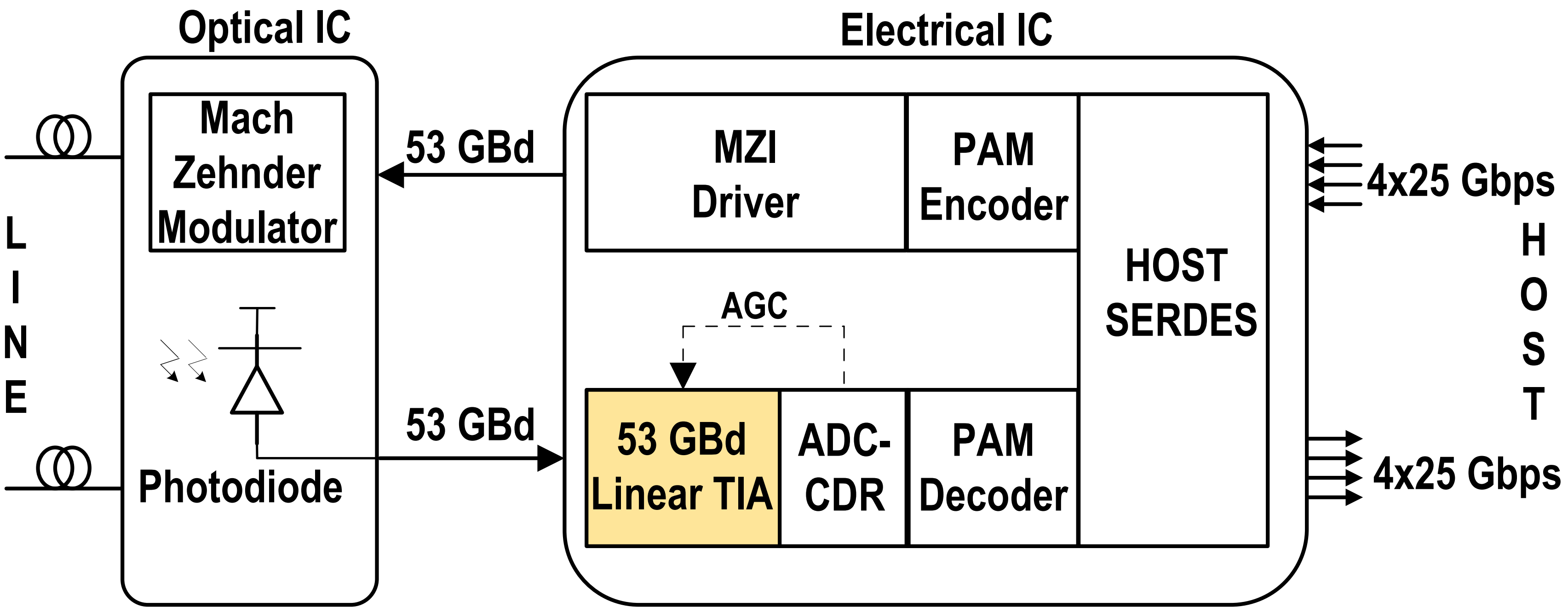
C Data Center to User (14.9%)

Web, email, internal VoD, WebEx…

Source: Cisco VNI Global Cloud Index, 2016–2021

- ■ **Data Center power increasing**
  - Interconnect power significant
  - Need low-power optical links

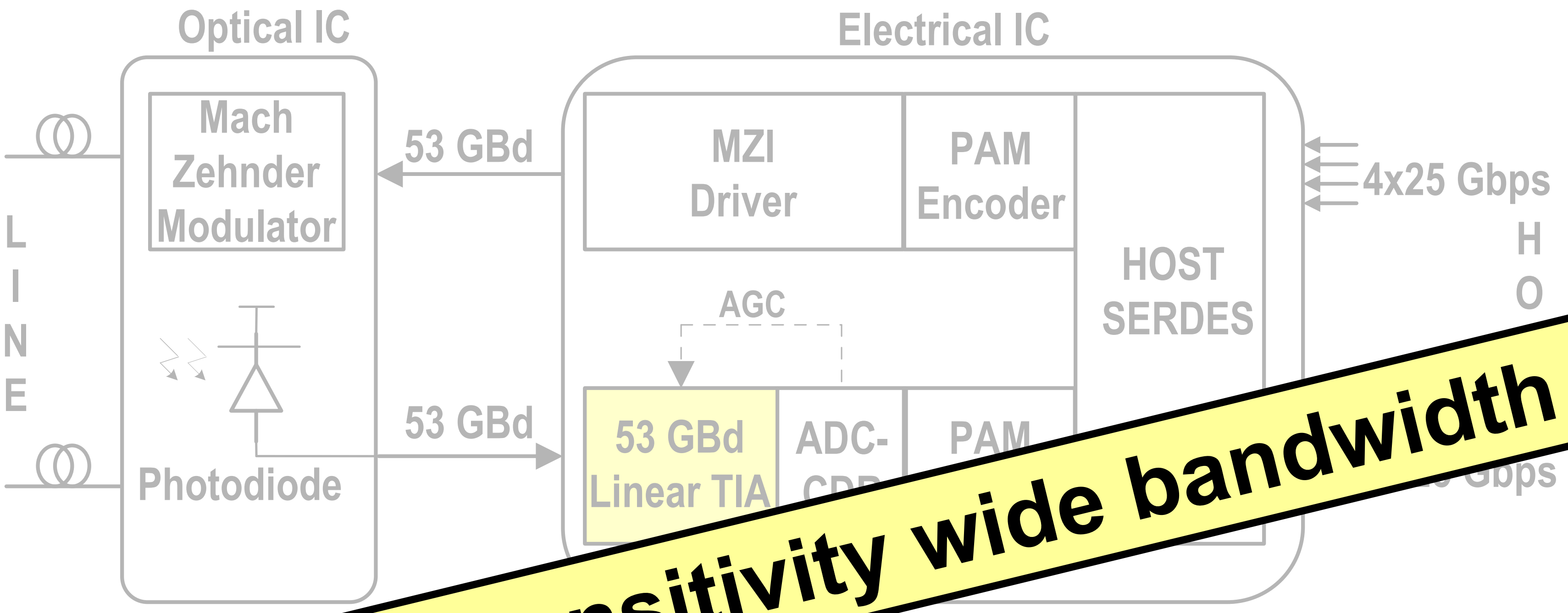
Electro-Optical System in Package



- **Integrated photonics/electronics**
  - Lower power
- **Challenges**
  - Advanced packaging
  - CMOS TIA integration

[Lakshmikumar, JSSC 2019]

Electro-Optical System in Package



Focus: High sensitivity wide bandwidth CMOS TIA

- photonics/electronics
  - Lower power
- Challenges
  - Advanced packaging
  - CMOS TIA integration

[Lakshmikumar, JSSC 2019]

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- Conventional differential TIA
- Proposed asymmetric differential TIA
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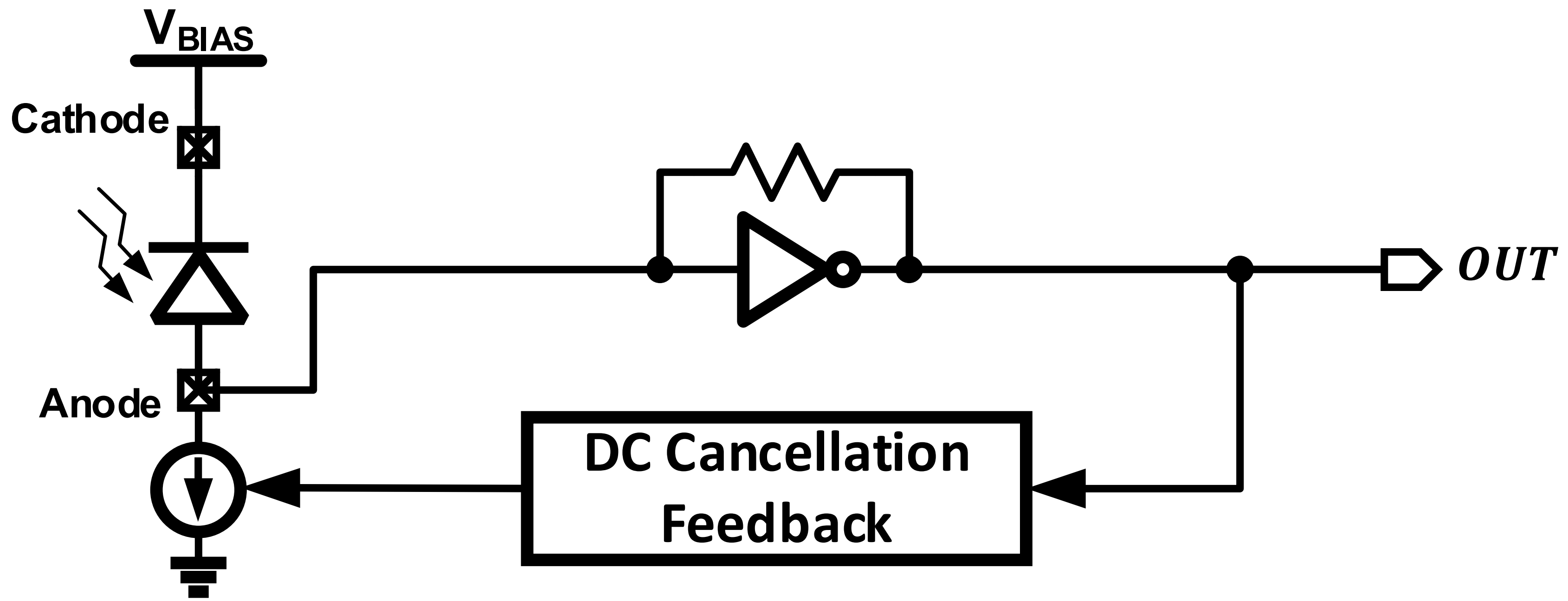
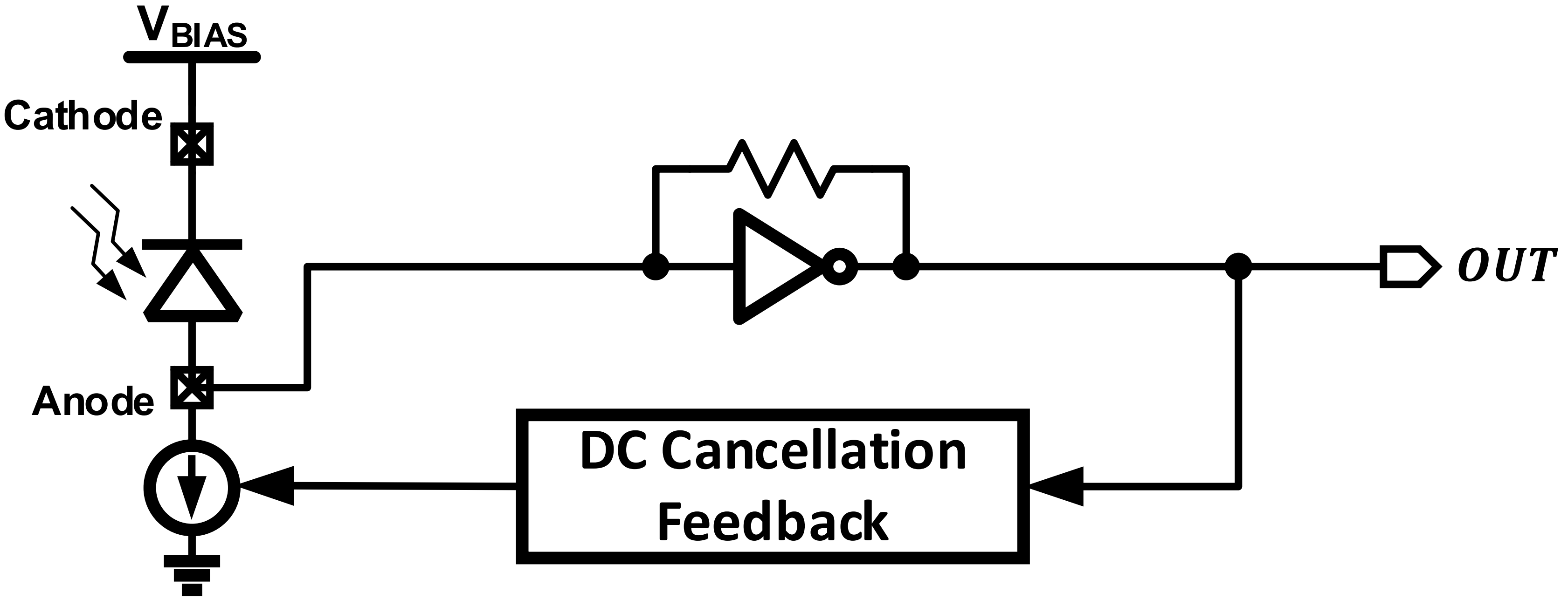
Single-Ended Shunt-Feedback TIA (SE-SF-TIA)



$$SNR = \frac{S}{\sqrt{\overline{N^2}}}$$

- **Favorable noise-bandwidth tradeoff**
  - Prior art 53.125 GBd TIA:16.7 pA/√Hz and 27 GHz bandwidth

SE-SF-TIA: Observations



$$SNR = \frac{S}{\sqrt{\overline{N^2}}}$$

- **DC Feedback removes dc component of photo current**
  - High-pass corner should be low to minimize baseline wander
- **Photo detector current on the anode side is only used**
  - Cathode side current is dumped to ac ground

Can we make use of the cathode current to improve SNR?

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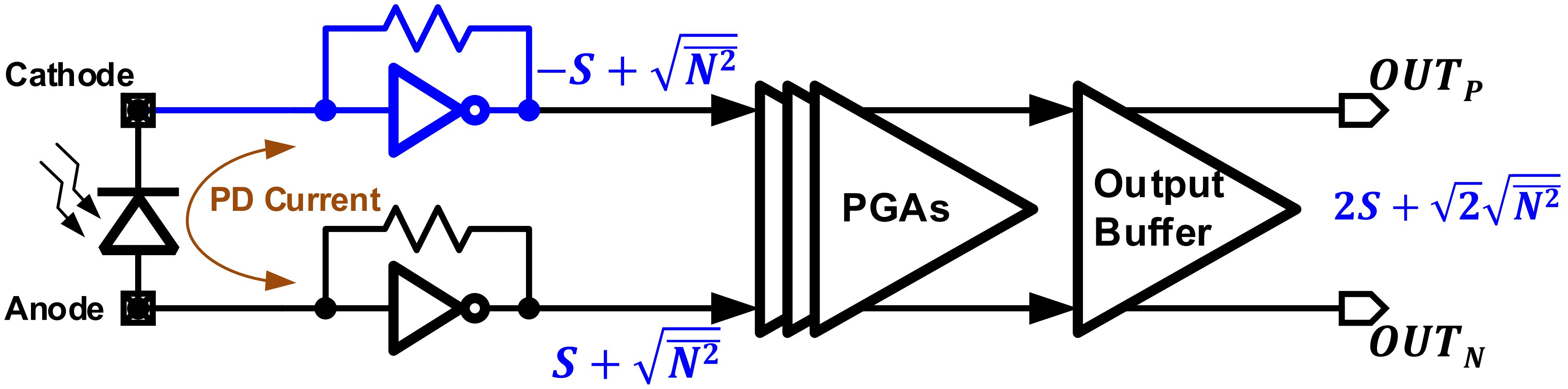
Conceptual Differential TIA



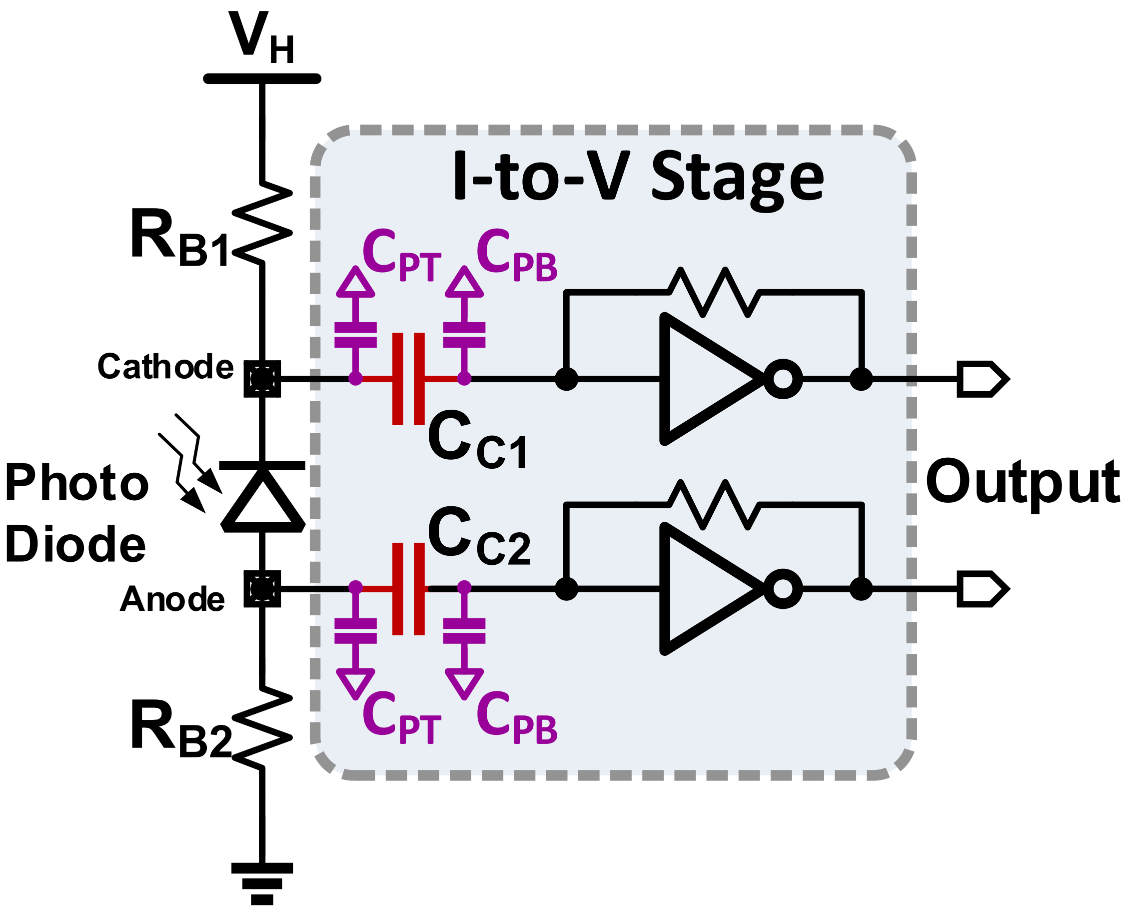
$$SNR = \sqrt{2} \cdot \frac{S}{\sqrt{\overline{N^2}}}$$

- Signal power doubles (6-dB)
- Noise power increases by 3-dB

→Theoretical SNR improvement of 3-dB

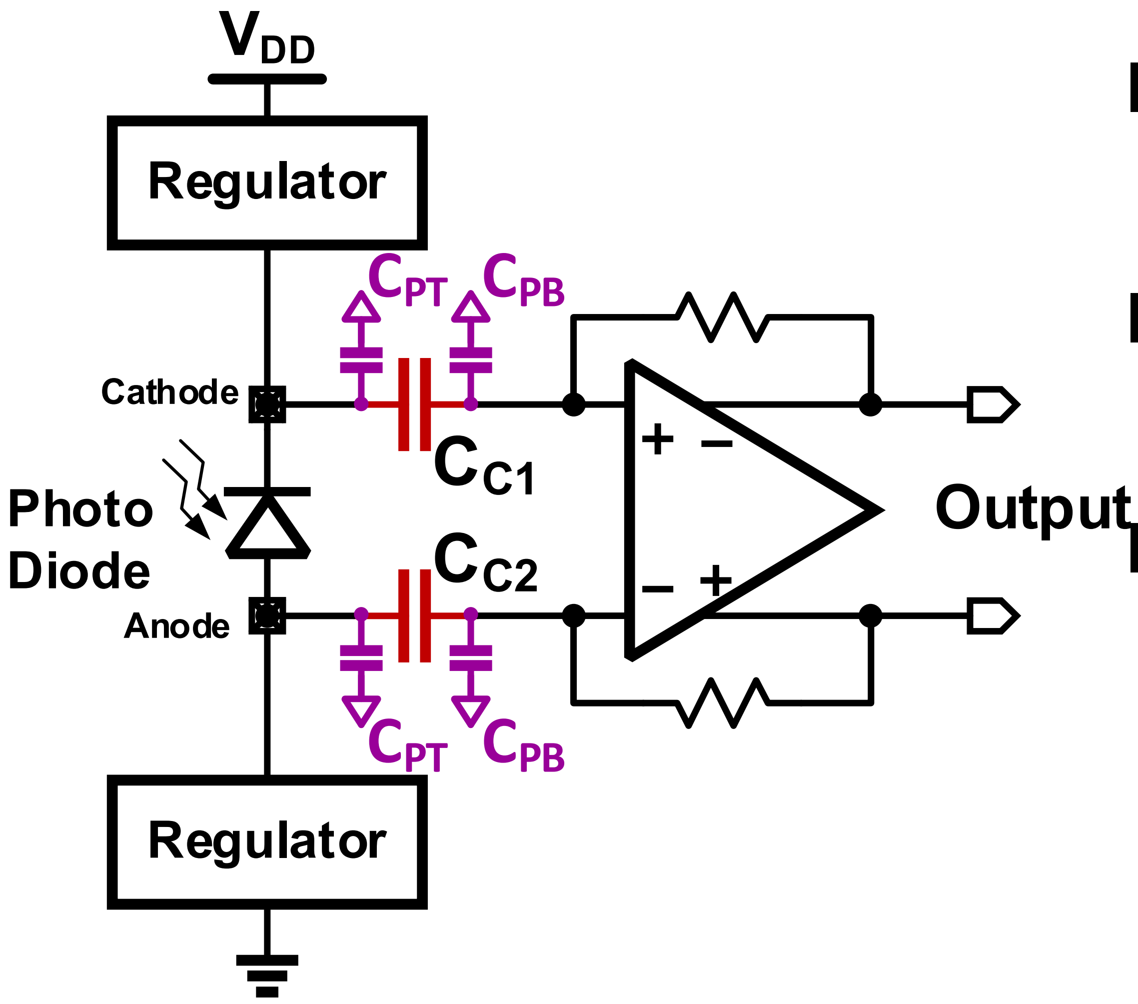
PD needs reverse bias to have high bandwidth

PD Biasing: Option # 1



- Resistors R_{B1} , R_{B2} bias PD
- TIA ac-coupled using C_{C1} , C_{C2}
- Unfavorable design tradeoffs
  - ⇓ Baseline wander requires:
    - ⇑ R_{B1} , R_{B2} → ⇓ voltage headroom
    - ⇑ C_{C1} , C_{C2} → ⇑ $C_{PT/B}$ → ⇓ BW, ⇑ noise
- < 3dB SNR improvement

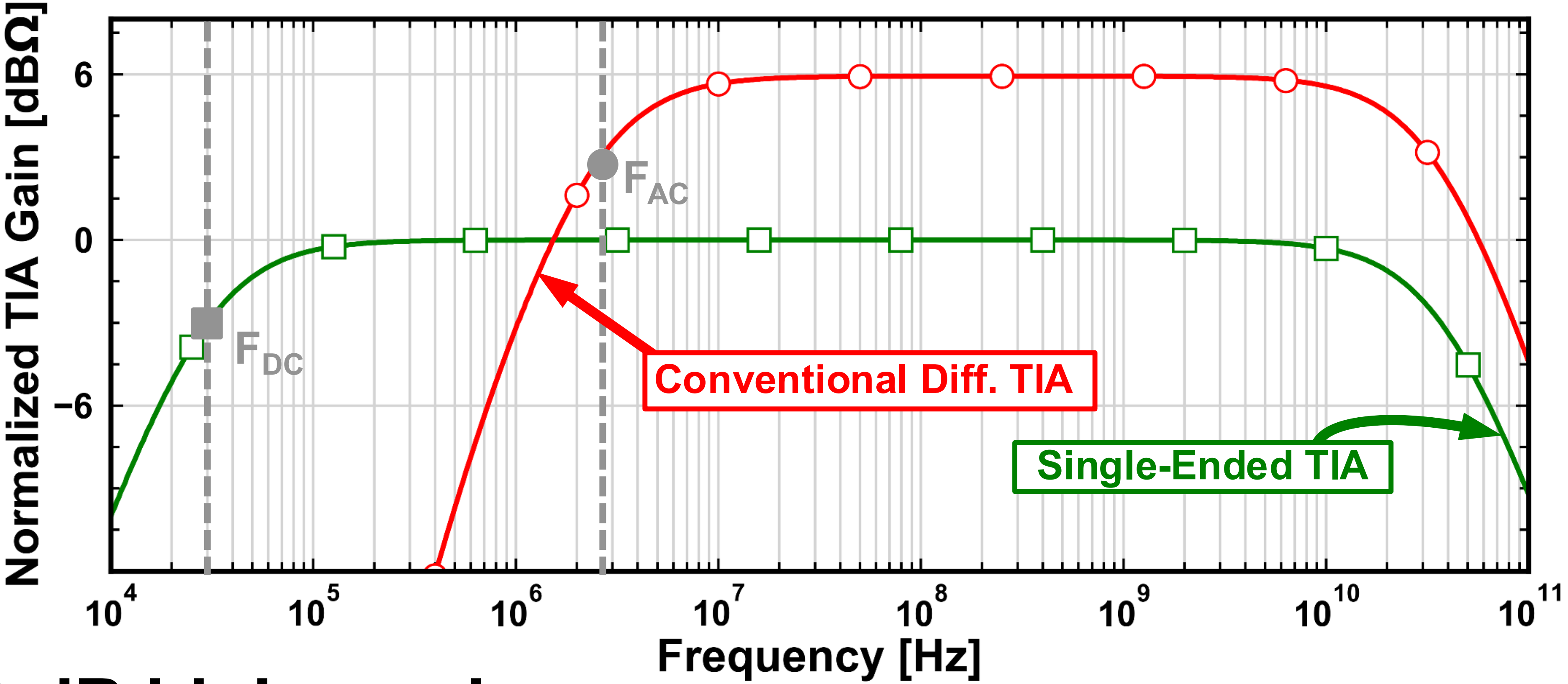
PD Biasing: Option # 2



- Regulators (LDOs) bias PD
- TIA ac-coupled using C_{C1} , C_{C2}
- Unfavorable design tradeoffs
  - ⇓ Baseline wander requires:
    - ⇓ LDO BW → ⇓ PSR
    - ⇑ C_{C1} , C_{C2} → ⇑ $C_{PT/B}$ → ⇓ BW, ⇑ noise
- < 3dB SNR improvement

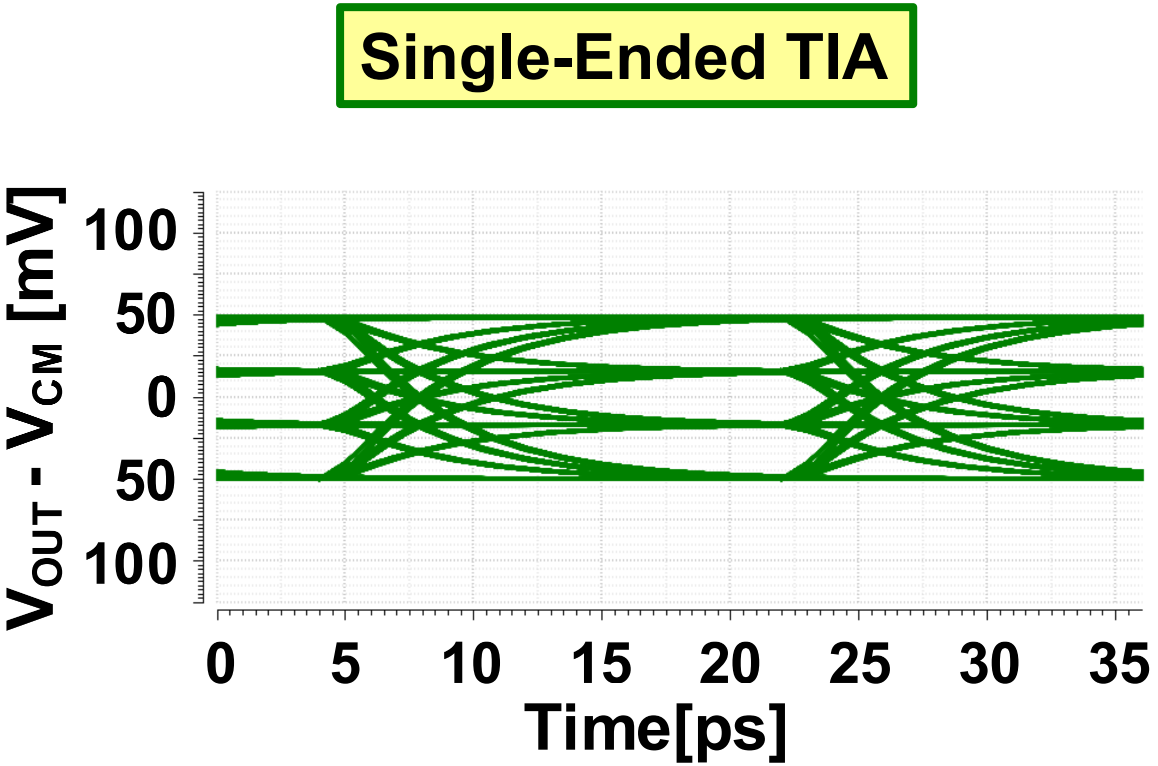
[J. Lambrecht, IEEE PTL, 2019]

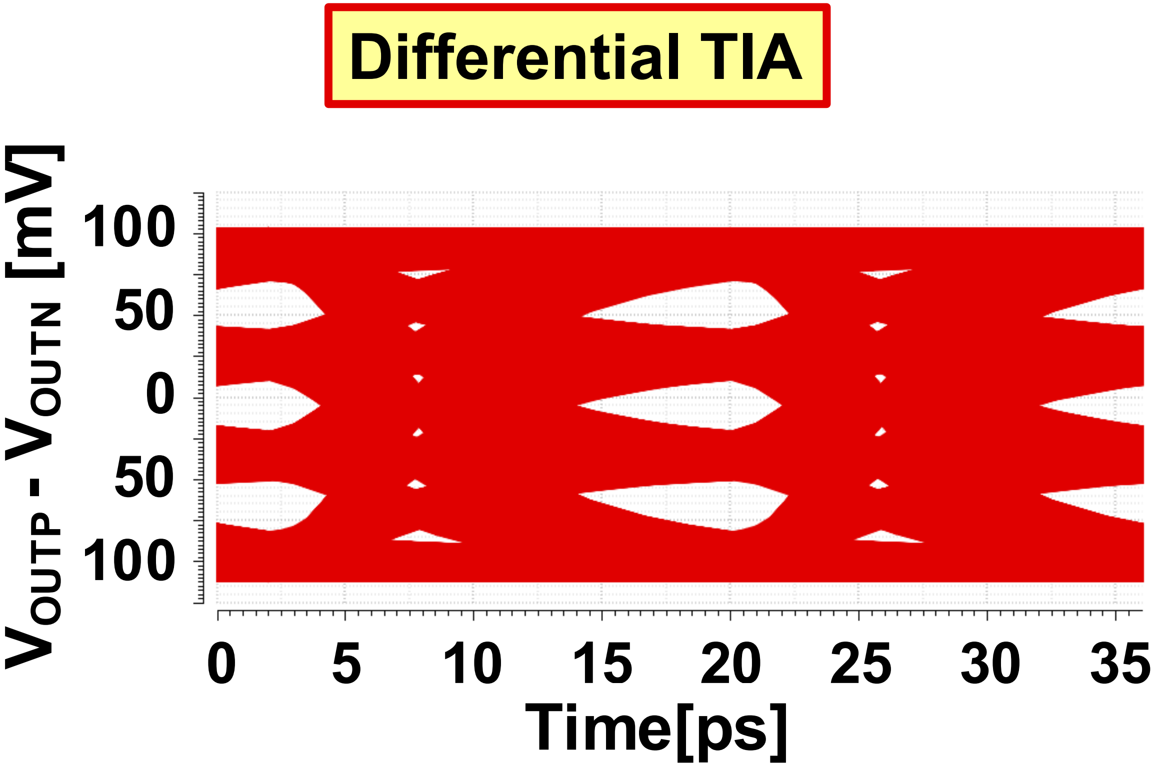
Simulated TIA Response: Frequency Domain



- 6-dB higher gain
- Higher low-frequency corner ($F_{DC} < F_{AC}$)
  - $\Downarrow F_{AC} \rightarrow \Uparrow C_C \rightarrow \Downarrow$ TIA bandwidth $\rightarrow \Uparrow$ Noise

Simulated TIA Response: Time Domain





Baseline wander degrades eye opening

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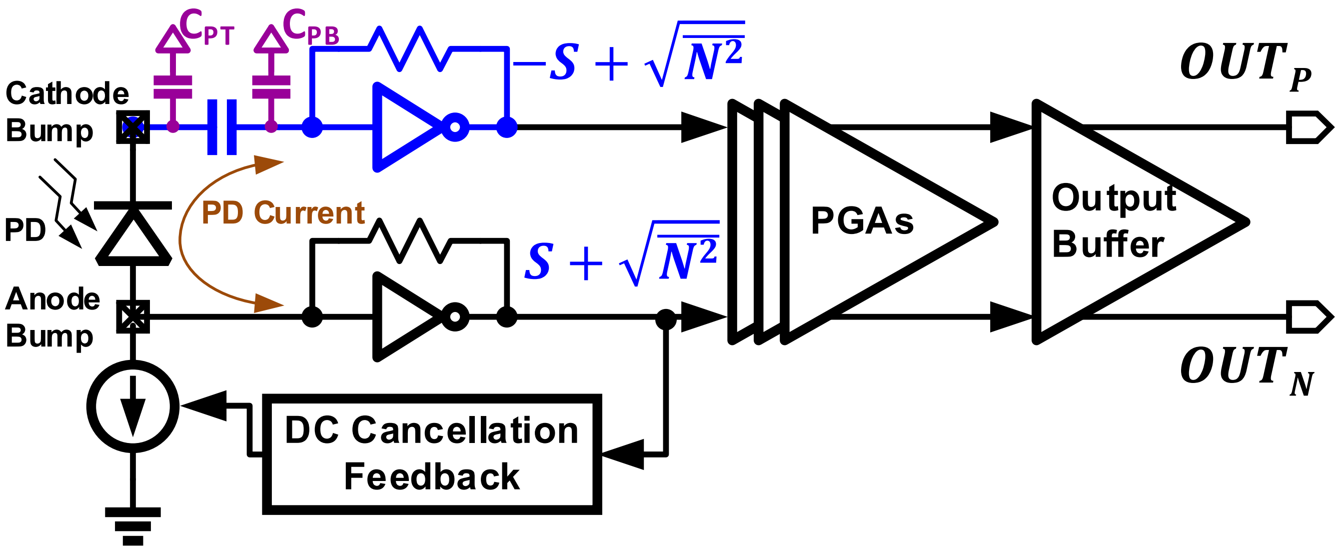
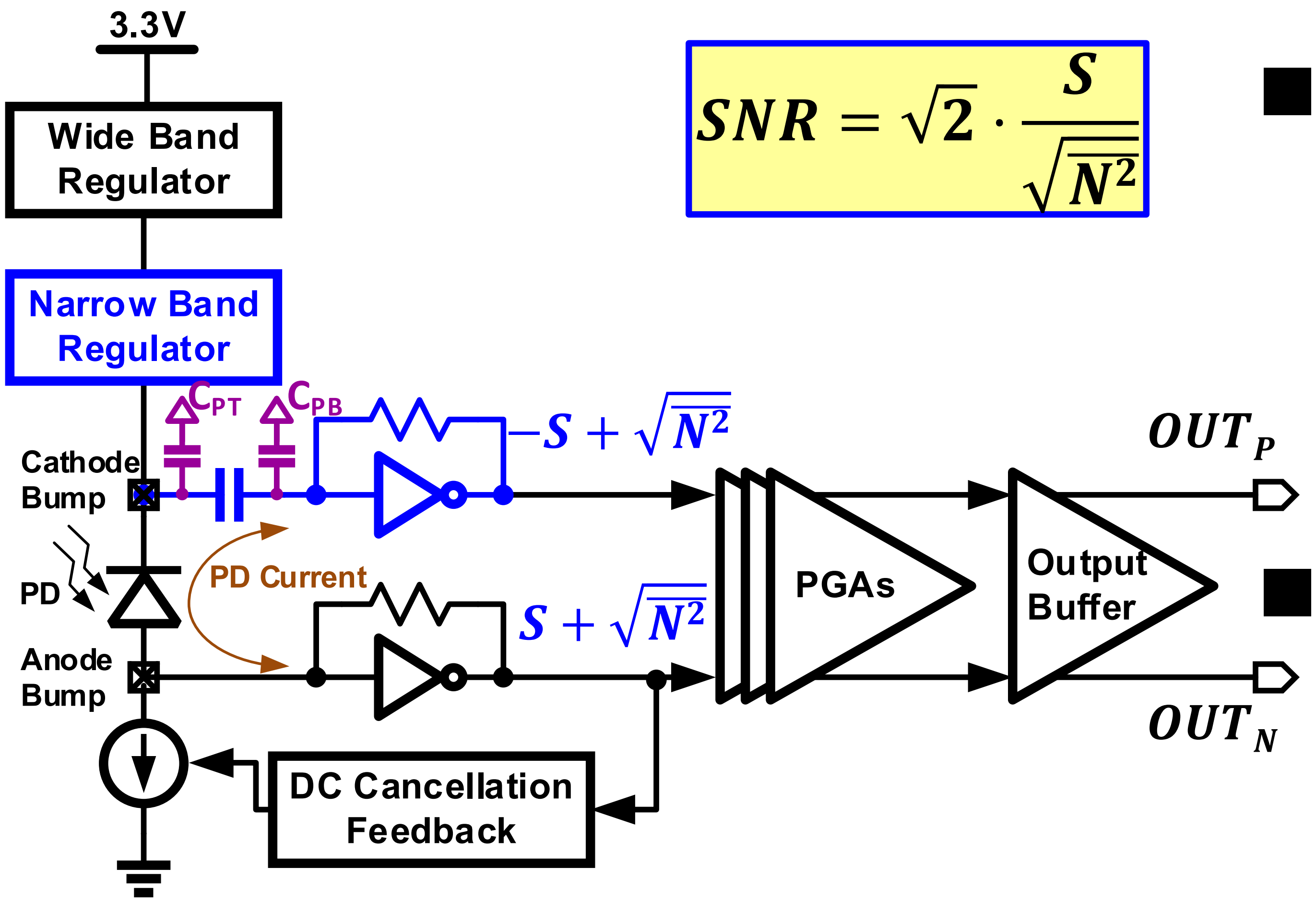
Proposed Differential $TIA_{1/2}$

$$SNR = \sqrt{2} \cdot \frac{S}{\sqrt{\overline{N^2}}}$$



- **Asymmetric signal paths**
  - Only cathode node is ac-coupled
  - Minimized parasitics effect
  - Reduced baseline wander

Proposed Differential $TIA_{2/2}$

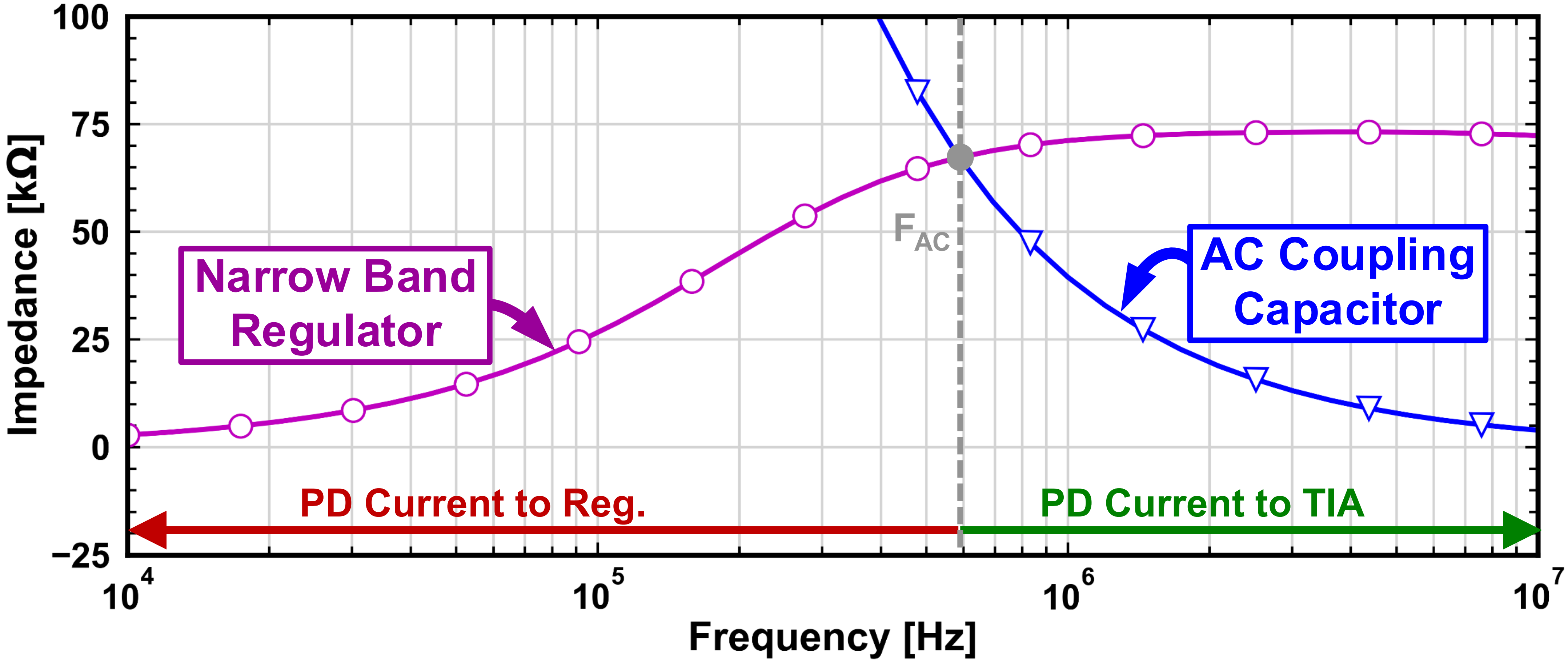


$$SNR = \sqrt{2} \cdot \frac{S}{\sqrt{\overline{N^2}}}$$

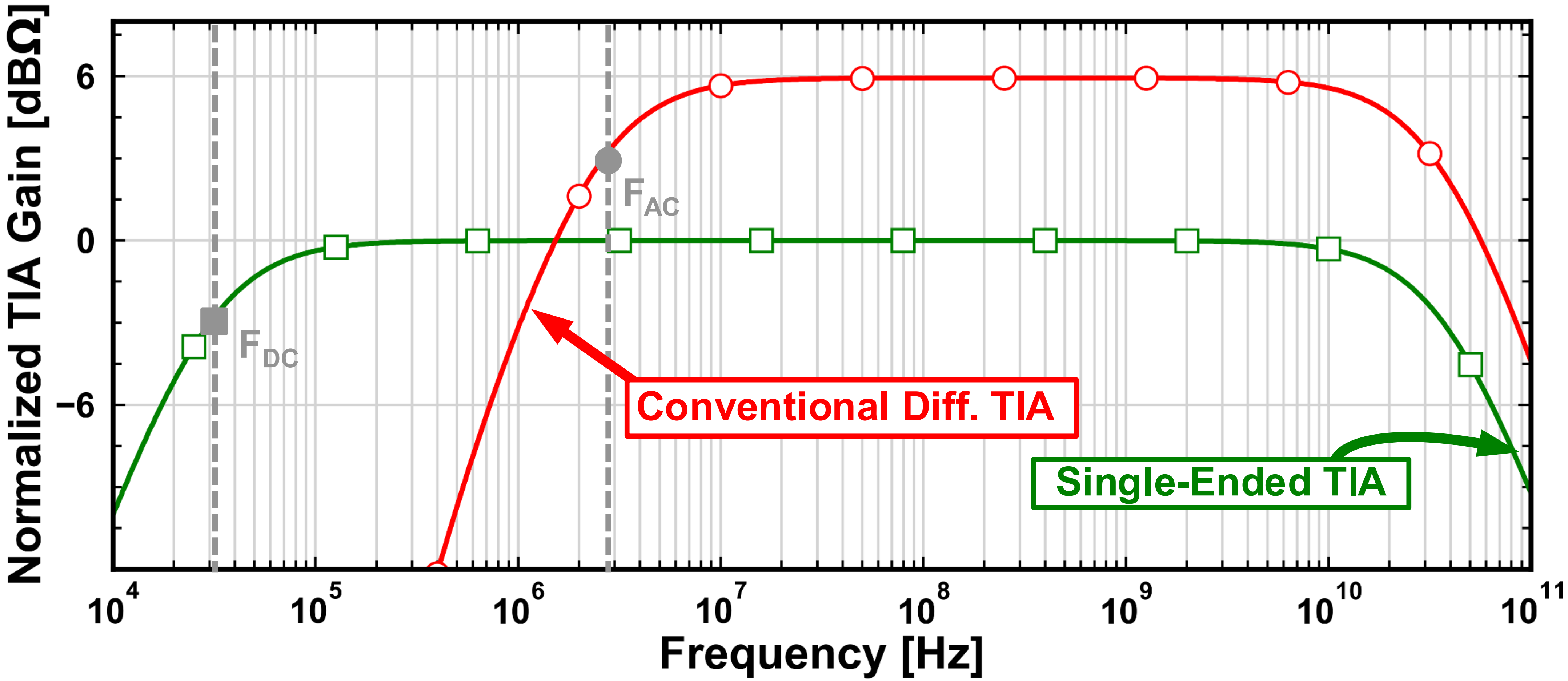
- **Asymmetric signal paths**
  - Only cathode node is ac-coupled
  - Minimized parasitics effect
  - Reduced baseline wander
- **Cascaded regulator**
  - NB regulator → ⇑ Impedance
  - WB regulator → ⇑ PSR

SNR improvement closer to theoretical limit of 3 dB

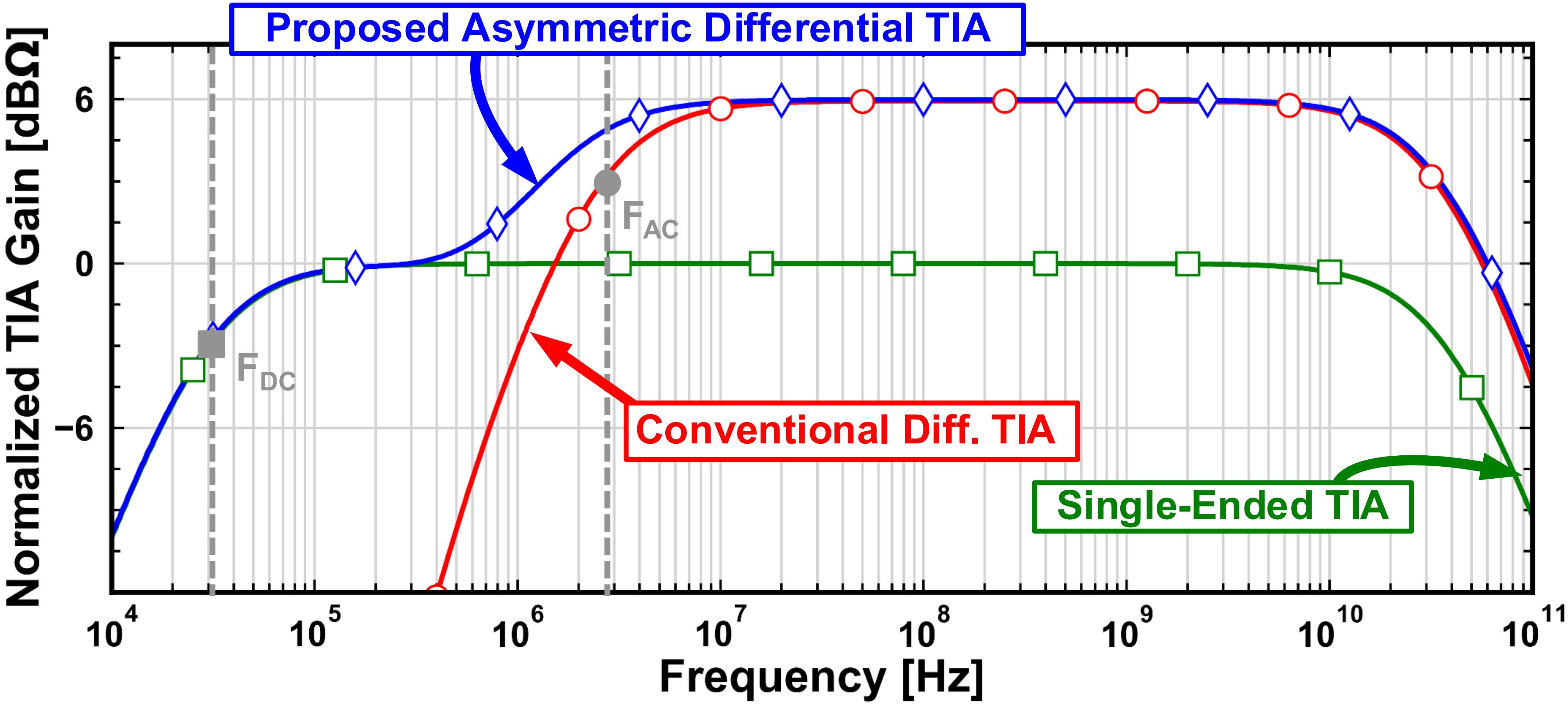
Simulation Results: Cathode Impedance



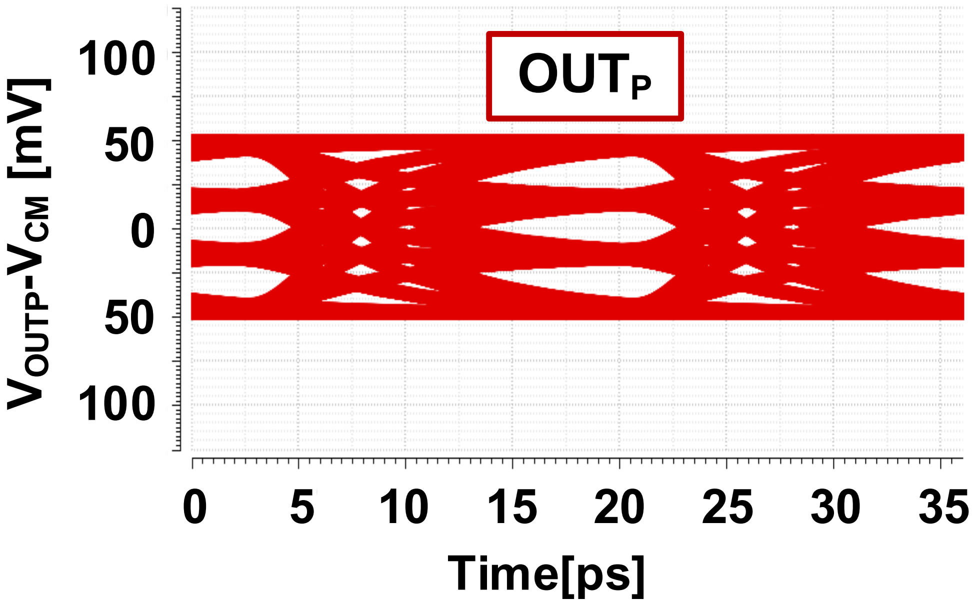
Simulation Results: Magnitude Response$_{1/2}$

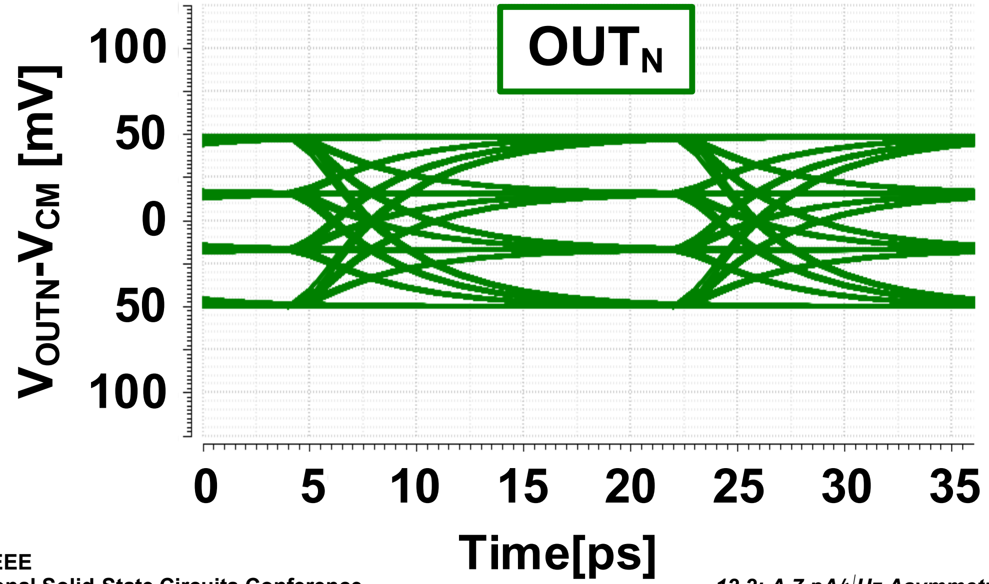


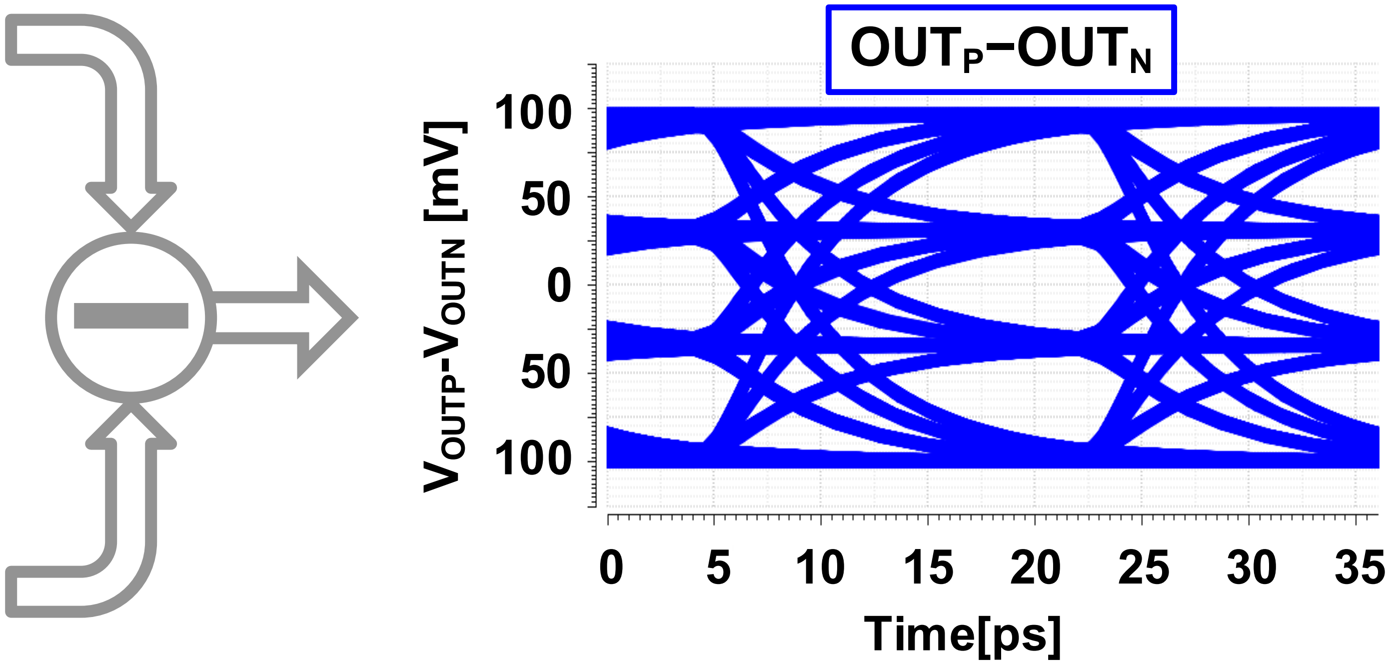
Simulation Results: Magnitude Response$_{2/2}$



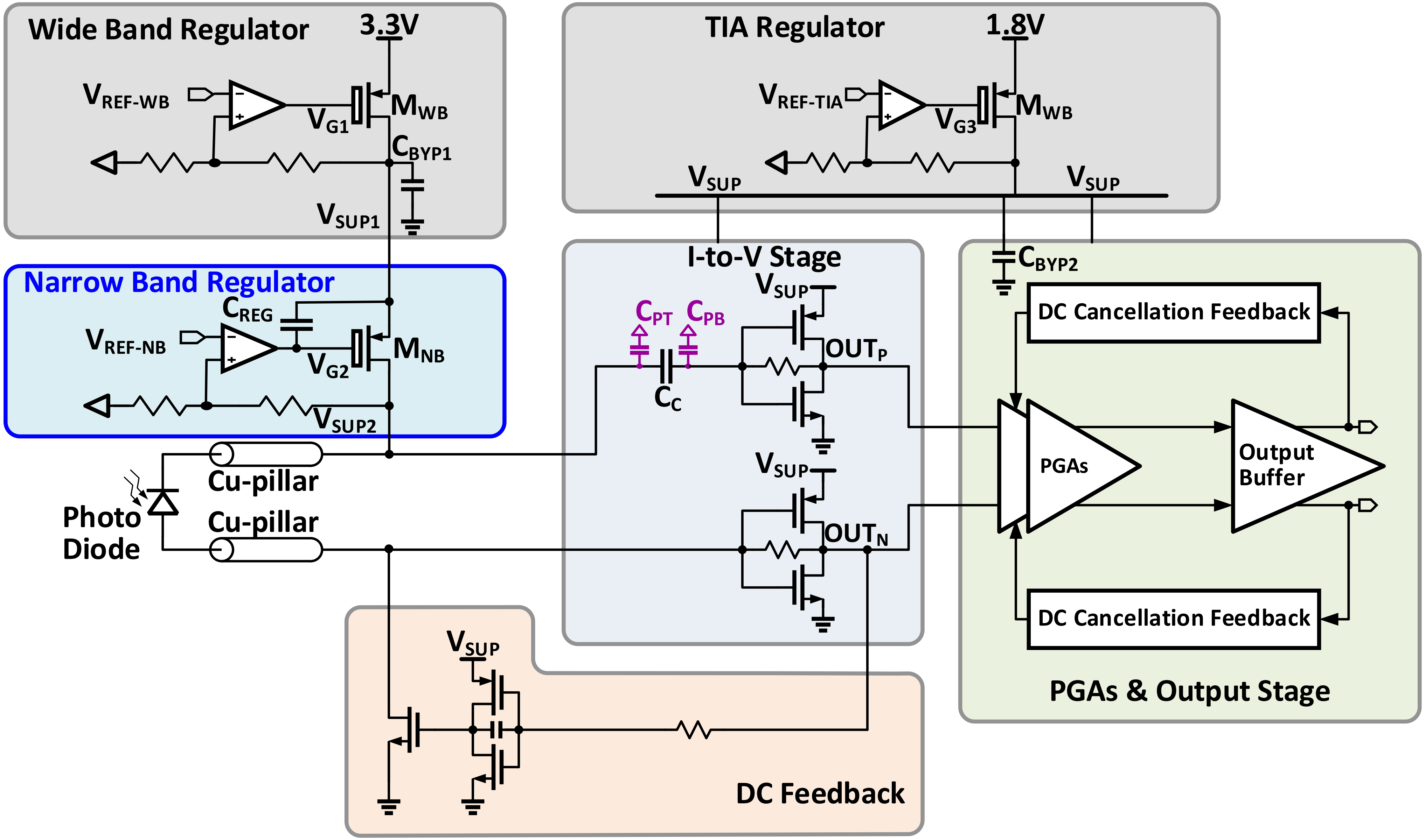
Simulation Results: SSPRQ Eye Diagrams



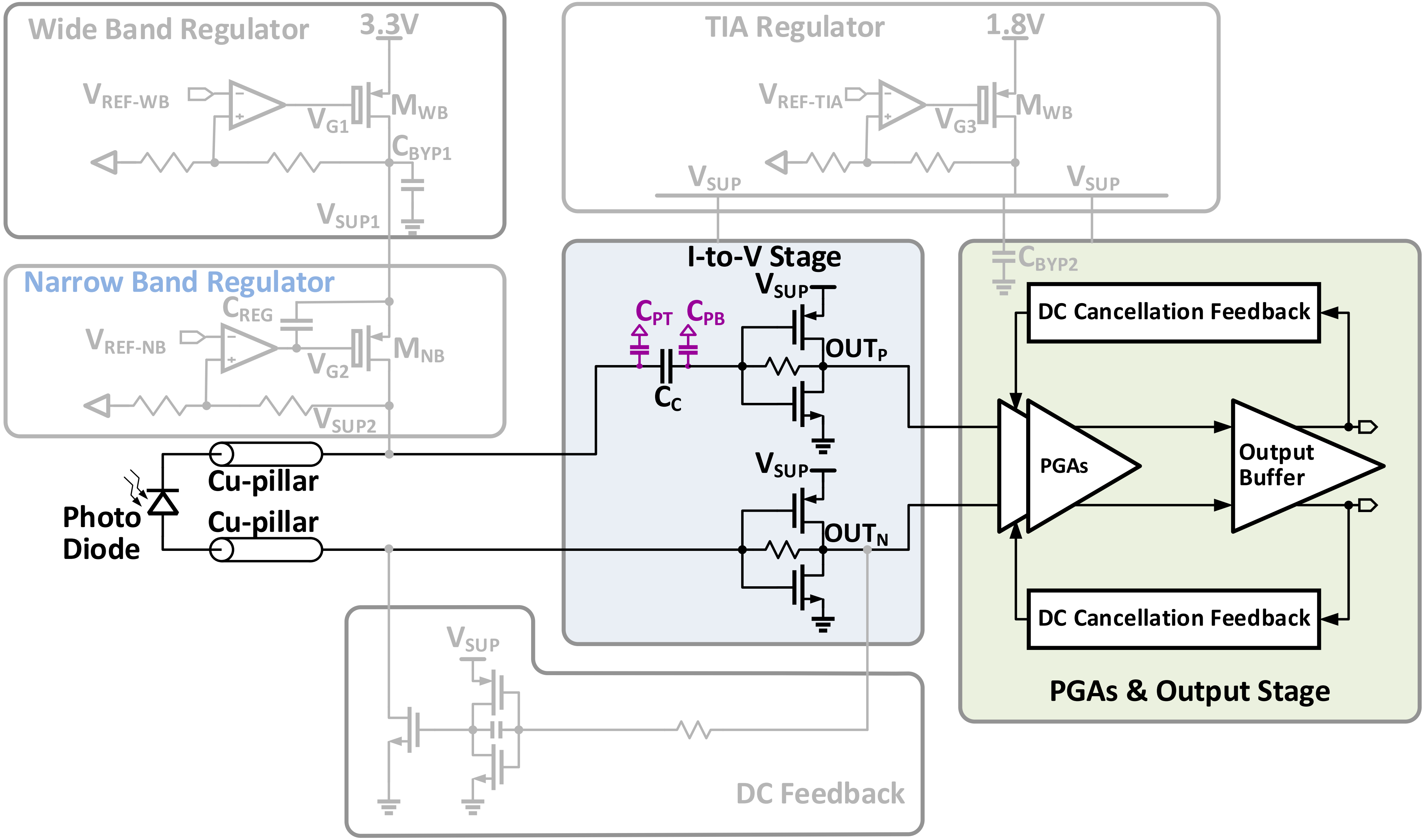




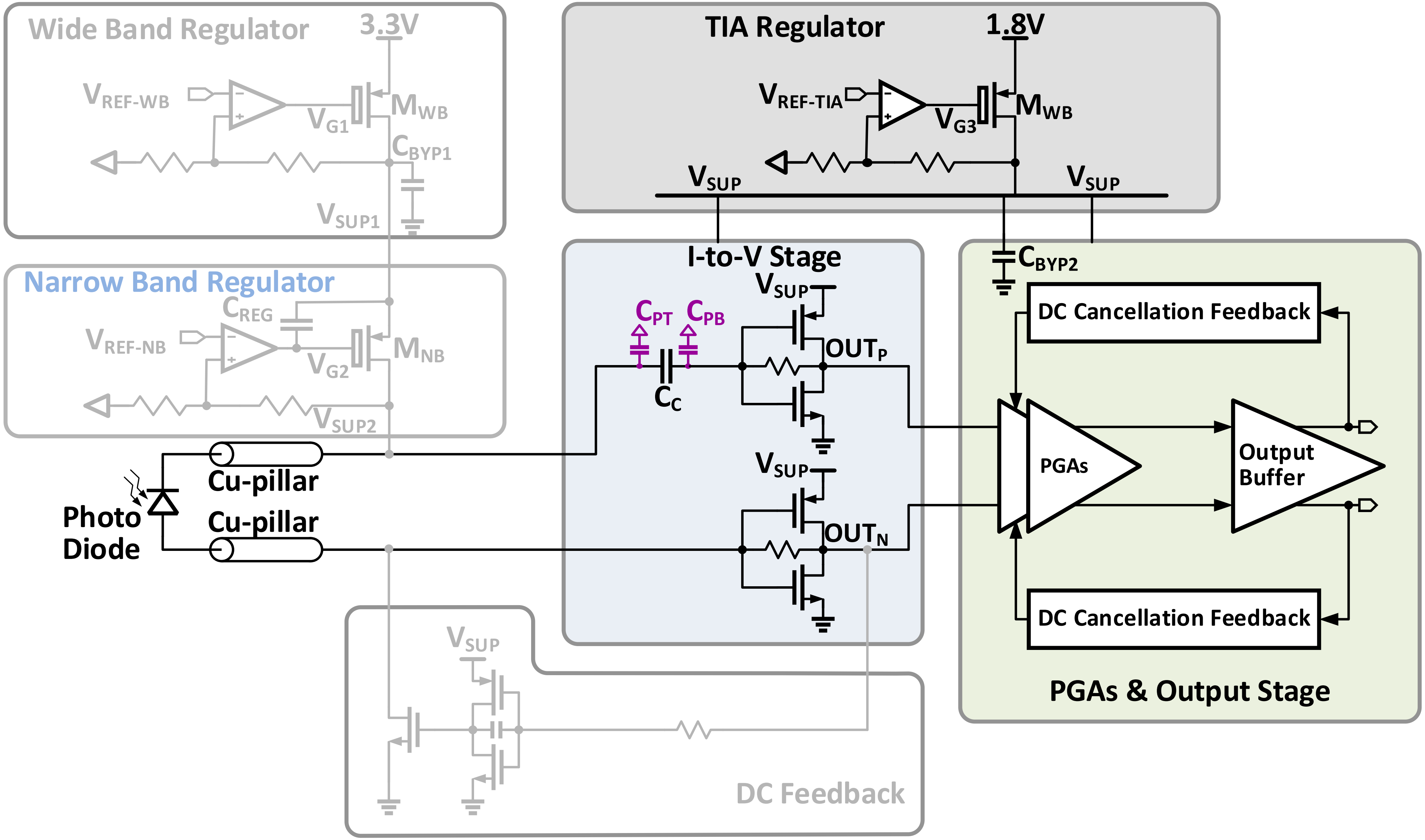
Complete Differential $TIA_{1/5}$



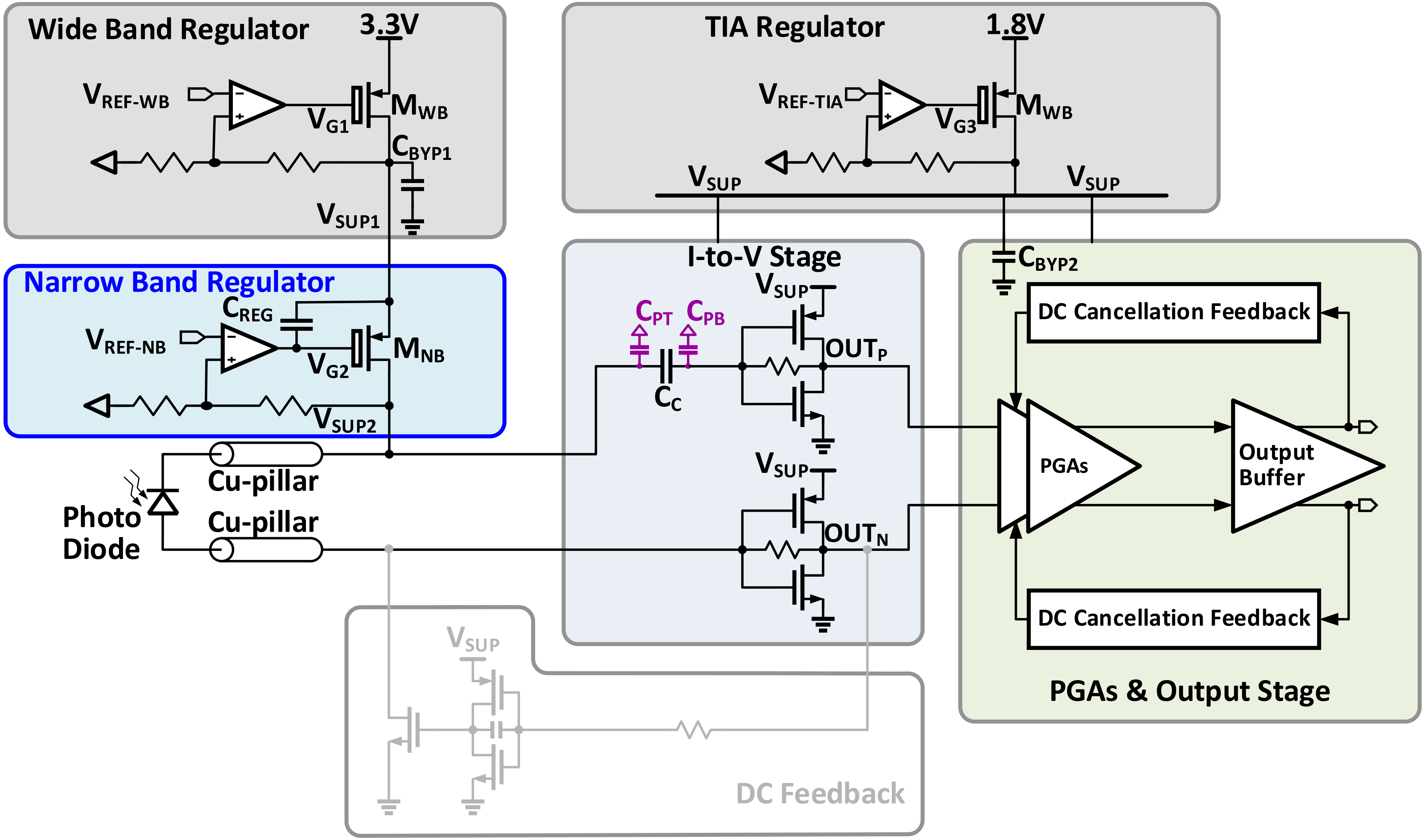
Complete Differential $TIA_{2/5}$



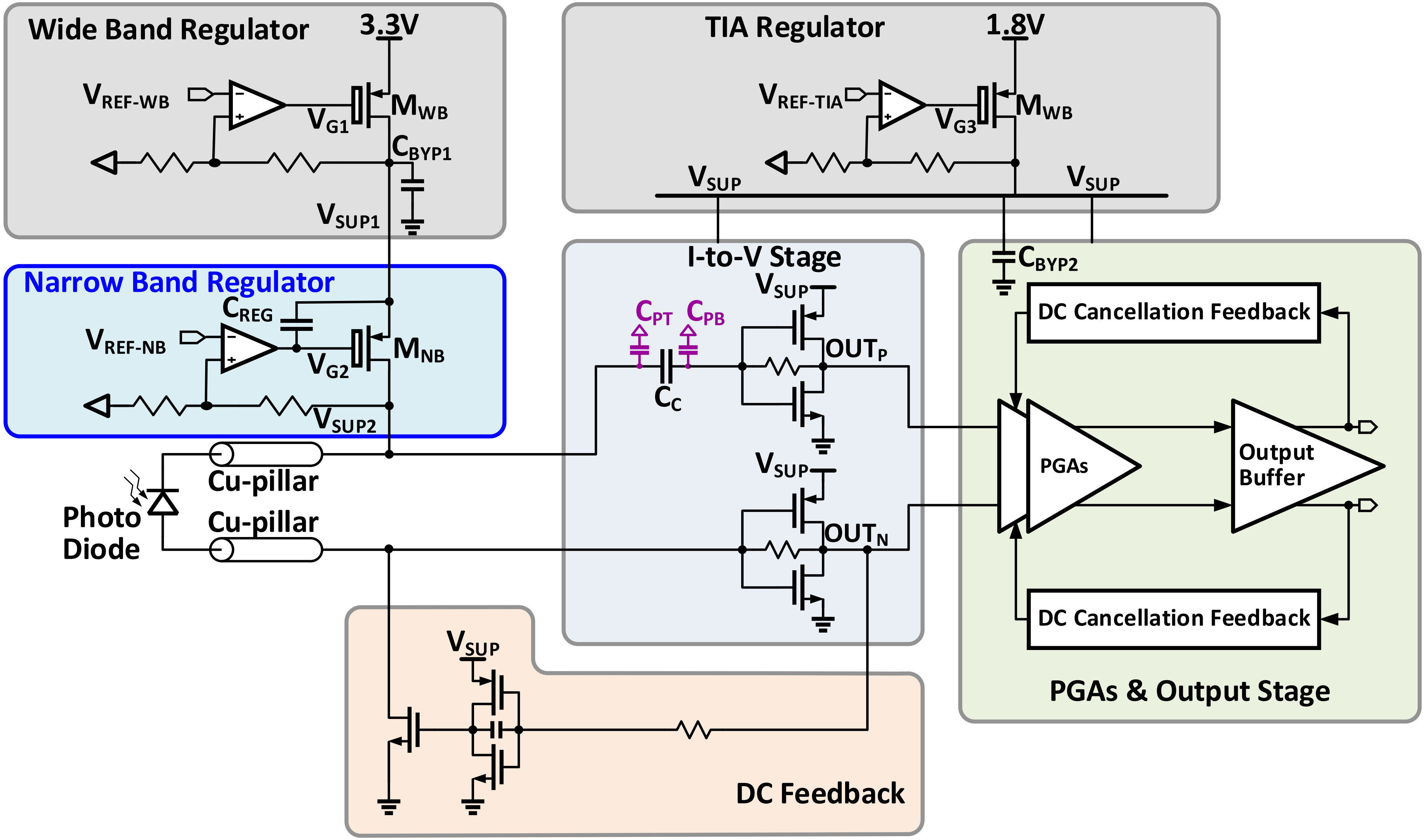
Complete Differential $TIA_{3/5}$



Complete Differential $TIA_{4/5}$



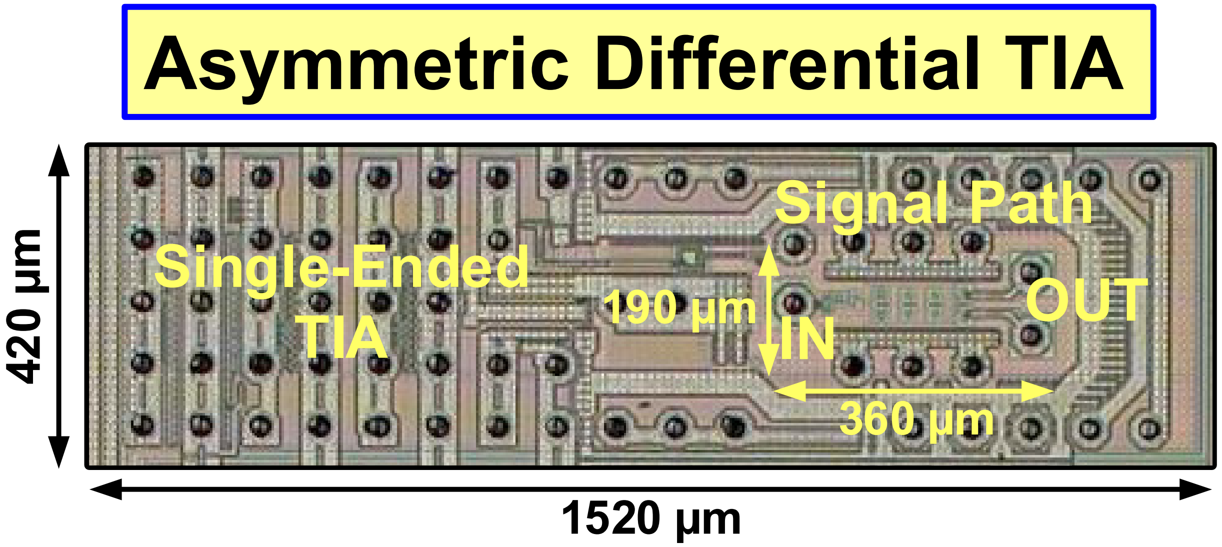
Complete Differential $TIA_{5/5}$

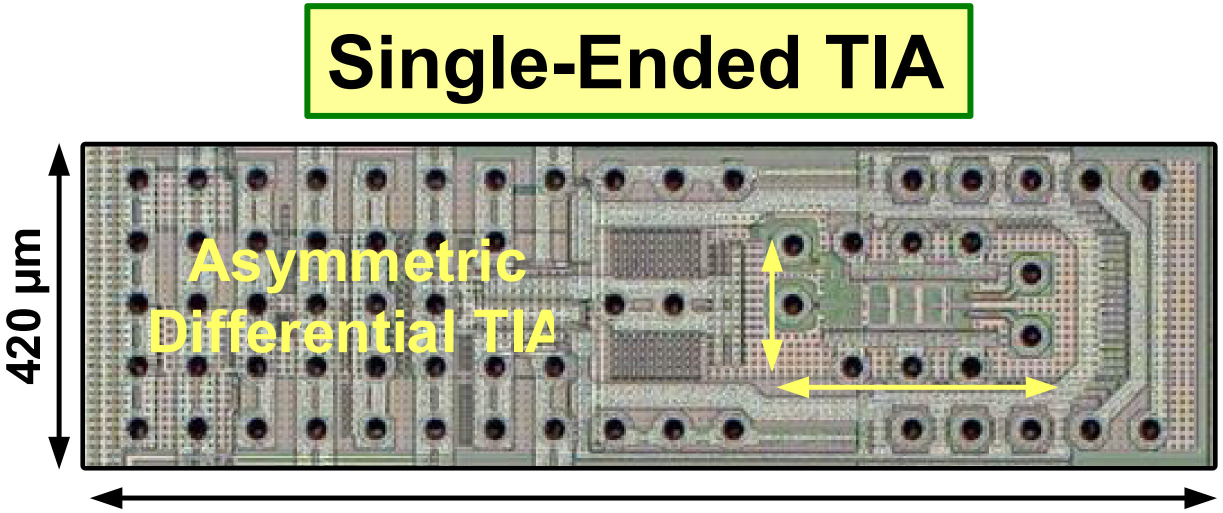


Outline

- Motivation
- Single-ended TIA
- Conventional differential TIA
- Proposed asymmetric differential TIA
- **Experimental validation**
- Conclusion

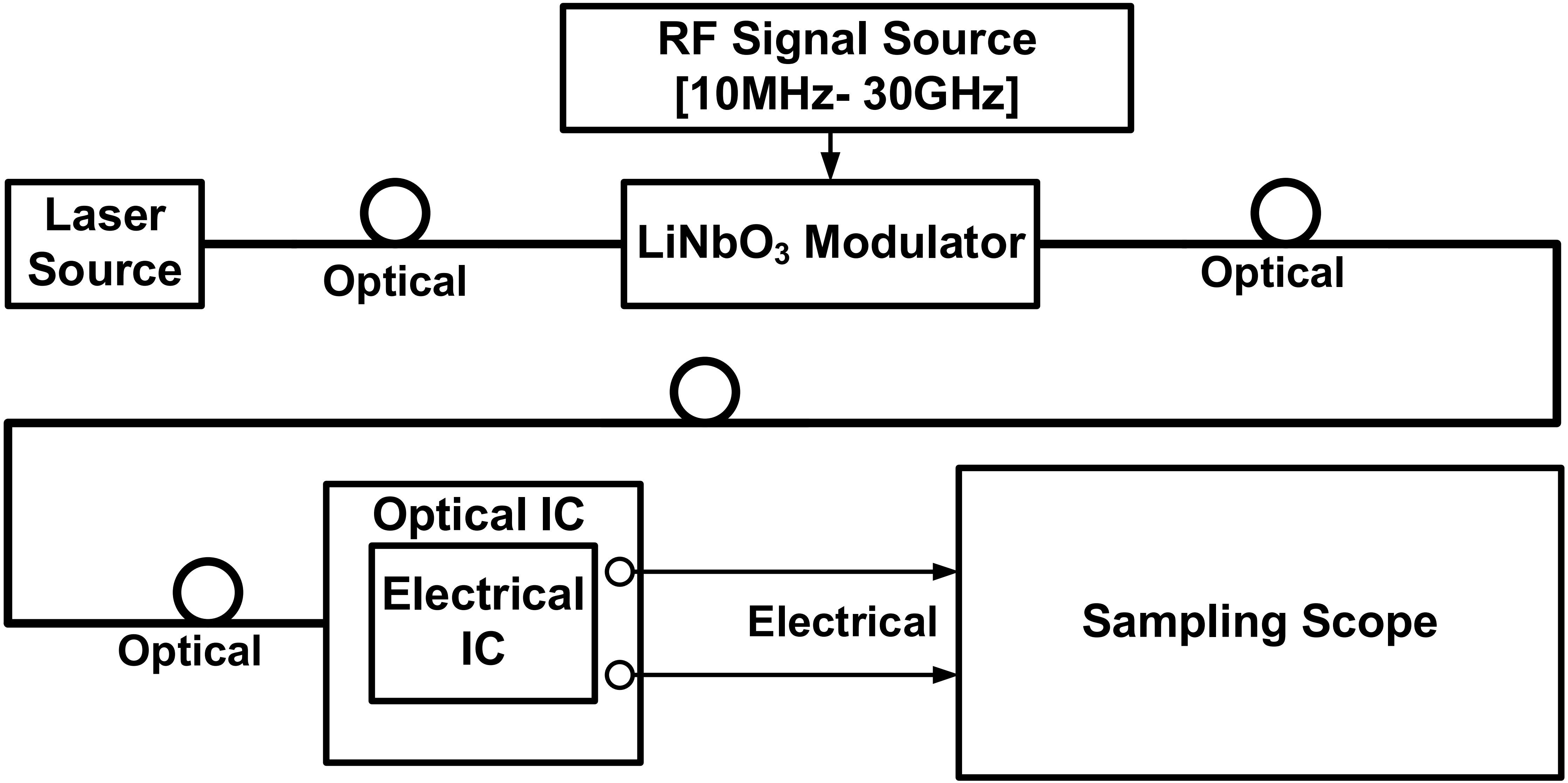
Experimental Prototypes



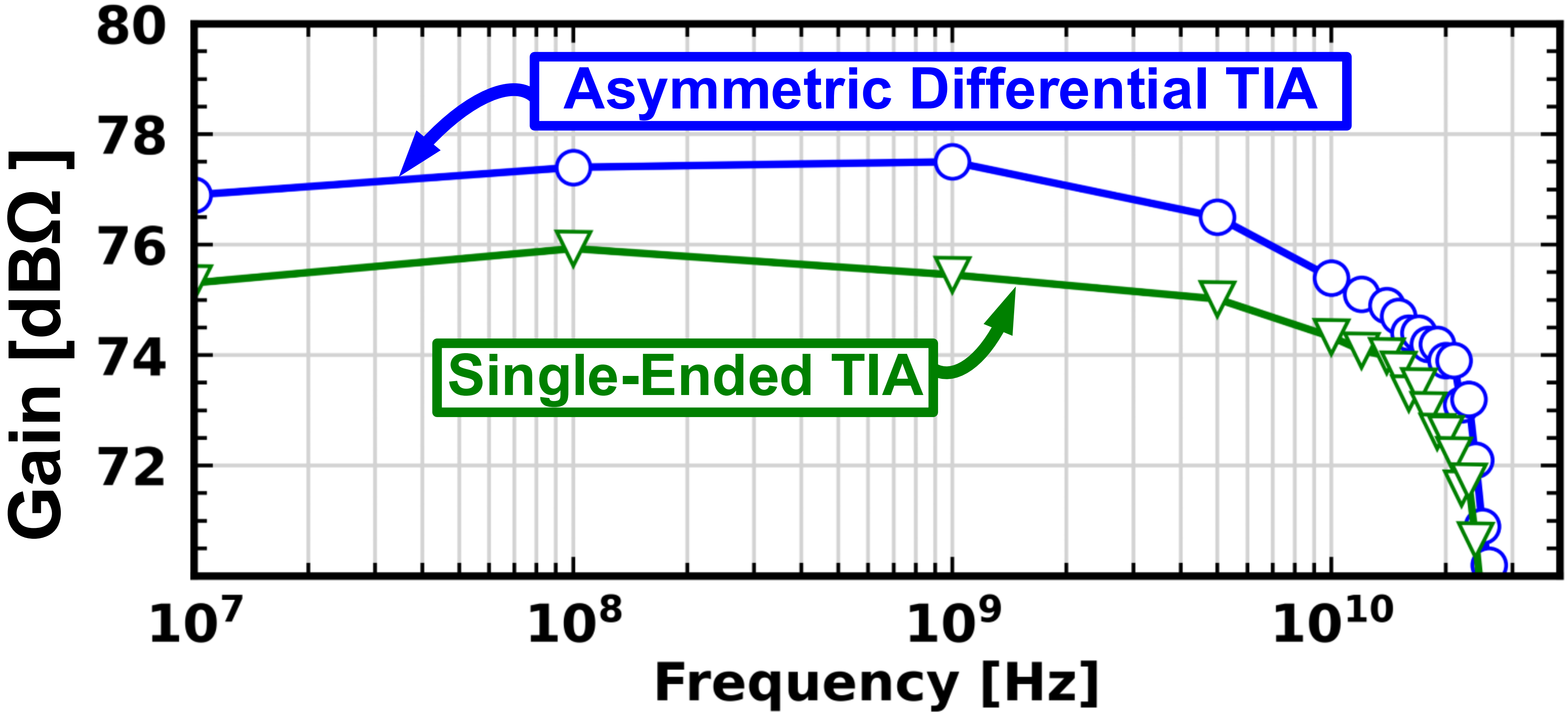


- 16nm FinFET CMOS
- Supply: 0.8 V/1.8 V/3.3 V
- Area: 1520 µm x 420 µm
- Power: 108 mW
- Single-ended TIA for fair comparison

Measurement Setup – Bandwidth



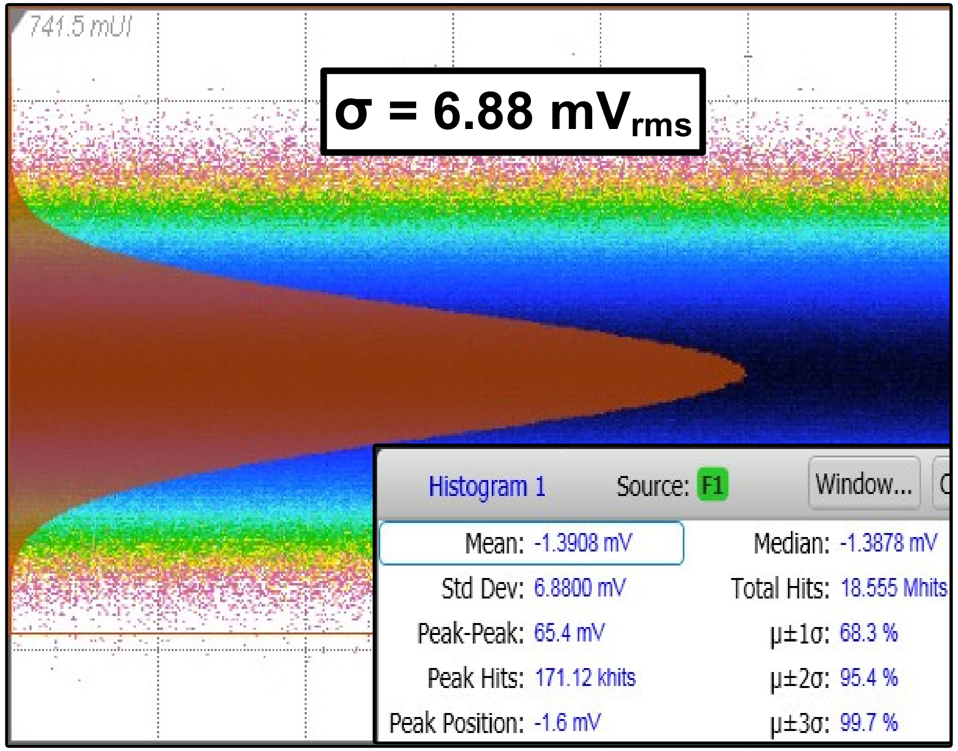
Large-Signal Bandwidth



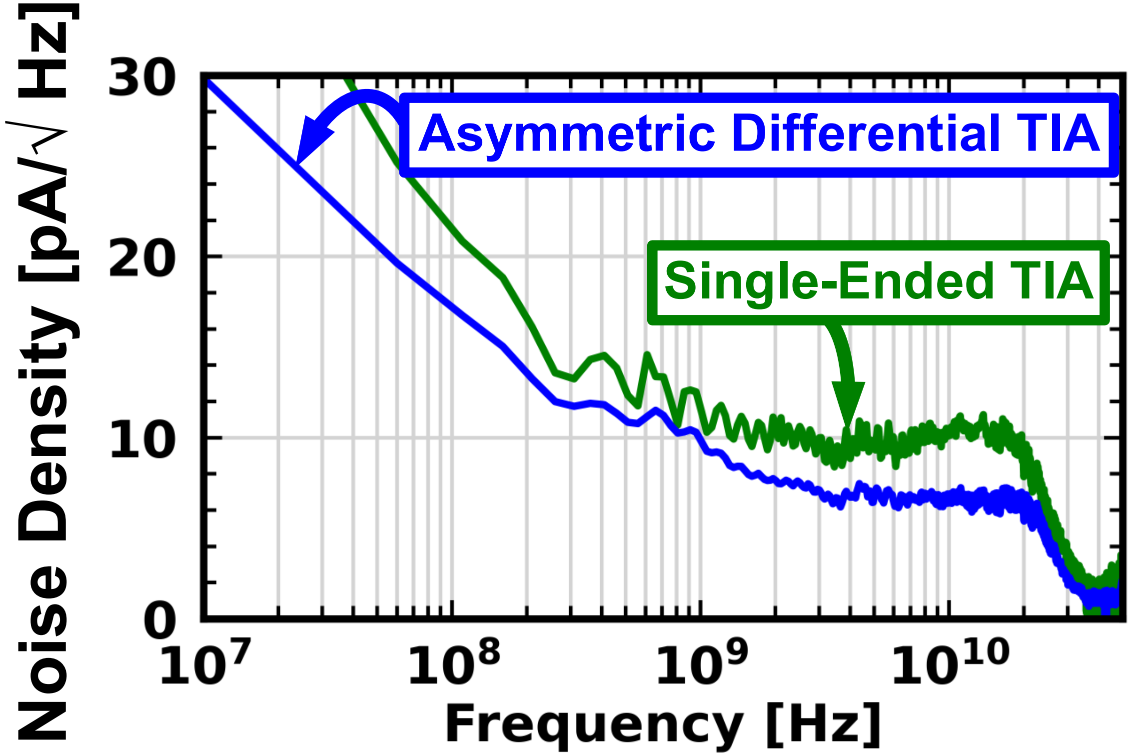
- Measured bandwidth ~18.4GHz @ max gain

Noise Measurement

Time Domain (Output Noise)

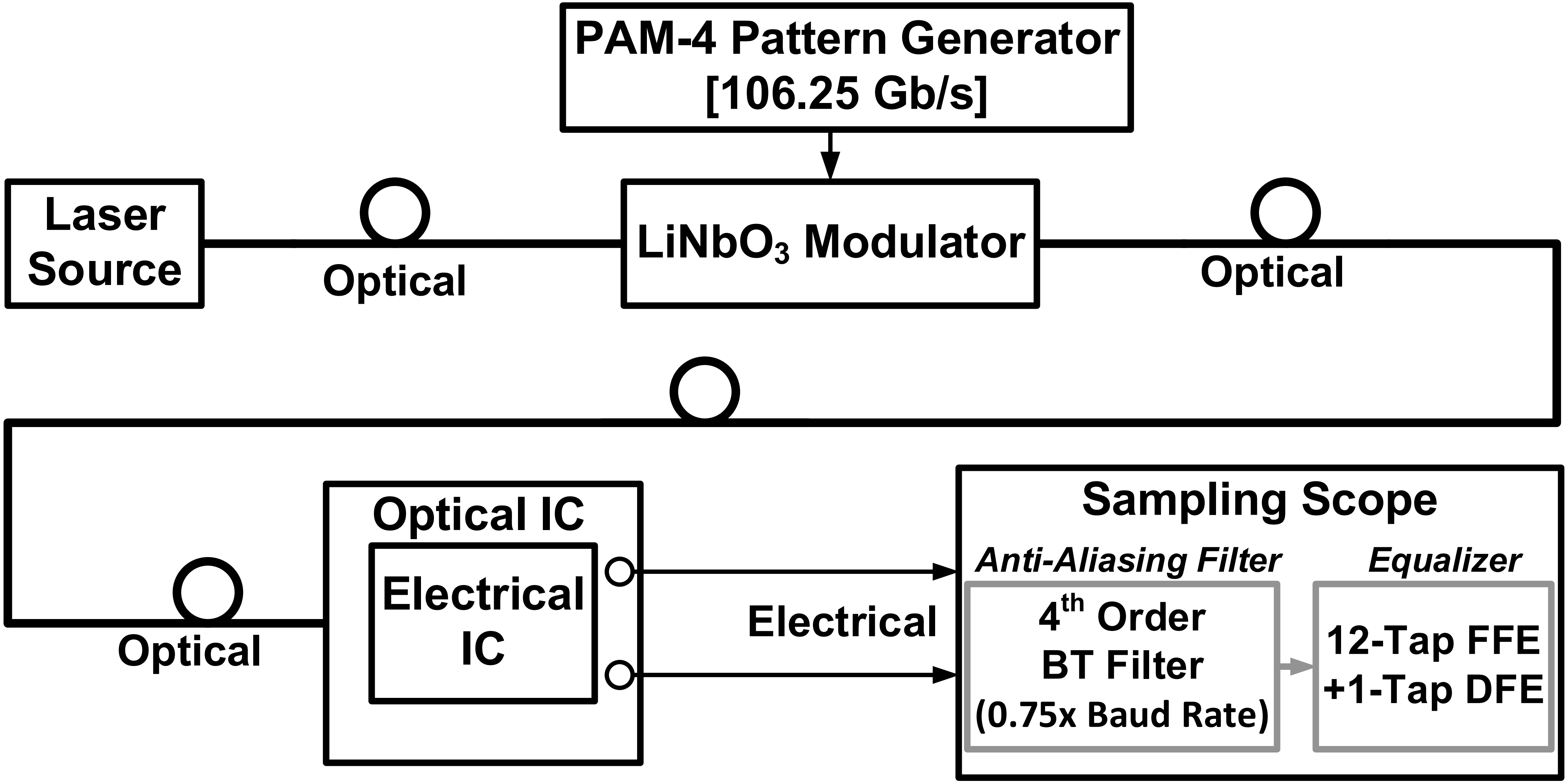


Frequency Domain (Input Referred)



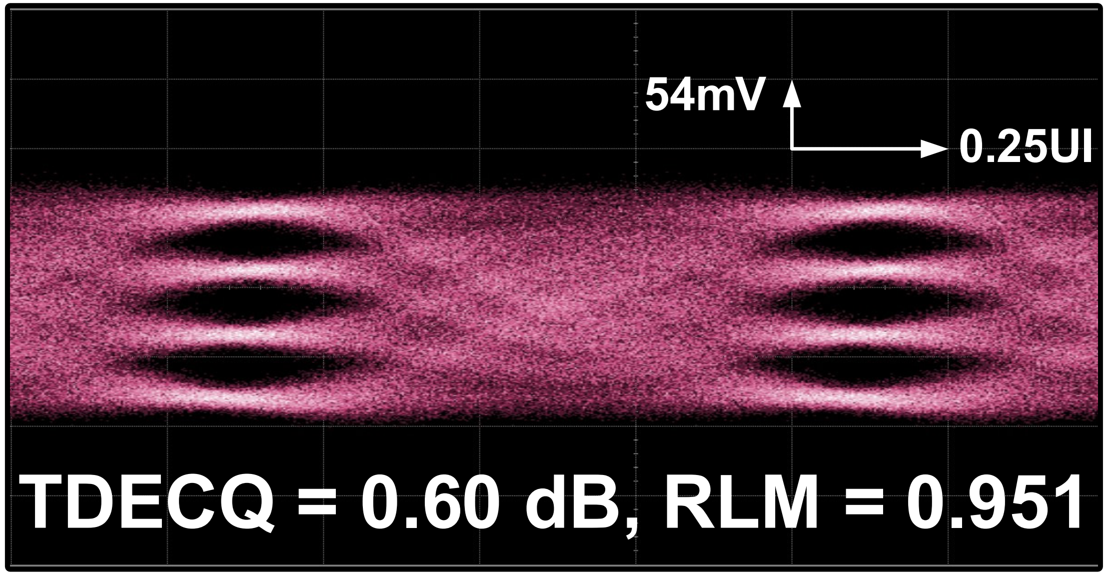
- **Input referred noise = 7 pA/√Hz over 27 GHz**
  - Output noise = 6.88 mV$_{rms}$, Scope noise = 0.6 mV$_{rms}$
  - Average Z_T = 77 dBΩ

Measurement Setup – Sensitivity

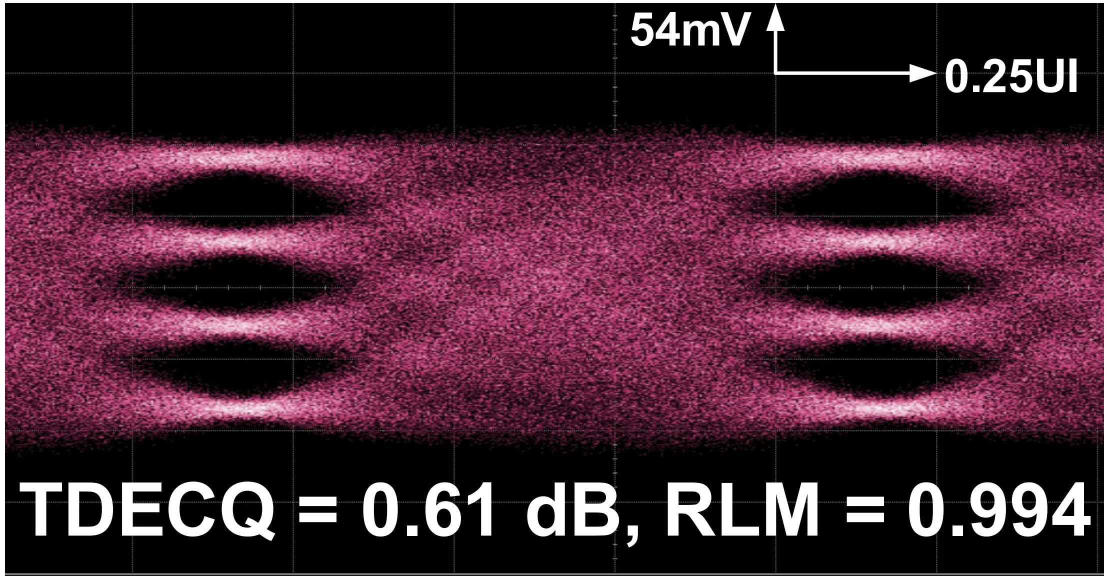


PRBS13Q Eye Diagrams @ 106.25Gb/s

Single-Ended TIA



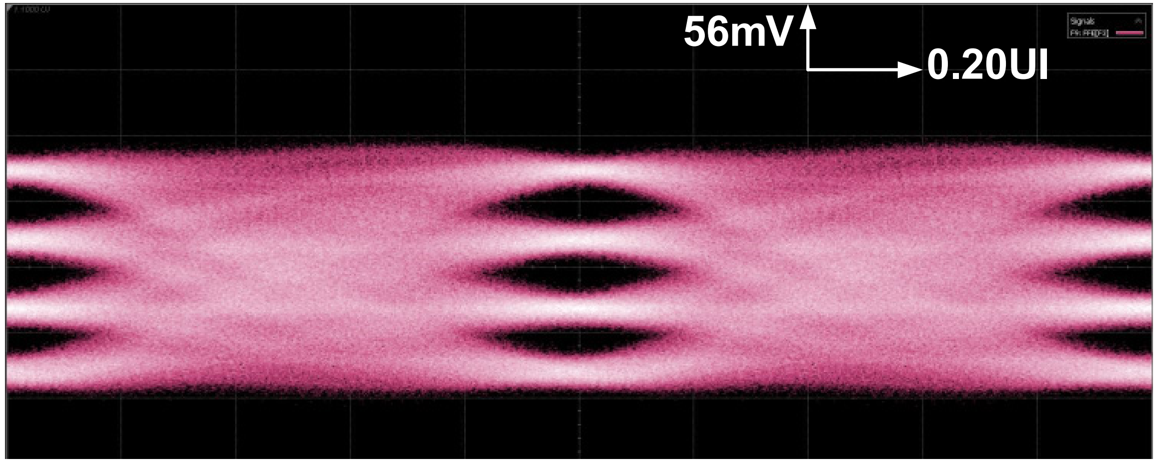
Asymmetric Differential TIA



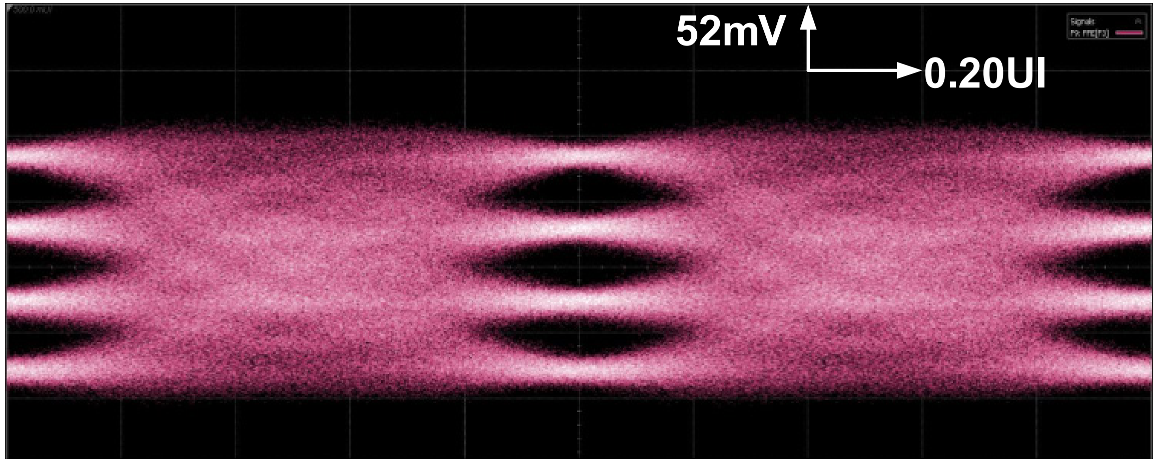
Similar linearity and bandwidth as Single-ended TIA

SSPRQ Eye Diagrams

Single-Ended TIA

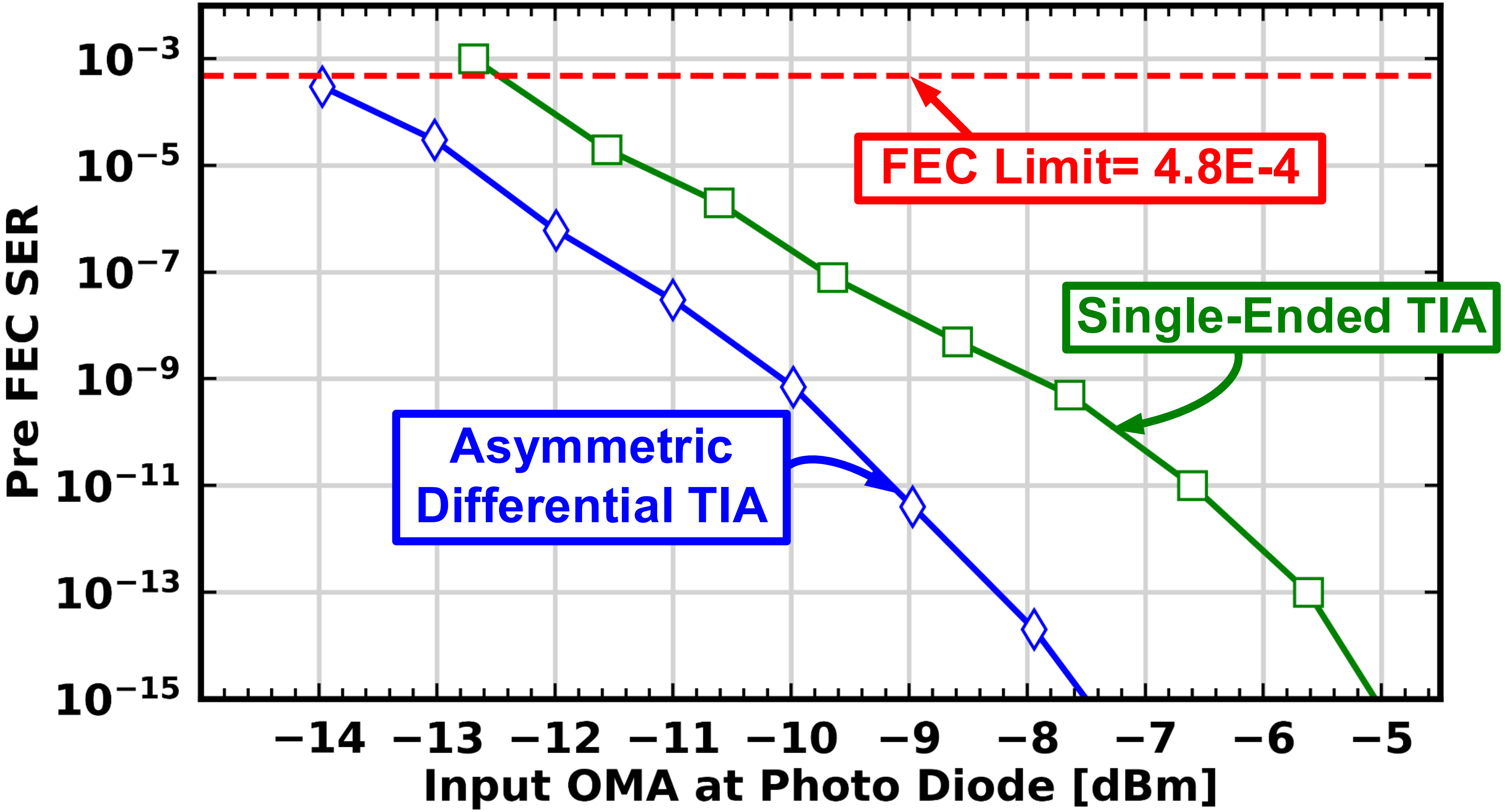


Asymmetric Differential TIA



Baseline wander similar to Single-ended TIA

Sensitivity at Photodiode



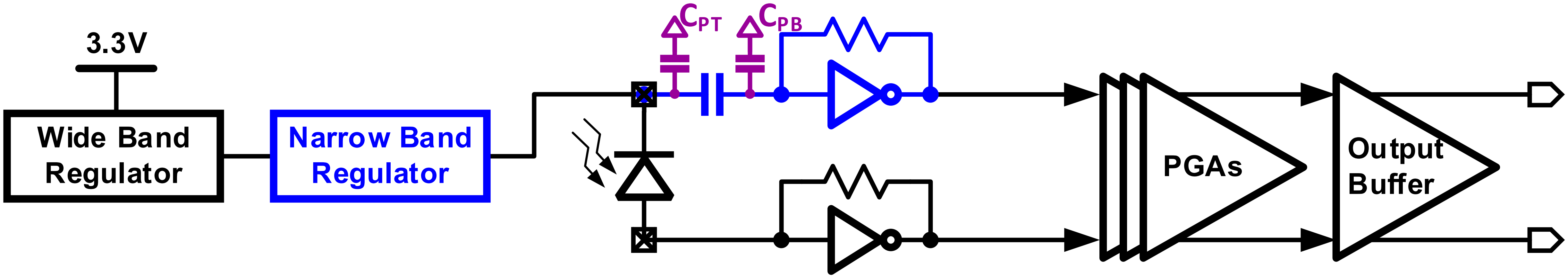
~1.5dBm improvement in optical sensitivity → 3dB higher electrical SNR

Performance Comparison

	JSSC'19 [1]	ESSCIRC'18 [2]	JSCC'22 [3]	CICC'22 [4]	PTL'19 [5]	This work	
Technology	16nm FinFET	28nm Bulk	28nm Bulk	16nm FinFET	55nm SiGe	16nm FinFET	
Data Rate (Gbps)	106.25	112	100	112	106	106.25	
Modulation Format	PAM-4	PAM-4	PAM-4	PAM-4	PAM-4	PAM-4	
Supply Voltage (V)	1.8	2.5/1.2	1.5	0.9	3.3/2.5	1.8	3.3/1.8
TIA Architecture	Single-Ended	Single-Ended	Single-Ended	Single-Ended	Differential	Single-Ended	Differential
Optical Measurements	Yes	No	Yes	Yes	Yes	Yes	Yes
Bandwidth (GHz)	27	60	20	32	N/A	18.4	18.4
Transimpedance (dBΩ)	78	65	66	63	66	75.5	77
Input ref. noise (μA_{rms})	2.7[1]	4.7	2.5	3	3.2	1.5	1.14
Input ref. noise density (pA/√Hz)	16.7	19.3	17	16.9	N/A	9.2	7
Power (mW)	60.8	107	117	47[4]	160	103.6	108
Output Swing (mVpp diff.)	600[2]	300	600[2]	450	N/A	300	300
Sensitivity at KP4 pre-FEC SER (dBm)	-11 (5-tap FFE)	-5.1[3] (5-tap FFE)	-8.9 (2-tap FFE + 2-tap DFE on-Chip)	-9.6 (4-tap FFE + 4-tap DFE)	-5[5]/-7[6]	-12.48 (12-tap FFE + 1-tap DFE)	-13.97 (12-tap FFE + 1-tap DFE)

[1]Calculated [2]W/O 50Ω termination [3]Simulated [4]No supply regulation [5]In-fiber OMA [6]Calculated w/ PD responsivity

Conclusion



- **Asymmetric signal path differential TIA**
  - SNR improvement ~ 3 dB over single-ended TIA
  - Improved baseline wander performance
- **Lowest reported noise for 100 Gbps PAM-4 TIAs**
  - Facilitates fully-integrated (TIA+DSP) solutions

Thank You!

A Carrier-Phase-Recovery Loop for a 3.2pJ/b 24Gb/s QPSK Coherent Optical Receiver

Ahmed E. Abdelrahman[1], Mostafa G. Ahmed[1,2], Mahmoud A. Khalil[1], Mohamed Badr Younis[1], Kyu-Sang Park[1], Pavan Kumar Hanumolu[1]

[1] University of Illinois, Urbana, IL

[2] now at Ain Shams University, Cairo, Egypt

Outline

- Motivation
- Proposed Coherent RX
- Implementation Details
- Measurement Results
- Summary

Growing Data Traffic Demand$_{1/2}$

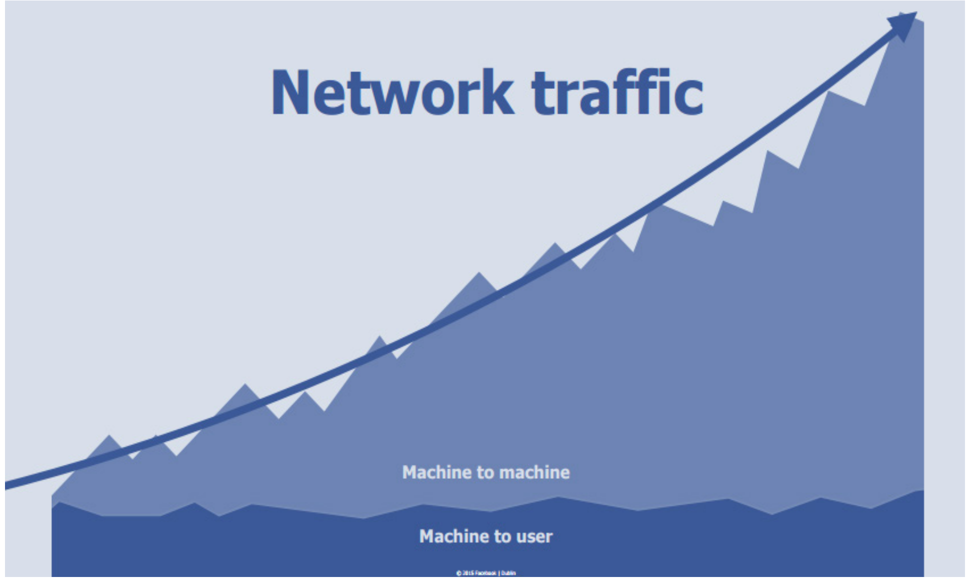


Figure Courtesy of Facebook

- **High-speed optical interconnects**
  - IM-DD: 50Gbaud per λ

Growing Data Traffic Demand$_{2/2}$

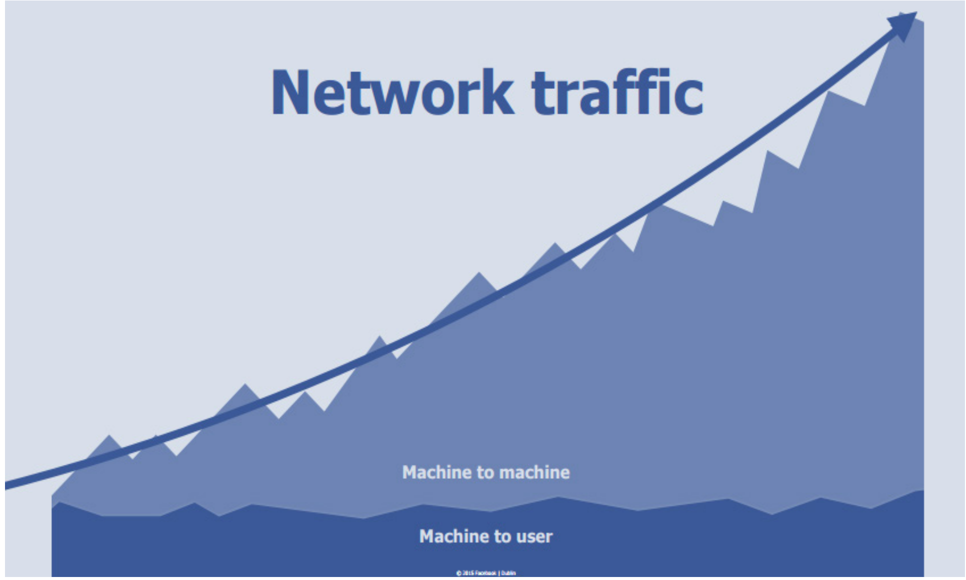
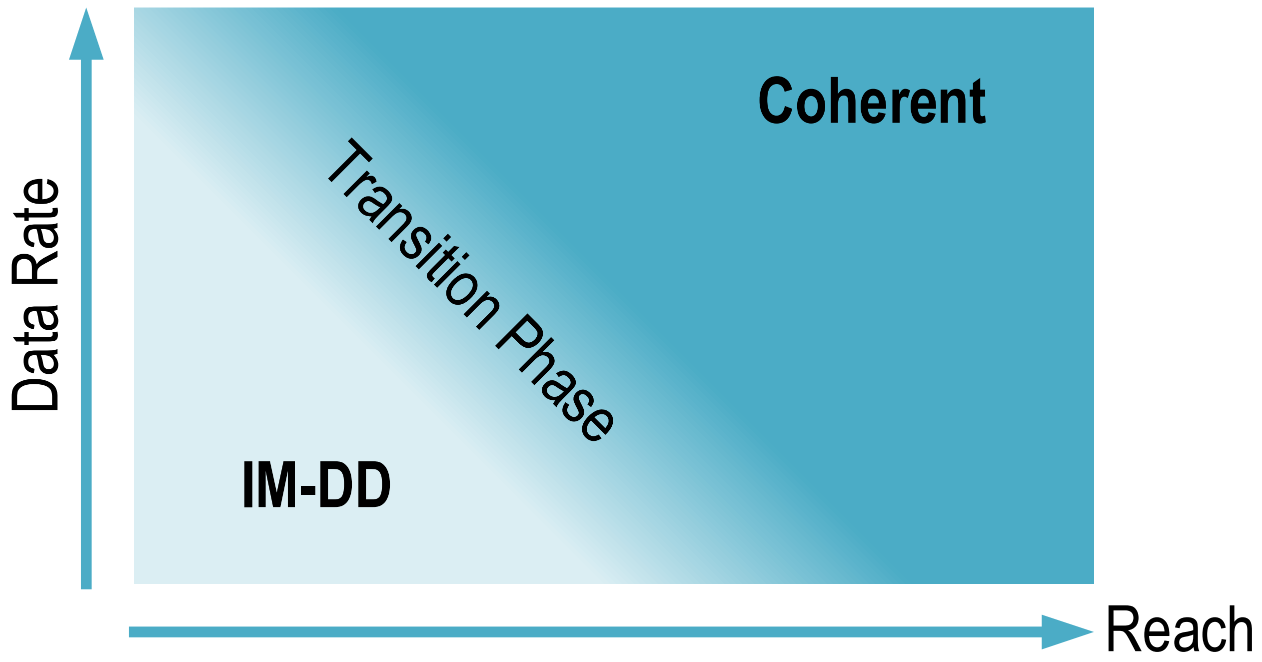


Figure Courtesy of Facebook

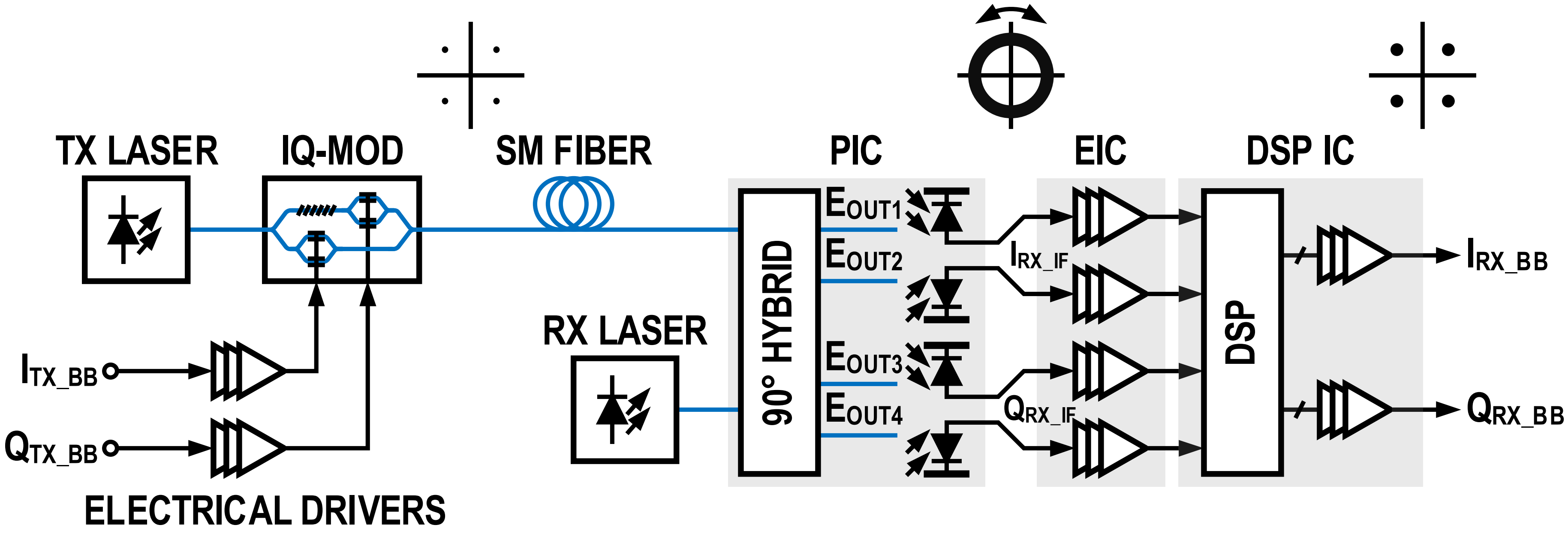
- **High-speed optical interconnects**
  - IM-DD: 50Gbaud per λ
- **Increasing data rate**
  - More wavelengths (WDM)
  - Higher modulation order

Coherent Communication



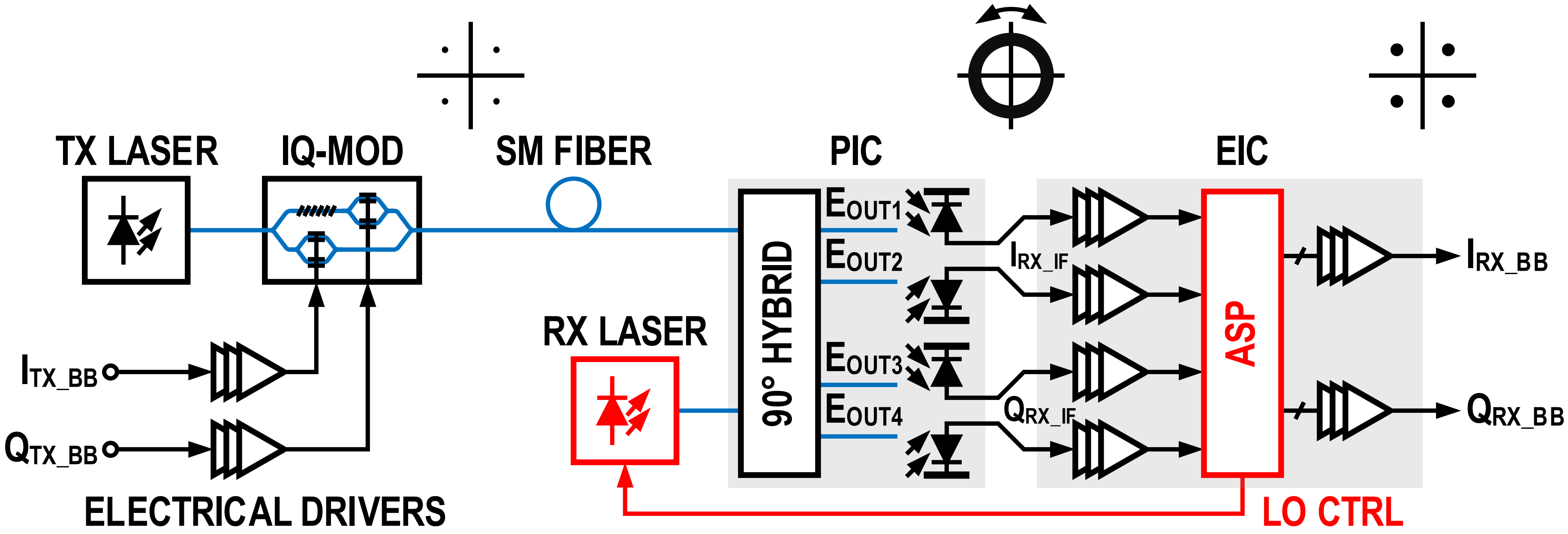
- Employed in long-haul communication
- Better spectral efficiency
- Complex signal processing

DSP-based Coherent Links



- **RX signal processing**
  - Polarization demultiplexing
  - Dispersion compensation/equalization
  - Carrier frequency and phase recovery
- **Power hungry**

ASP-based Coherent Links



- **Mixed-signal dispersion compensation/equalization**
  - Lower power
- **Requires**
  - Tunable lasers
  - High-bandwidth carrier phase recovery loops

Outline

- Motivation
- **Proposed Coherent RX**
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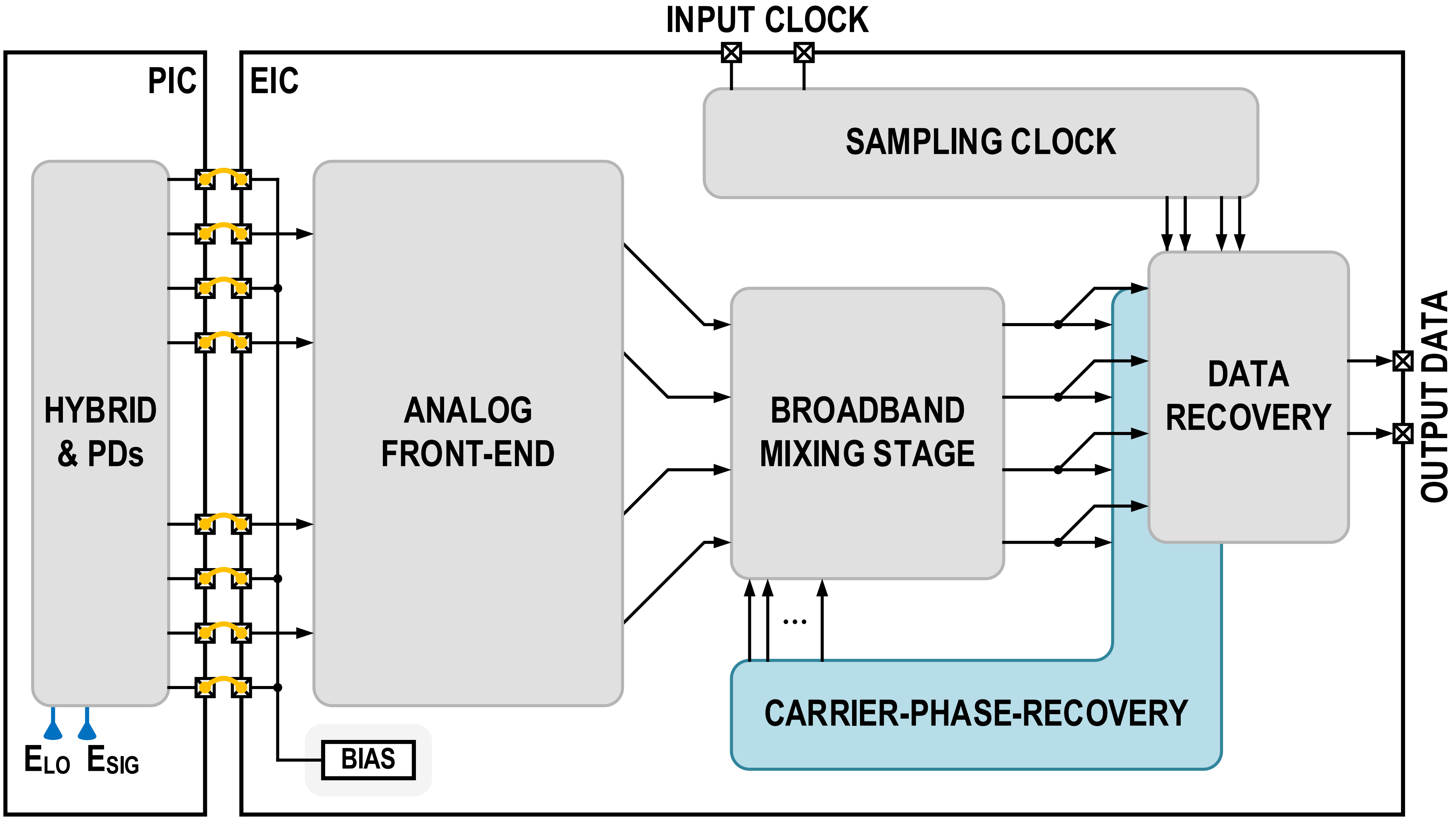
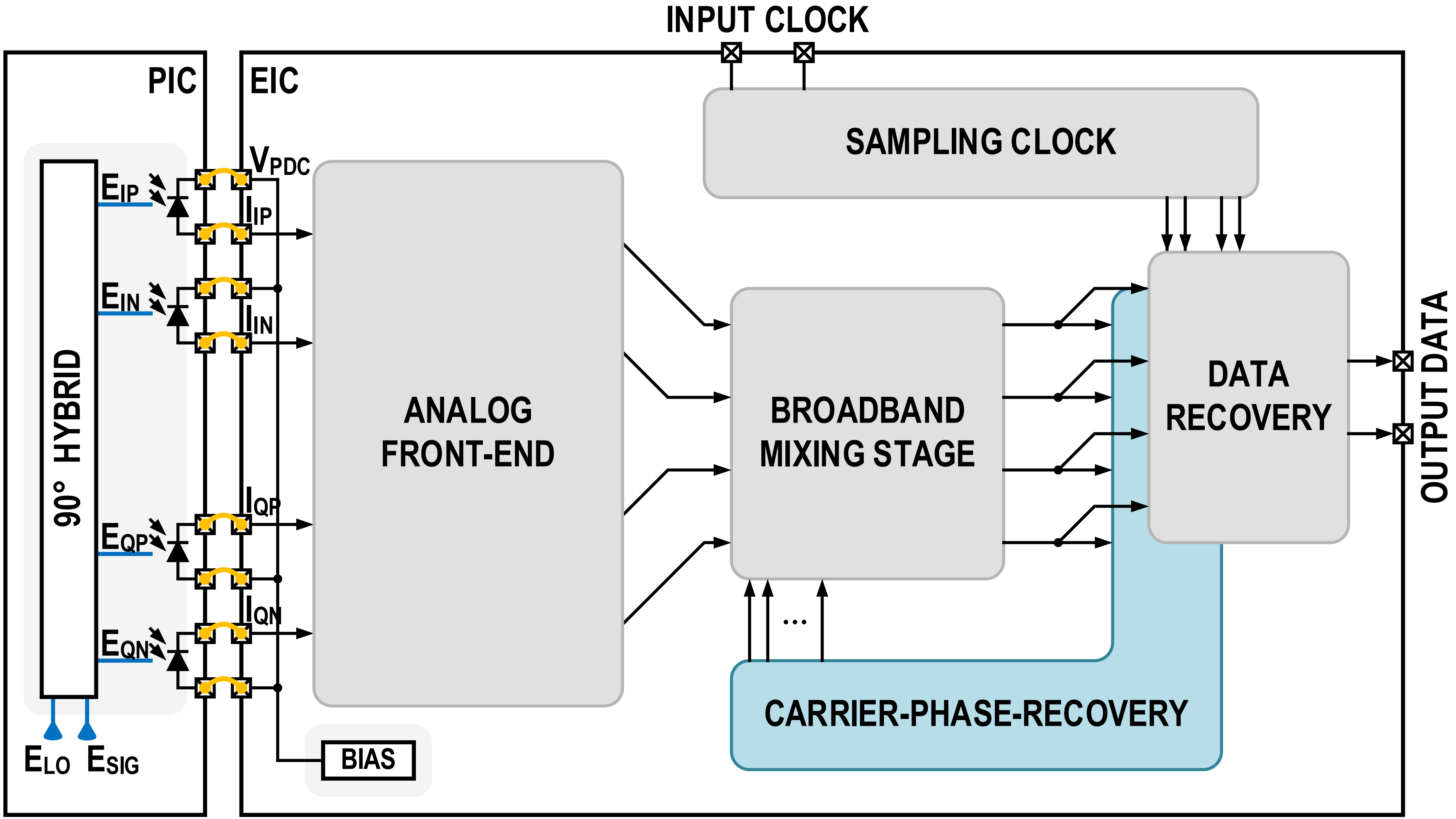
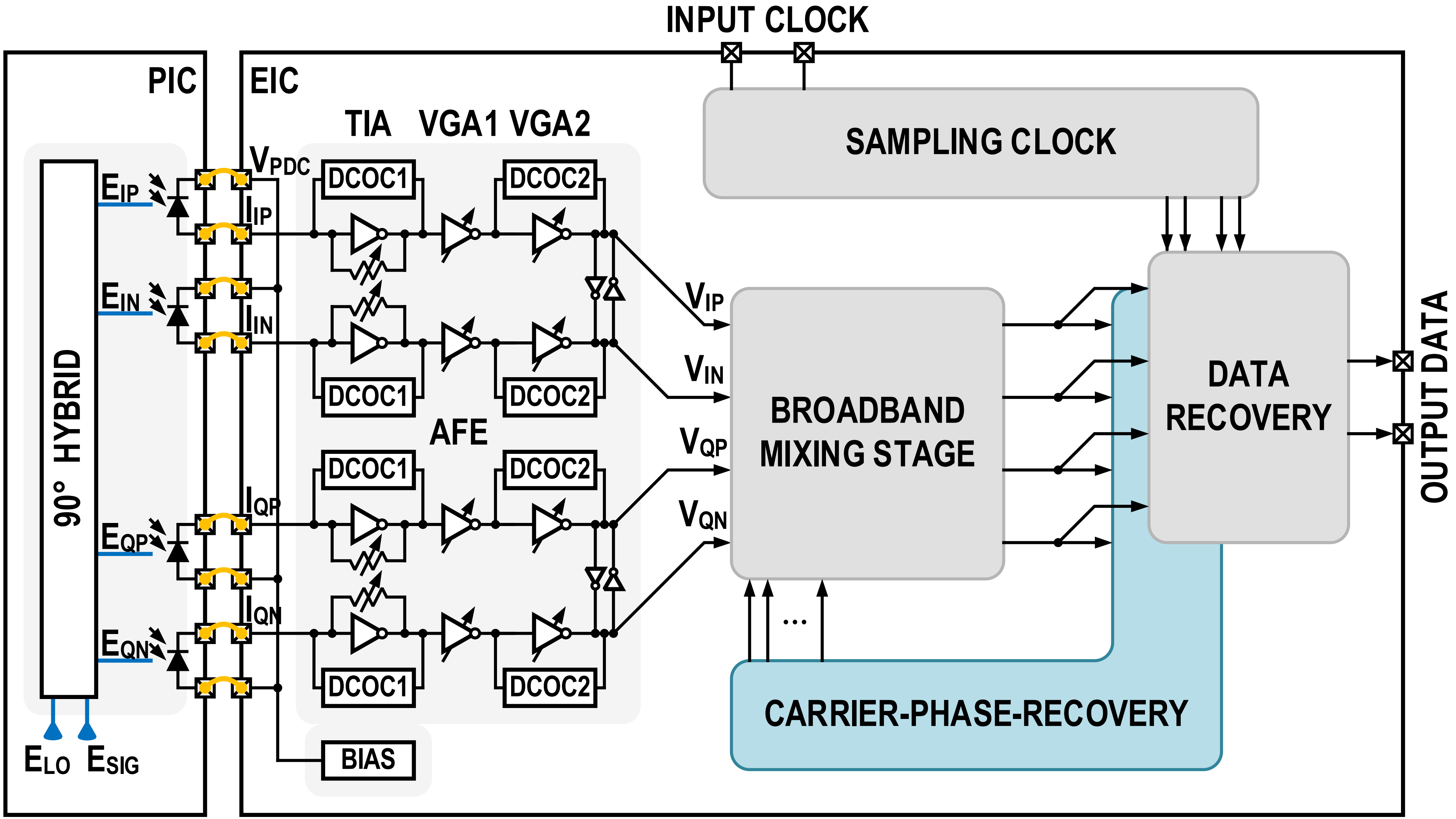
Proposed Coherent RX



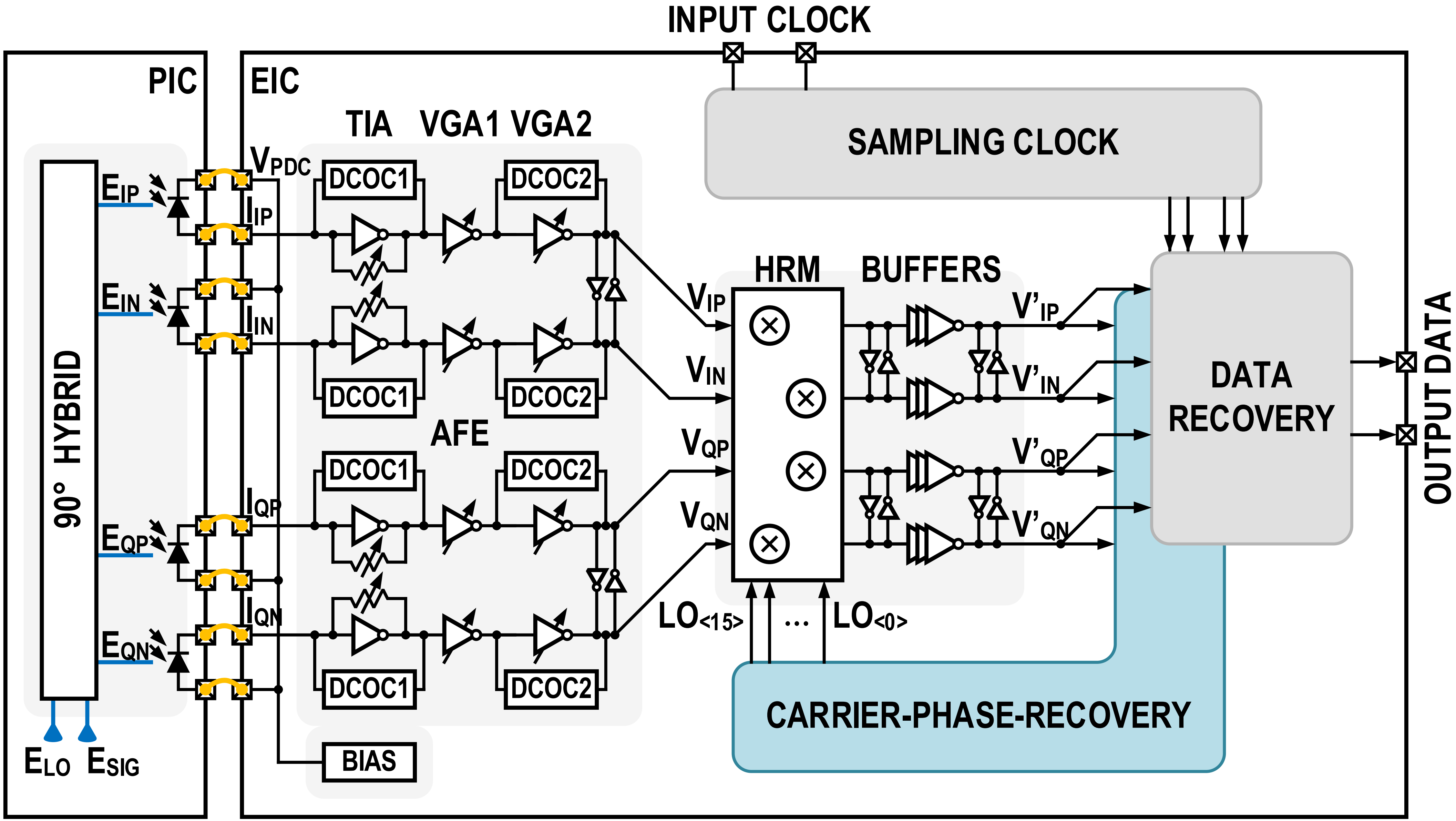
Photonics IC



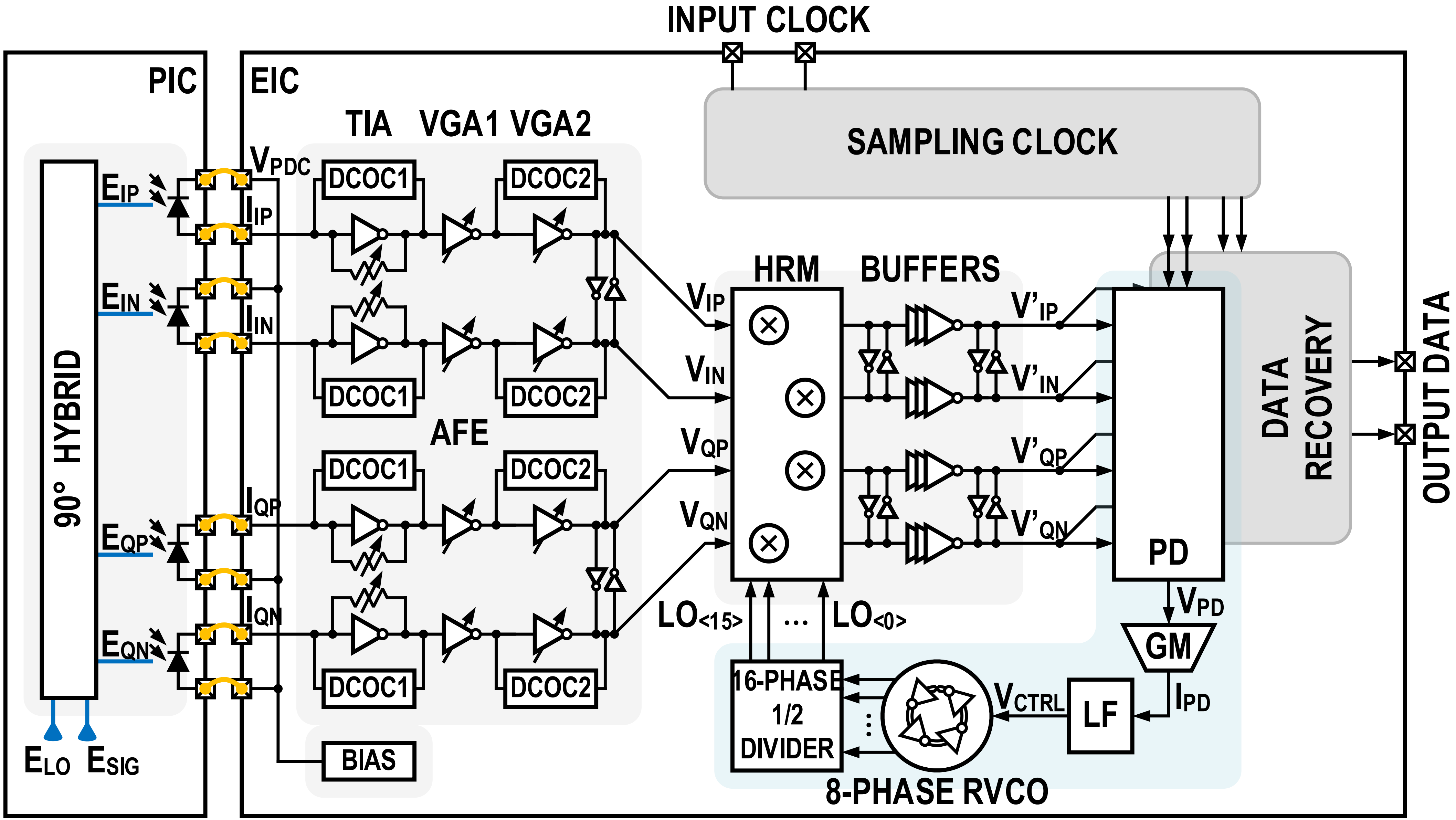
Analog Front-End



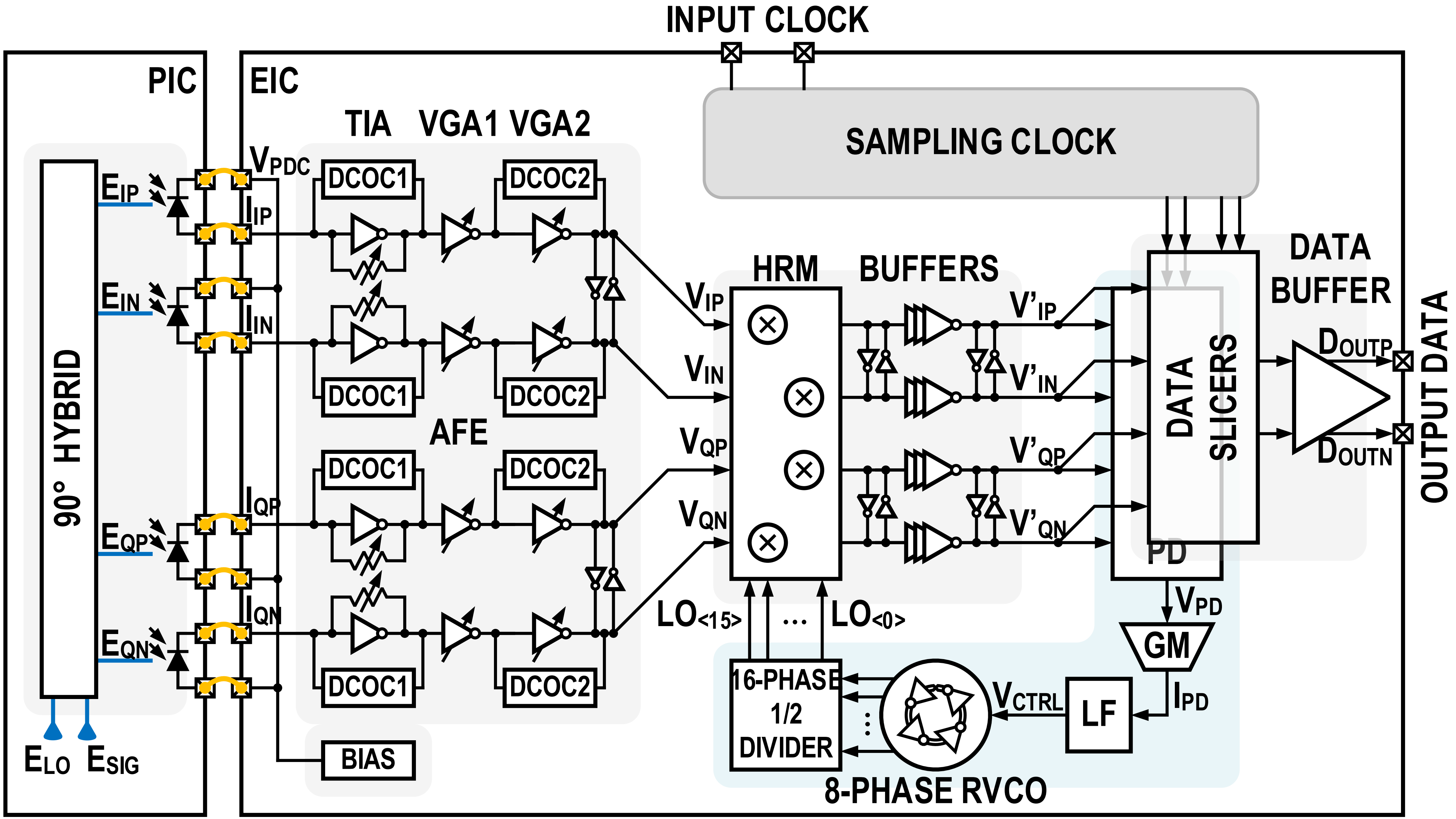
Broadband Mixing Stage



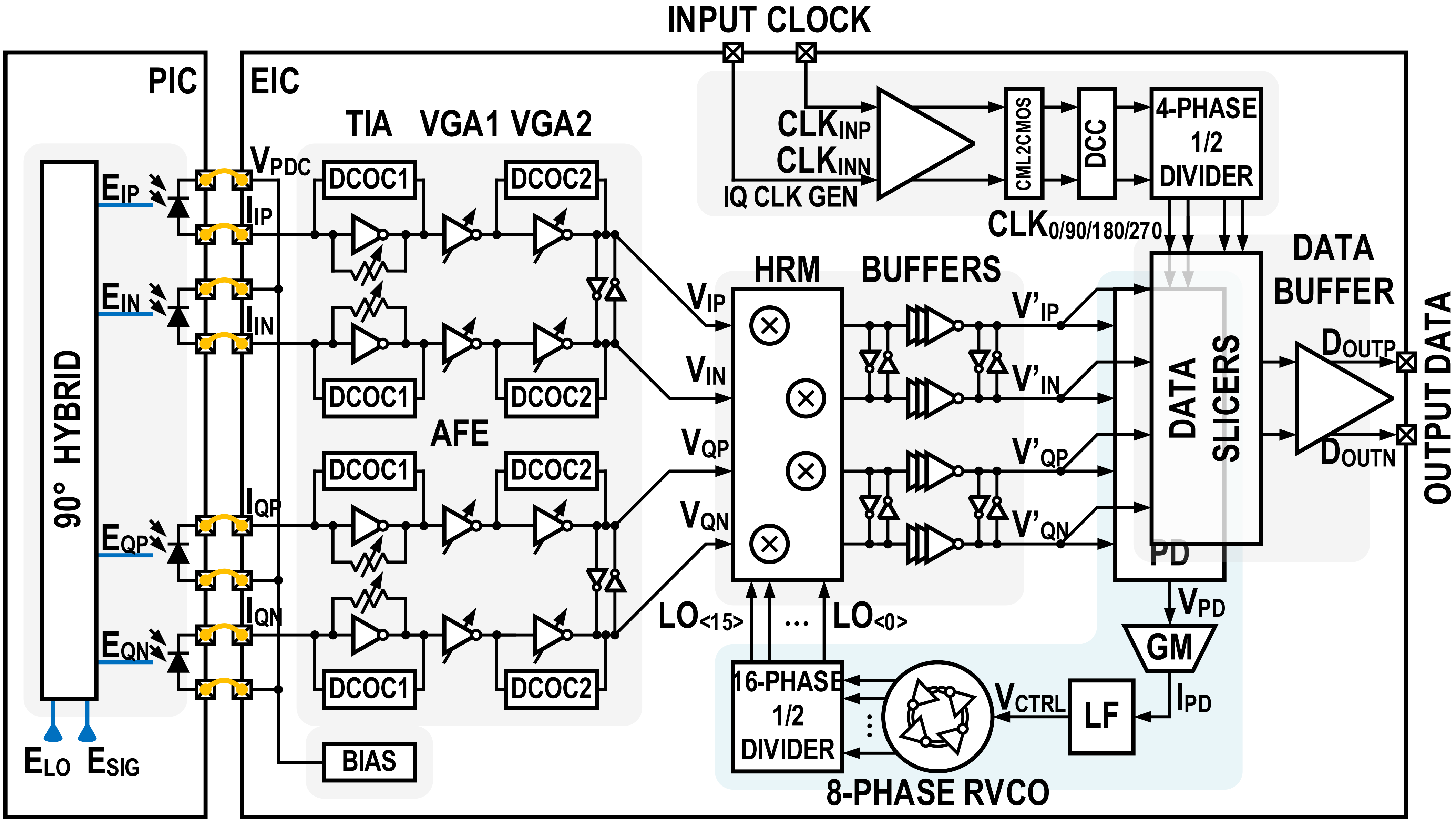
Carrier-Phase-Recovery Loop



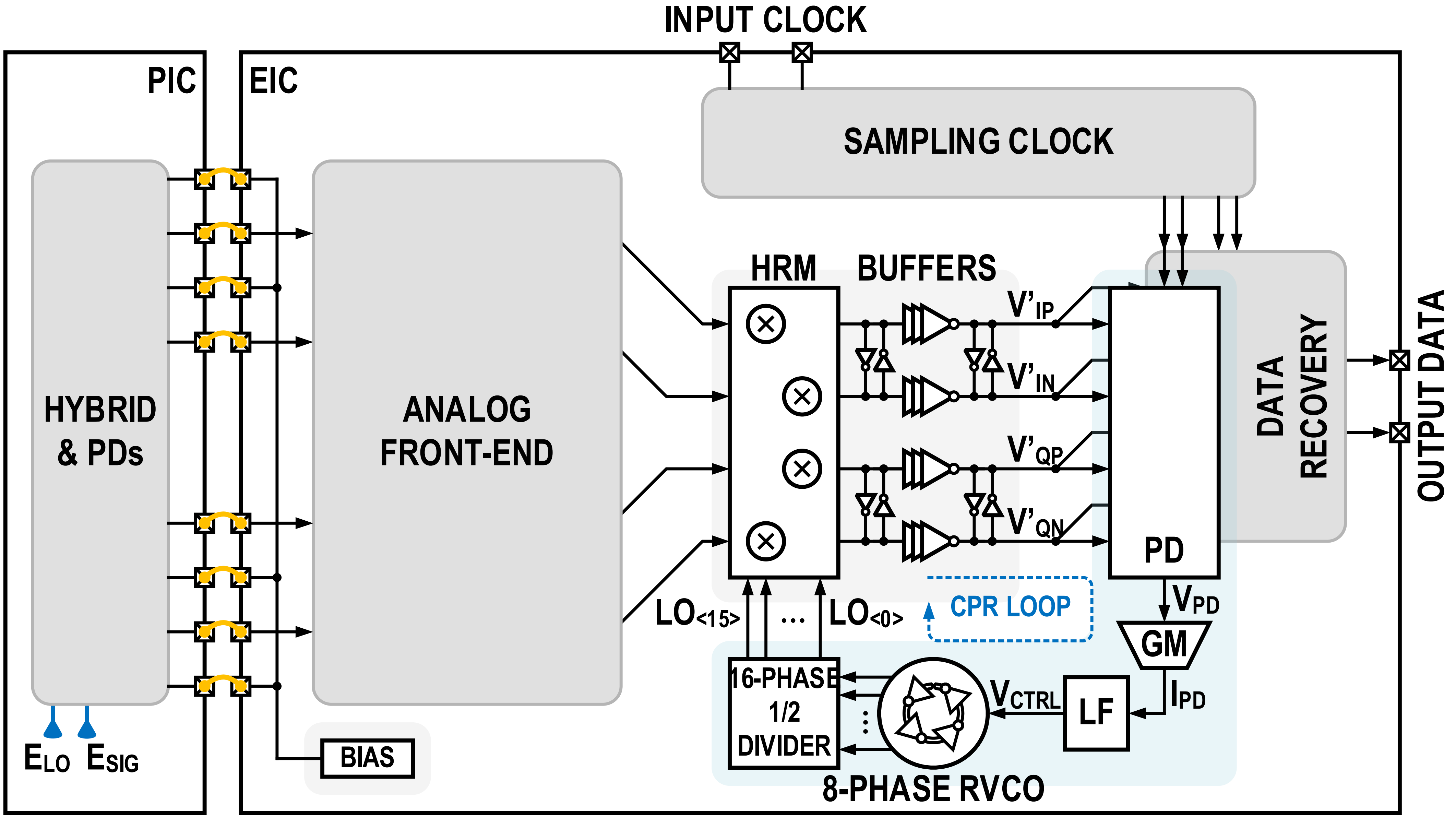
Data Recovery



Sampling Clock Path



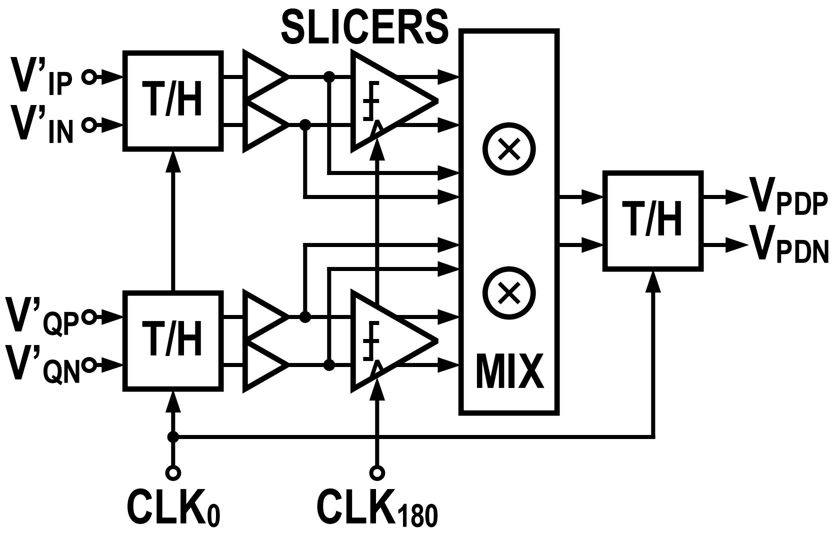
Focus: Carrier-Phase-Recovery Loop

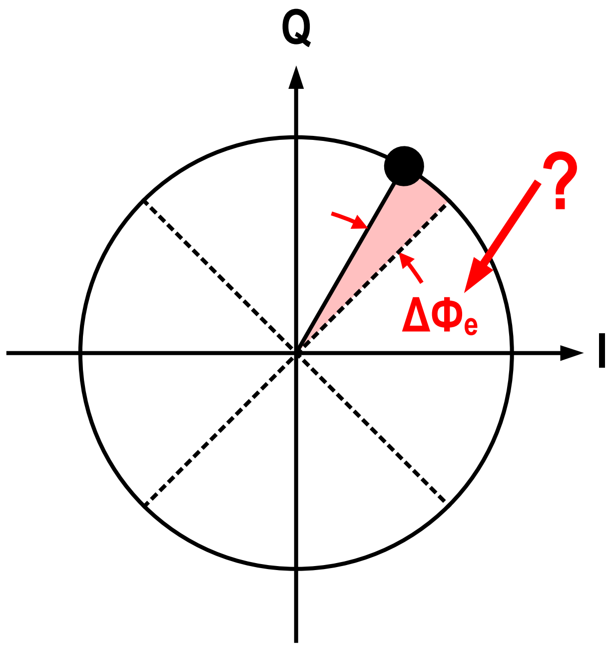


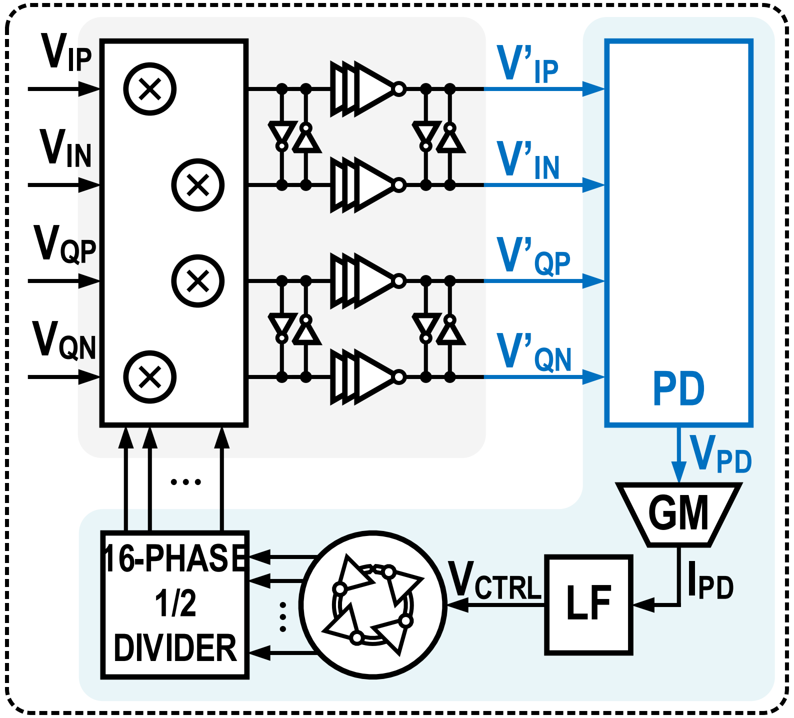
Outline

- Motivation
- Proposed Coherent RX
- **Implementation Details**
- Measurement Results
- Summary

Phase Detector$_{1/6}$

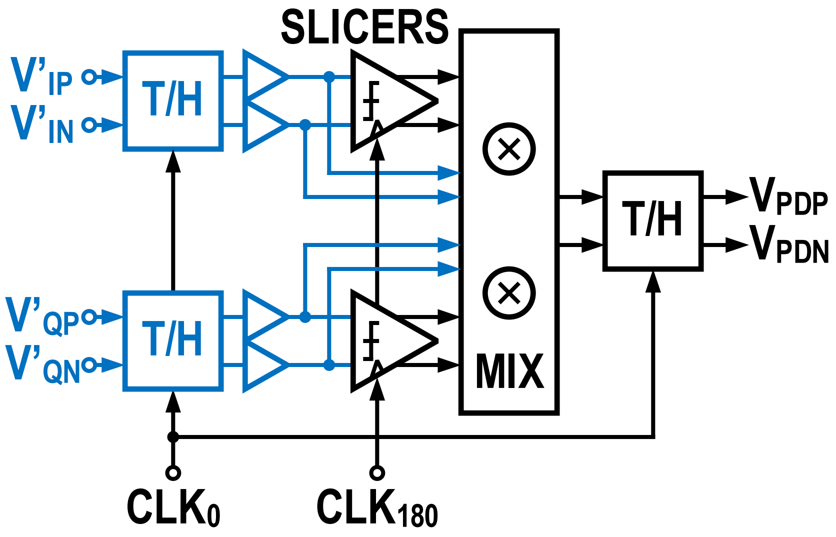


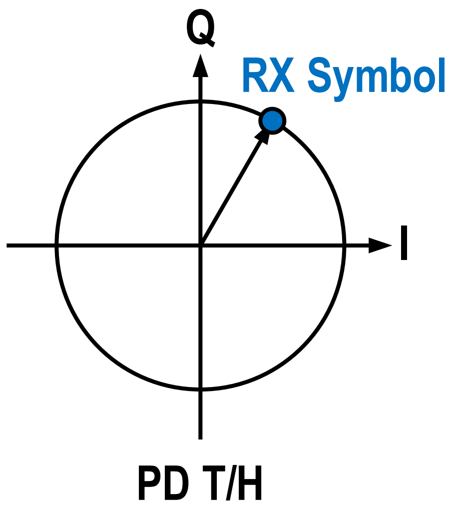




- **Decision-directed**
  - Removes data modulation through complex multiplication
  - Detects phase offsets that distort received I/Q eyes
- **Operates at quarter-rate**

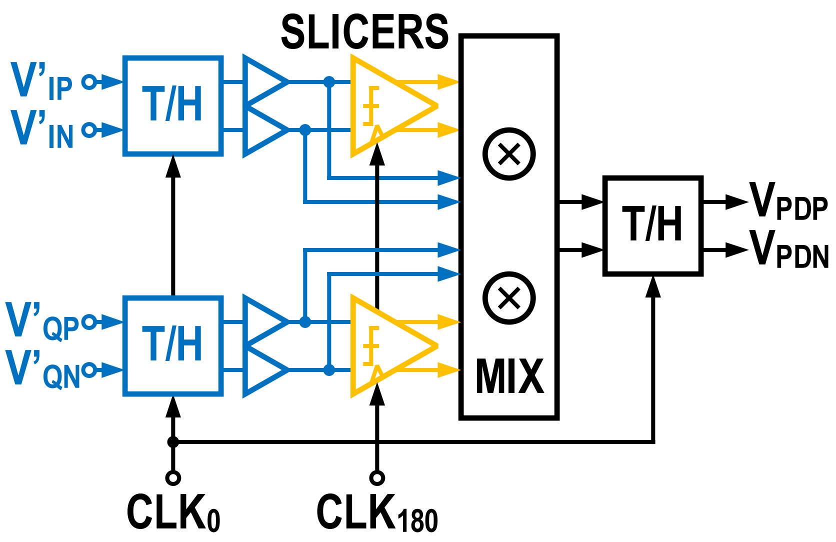
Phase Detector$_{2/6}$: Sampling

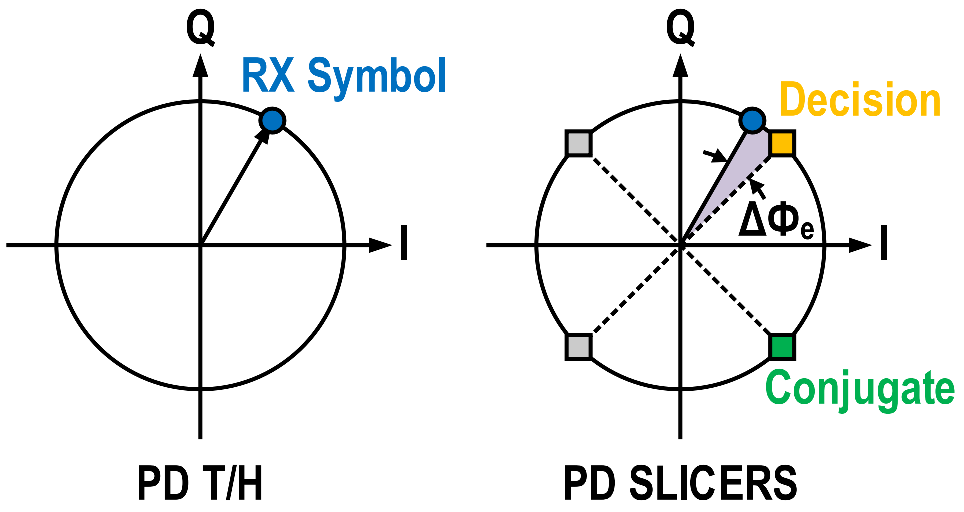




- **T/H tracks received analog signal during CLK_0**
  - Holds during CLK_{180}
- **Buffers shield the sampled signal**

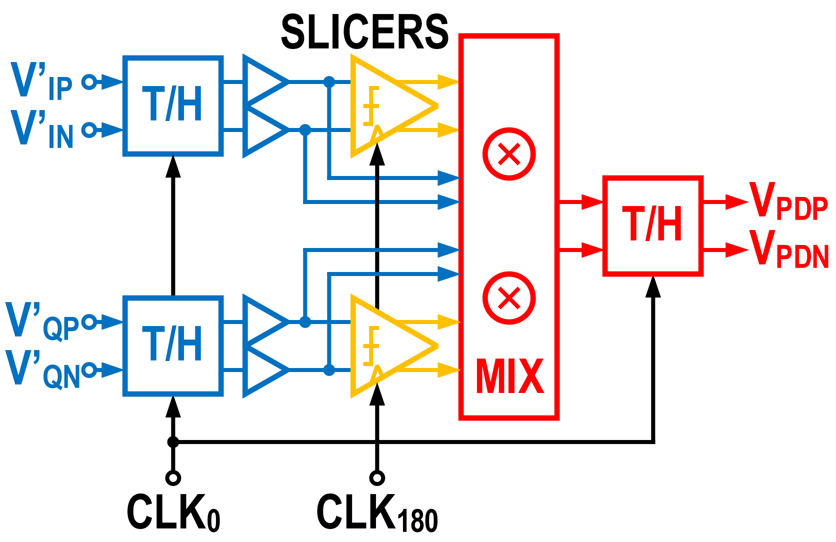
Phase Detector$_{3/6}$: Slicing

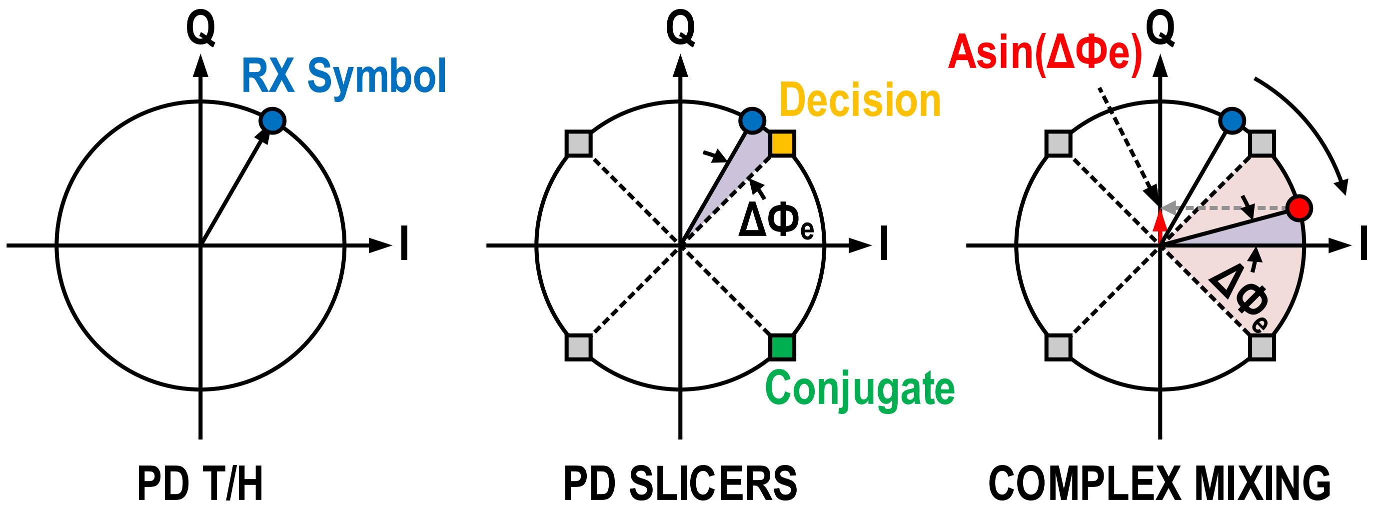




- **RX symbol is sliced during CLK$_{180}$**
  - Closest ideal constellation point is located
  - Conjugate is obtained by flipping Q-decision polarity

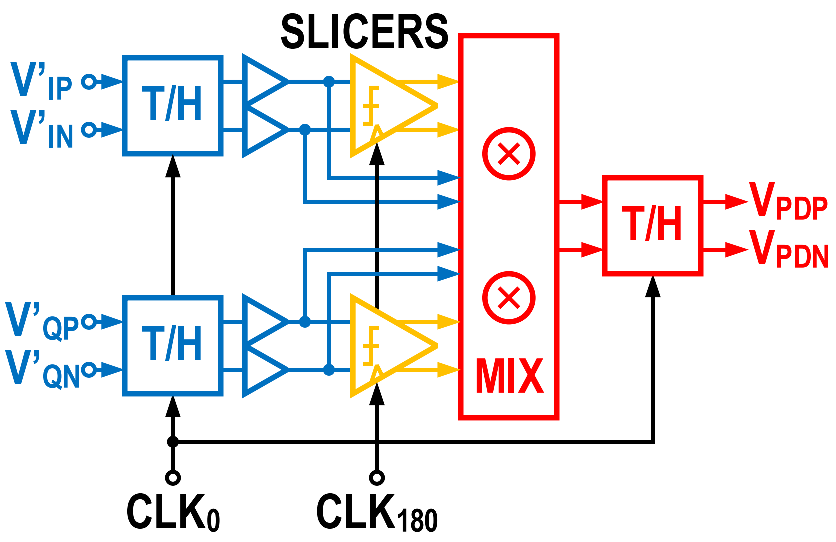
Phase Detector$_{4/6}$: Mixing

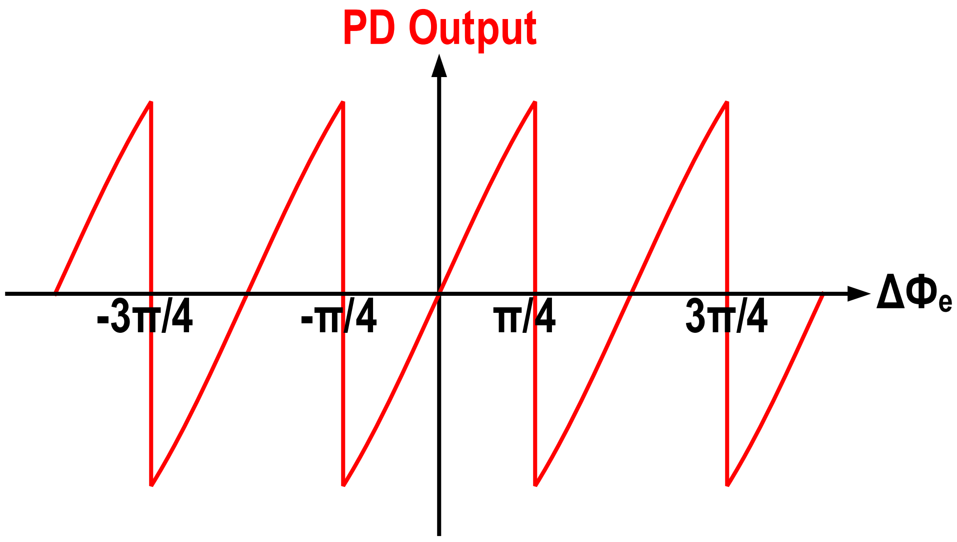




- **Complex mixing de-rotates RX symbol into –π/4 to π/4**
  - De-rotated symbol Q-component = Asin($\Delta\Phi_e$)
  - Phase-error is obtained

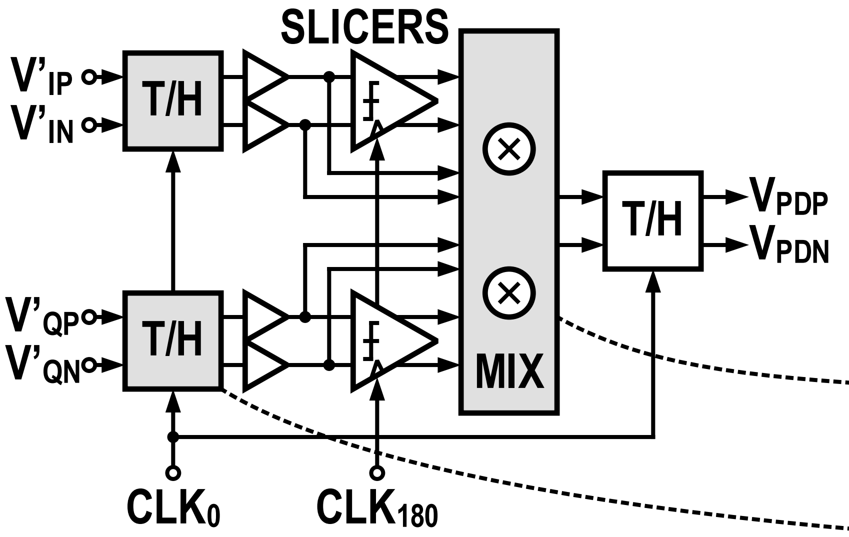
Phase Detector$_{5/6}$: Transfer Characteristics

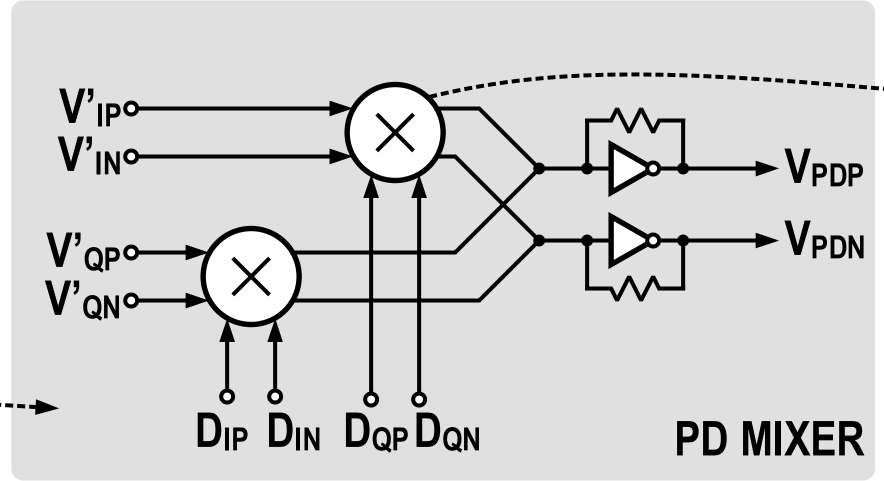


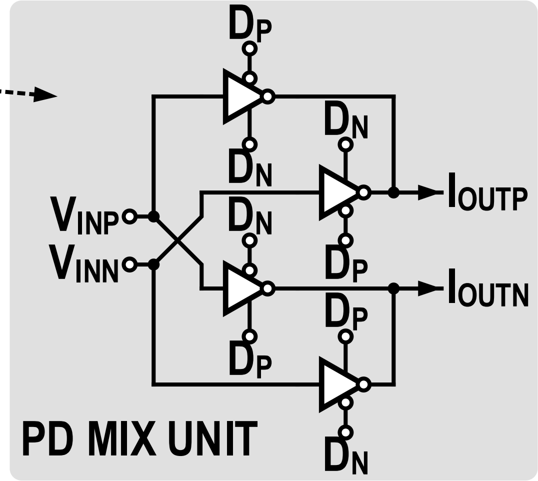


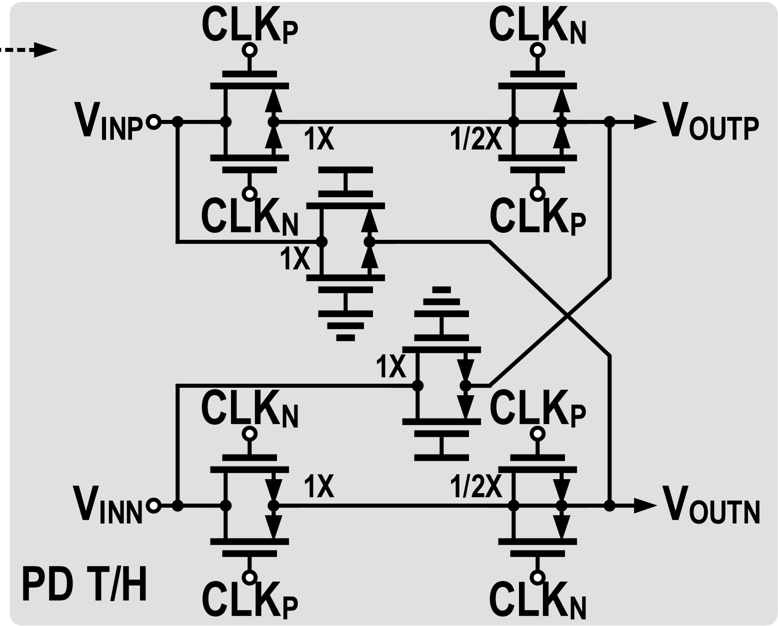
- **PD output = Asin($\Delta\Phi_e$)**
  - For small phase-errors ≈ A$\Delta\Phi_e$
- **PD gain ≈ A**
  - A is RX symbol magnitude

Phase Detector$_{6/6}$



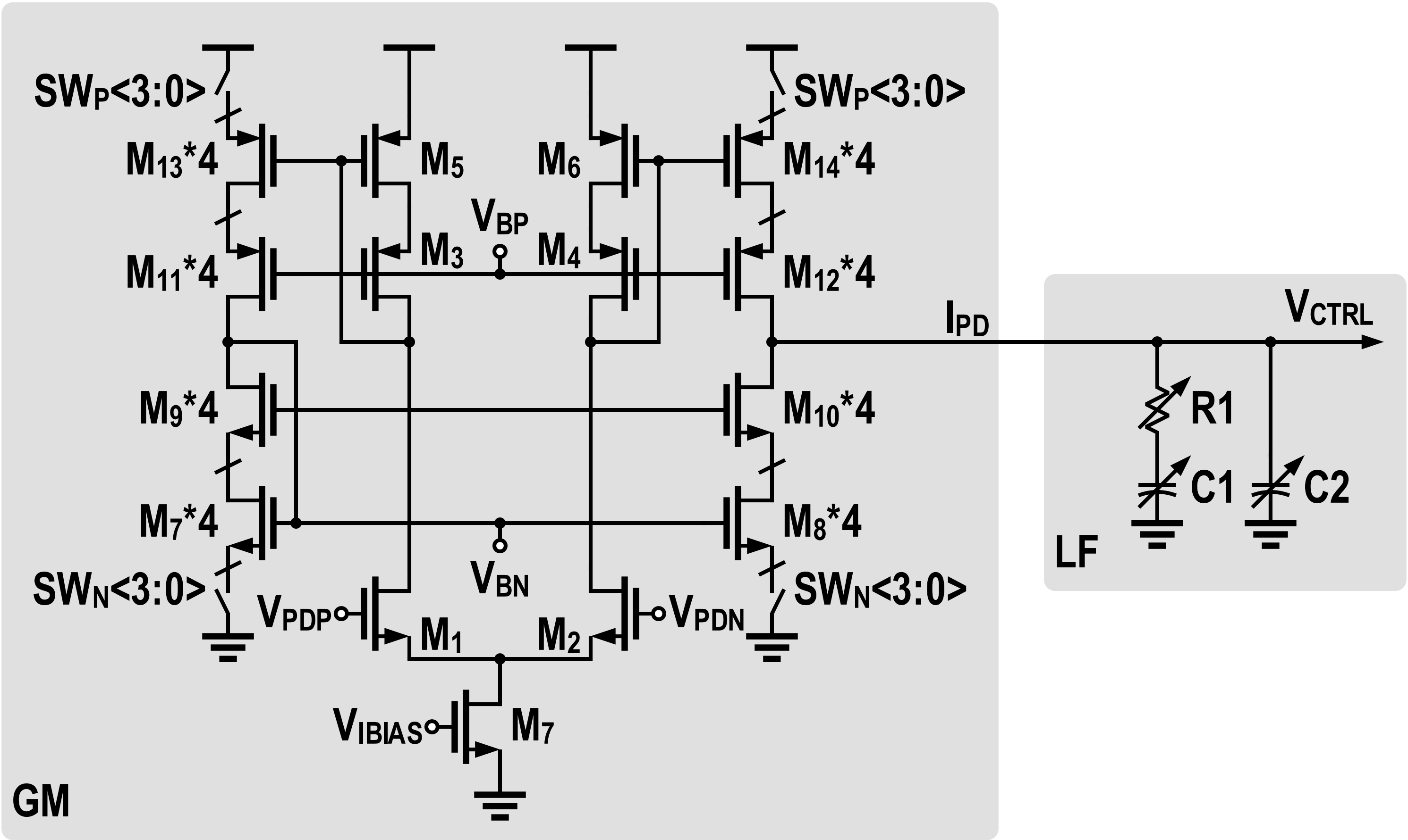


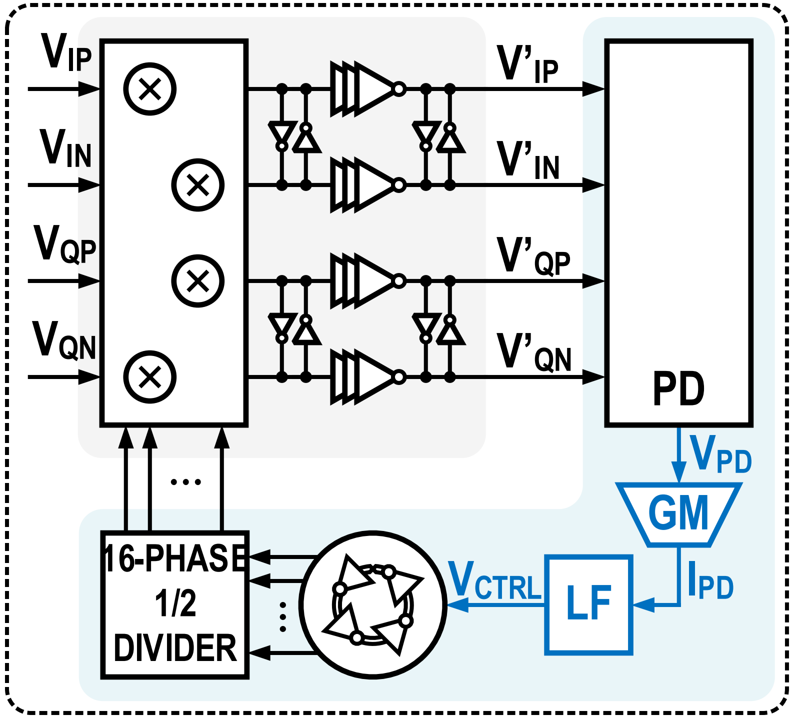




- Inverter-based mixing units
- TG-based T/H

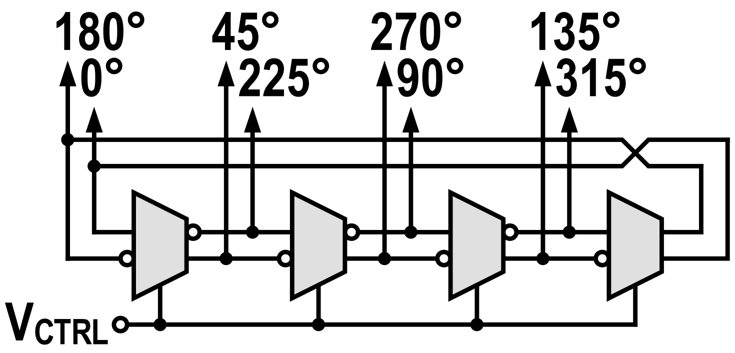
GM & LF



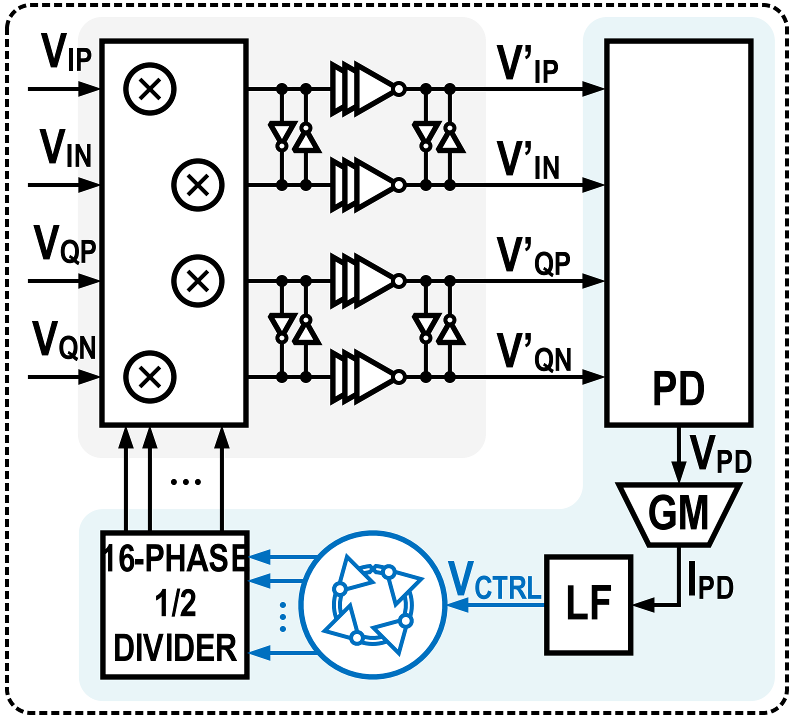


- GM: high-voltage-gain mirror-OTA
- LF: second-order passive filter

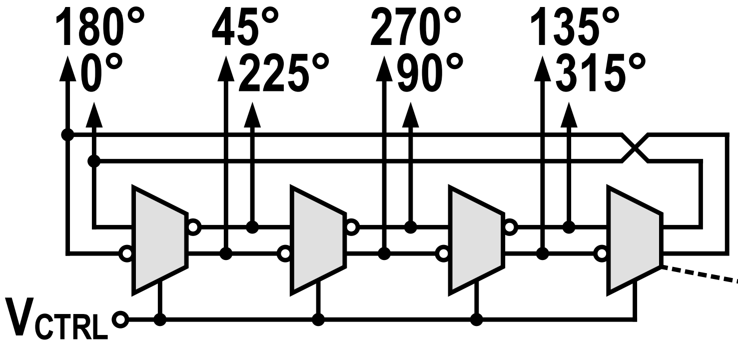
8-Phase Ring-$VCO_{1/2}$

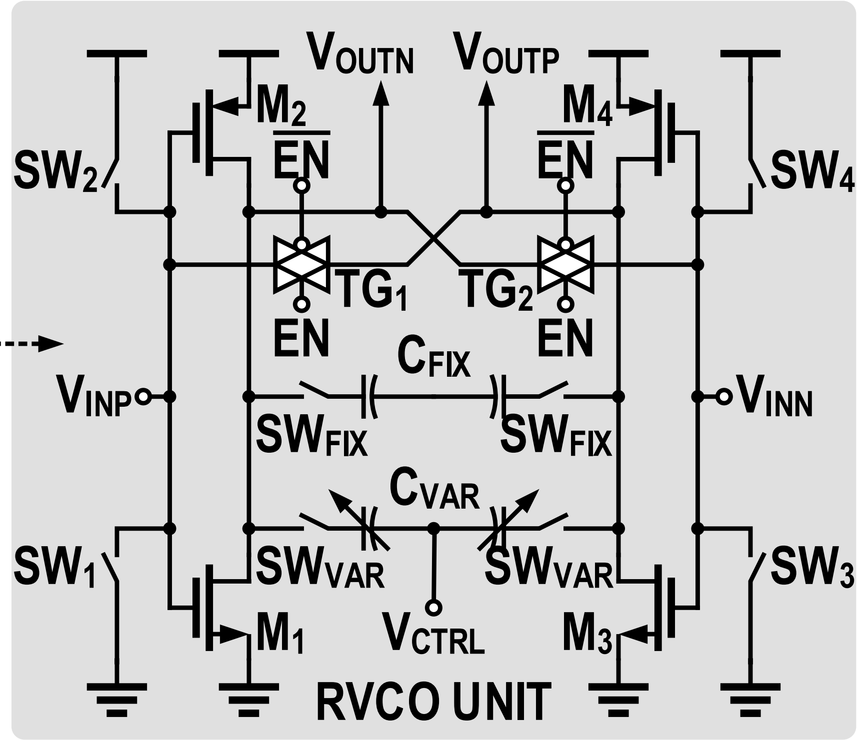


- Generates 8 phases at $2F_{IF}$



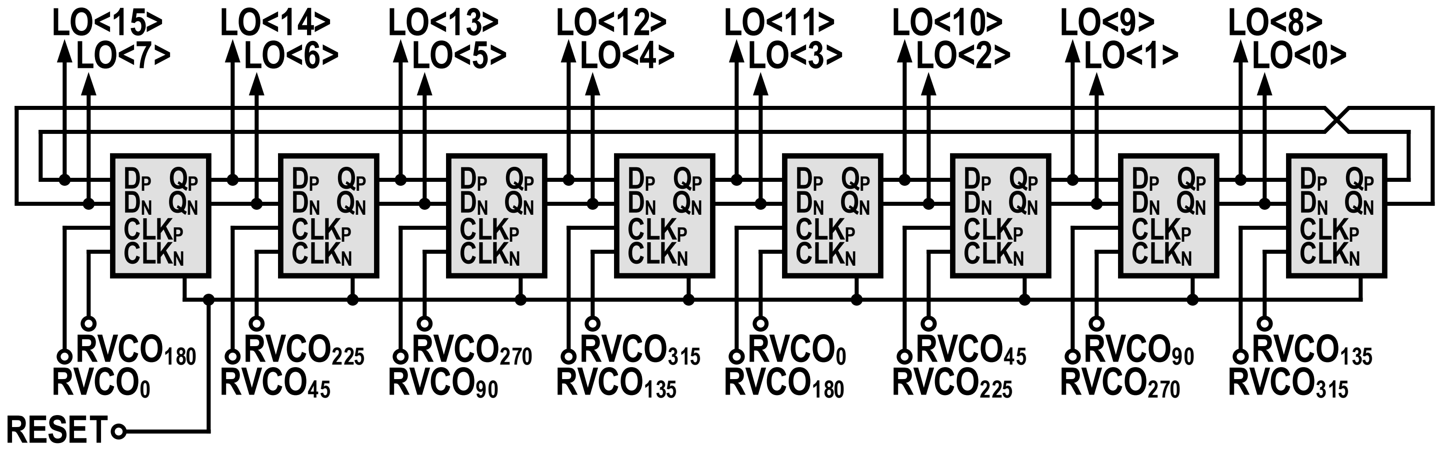
8-Phase Ring-$VCO_{2/2}$

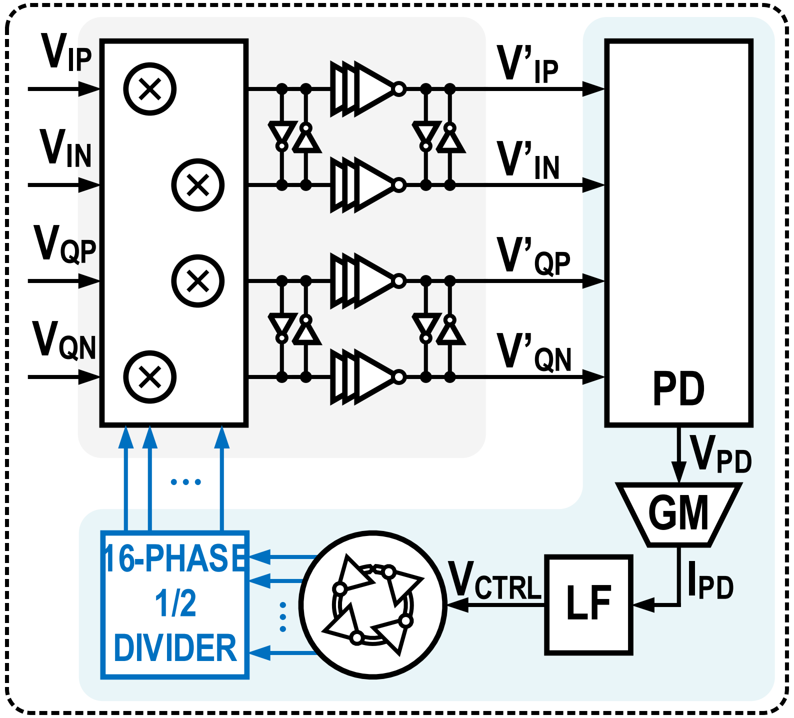




- **Generates 8 phases at $2F_{IF}$**
- **Tuning**
  - Fixed cap. bank → Center frequency
  - Varactor cap. bank → K_{VCO}
  - V_{CTRL} → Frequency tuning
  - VDD/VSS switches → Initial state and fast startup

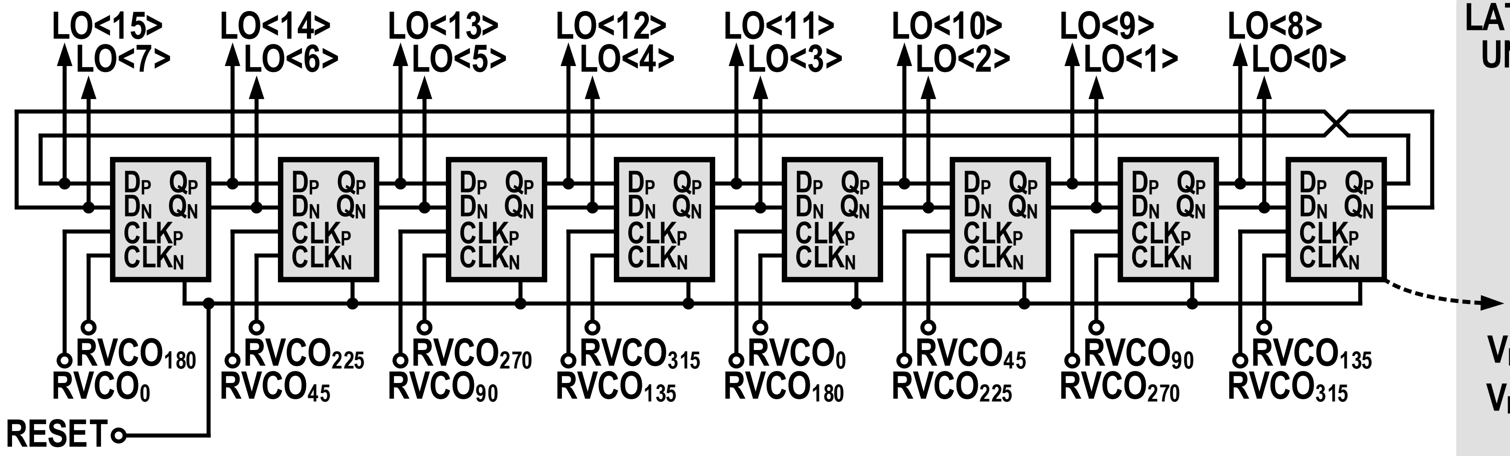
16-Phase ½ Divider$_{1/3}$

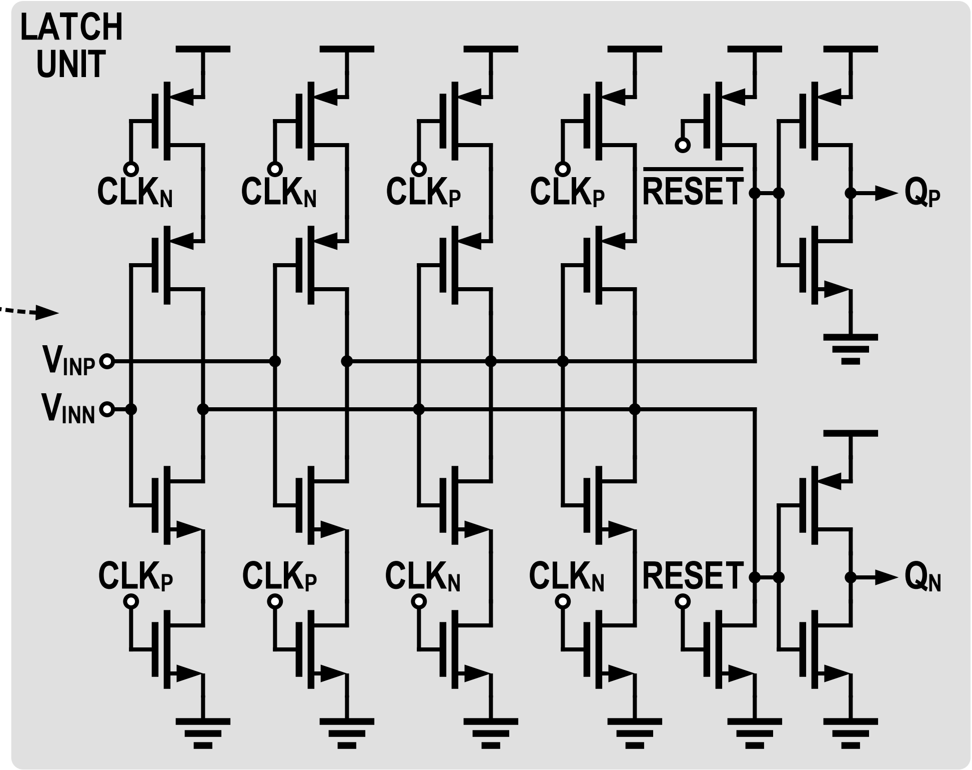




- Generates 50% duty cycle LO signals
- Converts 8 phases at $2F_{IF}$ to 16 at F_{IF}
  - Phases order is crucial → shift register implementation

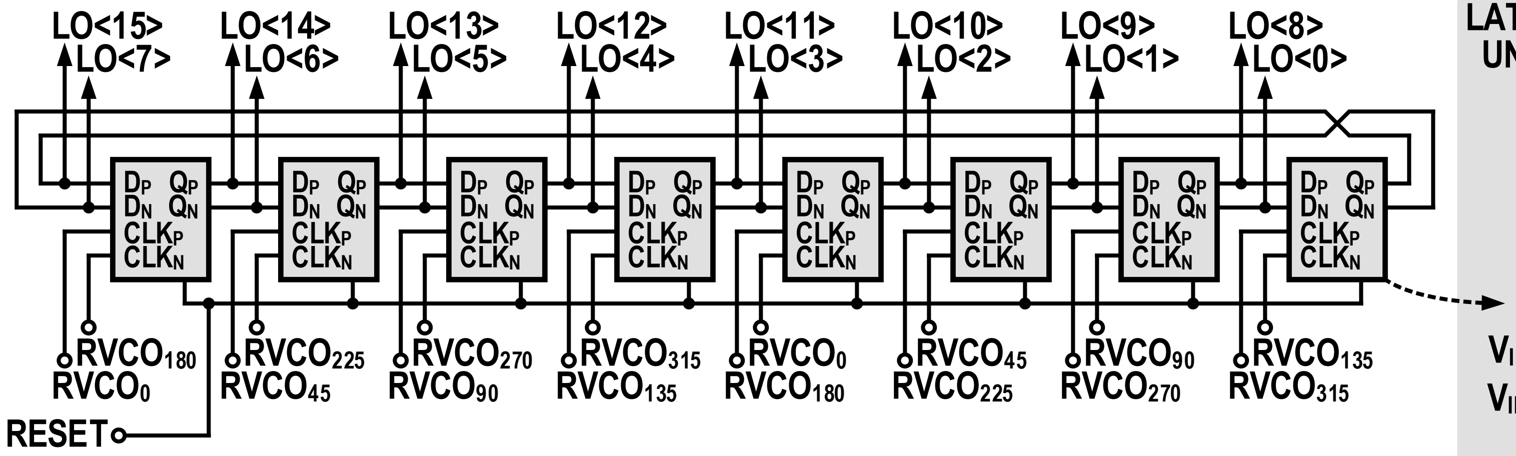
16-Phase ½ Divider$_{2/3}$

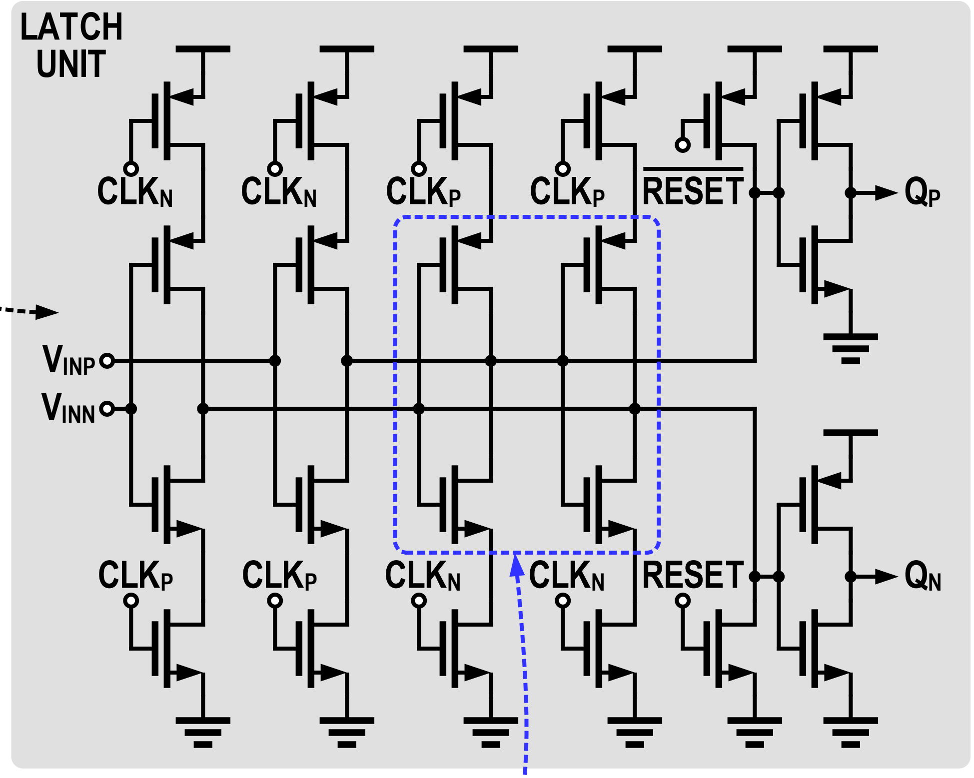




- **Generates 50% duty cycle LO signals**
- **Converts 8 phases at $2F_{IF}$ to 16 at F_{IF}**
  - Phases order is crucial → shift register implementation

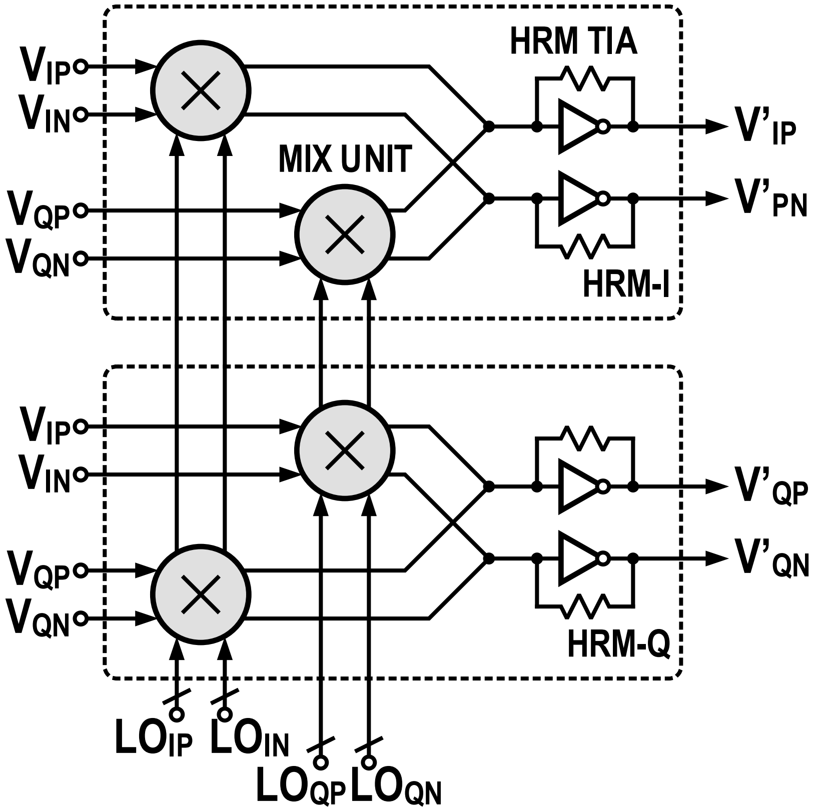
16-Phase ½ Divider$_{3/3}$

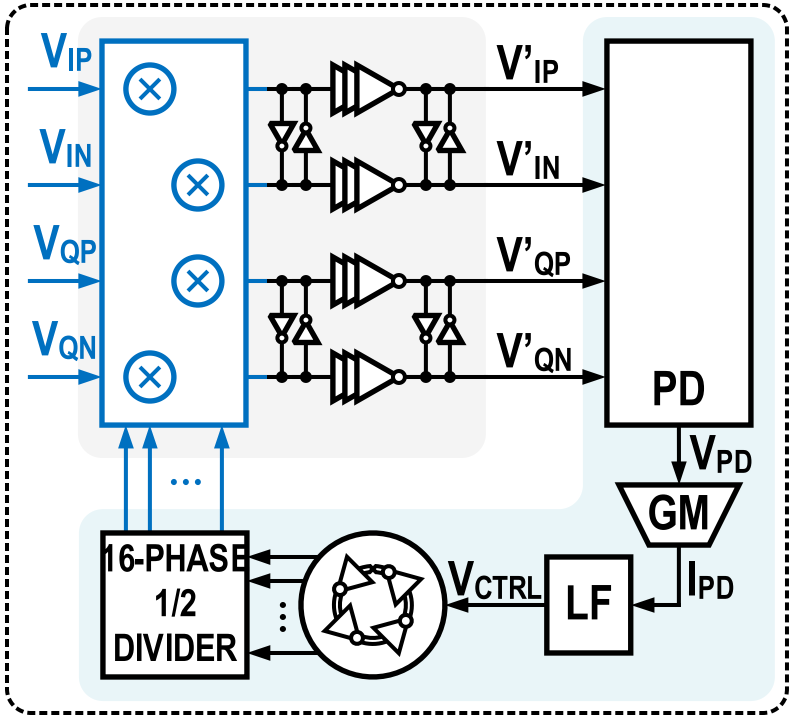




- **Generates 50% duty cycle LO signals**
- **Converts 8 phases at $2F_{IF}$ to 16 at F_{IF}**
  - Phases order is crucial → shift register implementation
- **Cross-coupled latches ensures differentiality**
  - Especially during start-up or after async. reset

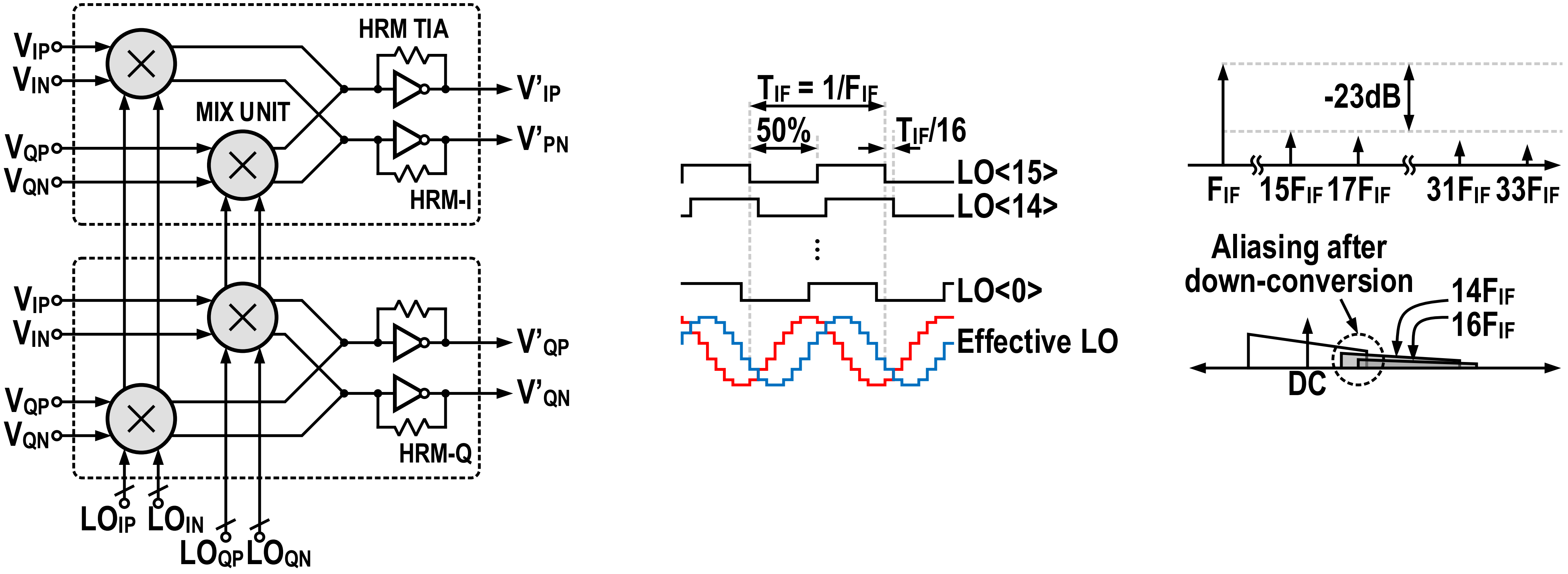
16-Phase Harmonic Rejection Mixer$_{1/4}$





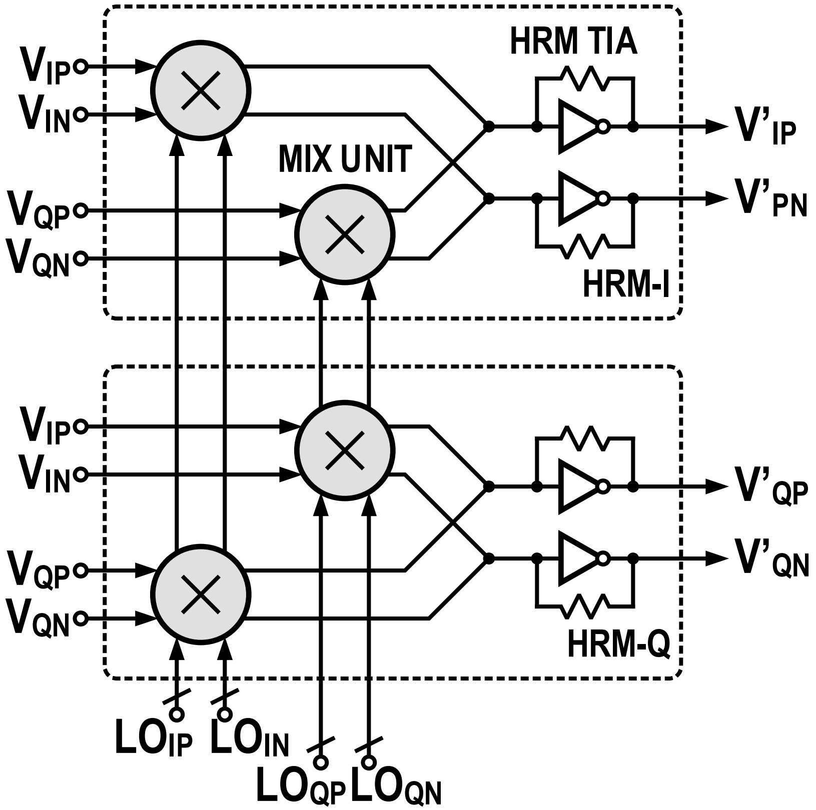
- **Broadband I/Q complex mixer**
  - Frequency shifter in frequency-domain

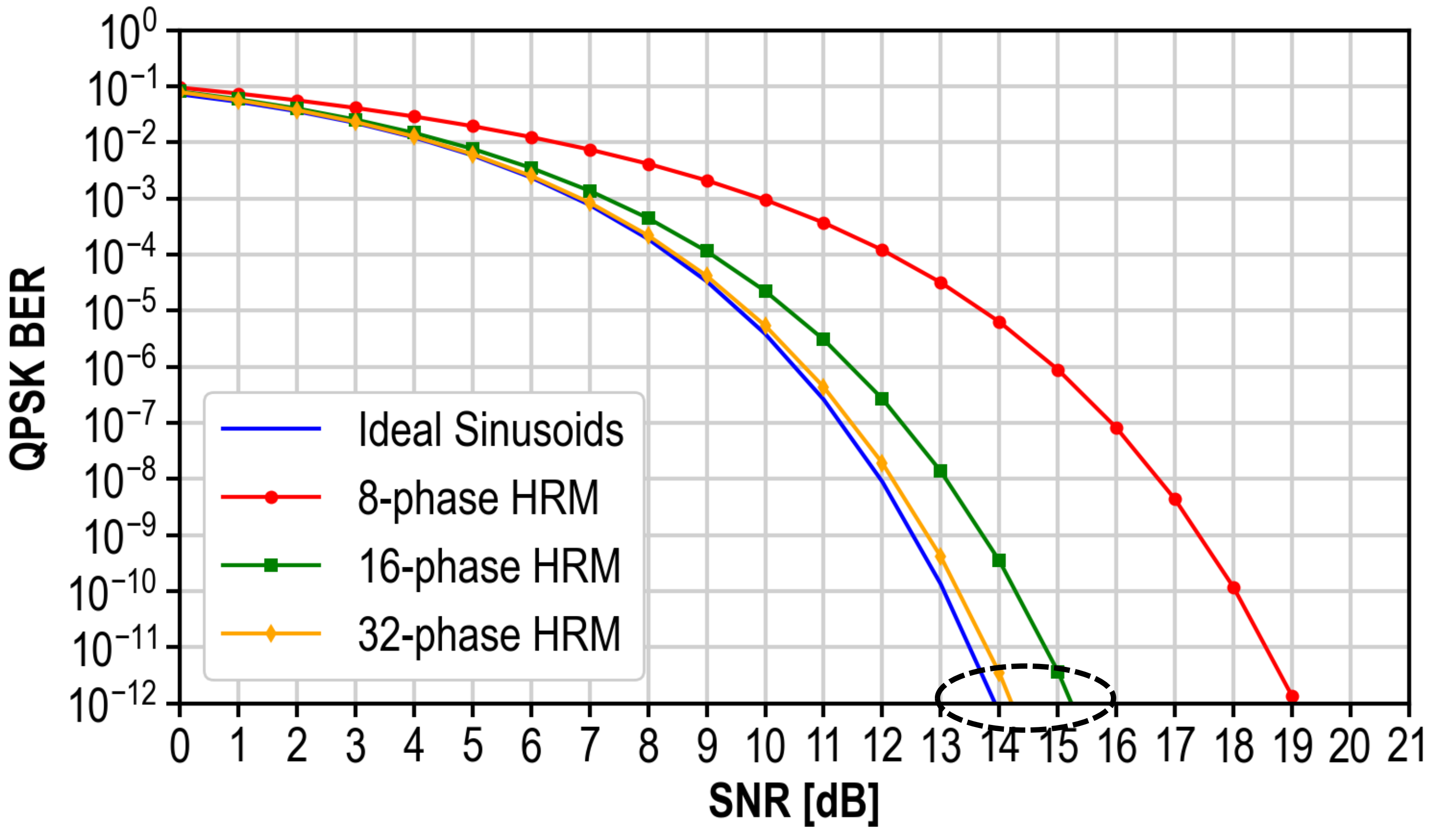
16-Phase Harmonic Rejection Mixer$_{2/4}$



- 16 phases cancel odd harmonics up-to the 15th harmonic
  - Minimizes down-conversion signal aliasing

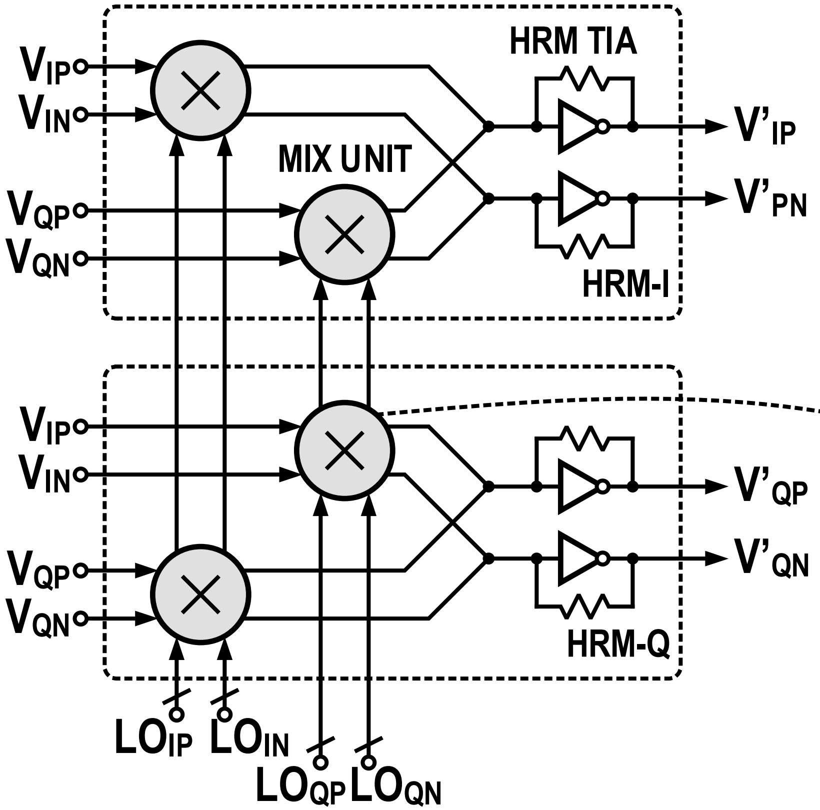
16-Phase Harmonic Rejection Mixer$_{3/4}$

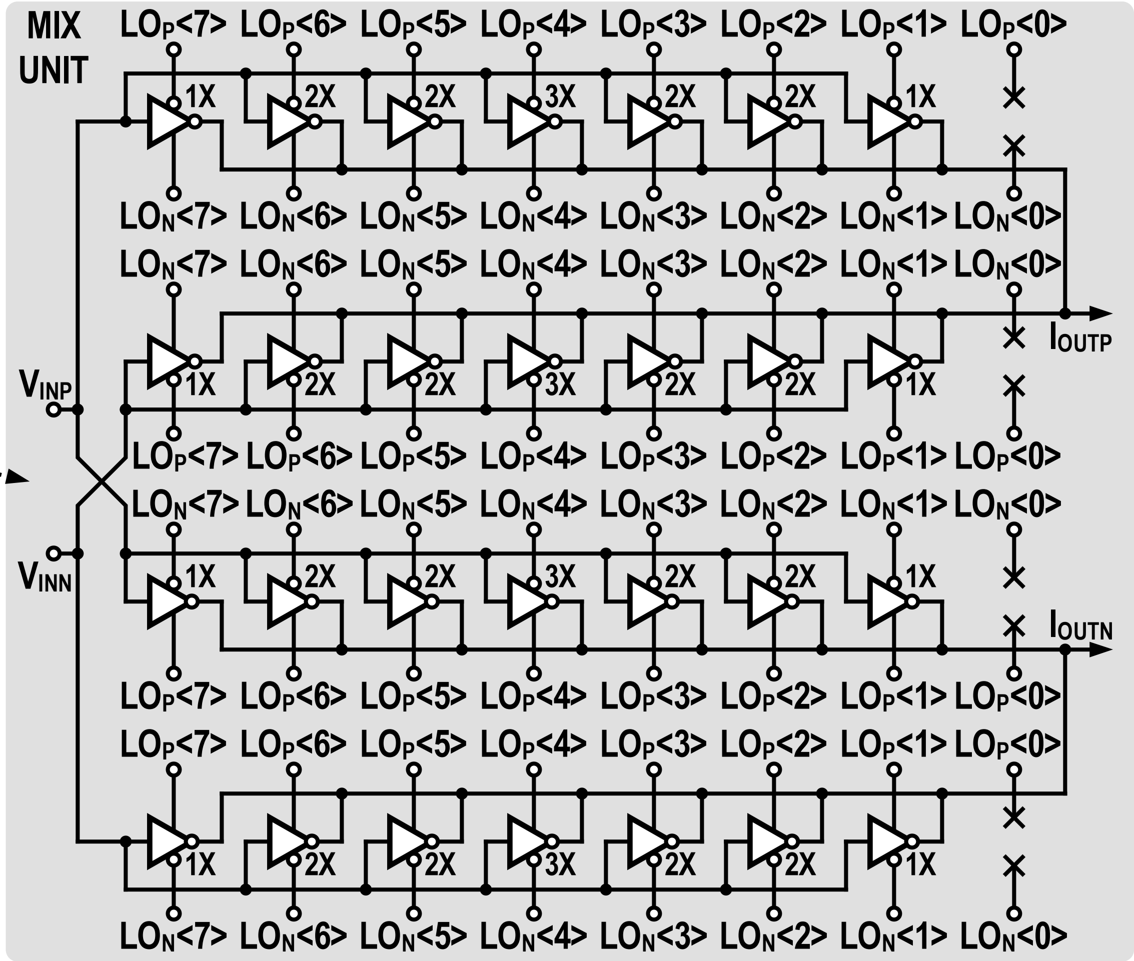




- **16 phases cancel odd harmonics up-to the 15th harmonic**
  - Minimizes down-conversion signal aliasing
  - ~1dB power penalty at 1E-12 BER

16-Phase Harmonic Rejection Mixer$_{4/4}$





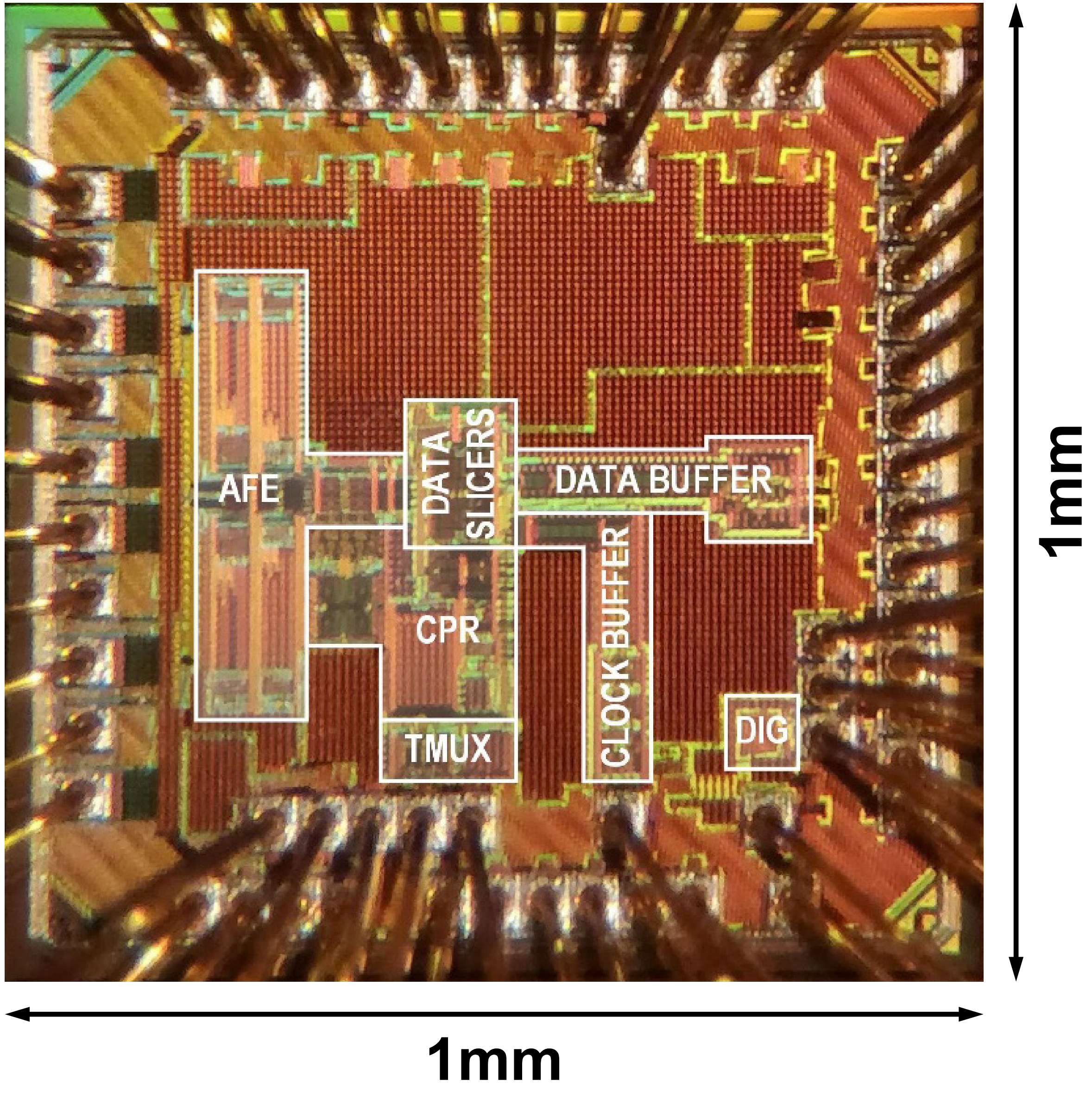
- **Inverter-based mixing units**
  - Better linearity and PVT tolerance
  - Mixing through a weighted sum of unit inverter currents

Outline

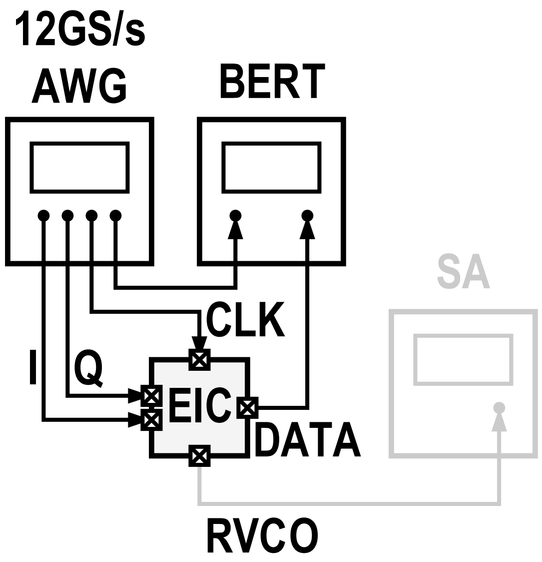
- Motivation
- Proposed Coherent RX
- Implementation Details
- **Measurement Results**
- Summary

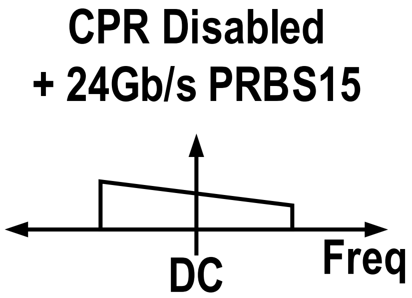
Die Photograph

- 28nm CMOS
- Active Area: 0.22mm^2
- Data rate: 24Gb/s
- Supply: 0.9V
- Power efficiency: 3.2pJ/b



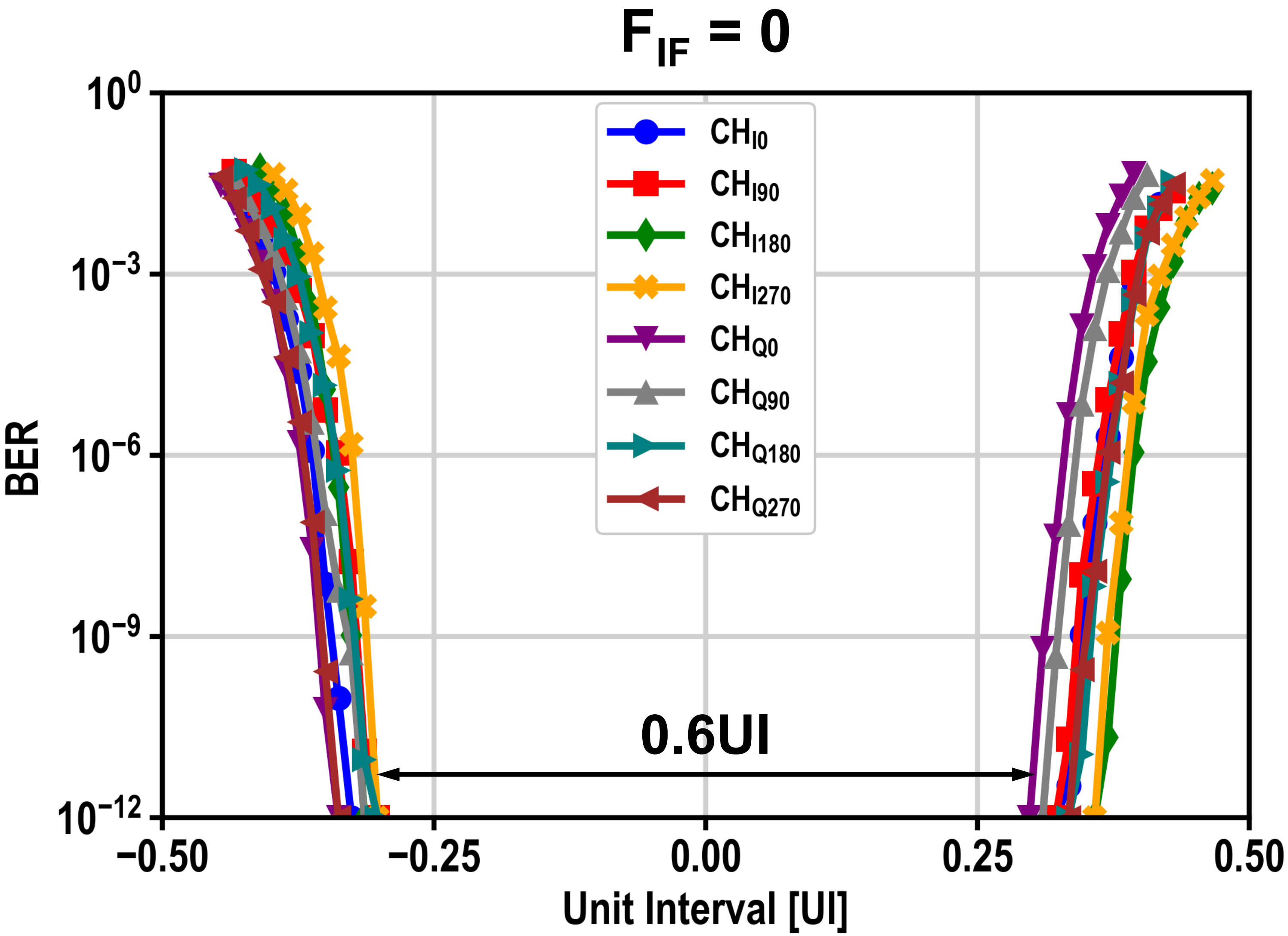
RX Performance$_{1/4}$





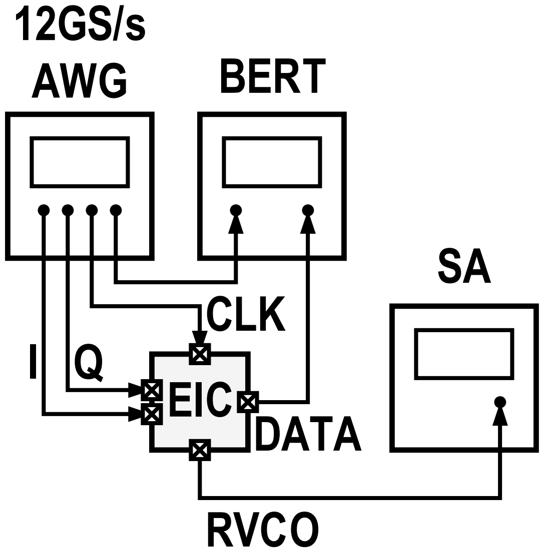
- **Baseband performance [CPR disabled]**
- Passband performance @ F_{IF} = 1.8GHz [w/o data modulation]
- Passband performance @ F_{IF} = 1.8GHz [w/ data modulation]
- CPR tracking performance

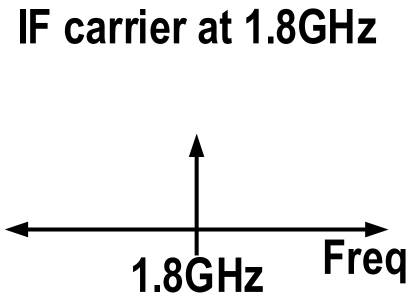
Baseband: BER @ 24Gb/s PRBS15 [CPR Disabled]



Error-free range: 0.6UI → **Baseline**

RX Performance$_{2/4}$

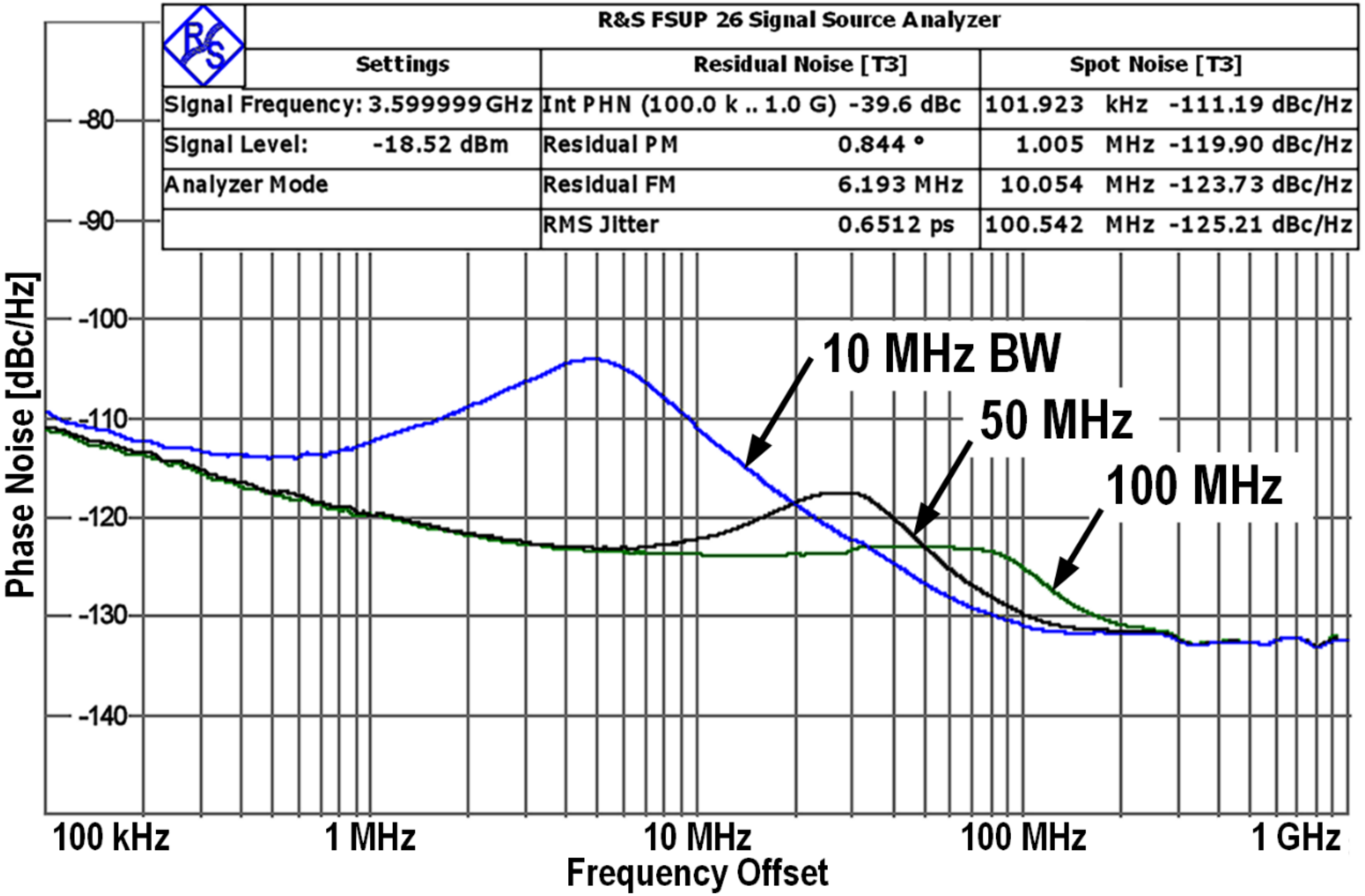




- Baseband performance [CPR disabled]
- **Passband performance @ F_{IF} = 1.8GHz [w/o data modulation]**
- Passband performance @ F_{IF} = 1.8GHz [w/ data modulation]
- CPR tracking performance

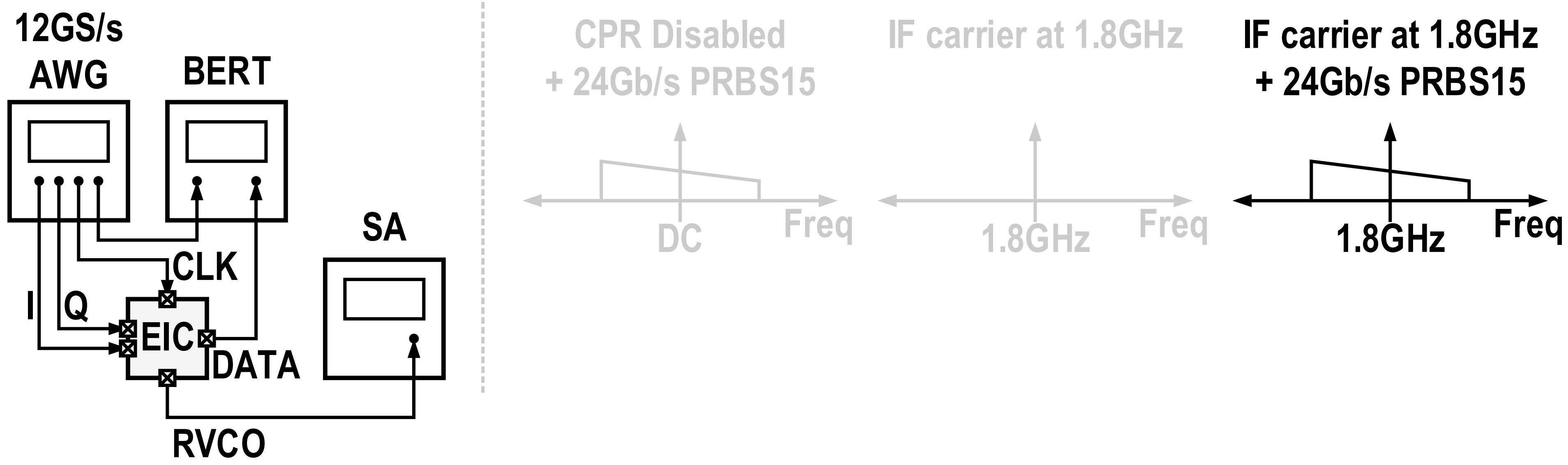
CPR Phase Noise [w/o Data Modulation]

F_{IF} = 1.8GHz



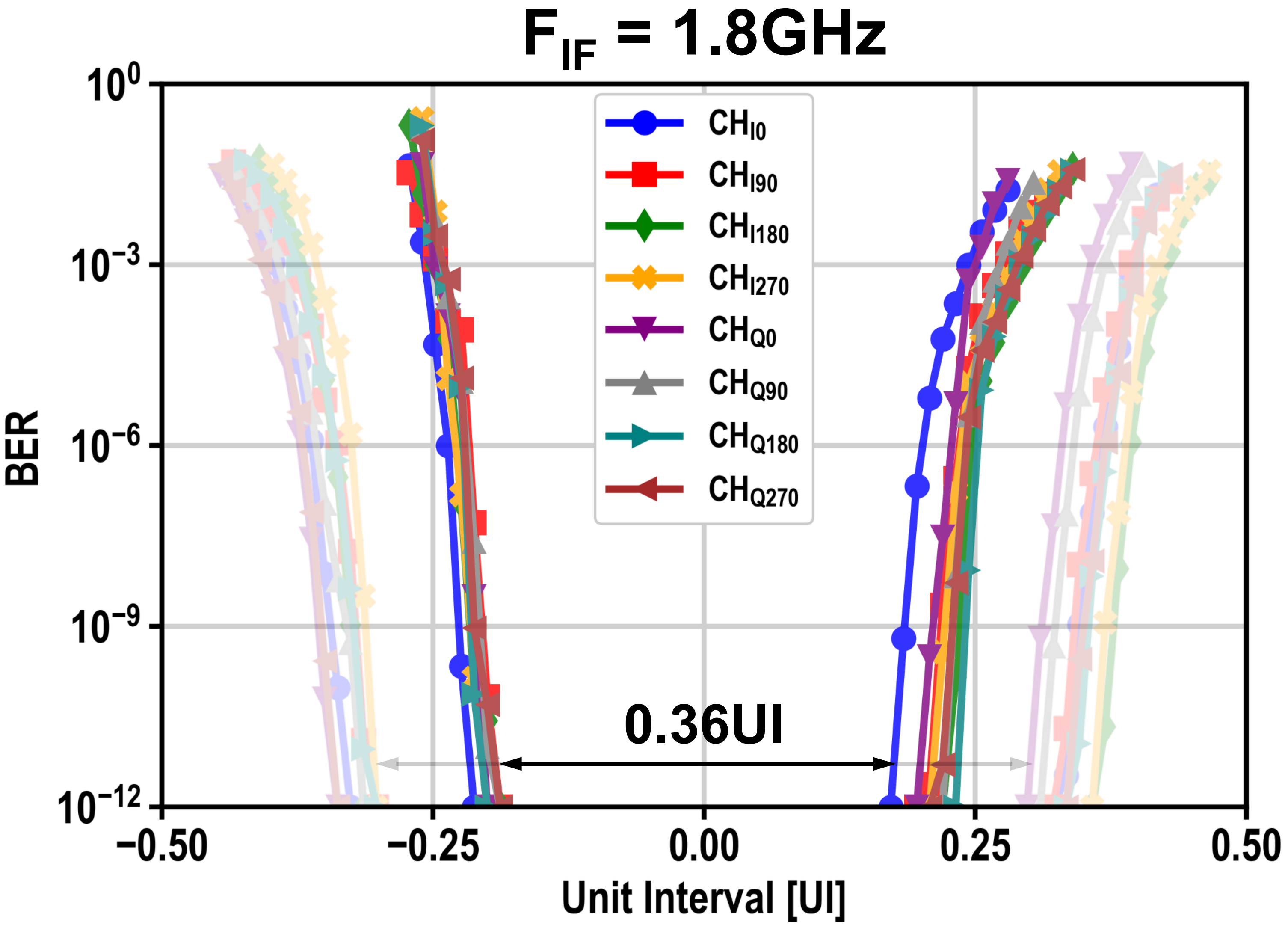
Residual PM: 0.84° → **0.42° after divider**

RX Performance$_{3/4}$



- Baseband performance [CPR disabled]
- Passband performance @ F_{IF} = 1.8GHz [w/o data modulation]
- **Passband performance @ F_{IF} = 1.8GHz [w/ data modulation]**
- CPR tracking performance

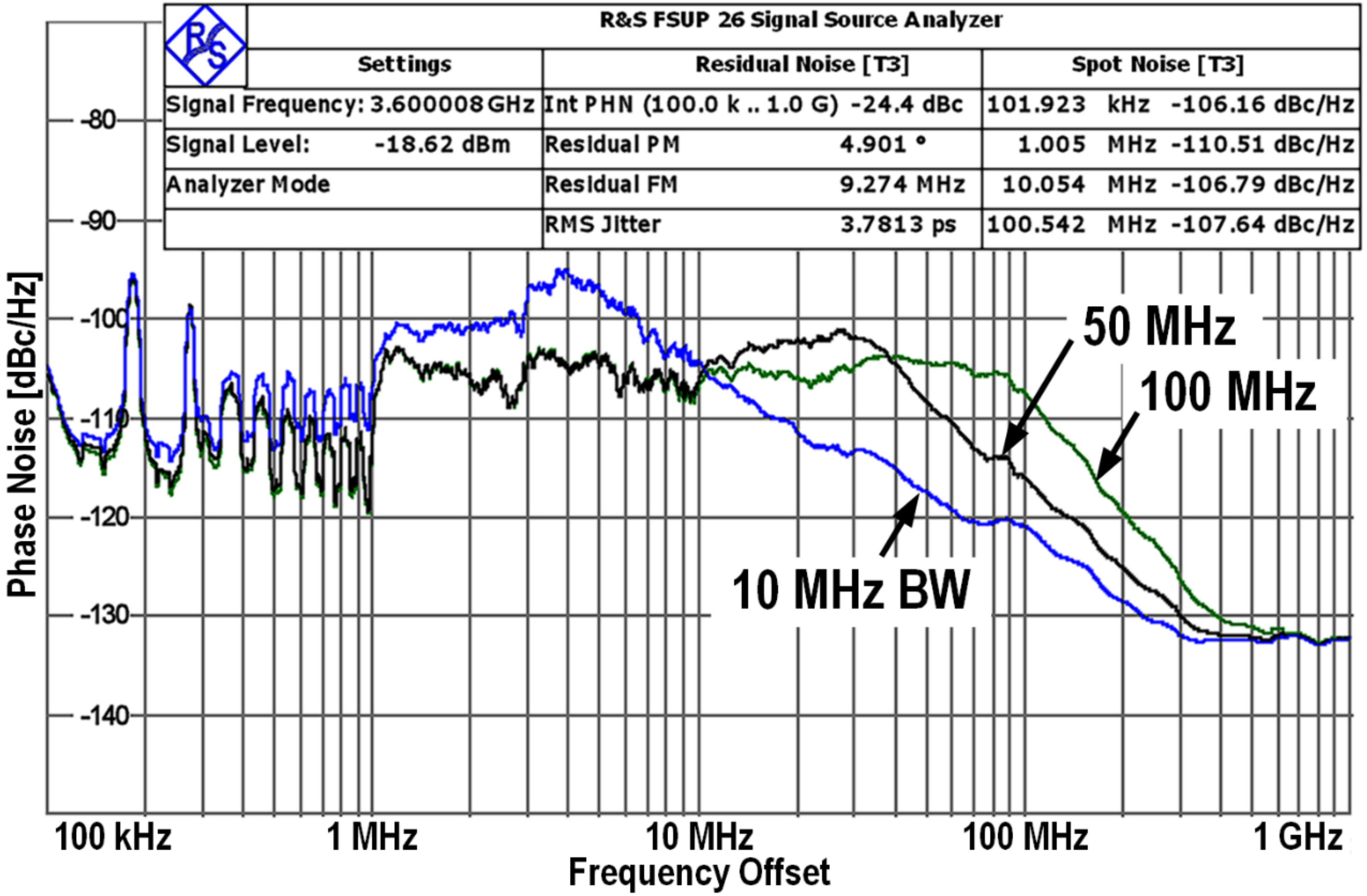
Passband: BER @ 24Gb/s PRBS15 [CPR Enabled]



Error-free range: 0.36UI

CPR Phase Noise [w/ Data Modulation]

F_{IF} = 1.8GHz + 24Gb/s PRBS15

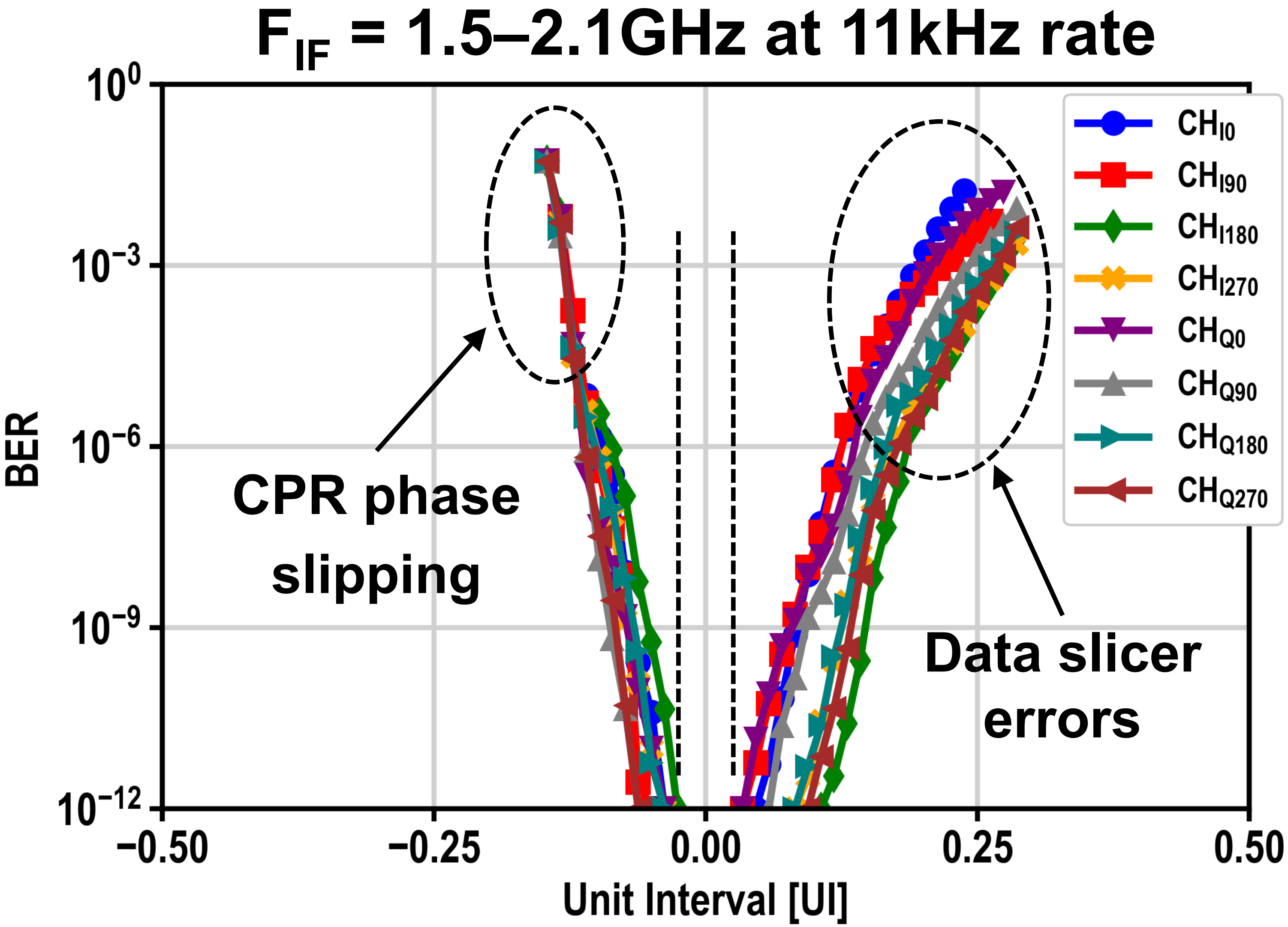


Residual PM: 4.90° → **2.45° after divider**

RX Performance$_{4/4}$

- Baseband performance [CPR disabled]
- Passband performance @ F_{IF} = 1.8GHz [w/o data modulation]
- Passband performance @ F_{IF} = 1.8GHz [w/ data modulation]
- **CPR tracking performance**

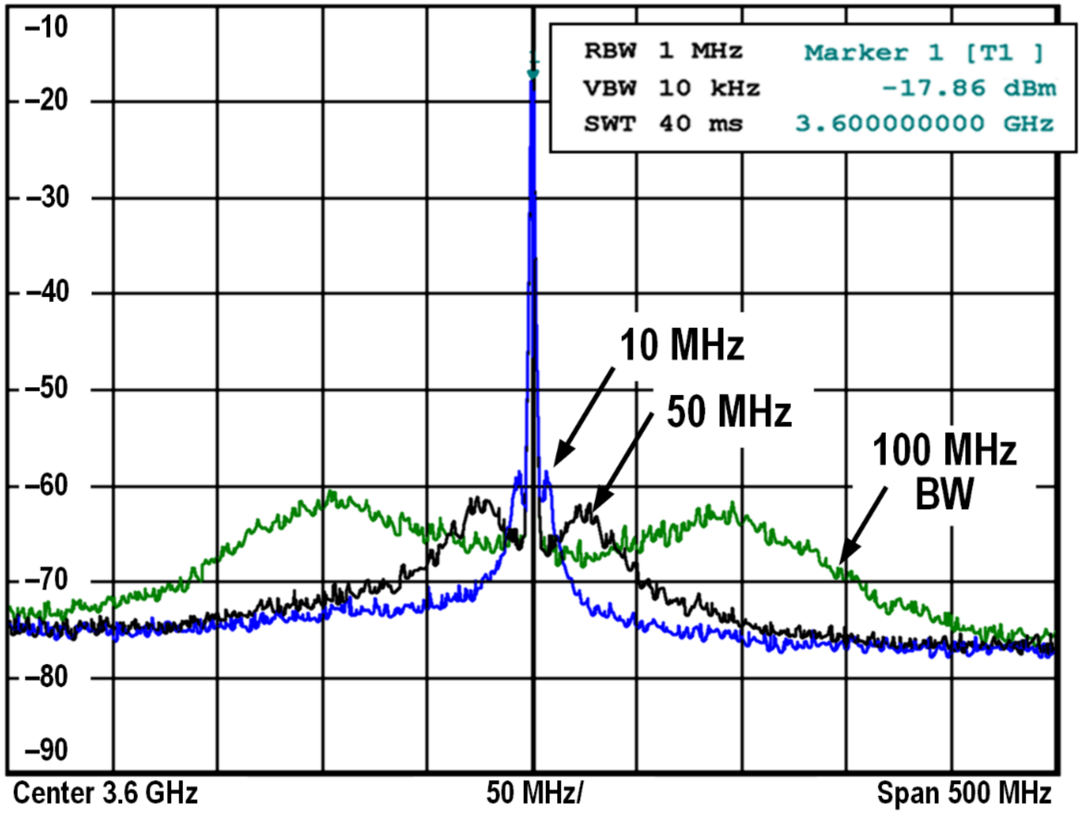
Passband: BER @ 24Gbps with PRBS15 and F_{IF} FM



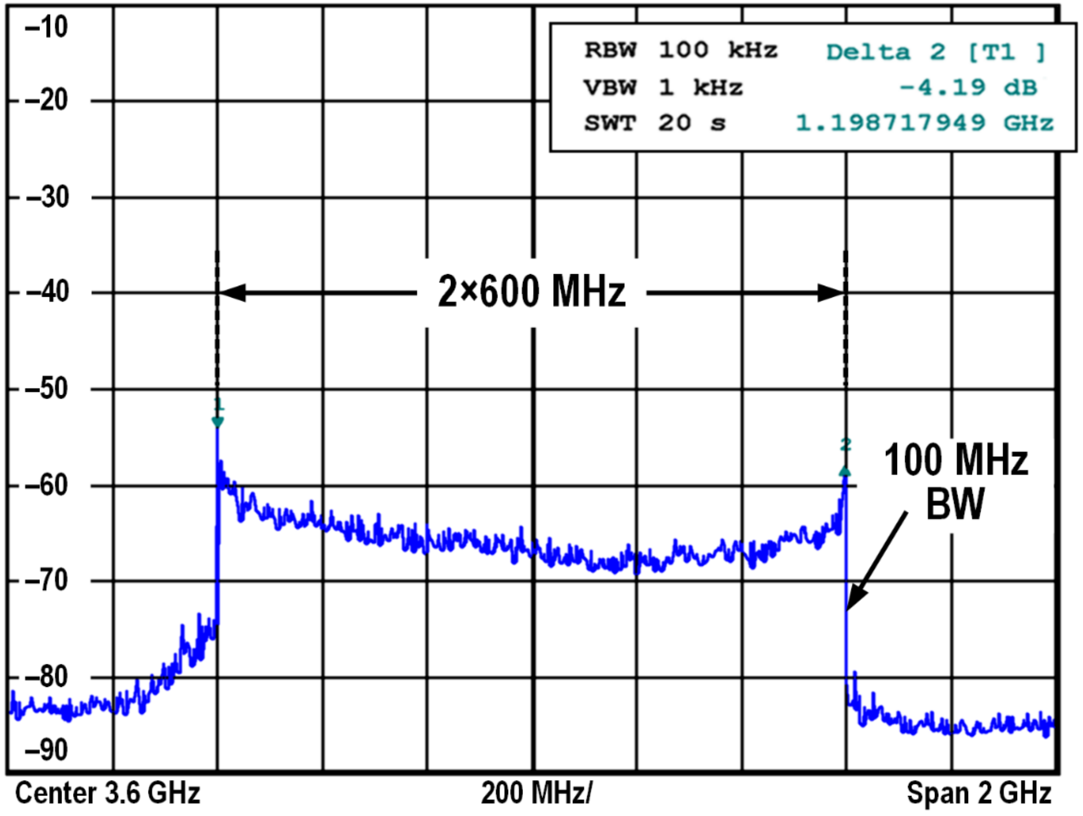
Error-free range: 0.06UI

CPR Spectra: w/o and w/ Frequency Modulation

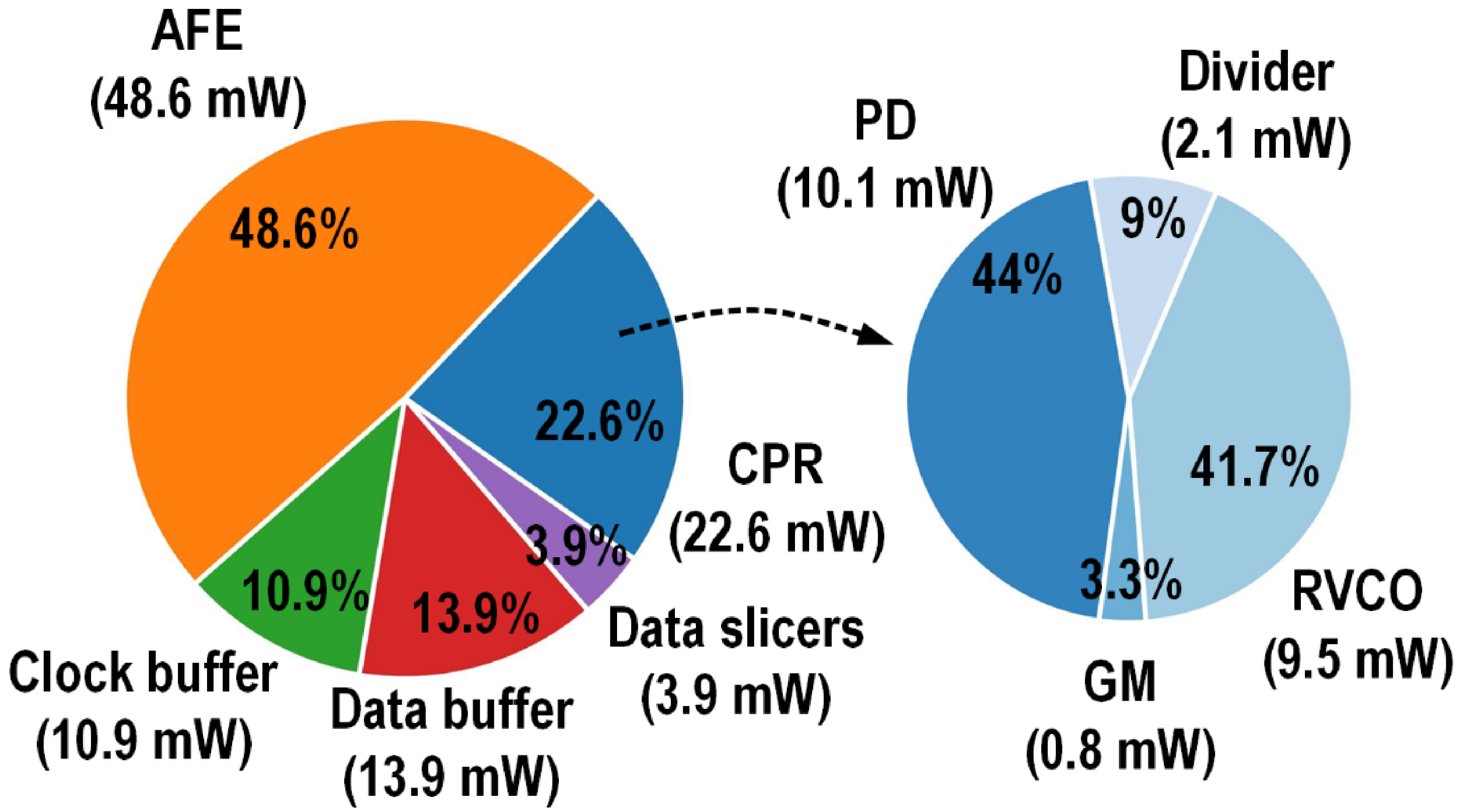
F_{IF} = 1.8GHz



F_{IF} = 1.5–2.1GHz at 11kHz rate



Power Breakdown



CPR: sub-pJ/b

AFE+CPR+Slicers: 3.2pJ/b

Performance Comparison$_{1/2}$

	This work	ISSCC 2022 [1]	OJSSCS 2022 [2]	JLT 2021 [3]	JLT 2013 [4]
Technology	28nm CMOS	28nm CMOS	130nm SiGe HBT	130nm SiGe BiCMOS	500nm HBT
RX architecture	Analog/Intradyne	Analog/Intradyne	Analog/Homodyne	Analog/Homodyne	Analog/Homodyne
Tunable RX laser	Not required	Required	Required	Required	Required
Modulation	QPSK	DP-QPSK	QPSK	DP-QPSK	BPSK
Data rate [Gb/s]	24	200	100	40	40
CPR bandwidth [MHz]	10–100	0.1*	382**	8.3**	1,100
CPR tracking range [MHz]	600	12	—	200	30 GHz***
Power consumption [mW]	76.8	920	534	412	3,000
Energy efficiency [pJ/b]	3.2	4.6	5.34	10.3	75
BER	1.0E-12	1.0E-10	1.0E-12	1.1E-03	1.0E-12
Active area [mm^2]	0.22	0.06	2.8	0.07	—

* Estimated from phase locking plot ** Simulation results *** Tunable laser range

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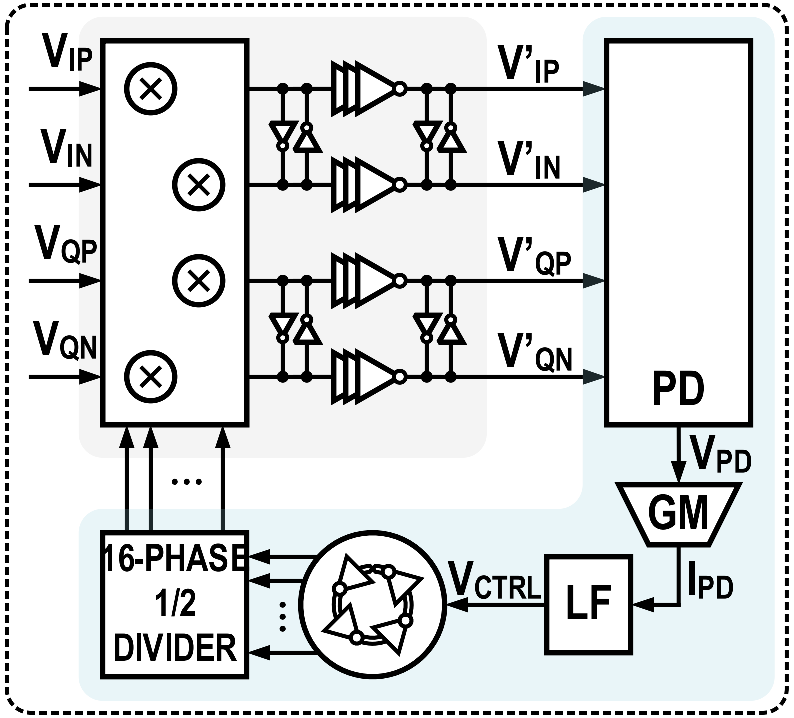
Summary

- **Power-efficient analog coherent RX**
  - **10–100 MHz CPR loop bandwidth**
  - **600MHz CPR tracking range**
  - **Inverter-based HRM and PD**
  - **3.2pJ/b power efficiency at 24Gb/s**



Thank You!