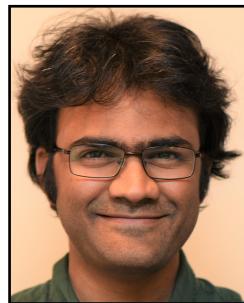


Session 19 Overview:

5G and Satcom: Receivers and Transmitters

WIRELESS SUBCOMMITTEE



Session Chair: Venumadhav Bhagavatula
Samsung Semiconductor, San Jose, CA



Session Co-Chair: Alireza Zolfagari
Broadcom, Irvine, CA

This session includes four papers presenting key advances in the fields of 5G and satellite communication systems. The first two papers describe wide bandwidth, high linearity front-end receiver architectures for 5G systems. In the next two papers, advances in the field of CMOS transceivers for satellite applications are discussed.

3:15 PM

19.1 A 300MHz-BW, 27-to-38dBm In-Band OIP3 sub-7GHz Receiver for 5G Local Area Base Station Applications

Mohammad Ali Montazerolghaem, Delft University of Technology, Delft, The Netherlands

In Paper 19.1, Delft University of Technology presents a 0.4-to-7.3GHz receiver achieving 300MHz RF bandwidth and up to 38dBm in-band OIP3 for base-station application. The proposed receiver utilizes a Rauch TIA with an extra compensation feedback between TIA and RF input to improve the linearity and enhance the receiver bandwidth.



3:45 PM

19.2 An Interferer-Tolerant Harmonic-Resilient Receiver with >+10dBm 3rd-Harmonic Blocker P_{1dB} for 5G NR Applications

Soroush Araei, Massachusetts Institute of Technology, Cambridge, MA

In Paper 19.2, Massachusetts Institute of Technology introduces a passive voltage-mode harmonic-resilient N-path mixer implemented in a receiver operating from 0.25 to 2.5GHz. Fabricated in 45nm SOI, the prototype achieves HB1-dB of greater than 10 and 4dBm at the 3rd and 5th harmonics, respectively.



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4:15 PM

19.3 A 2.95mW/element Ka-band CMOS Phased-Array Receiver Utilizing On-Chip Distributed Radiation Sensors in Low-Earth-Orbit Small Satellite Constellation

Xi Fu, Tokyo Institute of Technology, Tokyo, Japan

In Paper 19.3, Tokyo Institute of Technology and Axelspace present an ultra-low-power Ka-band phased-array receiver utilizing on-chip distributed radiation sensors for small satellite constellations. A distributed current-sharing LNA is introduced to reduce power consumption. On-chip distributed radiation sensors are presented to eliminate the non-uniform radiation influence. The proposed receiver achieves 2.95mW/element power consumption with 0.22dB/Mrad gain compensation performance



4:45 PM

19.4 A Small-Satellite-Mounted 256-Element Ka-Band CMOS Phased-Array Transmitter Achieving 63.8dBm EIRP Under 26.6W Power Consumption Using Single/Dual Circular Polarization Active Coupler

Dongwon You, Tokyo Institute of Technology, Tokyo, Japan

In Paper 19.4, Tokyo Institute of Technology and Axelspace present a small-satellite-mounted single/dual circular polarization 256-element Ka-band phased-array transmitter using 64 4-element ICs. Each front-end uses a reconfigurable coupler to enable efficient generation of single circularly polarized waveforms while also supporting single and dual polarizations.



19.1 A 300MHz-BW, 27-to-38dBm In-Band OIP3 sub-7GHz Receiver for 5G Local Area Base Station Applications

Mohammad Ali Montazerolghaem, Leo C. N. de Vreede, Masoud Babaie

Delft University of Technology, Delft, The Netherlands

Recently, the so-called sub-6GHz band of the 5G new radio (NR) has been extended to 7.125GHz to address the relentless customer demand for higher data-rate communication. This demands a new design approach for the local area base-station (LA-BS) receivers (RXs) to cover a wide operating frequency range of 0.41 to 7.125GHz. Moreover, for NR bands above 3GHz, the maximum RF bandwidth (BW) is as high as 400MHz, in which a -35dBm modulated in-band (IB) blocker can be present. These impose stringent BW and IB linearity requirements for the baseband amplifiers in the LA-BS receivers. In addition to IB interferences, a -15dBm continuous-wave (CW) out-of-band (OOB) close-in blocker can also be present at 60MHz offset frequency from the passband edges, thus demanding a highly selective RX. Finally, the blocker 1dB compression point (B_{1dB}) becomes a key parameter for local area co-location applications in which the power of the far-out OOB blocker can be as large as -4dBm.

Prior art conventionally tried to address those challenges by choosing mixer-first architectures. However, if the TIA's input impedance is used to satisfy the input matching [1], the RX IB linearity will be limited by the signal swing at the TIA's input. Hence, [2] added a series resistor prior to the TIAs to provide the input matching, and improve the IB linearity by making the TIA's input a virtual ground. However, the series resistor degrades the RX noise figure (NF). Therefore, [3] added an auxiliary noise-canceling path to remove the matching resistor noise, at the cost of doubling the number of wideband TIAs and thus RX's power consumption (P_{DC}). Alternatively, as shown in Fig. 19.1.1, an LNTA with a band-stop N-path filter in its feedback can be adopted to improve the NF without sacrificing P_{DC} , and a translational feedback network can be used to provide the input matching [4]. However, the filtering order, IB linearity, and operating frequency of this structure are insufficient for LA-BS stringent requirements. To improve on those limitations, this paper, for the first time, presents a sub-7GHz RX capable of providing the linearity requirements of the local area base-station applications.

It is observed that the RX operating frequency is limited at the LNTA output by its output resistance (R_o) and total parasitic capacitance (C_{par}) of the node. Since a larger R_o is required to operate in the current mode and reduce the TIAs' noise contribution to NF, C_{par} must be minimized. In prior art, two sets of switches are used for signal downconversion and N-path filtering. Interestingly, the N-path filter switches connected to the LNTA's output can be removed, and the right plates of the notch filter capacitors can be connected to the outputs of the corresponding phase of the downconverter switches, as shown in Fig. 19.1.1-top. Consequently, C_{par} is reduced, extending the operating frequency to above 7GHz.

The baseband filter has three main tasks. First, it should offer a high-order lowpass transfer function to attenuate close-in blockers sufficiently. Second, its input impedance must be low enough to minimize the voltage swing at the LNTA output and TIA input to improve RX IB and OOB linearity. Third, its loop gain should be large enough to suppress the TIA nonlinear terms.

Figure 19.1.2 shows the schematics of the conventional single-pole TIA (SP-TIA) and Rauch filter adopted in the proposed RX. In both structures, R_F determines the transimpedance gain, and C_{IN} should be large enough to ensure that the major part of the OOB blocker current goes to ground. Otherwise, the last stage of the amplifier should sink/source that current and stay linear, thus demanding high P_{DC} . Even considering the same C_{IN} and R_F values for a fair comparison, the Rauch filter offers several benefits over the conventional single-pole TIA. First, it inherently exhibits second-order filtering, thus improving OOB linearity. Second, as shown in Fig. 19.1.2, the transfer function and maximum input impedance (Z_{IN}) of the Rauch filter are mainly determined by the passive components with a negligible effect from the OpAmp's unity-gain BW (ω_u). This is a great feature, especially for highly linear and large BW receivers, in which maintaining the OpAmp DC gain (A_0) and simultaneously increasing ω_u lead to high P_{DC} and stability issues. On the contrary, the SP-TIA in-band impedance is inversely proportional to the OpAmp open-loop gain (A), and consequently, an extremely large Z_{IN} peaking is inevitable even when $\omega_u=100\times\omega_{3-dB}$, where ω_{3-dB} is the desired 3dB BW. Third, the Rauch TIA offers a larger loop gain at the passband edge and transition band due to the presence of two complex-conjugate zeros at $1/\sqrt{(R_F R_1 C_F C_{IN})}$, as shown in Fig. 19.1.2. By properly choosing R_1 , zeros can become smaller than ω_{3-dB} , and consequently compensate for TIA gain drop, improving IB and OOB linearity at the passband edge and transition band, respectively. Note that there is a tradeoff in choosing the R_1 value, as a larger R_1 increases the loop gain but, at the same time, leads to a higher Z_{IN} peak.

Figure 19.1.3 depicts the complete block diagram of the proposed RX. To improve the filtering order of the TIA, a third-order highpass filter, comprising two series capacitors

(C_H) and one shunt inductor (L_H), is placed in parallel with R_F . Ground ports of the inductors driven by complementary LOs are then connected to halve the number of baseband inductors. Each resulting inductor is then realized using a gyrator with a load capacitor (see Fig. 19.1.3 bottom right). Note that the gyrators' noise has a negligible contribution to the RX NF as it faces a highpass filter when traveling to the TIA output. Finally, a three-stage OpAmp is used as the TIA amplifier to ensure high loop gain for satisfying the IB linearity requirements of LA-BS applications. Miller and feed-forward compensation techniques are also used to stabilize the OpAmp and achieve enough phase margin. The first- and third-stage determine the OpAmp P_{DC} , as the former should satisfy the noise requirement, and the latter needs to stay linear while sinking/sourcing an IB blocker current.

To achieve a flat response within the channel BW, a second branch comprising a series capacitor (C_2) and a baseband amplifier with a gain of $-A_c$ is added in parallel with the main capacitor (C_1), as shown in Fig. 19.1.1-bottom. Here, the equivalent capacitance at the RX input is $C_{eq}=(C_1+C_2)-G_M Z_{IN}(A_c C_2 - C_1)$, where G_M is the LNTA transconductance. Due to its bandpass characteristic, Z_{IN} reaches its maximum just below the passband edge. Hence, C_{eq} reduces at those frequencies, thus enhancing the BW and flattening the IB response. Outside the BW, Z_{IN} reduces over frequency, thus increasing C_{eq} and filtering roll-off. Note that both the noise and linearity requirements of the added amplifiers are relaxed since their input is connected to an almost virtual ground and their noise experiences a notch filter when appearing at the RX output.

The proposed RX is fabricated in 40nm CMOS technology and occupies an active area of 0.4mm² (Fig. 19.1.7). Figure 19.1.4 shows small- and large-signal measurement results. The S_{11} is <-10dB across the RX operating frequency of 0.4 to 7.3GHz. The RX gain (NF) is 38dB (3.2dB) at 1GHz LO frequency (f_{LO}) and reaches 35.7dB (5.8dB) at $f_{LO}=7GHz$. As shown in Fig. 19.1.4, the measured BW is disrupted by the TIA's impedance peaking when A_c is OFF. Turning ON the A_c and adjusting C_2 recovers the BW and the filtering order of the RX. Moreover, enabling the active inductors in Rauch TIAs improves the filtering order by 10dB/dec. The measured IB linearity is +38dBm at low IB frequencies, and reduces to +27dBm near ω_{3-dB} . The OOB linearity performance is also depicted in Fig. 19.1.4, in which the IIP2, IIP3, and B_{1dB} are respectively +67.7dBm, +11dBm, and -4.8 dBm at $\Delta f/\omega_{3-dB}=3$, where Δf is a frequency offset from f_{LO} . The RX NF is only degraded by 5.5dB when facing a 0dBm CW blocker at $\Delta f/\omega_{3-dB}=5$ (see Fig. 19.1.4).

Figure 19.1.5 shows the EVM measurement results in different scenarios. Based on the 3GPP standard, the RX throughput must be >95% for reference sensitivity, in-band, close-in, and far-out blocking tests. In the reference sensitivity test, a 96% throughput is achieved when a 50MS/s -87.7dBm QPSK signal is applied to the RX. Then, the desired signal power is increased by 6dB for the blocking tests. Thanks to the RX high IB linearity, all symbols are appropriately received in the presence of a -35dBm 20MS/s modulated IB blocker. In the close-in blocking test, when facing a -15dBm CW close-in blocker at 60MHz offset from the BW edge, all desired symbols are received correctly due to the high-order filtering of the RX. Then, based on the co-location requirements, a -4dBm CW far-out blocker is applied to the RX, and a 100% throughput is achieved. Thus, the proposed RX satisfies all of the 3GPP requirements with enough margin. Finally, as depicted in Fig. 19.1.5-bottom, the RX performance is also tested with higher order modulation schemes, and the measured EVM for a -55dBm 100MS/s 64-QAM (256-QAM) signal is -31dB (-30.2dB).

Compared with prior art with a similar operating frequency range and BW [3-5] in Fig. 19.1.6, this work demonstrates higher IB linearity and sharper filtering roll-off. Moreover, it was tested and passed all the 3GPP requirements, thus making it a proven architecture for the LA-BS applications.

Acknowledgement:

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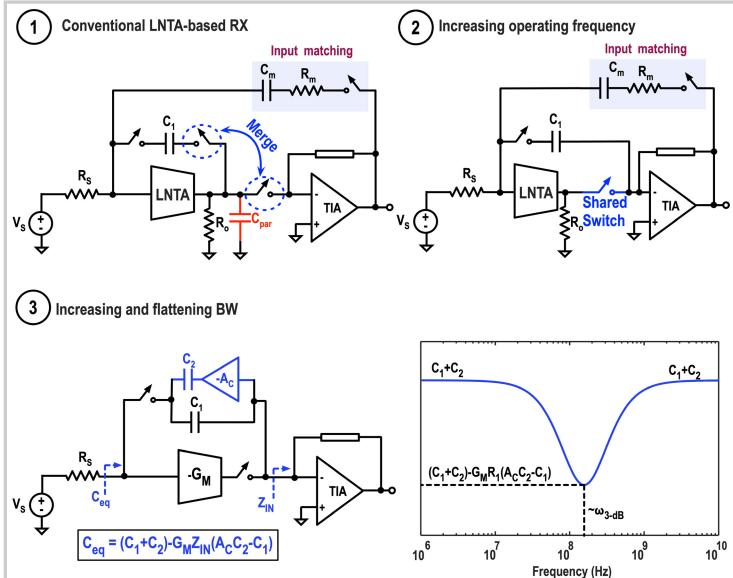


Figure 19.1.1: Proposed techniques for improving the receiver's operating frequency, bandwidth, and in-band flatness.

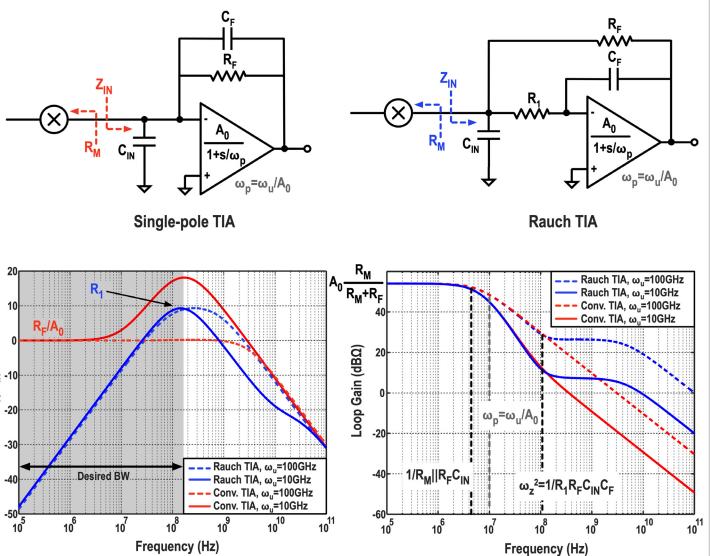


Figure 19.1.2: Comparison between the schematic, input impedance, and loop gain of the single-pole and Rauch transimpedance amplifiers adopted in the proposed RX.

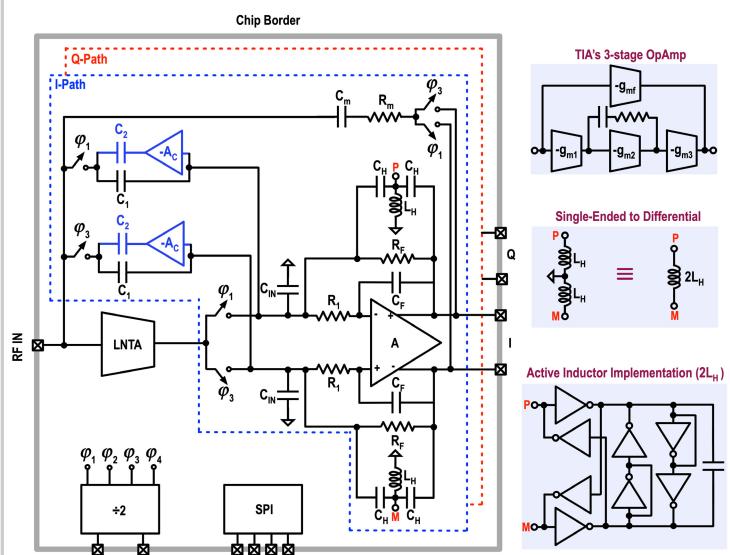
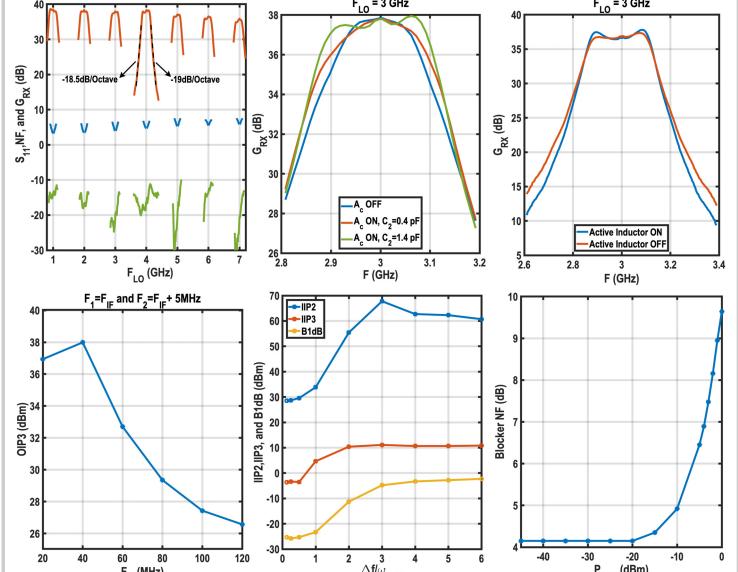


Figure 19.1.3: Block diagram of the proposed receiver.



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Figure 19.1.4: Small- and large-signal measurement results.

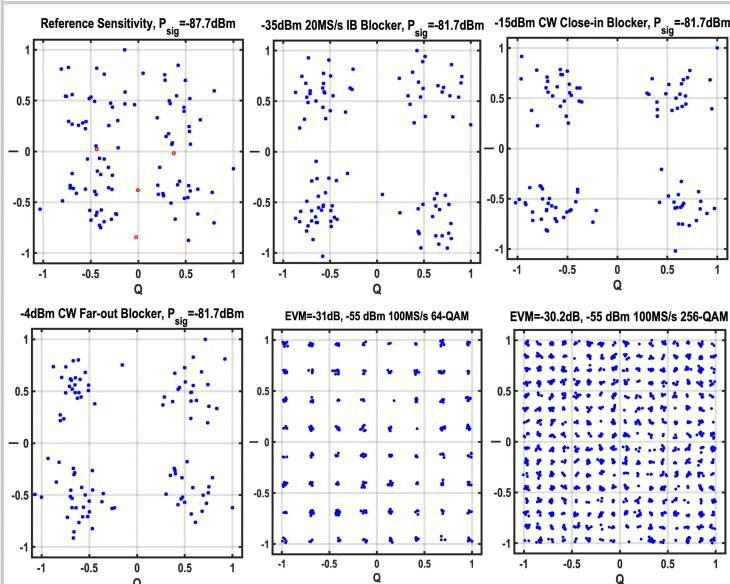


Figure 19.1.5: Measured constellation diagram and EVM in different scenarios.

Lien JSSC 2018 [1]	Bhat JSSC 2022 [3]	Montazerolghaem ISSCC 2021 [5]	Razavi JSSC 2022[4]	This Work
Architecture	Mixer first	Mixer first	LNTA based	LNTA based
Technology	45 nm SOI	22 nm SOI	40 nm	28 nm
f _{RF} (GHz)	0.2 - 8	1 - 6	0.4 - 3.2	0.4 - 6
Gain (dB)	21	22.4	36	54
Flat BW	Yes	No	Yes	No
Single Ended Input	No	No	Yes	Yes
BW (MHz)	20	350	160	0.2 - 160
NF (dB)	2.3 - 7	2.5 - 5	2.7 - 3.6	2.1/4.4 ²⁸
0dBm Blocker NF (dB)	4.7	N/A	8.4	5.2/7.4 ⁸
Filtering roll-off (dB/oct)	-40	-20	-55	-60
IB OIP3 (dBm)	21	28.5-34.4	17	19 ⁸
OOB IIP ₃ (dBm)	39	18	10	3 ⁸
Δf/ω _{3-dB} = 8	Δf/ω _{3-dB} = 5.7	Δf/ω _{3-dB} = 3	Δf/ω _{3-dB} = 12.5	Δf/ω _{3-dB} = 3
OOB IIP ₂ (dBm)	88	N/A	50	20 ⁸
Δf/ω _{3-dB} = 8	Δf/ω _{3-dB} = 3	Δf/ω _{3-dB} = 3	Δf/ω _{3-dB} = 12.5	Δf/ω _{3-dB} = 3
B1dB(dBm)	12	3	-5	-4.8
Δf/ω _{3-dB} = 4	Δf/ω _{3-dB} = 5.7	Δf/ω _{3-dB} = 5	N/A	Δf/ω _{3-dB} = 3
EVM (dB)	N/A	N/A	-26.4 ⁸	-25.3 ⁸
Supply (V)	1.2	0.83	1.3/1.2	1
Active Area (mm ²)	0.8	0.48	0.6	1.9
Power (mW)	50mW+ 30mW/GHz	172	58.5+ 17.6mW/GHz	23 - 49
				100+ 13mW/GHz

[†]Low noise mode, [‡] Harmonic reject mode, [§] Maximum bandwidth, [¶] -57dBm 80MS/s 64-QAM, [¤] -60dBm 140MS/s 64-QAM, ^{¤¤} -55dBm 100MS/s 64-QAM.

Figure 19.1.6: Performance comparison with state-of-the-art receivers operating over a wide frequency range.

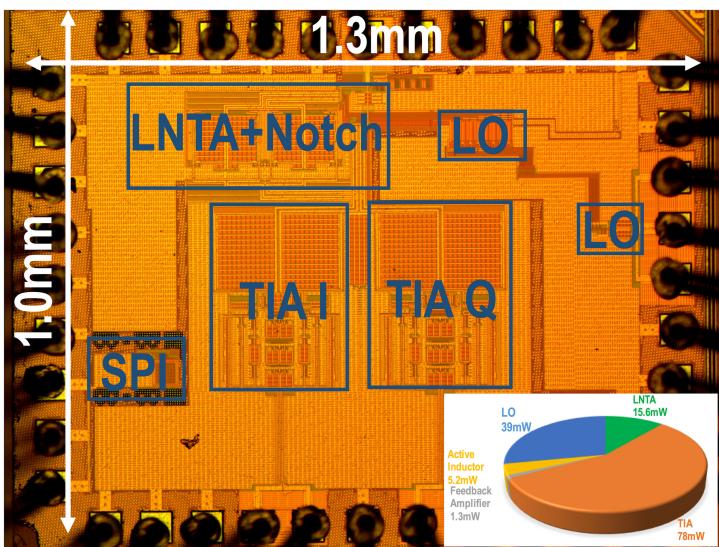


Figure 19.1.7: Die micrograph and power consumption breakdown at 3GHz LO frequency.

19.2 An Interferer-Tolerant Harmonic-Resilient Receiver with >+10dBm 3rd-Harmonic Blocker P_{1dB} for 5G NR Applications

Soroush Araei, Shahabeddin Mohin, Negar Reiskarimian

Massachusetts Institute of Technology, Cambridge, MA

The sub-6GHz spectrum is heavily utilized by 5G New Radio (NR), as well as traditional cellular and WiFi technologies. A major challenge in designing SAW-less wideband radio receivers (especially targeting the sub-2GHz range) is rejecting interferers at or around the operation frequency and its harmonics that are within the congested sub-6GHz spectrum. Given the stringent linearity requirements of 5G systems, the harmonic rejection should happen early in the receiver (RX) chain to avoid desensitizing the receiver and achieve a high harmonic blocker 1dB compression point (HB_{1dB}).

Traditional harmonic-rejecting (HR) receivers employ weighted harmonic recombination at baseband (BB) to achieve harmonic rejection only at the receiver output and hence do not protect the RF front-end from large harmonic blockers [1]. The noise-canceling mixer-first RX with HR-TIAs in [2] is susceptible to downconverted harmonics at the TIA input. Furthermore, the weighted LNA combined with N-path filtering implemented in [3] is ineffective in attenuating harmonics and out-of-band blockers at the LNA input. More recent approaches have shown harmonic rejection by using parallel active harmonic traps [4], or a harmonic-selective negative feedback loop [5] aiming to protect the input of the RX. However, the active nature of the technique discussed in [4] makes it suitable only for small-signal blockers, while the feedback loop in [5] increases the complexity of the design, its power consumption and noise and reduces its operating frequency range.

In this work, we present a low-loss fully passive HR mixer structure that can be incorporated seamlessly into any passive-mixer-based voltage-mode receiver to enhance its resilience to harmonic blockers, and an interferer-tolerant harmonic-resilient mixer-first RX demonstrating HB_{1dB} of >+10dBm/>+4dBm at the 3rd/5th harmonics. The low-loss fully passive HR N-path mixer is inspired by the concept of “block digital filtering” [6] (Figure 19.2.1) and rejects all LO harmonics up to the N-1th harmonic. Translating this FIR filtering technique to the analog domain within the N-path structure is not straightforward, since it requires ideal sensing and summation of voltages stored on the BB capacitors across multiple paths without creating undesired interactions. However, two techniques, namely charge sharing and capacitor stacking, can be employed to create FIR filter taps and perform necessary summations within each path.

Figures 19.2.1 and 19.2.2 show the evolution of the low-loss fully passive HR mixer and its operation in the time-domain. For the sake of simplicity, the operation of a single-ended 8-path unit rejecting odd harmonics (3rd and 5th) is discussed. The fully differential circuit is shown in Figure 19.2.3. As shown in Figure 19.2.1, in a conventional 8-path mixer driven by 12.5% non-overlapping clocks, the signals at f_{LO} and 3f_{LO}/5f_{LO} are downconverted to BB resulting in harmonic responses. One method of implementing FIR filtering to reject harmonics within the 8-path mixer is to split the BB capacitor with a 1: $\sqrt{2}$:1 ratio, charging them with consecutive clock phases and performing charge-sharing with an additional set of switches. Even though this approach is capable of creating an effective LO with no 3rd/5th-harmonic content, it involves multiple charge-sharing occurrences and substantial losses are to be expected for in-band signals for a high-Q filter profile, prohibiting its use in a mixer-first RX. Stacking pre-charged capacitors is another way to incorporate an FIR filter in a switch-capacitor circuit. Since charge sharing is no longer an issue, stacking can lead to passive gain. However, the FIR filter formed in such a way is independent of capacitor ratios. In order to achieve high HR ratios, the irrational ratio 1: $\sqrt{2}$ has to be precisely implemented. In the absence of the capacitor ratio as a tuning knob, however, a higher level of HR requires a greater number of stacked stages. Clearly, this complex circuit is highly susceptible to parasitics at intermediate nodes, which suggests passive mixers cannot achieve high levels of harmonic rejection by means of capacitor stacking alone.

To achieve a practical low-loss harmonic-tolerant fully passive mixer, both of the abovementioned techniques must be applied simultaneously (Figure 19.2.1 bottom right). As shown in Figure 19.2.2, similar to the conventional circuit, C_a, C_b, and C_c are sequentially connected to the input source during LO_{m-1}, LO_m, and LO_{m+1} respectively. When LO_{m+2} goes high, the two stacked C_a capacitors are placed in parallel to C_b, forming a charge-sharing loop. Stacking is responsible for generating the first and third taps with a magnitude of “1”, and with a proper C_a/C_b ratio, charge sharing realizes the second tap of the filter with a “ $\sqrt{2}$ ” weight. With this arrangement, the trade-off between high-Q filtering at the RF node and in-band signal loss is significantly reduced compared to the charge-sharing-only approach, which allows high levels of harmonic rejection to be achieved with only a slight reduction in gain.

Figure 19.2.3 shows the block diagram of the interferer-tolerant harmonic-resilient mixer-first RX implemented in a 45nm SOI CMOS technology with an active area of 0.65mm² (Figure 19.2.7). The differential low-loss fully passive HR mixer employs capacitors within its two branches that are scaled with 17/12 ratio for proper harmonic recombination through capacitor stacking and charge sharing. The switches of the mixer are driven by 8-phase 12.5% non-overlapping clocks. Bandwidth tuning at RF is performed by placing C_{BB} at the BB LNA input. The BB LNAs use an inverter-based design with added PMOS devices to achieve common-mode feedback [7] and are designed for 20dB gain. The sizes of the inverter devices are optimized to improve IB IIP3. The feedback resistor provides input matching. A second stage of harmonic recombination at BB further improves the harmonic rejection ratio. The BB G_m cells used for the second-stage harmonic recombination are based on a differential design with local feedback and resistor degeneration to improve linearity. Similar to other mixer-first structures, this work achieves a high-Q 2nd-order filtering profile at the antenna interface that attenuates out-of-band blockers and improves OOB IIP3. Moreover, the proposed circuit provides +10dB/+15dB 3rd- and 5th-harmonic rejection (HR3/HR5) at the RX input, which improves linearity with respect to blockers around the harmonics. Additional harmonic rejection at the output of the mixer ensures linear operation of the BB LNA even in the presence of large harmonic blockers.

Figure 19.2.4 shows the measured performance of the interferer-tolerant HR RX. The measured RF-to-BB conversion gain and S₁₁ are respectively >35dB and <-16dB across the operation frequency of 0.25 to 2.5GHz. The conversion gain and NF vs BB frequency for a clock frequency of 500MHz and a BB BW of 15MHz are shown. The NF varies between 3.5 and 5.5dB across the tuning range measured under optimal HR3/HR5. An in-band IIP3 of -8dBm and a maximum out-of-band IIP3 of +28dBm are achieved. The normalized harmonic rejection profile of the RX is shown in Figure 19.2.5. A harmonic-rejection-ratio (HRR) of >52dB has been achieved for all harmonics below the 7th harmonic measured across 5 chips. B_{1dB} at close-in frequencies is -15dBm and increases up to +8dBm at large blocker offsets measured at 1GHz clock frequency. The HB_{1dB} for the 3rd harmonic is >+10dBm regardless of the offset frequency. The HB_{1dB} for the 5th harmonic is between +4 and +7dBm and is limited in our current setup by the frequency range of the input balun. The 0dBm OOB blocker NF (BNF) is 7.8dB at f_{LO}=1GHz for Δf/BW=12. The harmonic BNF is <9dB for a blocker up to 3.5dBm at 3f_{LO}.

Figure 19.2.6 summarizes the measured performance. Compared to prior HR receivers [1-5], this work achieves the highest HB_{1dB} with a minor noise penalty for harmonic blockers up to -5dBm. Furthermore, the implemented low-loss fully passive HR mixer requires no additional circuitry beyond extra switches and benefits from technology scaling. Compared to other recent LNTA-based blocker-tolerant receivers [8,9], this work has superior linearity. More importantly unlike this work, such LNTA-based approaches would be heavily impacted by large-signal harmonic blockers.

Acknowledgement:

The authors would like to thank MIT MTL faculty for equipment assistance.

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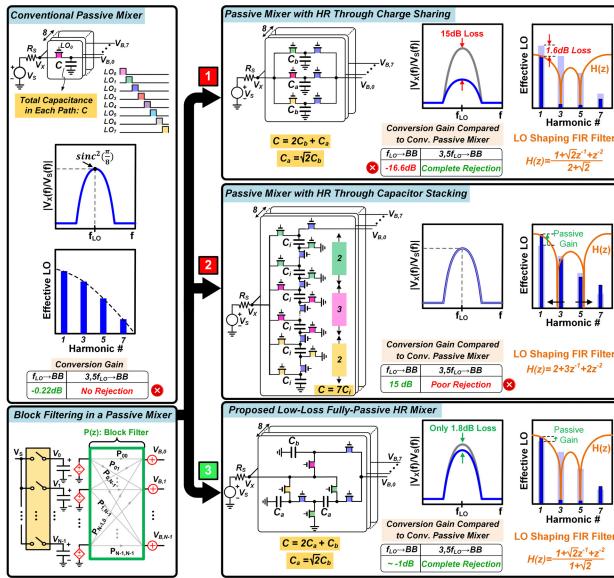


Figure 19.2.1: The evolution of the proposed single-ended low-loss fully passive HR mixer based on charge sharing and capacitor stacking.

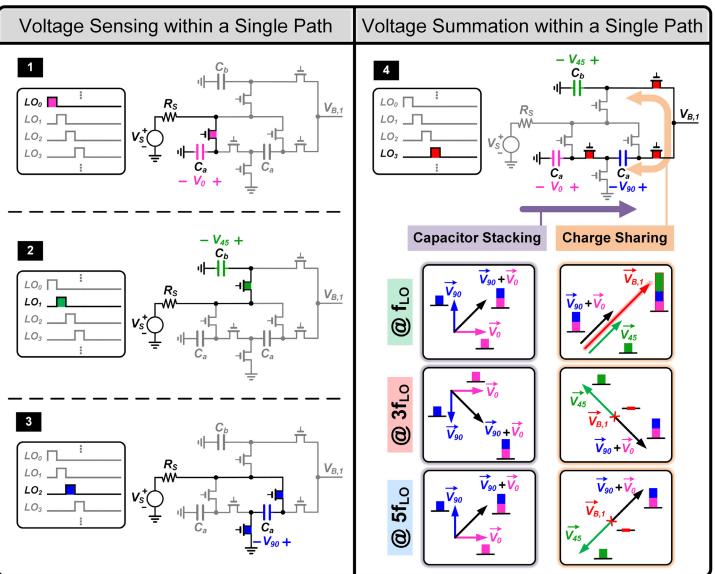


Figure 19.2.2: Time-domain operation of the proposed single-ended low-loss fully passive HR mixer.

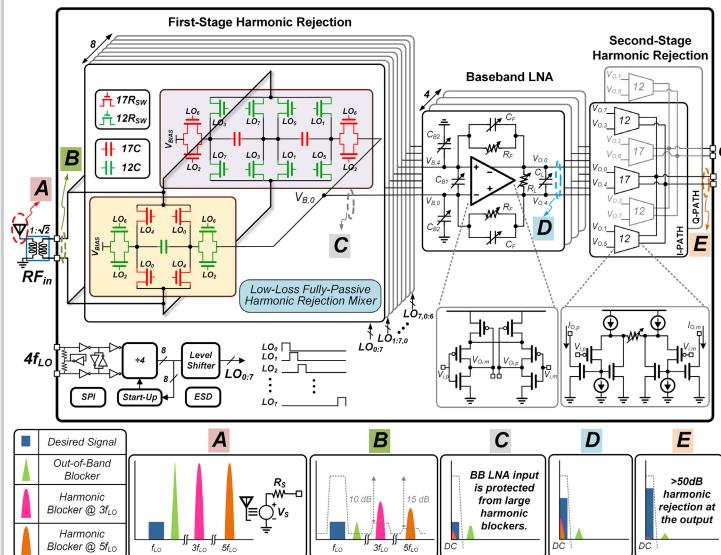


Figure 19.2.3: The block diagram of the proposed 0.25-to-2.5GHz interferer-tolerant harmonic-resilient mixer-first RX.

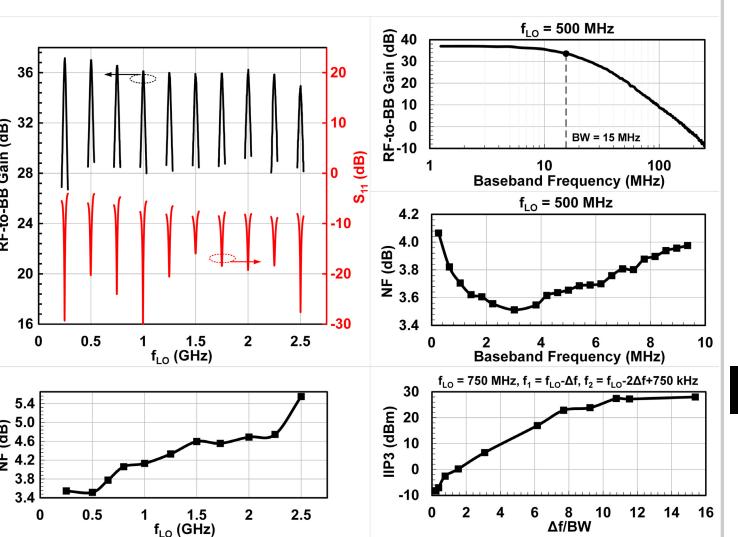


Figure 19.2.4: Measured RF-to-BB gain, S_{11} and NF across operation frequency and BB frequency, and IIP3 vs carrier offset frequency.

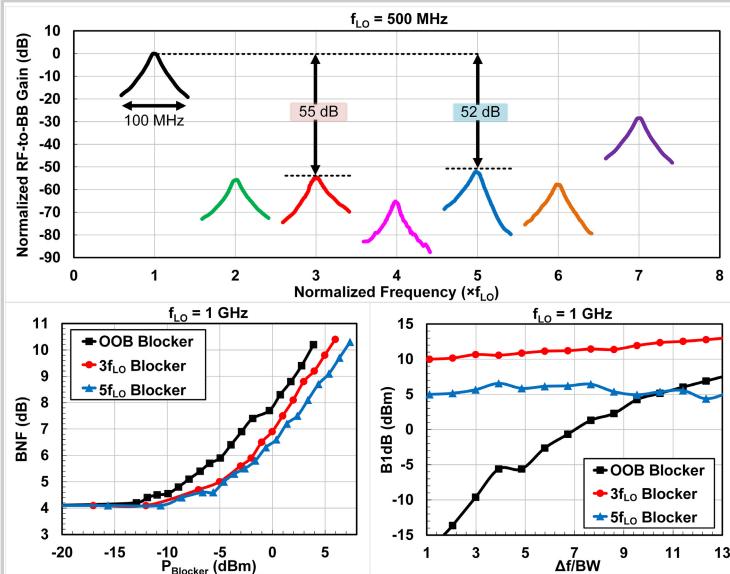


Figure 19.2.5: Measured harmonic rejection profiles (x-axis is not drawn to scale), BNF and harmonic BNF vs blocker power and B_{1dB} and HB_{1dB} vs carrier offset.

	Montazerolgham, ISSCC 2021 [8]	Wang, ISSCC 2019 [9]	Xu, JSSC 2018 [3]	Murphy, ISSCC 2014 [2]	Rayudu, RFIC 2022 [5]	Razavi, JSSC 2022 [4]	This Work
CMOS Technology	40nm	45nm SOI	65nm	28nm	65nm	28nm	45nm SOI
RF Input	Single-Ended	Single-Ended	Differential	Differential	Differential	Single-Ended	Differential
Frequency Range [GHz]	0.4-3.2	0.2-2	0.2-1	0.1-3.3	0.1-0.5	0.4-6	0.25-2.5
RX Gain [dB]	36	40	36	NR	33	54	35
BB BW MHz	80	10	2	0.2-3	10	0.1-80	6-15
NF [dB]	2.7-3.6	2.1-2.5	5.4-6	1.7	6.9	3.7-4.2 ^a	3.5-5.5
0dBm OOB BNF [dBm]	8.4 ($\Delta f/BW=6.25$)	6.7 ($\Delta f/BW=8$)	NR	5 ($\Delta f=80MHz$)	NR	7.4 ^b	7.8 ($\Delta f/BW=12$) ^c
OOB B _{1dB} [dBm]	-6 ($\Delta f/BW=5$) ^d	-5 ($\Delta f/BW=8$) ^d	NR	-2.4 ($\Delta f/BW=10$)	-2.0 @ $V_{DD}=1.8V$	-2.5 ($\Delta f/BW=40$)	-5.5 ($\Delta f/BW=5$) ^e +7 ($\Delta f/BW=13$) ^f
OOB IP3 [dBm]	+13 ($\Delta f/BW=5$)	+14 ($\Delta f/BW=6$)	+9 ($\Delta f/BW=10$)	+11.5	NR ^g	+9.4 ($\Delta f/BW=50$) ^h +27 ($\Delta f/BW=11$) ⁱ	+13 ($\Delta f/BW=5$) ^j
Power Consumption [mW]	65.5-114.8	68-95	62.70 ^k	36.8-62.4	110-121	23-49	32.4-54
Supply Voltage [V]	1.3/1.2	1.2	1.2/2.5	1	1.1/1.3	1	1/1.2
Active Area [mm ²]	0.6	1.05 ± 2 off-chip RF chokes	400nH off-chip inductor	5.2	2.55	1.9	0.65
Total 3f _{LO} /5f _{LO} HRR [dB]	NR	NR	>51/52	60/60	44/46	60.5/62.3	>55/52
Harmonic B _{1dB} [dBm]	NR	NR	-2.8 (3f _{LO}) ^j -3 (5f _{LO}) ^j	-6.5 (3f _{LO}) ^j 6.9 (5f _{LO}) ^j	NR	5 @ -5dBm (3f _{LO}) ^j 9 @ -5dBm (3f _{LO}) ^j 4.8 @ -5dBm (5f _{LO}) ^j 9 @ 5dBm (5f _{LO}) ^j	>10 (3f _{LO}) ^j >4 (5f _{LO}) ^j
Harmonic BNF [dB]	NR	NR	NR	9 @ -5dBm (3f _{LO}) ^j	NR	NR	NR

^aLow due to being a noise cancelling RX. ^bReported with harmonic-traps turned on up to 2GHz. ^cEstimated from plots. ^dCalculated from the reported current and V_{DD} numbers.

^eOOB IP3 is only reported around 3f_{LO} and 5f_{LO}. No data reported for interferences near f_{LO}, f_{LO}+500MHz, f_{LO}+1GHz, f_{LO}=750MHz. B_{1dB} without the HR feedback loop is -4dBm (0dBm) for 3f_{LO} (5f_{LO}) blockers which indicates that NF was sacrificed for linearity.

Figure 19.2.6: Comparison with the state-of-the-art HR- and interferer-tolerant receivers.

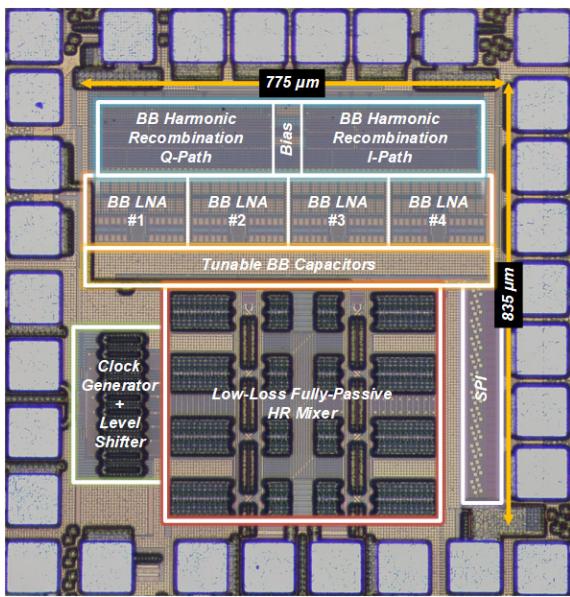


Figure 19.2.7: Die micrograph.

19.3 A 2.95mW/element Ka-band CMOS Phased-Array Receiver Utilizing On-Chip Distributed Radiation Sensors in Low-Earth-Orbit Small Satellite Constellation

Xi Fu¹, Dongwon You¹, Xiaolin Wang¹, Michihiro Ide¹, Yuncheng Zhang¹, Jun Sakamaki¹, Ashibir Aviat Fadila¹, Zheng Li¹, Yun Wang¹, Jumpei Sudo², Makoto Higaki², Soichiro Inoue², Takashi Eishima², Takashi Tomura¹, Jian Pang¹, Hiroyuki Sakai¹, Kenichi Okada¹, Atsushi Shirane¹

¹Tokyo Institute of Technology, Tokyo, Japan

²Axelspace, Tokyo, Japan

Small satellite technology has the potential to further extend the current satellite constellation in low-earth orbit (LEO) by realizing a wider coverage and more robust networks all over the world. Compared with conventional satellites, small satellites can drastically reduce launch costs and increase the number of satellites in LEO. However, small satellites face the more severe issues in terms of power consumption and radiation tolerance due to the limited size of solar panels and more than ten times thinner radiation shield than conventional sizeable satellites. In addition, since the small satellites cannot have the large-size antenna installed on the main body, a deployable membrane is attached to the main body for the large phased-array antenna. In that case, the radiation degradation by total ionizing dose (TID) becomes non-uniform due to the shadowing by the main body. The non-uniform gain dropping in the phased-array causes a degradation of beam-pattern performance. Figure 19.3.1 shows an estimated result for the conventional design regarding the non-uniform gain degradation, resulting in 3.1dB main-lobe degradation for one year. Thus, a phased-array receiver with on-chip distributed TID sensors is proposed in this work to solve the non-uniform gain degradation. Compared with the conventional received-signal-strength-indicator-based gain detector, the proposed on-chip distributed TID sensors detect the gain variations between chips and the gain variations inside the chip with radiation hardness features. Thus, the influence on the beampattern can be mitigated by the compensation feedback and distributed TID sensors.

Figure 19.3.2 shows the system block diagram of the proposed low-power circularly polarized beamforming receiver with on-chip TID sensors. A single path consists of a three-stage distributed current-sharing LNA, a reflective type phase-shifter (RTPS), two low-loss single-port-double-throw RF switches, and a two-stage voltage-steering current-sharing variable-gain amplifier (VGA). A common path comprises a 4:1 lumped Wilkinson combiner, a two-stage low-power buffer, a two-stage current-sharing VGA, and an RTPS. H and V signal paths are separately and symmetrically implemented in this work for supporting linear polarization, dual-linear polarization, and circular polarization modes. Two 4:1 lumped Wilkinson combiners combine received signals from each element in a single-ended configuration. Hence, the influence of impedance variation caused by the phase tuning can be mitigated by the high port-to-port isolations. After that, a two-stage RF buffer is inserted to minimize the signal-chain insertion loss. Figure 19.3.2 also highlights the proposed on-chip distributed TID sensors for non-uniform TID detection. The TID detection voltage values are multiplied with the pre-designed slope control ratio (~1.66 for all blocks) and then multiplied with the look-up-table biases. Then, the bias values are used for setting all relative key amplifier blocks by implementing the distributed compensation techniques. The full receiver is capable of resisting the non-uniform radiation influence. Thanks to the proposed on-chip distributed TID sensor-based compensation technique and the distributed current-sharing common-gate (CG) LNA, the proposed receiver realizes less than 10% of the typical gain variations caused by the non-uniform TID with low power consumption.

Figure 19.3.3 illustrates the circuit schematic of the proposed distributed current-sharing CG LNA and the proposed voltage-steering current-sharing VGA. Compared with the conventional current-sharing CG LNA, the proposed distributed current-sharing LNA eliminates the existence of one stage current I_3 , and thus the required power consumption is reduced. Simultaneously, the noise figures NF_{tot} stays the same owing to the same g_m and R_{equ} values of the first stage. The non-linearities have a negligible effect on the receiver performance because the satellite receiver operates at small received signal levels. The proposed voltage-steering current-sharing VGA is also introduced to reduce the receiver power consumption further. The variable resistor steers the controlling voltage V_{GS2} and midterm supply voltage V_{MID} ; thus, VGA gain is changed. Compared with the conventional current-steering VGA with pseudo transistor pair, the proposed voltage-steering current-sharing VGA is configured to utilize both upper and lower transistors for gain contributions to save power consumption. The power consumption is reduced from 15.6mW to 2.65mW with the compatible gain tuning range, minimum RMS phase error, and IIP3.

Figure 19.3.4 shows the measured results of the proposed single-element, single-path, and distributed TID sensors. The single-element output power and IM3 are measured using stand-alone TEG with an on-wafer probe station, and the signal-to-noise-and-

distortion ratio (SNDR) is calculated with 400MHz signal bandwidth. At 29GHz, the peak SNDR is 42dB. The measured single-element S11, S21, and noise figure at 29GHz are -20dB, 8.1dB (with two RF switches), and 3.6dB, respectively. The measured 3dB bandwidth is within 25.9GHz to 30.1GHz, which covers the 27.5GHz to 30GHz frequency band for the satellite communication uplink. Figure 19.3.4 also indicates the measured single-path phase-shifting coverage and RMS errors at 29GHz. The phase-shifter is capable of covering 360° when sweeping switched registers. The single-path RMS gain and phase errors are 0.08dB and 0.19°, without any gain and phase calibration. Regarding the VGA gain-tuning range, the measured result is 12.5dB, and the single-path RMS phase error for all gain tuning steps is only 0.65° at 29GHz. As shown in Fig. 19.3.4, the locations of phased-array elements and distributed TID sensors are represented by black dots. The measured non-uniform TID values show that the proposed distributed TID sensors can detect the realistic non-uniform TID distribution. Compared to the measured gain-pattern result without the compensation technique, the results with compensation show that the maximum gain variation caused by the non-uniform TID is dramatically reduced to 0.12dB for 0.5Mrad average TID.

In this work, the full array module PCB has 64 chips on the front with 16×16 H+V linear-polarized, dual linear-polarized, and circularly polarized patch antennas on the back. Each chip has 4H and 4V RF signal input ports, which are connected to the 16×16 array module. As shown in Fig. 19.3.5, the H and V azimuth-plane beam patterns are measured with an 8×8 sub-array module, which covers both beam angles from -50° to 50° with less than -10dBc sidelobe level. Figure 19.3.5 shows the measured linear, dual linear, and circularly polarization EVMs in 1-m OTA configuration with DVB-S2X APSK modulated signals. The OTA EVMs are measured using 256APSK with 1GHz and 1.5GHz symbol rates. The proposed low-power phased-array receiver realized 256APSK EVMs of -31.15dB, -31.25dB, and -32.37dB with linear, dual linear, and circular polarization modes, respectively. The peak OTA EVM at 29GHz is -32.37dB with 1GHz 256APSK modulated signal for right-hand circular polarization mode. The highest OTA data-rate of 24Gb/s is achieved with a 1.5GHz dual linear polarization 256APSK modulation signal.

Figure 19.3.6 compares this work with the state-of-the-art phased-array ICs. This work achieves 0.22dB/Mrad main lobe degradation by utilizing the on-chip distributed TID sensor-based compensation technique. Simultaneously, the work realizes the lowest PS RMS gain and VGA RMS phase errors without any gain or phase calibration. The lowest power consumption per element is realized using the distributed current-sharing LNA and low-loss RF switches.

The phased-array receiver is fabricated in a standard 65nm CMOS process with a WLCSP. Figure 19.3.7 shows the die micrograph. The total chip area, including bumps, is 11mm², whereas the single-element active area without D-VGA is 0.24mm².

Acknowledgement:

This work is partially supported by NICT(00601 and 00801), MIC/SCOPE (#192203002 and #192103003), JSPS (JP20H00236), MIC (JPJ000254), JST A-STEP (JPMJTR211D), STAR, and VDEC in collaboration with Cadence Design Systems, Inc., Mentor Graphics, Inc., and Keysight Technologies Japan, Ltd.

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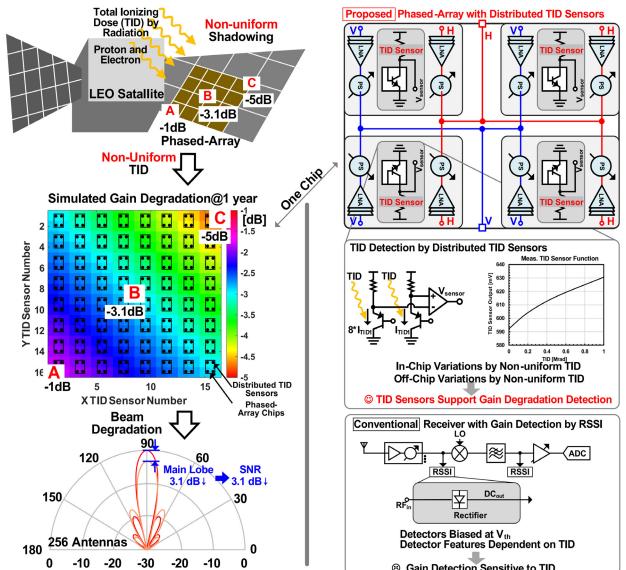


Figure 19.3.1: Non-uniform TID considerations and on-chip distributed TID sensors for LEO small satellite constellation.

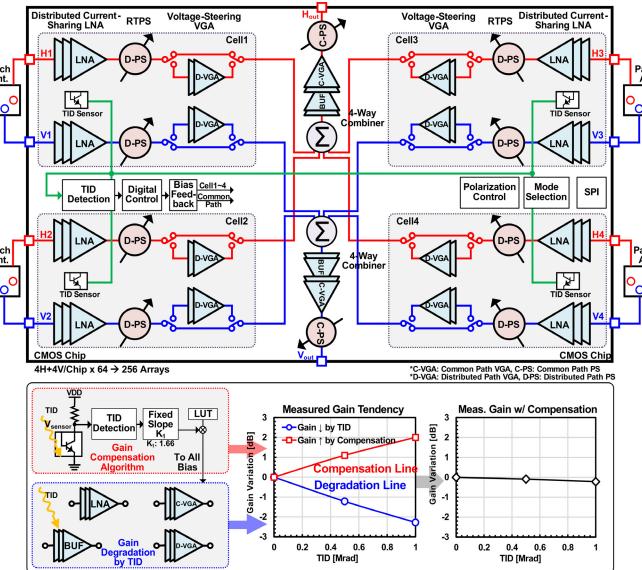


Figure 19.3.2: Block diagram of the proposed phased-array receiver with on-chip distributed-TID-sensors-based gain compensation technique.

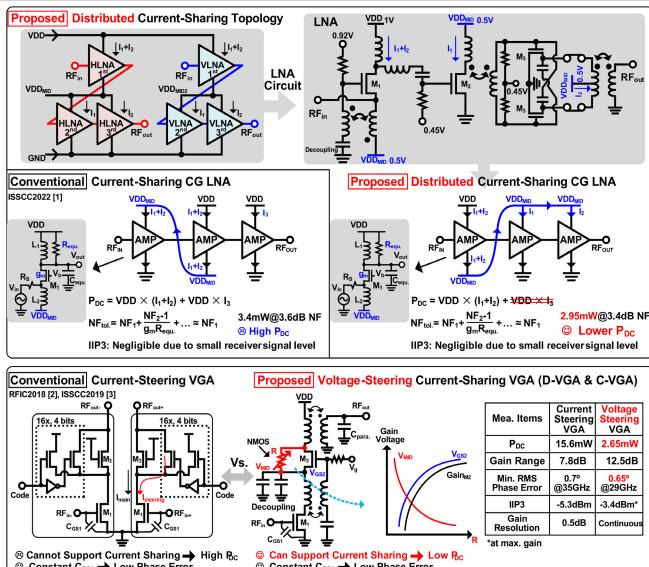


Figure 19.3.3: The proposed distributed current-sharing LNA and voltage-steering VGA for ultra-low-power considerations.

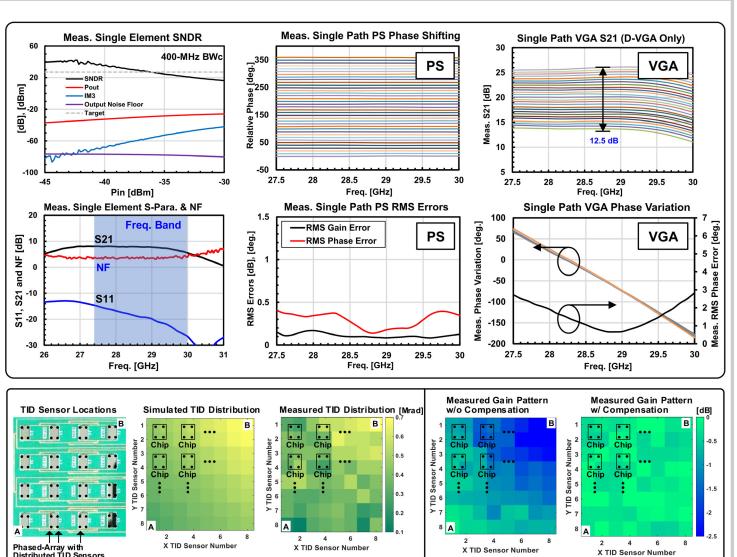


Figure 19.3.4: The proposed single-element, single-path, and radiation-compensation measured results.

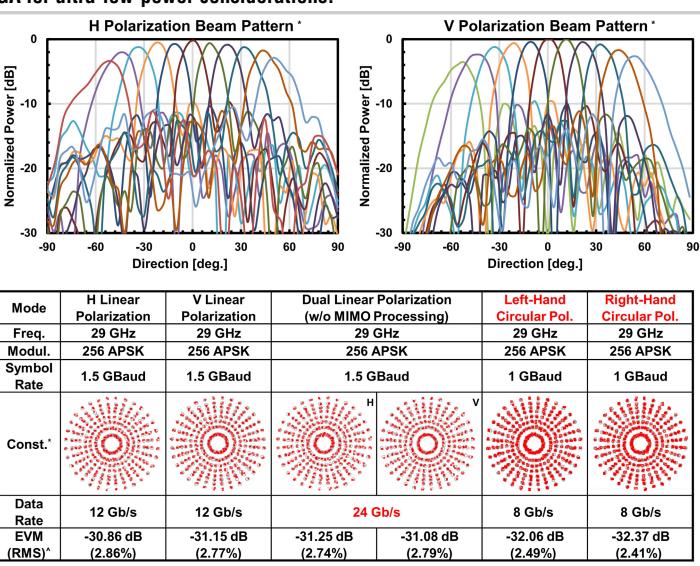


Figure 19.3.5: Measured beam patterns for sub-array module and RX constellations for 1m-OTA.

	This work	Samsung RFIC2021[4]	Zhejiang Univ. ISCC2021[5]	Samsung JSSC2020[6]	Tokyo Tech TMTT2021[7]	UCSD TMTT2021B[8]	Tokyo Tech ISCC2022 [1]
Process	65nm CMOS	28nm CMOS FD-SOI	65nm CMOS	28nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS
Application	SATCOM, 6G	5G	5G	5G	5G	SATCOM, 6G	SATCOM, 6G
Operation Band	25.9-30.1GHz	24.25-29.5GHz	25.9-30.1GHz	24.25-29.5GHz	27.7-19.2GHz	37-40GHz	27.5-30.5GHz*
Integration/ chip	8xBeamformer 4H+4V RX	2xBeamformer RX	8xBeamformer RX	16TxRx IF, LO	8xBeamformer RX	16xBeamformer (External LNA)	8xBeamformer RX
Supply Voltage	1V	1.1V	-	0.9V/1.8V	1V	1V/2.3V	0.8V
NF	3.6dB ^a	4.3-6.4dB	3.2-4.6dB	4.2-4.6dB @29GHz	5.2dB	1.6dB ^b	3.8dB ^d
Gain	17.4dB (26dB w/ D-VGA)	29dB ^c	19dB ^c	4-47dB	19-21dB	31dB ^c	17dB
IIP3	-20dBm ^c	-37.6dBm ^c	-17.4dBm ^c	-	-20dBm*	-42dBm ^c	-22dBm ^c
P _{DC} /Element	2.95mW^e	17.3mW ^f	74mW ^f	39mW	61mW ^f	45mW ^f	3.4mW ^f
Area/Element (0.32mm ²)	0.24mm ²	0.46mm ² k	1.6mm ²	0.94mm ²	0.48mm ²	6.1mm ² **	0.196mm ² k
PS Gain Error (RMS)	0.08dB @29GHz ^g	0.9dB	0.22dB	0.33dB	0.25dB @29GHz ^g	-	0.14dB @29GHz ^g
VGA Phase Error (RMS)	0.65° @29GHz ^g	-	-	-	2.3° (Variation)	-	-
OTA?	YES	NO	NO	YES	YES	NO	YES
Modulation	DVB-S2X 256APSK	64QAM OFDM	-	64QAM OFDM	256QAM OFDM	-	256APSK
Polarization Mode	Dual Linear Polarization	Circular Polarization	-	Linear Polarization	Dual Linear Polarization	Dual Linear Polarization	Linear Polarization
EVM	-31.25dB	-31.08dB	-31.08dB	-32.06dB	-32.37dB	-32.37dB	-33.2dB
Data-Rate	12 Gb/s	12 Gb/s	24 Gb/s	8 Gb/s	8 Gb/s	-	12.8Gb/s
Main Beam Degradation by TID	-2.4dB /Mrad	-0.22dB /Mrad	-	-	-	-	-

*Measured by 64H + 64V sub-array module
^Measured EVMs are referred to the RMS magnitude

Figure 19.3.6: Performance comparison with state-of-the-art works.

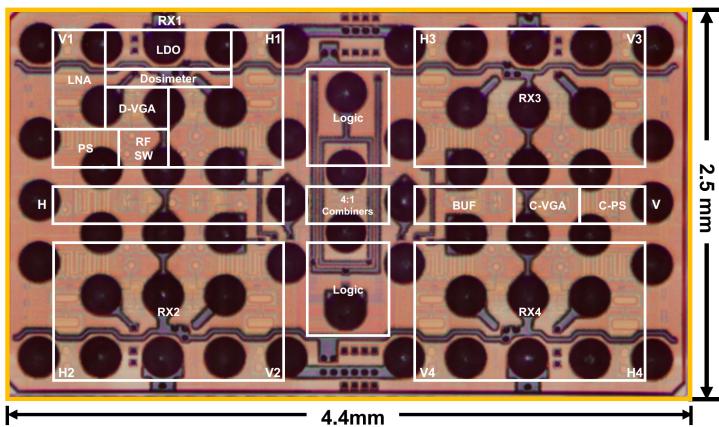


Figure 19.3.7: Die micrograph.

19.4 A Small-Satellite-Mounted 256-Element Ka-Band CMOS Phased-Array Transmitter Achieving 63.8dBm EIRP Under 26.6W Power Consumption Using Single/Dual Circular Polarization Active Coupler

Dongwon You¹, Xi Fu¹, Xiaolin Wang¹, Yuan Gao¹, Wengqian Wang¹, Jun Sakamaki¹, Hans Herdian¹, Sena Kato¹, Michihiro Ide¹, Yuncheng Zhang¹, Ashbir Aviat Fadila¹, Zheng Li¹, Chun Wang¹, Yun Wang¹, Jumpei Sudo², Makoto Higaki², Nahoka Kawaguchi², Masaya Nitta², Soichiro Inoue², Takashi Eishima², Takashi Tomura¹, Jian Pang¹, Hiroyuki Sakai¹, Kenichi Okada¹, Atsushi Shirane¹

¹Tokyo Institute of Technology, Tokyo, Japan, ²Axespace, Tokyo, Japan

Environmental monitoring, the earth-observation, and non-terrestrial networks using small satellite constellations have become promising space applications for next-generation society. There are three key design considerations in small satellite systems. First is the limitation of power consumption due to not only the limited energy from solar panels but also severe thermal management in space. Second is the requirement of beam steerability with large equivalent isotropically radiated power (EIRP) to communicate from 500km to 2000km in low earth orbit (LEO). Active phased-array technology is a prominent satellite transmitter (TX) solution. When the element number increases by N times, single-power-amplifier (PA) output power and total power consumption can be reduced by N^2 times and N times, respectively, under the constant EIRP condition. Thus, reducing PA output power and increasing the number of elements are the most efficient design strategies for lowering power consumption. This is illustrated in the upper left graphs in Fig. 19.4.1. The third consideration is that the satellite TX needs to generate accurate single and dual circular polarization (CP) signals for several situations: single polarization for polarization-multiplexing under a multi-satellite environment; dual circular polarization for high data throughput downlink. Especially in both cases, the cross-polarization discrimination (XPD), which represents the accuracy of CP, is the essentially required performance to avoid conflict between two satellite communication systems and/or interference between two signals in a single satellite communication system as the scenario is demonstrated in the upper right figure in Fig. 19.4.1.

Recent publications have demonstrated the implementation of single/dual-CP in phased-array transmitters (TX) in various ways [1-3] as described graphically in the lower table in Fig. 19.4.1. Like most satellite systems utilizing circular antennas, as in [1], CP patch antennas are used for phased-array implementation. However, circularly polarized patch antennas have a critical problem of difficulty in wide bandwidth implementation and low XPD caused by process variation. For wideband and high XPD implementation of a circularly polarized phased-array, phase-shifters (PS) are utilized to generate a 90° offset between H- and V-paths [2]. However, this type of CP generation by the PS cannot generate dual-CP and is required to turn on both H- and V- paths for single-CP, while consuming doubled power consumption compared with the CP antenna implementation [1].

In this work, a Ka-Band 256-element dual circularly polarized CMOS active phased-array TX is implemented to break through the aforementioned issues. Supported by a novel single/dual CP active coupler, the proposed TX realizes 1) low power consumption, 2) high XPD in single-CP mode, and 3) Single/Dual polarization (SP/DP) mode reconfigurability. A system block diagram is shown in Fig. 19.4.2. In a single chip, eight paths of single TXs are integrated. Four single TXs are for driving the H-ports of dual linearly polarized patch antennas, and the other four single TXs are for driving the V-ports of the patch. Each TX utilizes a variable-gain amplifier (VGA) and PS in a centralized- and distributed- path (C-/D-). A VGA and a PS in C-path are adopted to calibrate XPD in dual-CP mode independently of beam steering, which is set by a VGA and a PS in D-path. As one of the H-path single TXs and one of the V-path TXs form one pair, two paths are coupled by the proposed single/dual CP active coupler between D-VGA and power amplifier (PA). To build up a complete phased-array module, 64 chips are soldered onto a 256-element phased-array PCB. H-path inputs and V-path inputs of the 64 chips are distributed by a 64-way T-junction power divider, respectively. Various CP operation modes by the proposed single/dual CP active coupler are also shown in Fig. 19.4.2. Here, the right-handed circular polarization (RHCP) signal path is denoted by a blue outline, left-handed circular polarization (LHCP) by a red outline, and dual-CP (both LHCP and RHCP) by a purple outline. As SP mode is switched on, all the preceding stages from the D-VGA in V-path (grey outline) are turned off. This may include off-chip frequency conversion and additional gain stages. The quarter-wavelength grounded coplanar waveguide (GCPW) shifts the coupled signal by 90° to drive the V-port of the patch antenna. The power breakdown table supports how the proposed single/dual CP active coupler can save power consumption in SP mode. 28% of DC power consumption can be saved compared to the conventional single-CP generation method. If off-chip

power-consuming blocks are considered, then far more power will be saved. In DP mode, two coupled driver amplifiers (DA) are turned off, and switches are also shorted to the ground. Then, the shunt quarter-wavelength GCPWs act as open circuits; thus, two H- and V-paths are isolated.

To further explain the polarization calibration methodology in SP mode, circuit diagrams and measured results are shown in Fig. 19.4.3. The inputs of H-path coupled DA and V-path direct DA are shorted to the ground; thus, the two DAs now have the role of varactor by changing their bias (phase-compensating DAs). The measured gain and phase by sweeping capacitance control voltage of phase-compensating DAs are shown on the upper right side in Fig. 19.4.3. The result shows wide phase coverage while the amplitude varies only 3dB. To calibrate the 3dB amplitude variation, DAs on signal paths can be used as amplitude tuners. The gain and phase are measured and shown in the mid-right graph to evaluate the amplitude and phase tuning performance between H- and V-outputs. From the gain and phase offset measured data, the XPD is also calculated in the lower right graph in Fig. 19.4.3. While the XPD is only near 10dB when the two phase-compensating DAs are turned off, 36.8dB of maximum XPD is achieved after the calibration.

Figure 19.4.4 demonstrates measured single TX S-parameter results and measured single-tone performances; beam pattern, XPD in SP mode, and EIRP under swept input power. The S-parameter results show that the proposed TX fully covers the earth-exploration-satellite-service (EESS) downlink band. Even without inter-element amplitude and phase calibration, the beam-pattern measurement shows clear beam patterns.

The measured XPD results in the lower left graph in Fig. 19.4.4 strengthen the idea of the proposed single-CP calibration technique. To evaluate CP calibration performance, Vector Telecom's VT260CPHA15KR (RHCP) and VT260CPHA15KL (LHCP) are used for receiver (RX) antennas. After the proposed CP calibration, the measured XPD at the boresight angle improved to 43.2dB from 16.9dB. Over the scan range from -50° to +50°, more than 35dB XPD is achieved.

The last graph in Fig. 19.4.4 describes how the proposed single/dual CP active coupler works efficiently in SP mode. As a comparison target, the same methodology of CP generation as the method in [2] and [3] is used and drives the proposed TX. The apparent current saving is shown in the graph with -38% of the maximum power consumption saving. Two different CP generations achieve the same saturated EIRP of 63.8 dBm.

For a further comprehensive evaluation of wireless communication with CP transmitting, error-vector-magnitude (EVM) is also measured over-the-air (OTA). A 64-element array is used in the TX configuration, and Vector Telecom's circular horn antenna is used on the RX side at 2m away from the TX. The upper table in Fig. 19.4.5 describes single-CP EVM results. The proposed TX achieved -33.7dB EVM with a QPSK 2GHz signal. Also, -32.3dB EVM with 256APSK 2GHz is achieved as well. EVM analysis under dual CP transmission configuration is shown in a lower table in Fig. 19.4.5. A -30.1dB of the maximum EVM under DP condition is achieved with 250MHz QPSK signal and -27.1dB EVM with 256APSK modulation with the proposed phased-array TX.

Figure 19.4.6 summarizes the performance of this work and compares it with other published satellite communication (SATCOM) and 5G phased-array TX. This work presents the Ka-band single/dual CP phased-array transmitter mounted to a small satellite with low power consumption and high XPD. The proposed TX achieves 63.8dBm EIRP with 26.6W power consumption, which is a 62% reduction compared to the state-of-the-art TX [4] with the same level of EIRP. The proposed single/dual CP active coupler not only lowers the power consumption but also improves the XPD as high as 35dB by tuning the phase offset between H- and V-paths. The die micrograph is shown in Fig. 19.4.7. The proposed phased-array chip is fabricated in a 65nm bulk CMOS process with a wafer-level chip-scale package (WLCSP) in 4.4mm×2.5mm die size.

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References:

- [1] X. Luo et al., "A Scalable Ka-Band 1024-Element Transmit Dual-Circularly-Polarized Planar Phased Array for SATCOM Application," *IEEE Access*, vol. 8, pp. 156084-156095, 2020.
- [2] K. K. W. Low et al., "A 27–31-GHz 1024-Element Ka-Band SATCOM Phased-Array Transmitter With 49.5-dBW Peak EIRP, 1-dB AR, and ±70° Beam Scanning," *IEEE TMTT*, vol. 70, no. 3, pp. 1757-1768, March 2022.
- [3] D. You et al., "A Ka- Band Dual Circularly Polarized CMOS Transmitter with Adaptive Scan Impedance Tuner and Active XPD Calibration Technique for Satellite Terminal," *IEEE RFIC*, pp. 15-18, 2022.

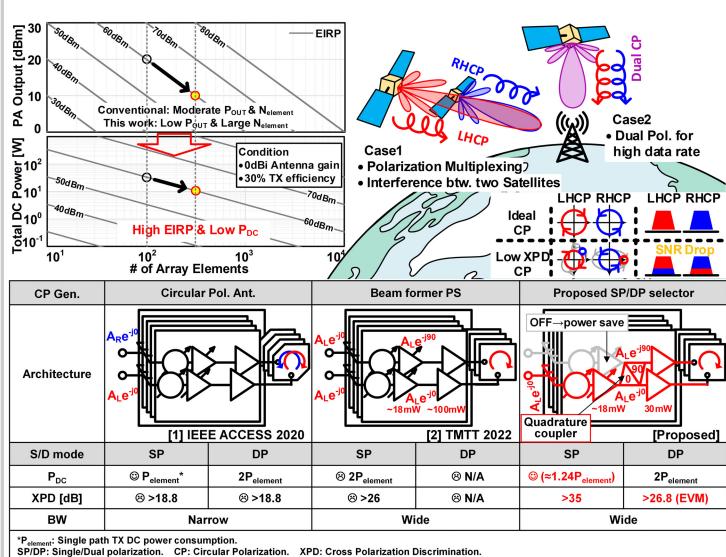


Figure 19.4.1: Design considerations for low power single/dual circular polarization TX and comparison.

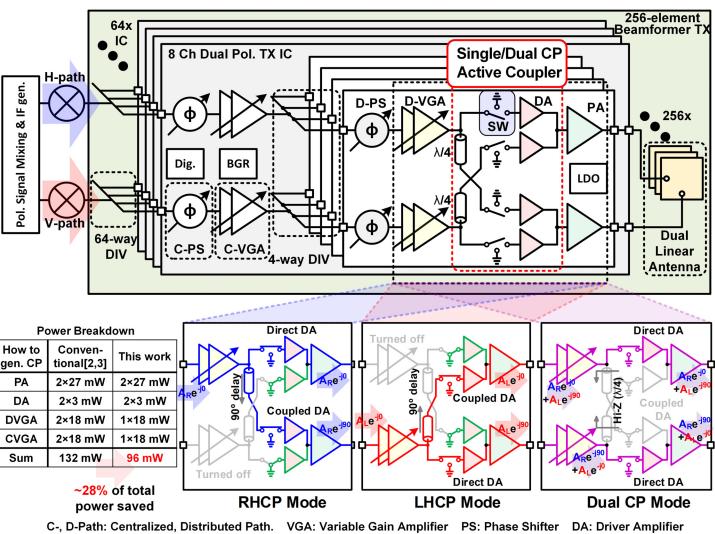


Figure 19.4.2: Block diagram for single/dual circular polarization TX with single/dual circular polarization active coupler and power breakdown.

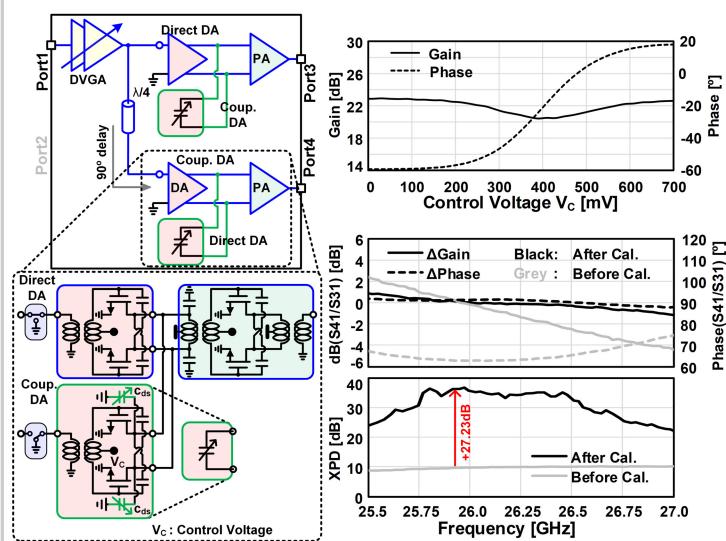


Figure 19.4.3: Circuit diagrams of proposed single/dual circular polarization active coupler, circular polarization calibration, and measured results.

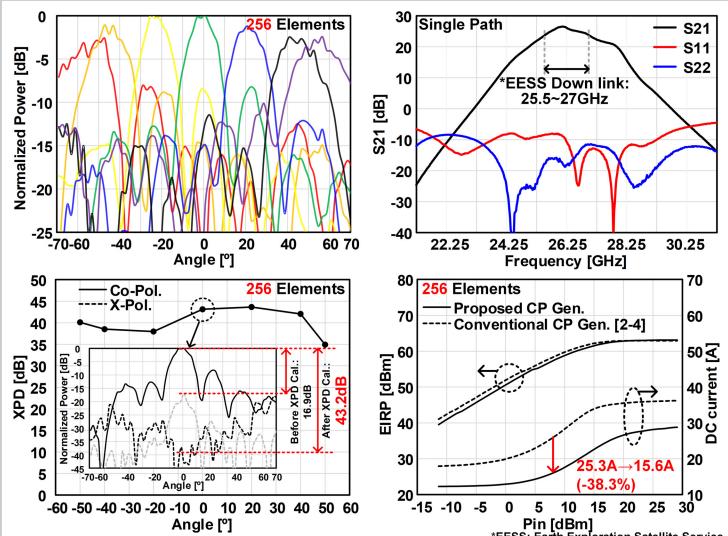


Figure 19.4.4: S-parameters of single path and over-the-air measurement summary: Beam pattern, XPD, Power consumption comparison between proposed and conventional circular polarization.

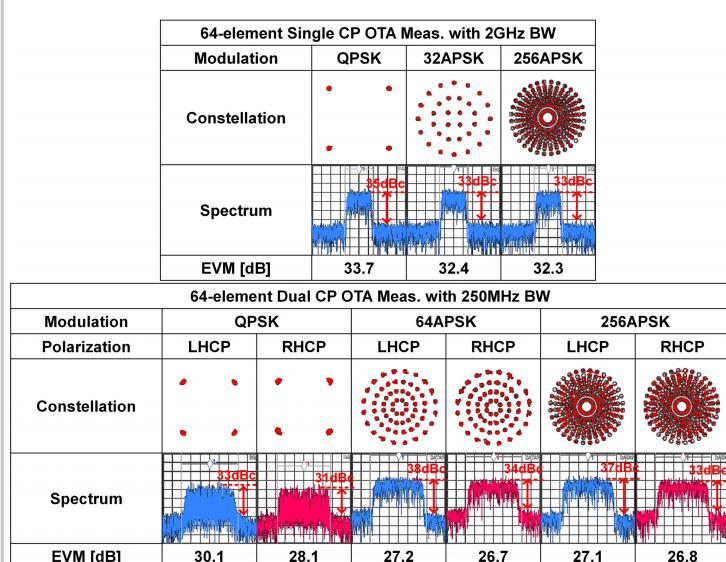


Figure 19.4.5: EVM results for single and dual circular polarization.

	This Work	[2] TMTT 2022	[1] IEEE Access 2020	[5] ISSCC 2022	[4] IMS 2019	[3] RFIC 2022
Process Tech.	65nm Bulk CMOS	SiGe BiCMOS	65nm Bulk CMOS	130nm SiGe BiCMOS	SiGe BiCMOS	65nm Bulk CMOS
Frequency [GHz]	25.5-27.2	27-31	29.5-30	24-30	28-31	25.4-27.4
Chip area [mm ²]	4.4×2.5	4.6×3.8	6×6	6.6×5.6	4.6×3.8	4×1.5
Application	SATCOM downlink (Satellite Mounted)	SATCOM uplink (Earth Station)	SATCOM uplink (Earth Station)	5G NR (Terrestrial)	SATCOM uplink (Earth Station)	SATCOM downlink (Sat Terminal)
# of elements	256	1024	1024	256	256	32
Polarization	Dual Circular	Single Circular	Single Circular	Dual Linear	Single Circular	Dual Circular
CP gen.	Active Coupler	BF PS	CP antenna	N/A	BF PS	DBB
Supply voltage [V]	1	2.3	1	N/A	N/A	1
Areal/Path [mm ² /m]	0.42	N/A	N/A	1.2	N/A	0.38
Single TX						
Modulation	QPSK 32APSK 256APSK					
Polarization	LHCP RHCP	LHCP RHCP	LHCP RHCP			
Constellation						
Spectrum						
EVM [dB]	33.7 32.4 32.3					
Array						
Modulation	QPSK 64APSK 256APSK					
Polarization	LHCP RHCP	LHCP RHCP	LHCP RHCP			
Constellation						
Spectrum						
EVM [dB]	30.1 28.1 27.2 26.7 27.1 26.8					

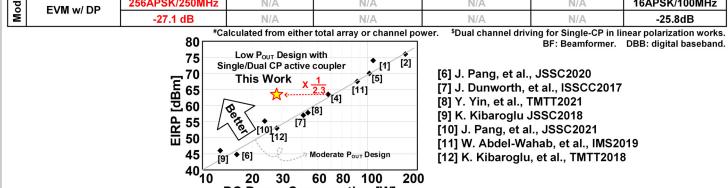
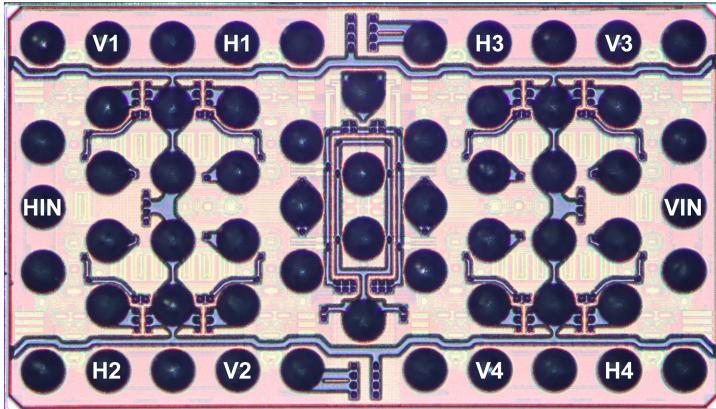


Figure 19.4.6: Performance comparison of Ka-band phased-array transmitters.



- 65nm Bulk CMOS
- 4.4×2.5 mm²
- WLCSP
- 8 Path TX

Figure 19.4.7: Die micrograph.

Additional References:

- [4] K. K. Wei Low et al., "A Scalable Circularly-Polarized 256-Element Ka-Band Phased-Array SATCOM Transmitter with ±60° Beam Scanning and 34.5 dBW EIRP," *IEEE IMS*, pp. 1064-1067, 2019.
- [5] B. Sadhu et al., "A 24-to-30GHz 256-Element Dual-Polarized 5G Phased Array with Fast Beam-Switching Support for >30,000 Beams," *ISSCC*, pp. 436-437, Feb. 2022.