

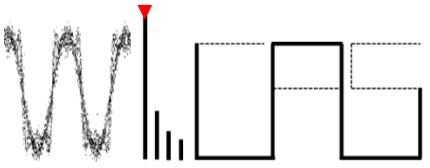


ISSCC 2023

SESSION 25

RF Transceiver

Building Blocks



A 4.1W Quadrature Doherty Digital Power Amplifier with 33.6% Peak PAE in 28nm Bulk CMOS

Jiaxiang Li¹, Yun Yin¹, Hang Chen², Jie Lin¹, Yicheng Li¹,
Xianglong Jia¹, Zhen Hu¹, Xiuyin Zhang², Hongtao Xu¹

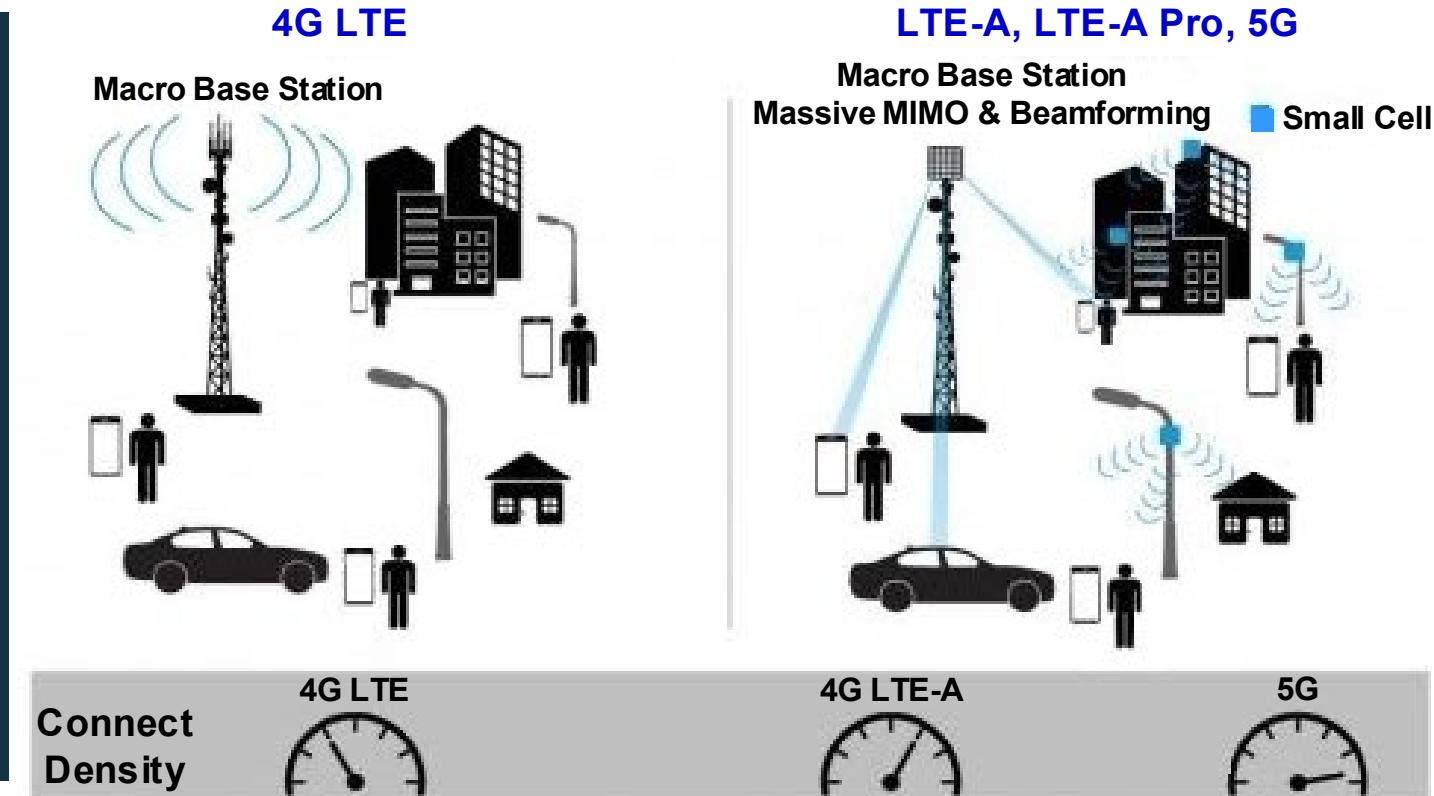
¹Fudan University, Shanghai, China

²South China University of Technology, Guangzhou, China

Outline

- Motivation
- Operation Principles of 8-way Differential Power Combined Quadrature DPA
- Circuit Implementation
- Measurement Results
- Conclusions

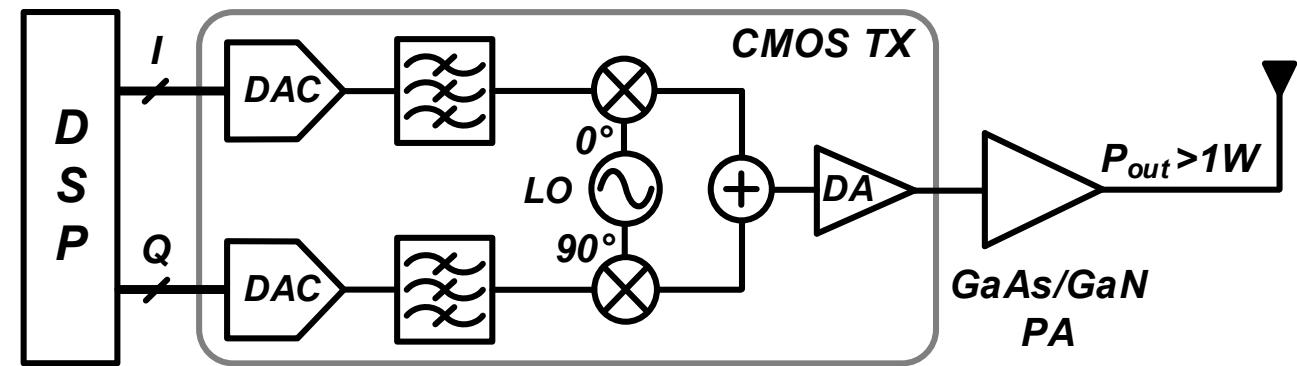
Motivation (1/2)



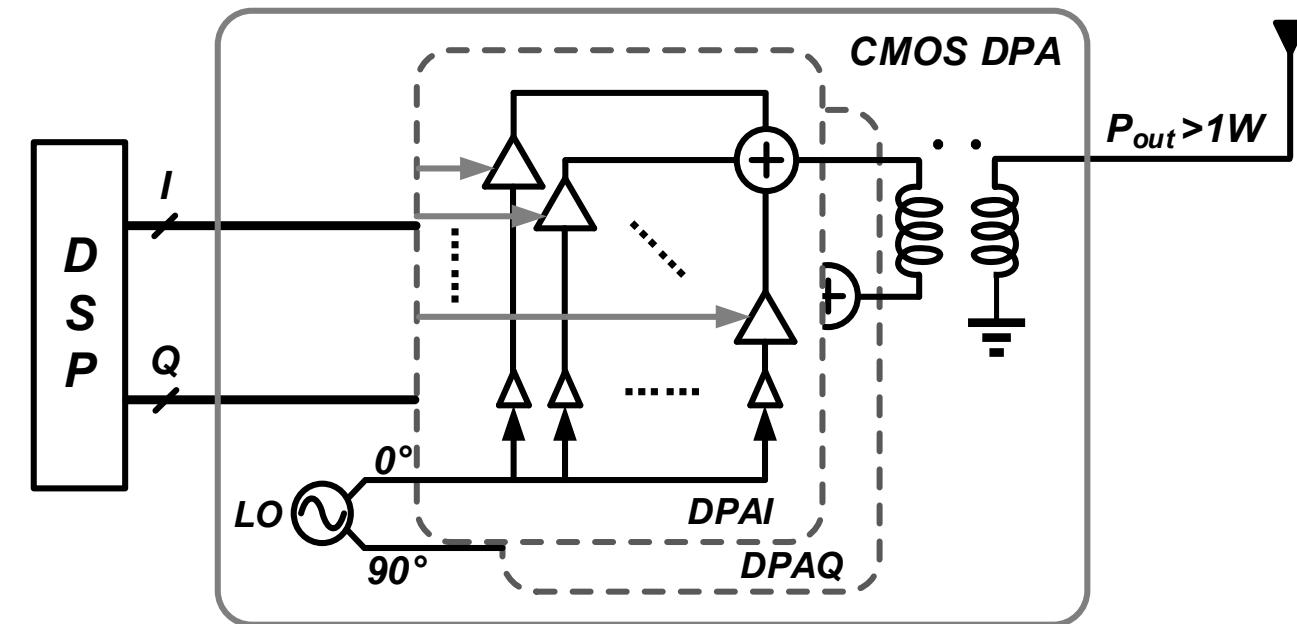
- Higher requirements at base station for 5G mobile communication
 - Higher throughputs, complex high-order QAM modulation & high PAPR
 - Higher output power for wide coverage
 - Higher connection density, etc.

Motivation (2/2)

Traditional High-Pout TX Architecture



Proposed High-Pout CMOS DTX Architecture



	Traditional High-Pout TX	Proposed High-Pout DTX
Output Power	High	Medium
System Efficiency	Medium	High
Integration Level	Low	High
Cost	High	Low
Process Scaling-Friendly	Bad	Good
Architecture Flexibility	Bad	Good

Digital Transmitter Architecture

	Polar DTX	Quadrature DTX	
Pros	High Pout High PAE	Mature architecture Wide bandwidth	<ul style="list-style-type: none">■ Load modulation■ Supply modulation■ Sub-harmonic switching■ Combination of above techniques
Cons	CORDIC Phase modulator AM-PM alignment AM&PM bandwidth expansion	<p>Lower PAE</p> <p>Lower Pout</p>	<ul style="list-style-type: none">■ Transistor stacking■ Power combining■ IQ-cell sharing

Boost PAE *Boost Pout*

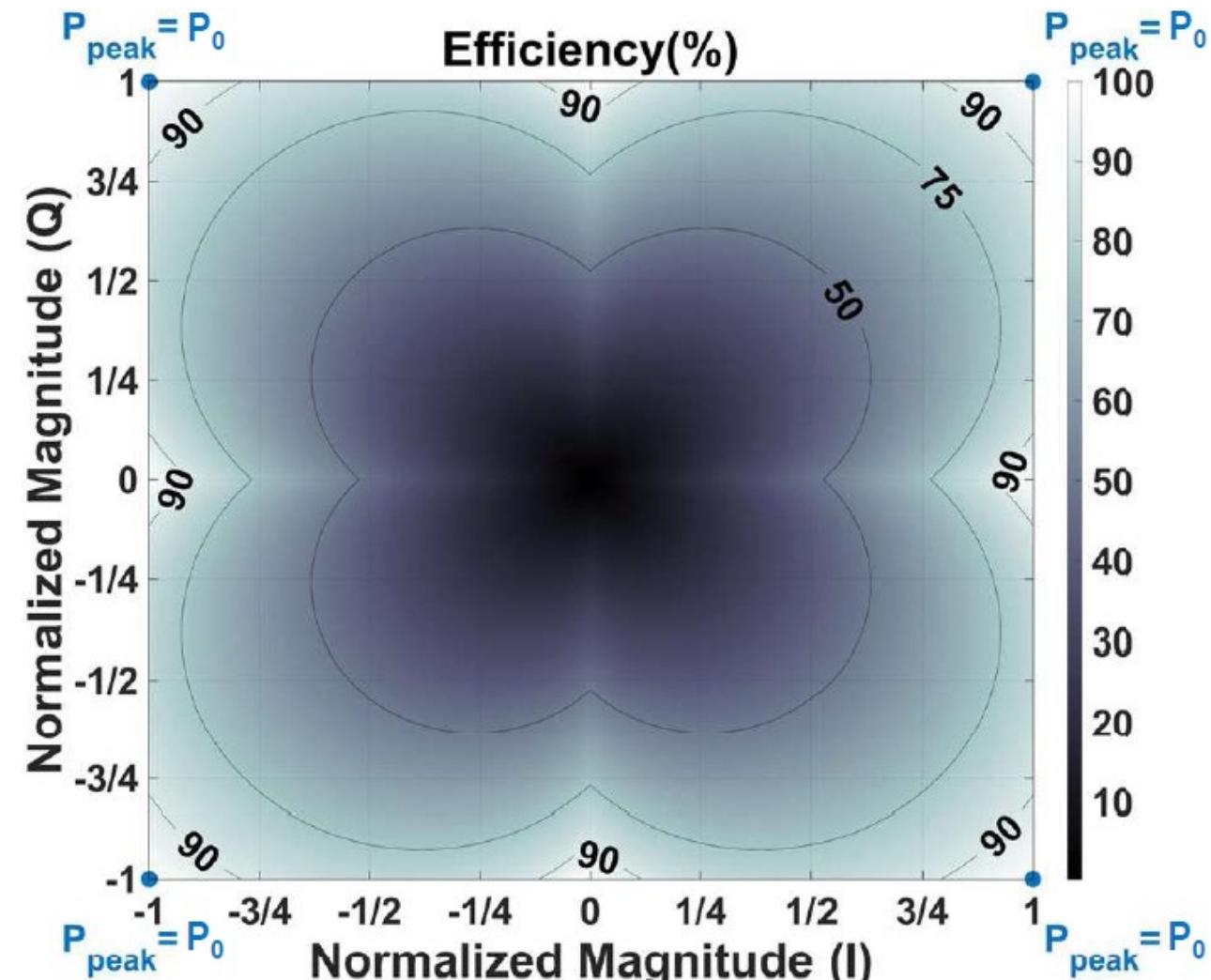
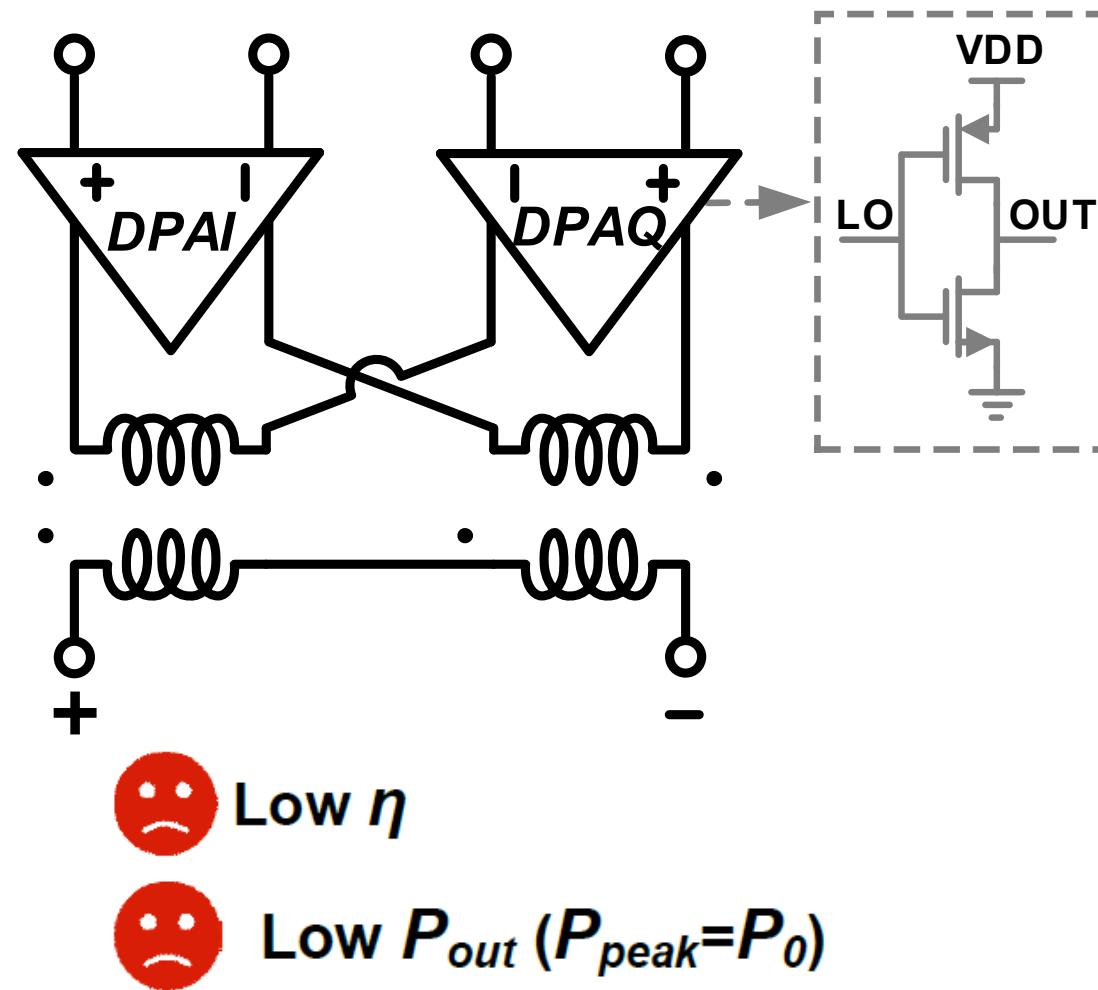
Quadrature DTXs with high Pout and high PAE are desirable for 5G communications

Outline

- Motivation
- Operation Principles of 8-way Differential Power Combined Quadrature DPA
- Circuit Implementation
- Measurement Results
- Conclusions

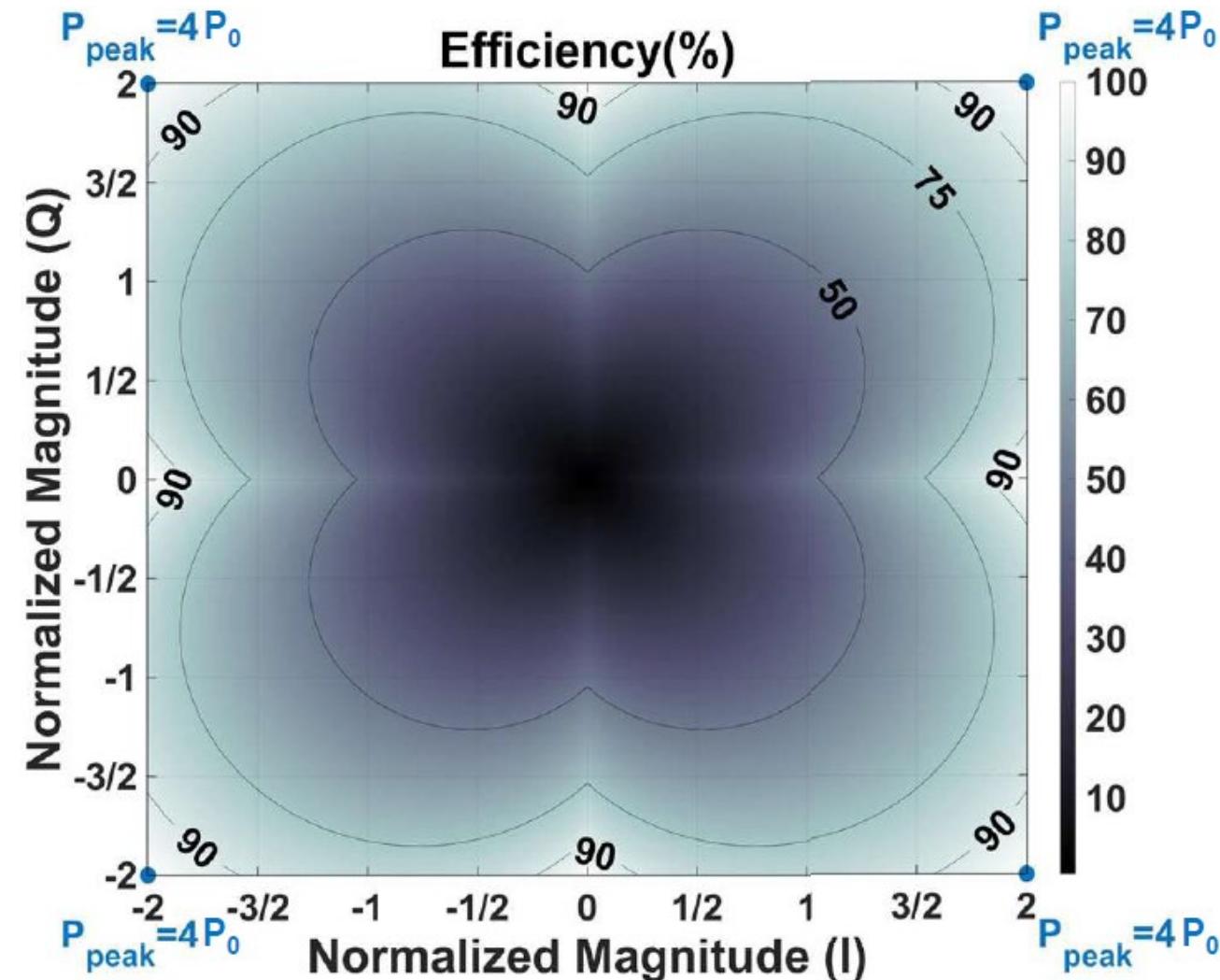
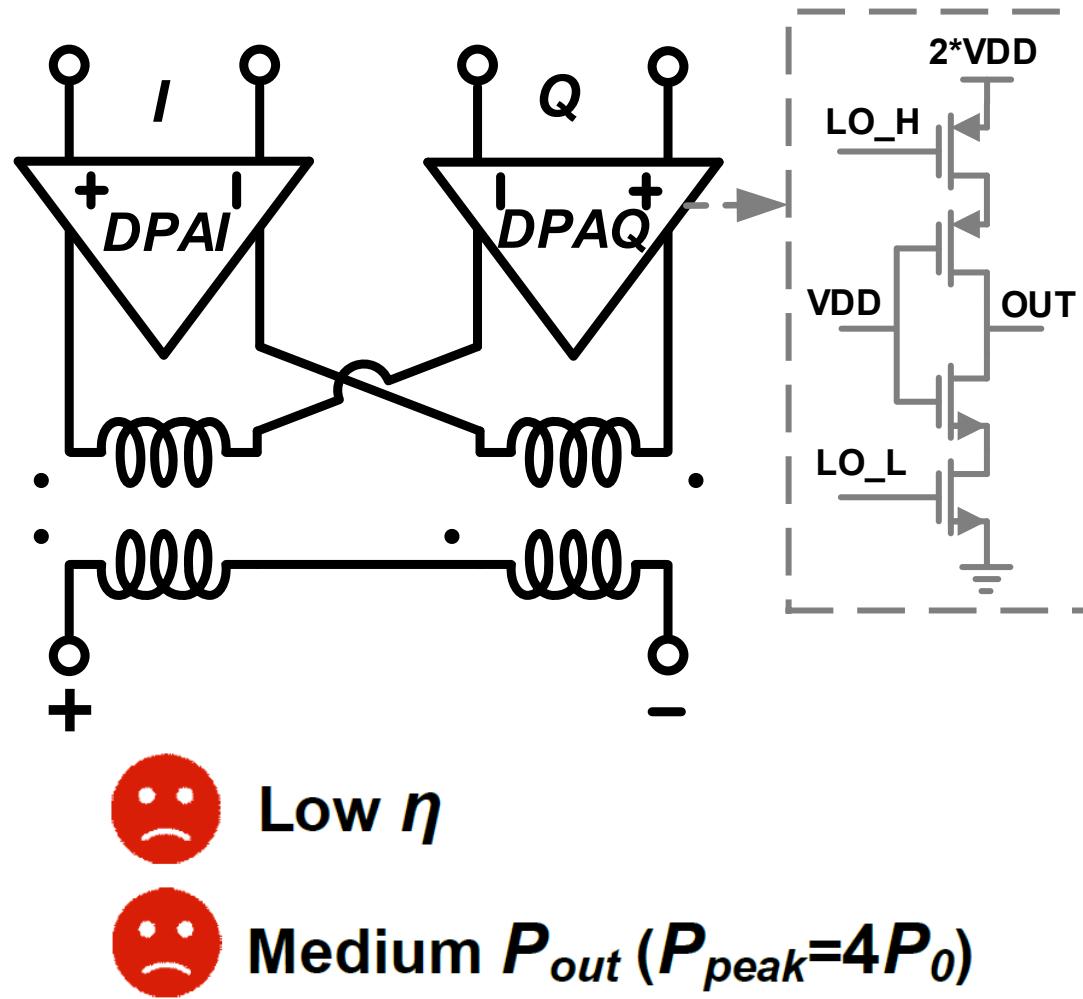
Pout & PAE Enhancement Techniques (1/4)

Quadrature Doherty SCPA:



Pout & PAE Enhancement Techniques (2/4)

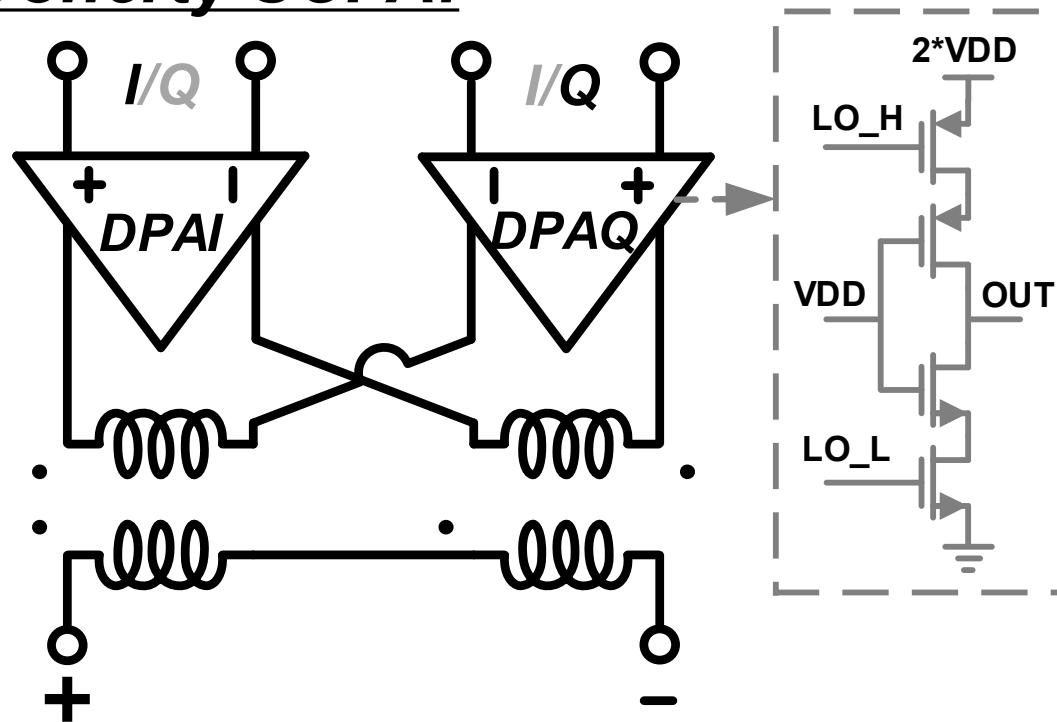
Quadrature Cascode Doherty SCPA:



Pout & PAE Enhancement Techniques (3/4)

Quadrature IQ-Reuse Cascode

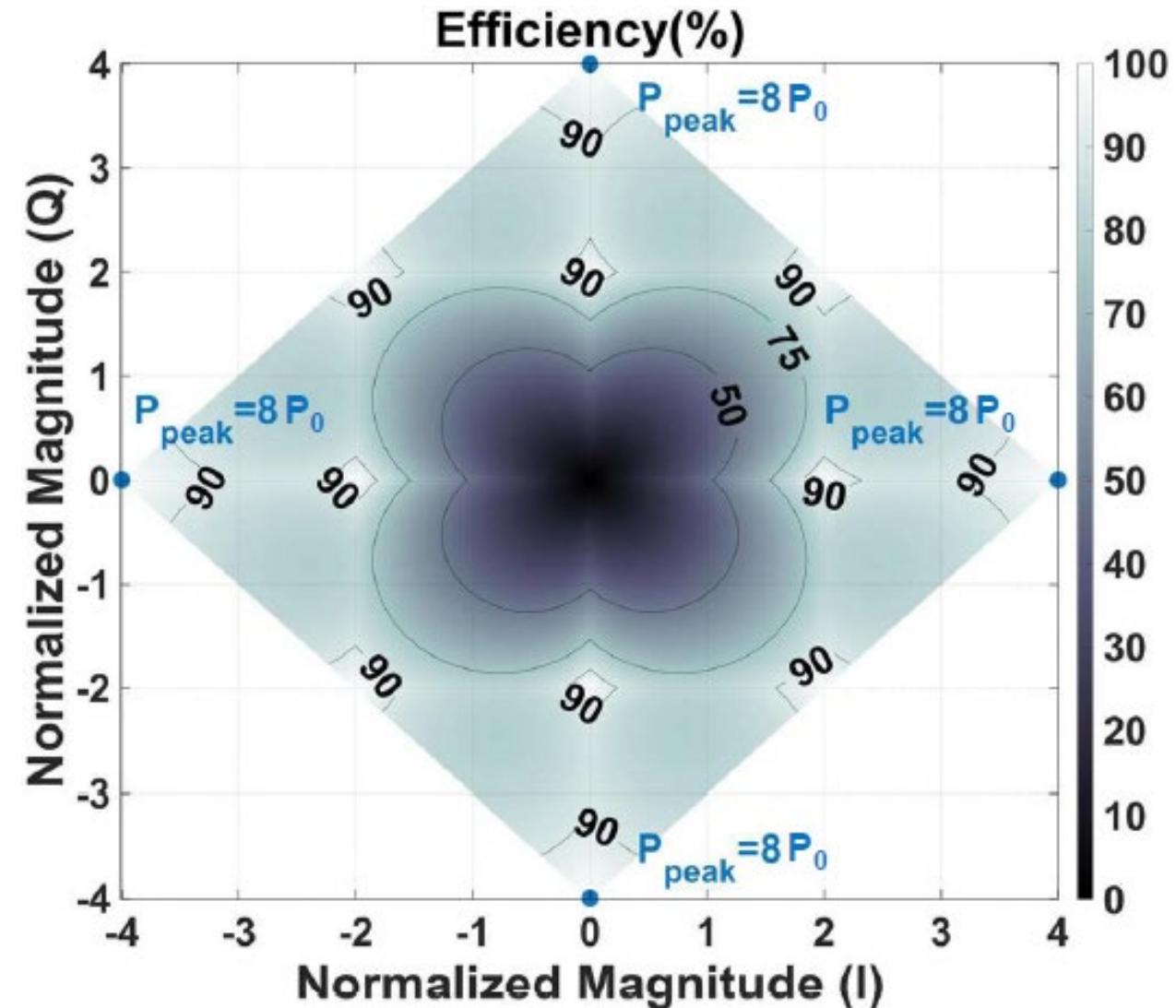
Doherty SCPA:



Improved η



High P_{out} ($P_{peak}=8P_0$)

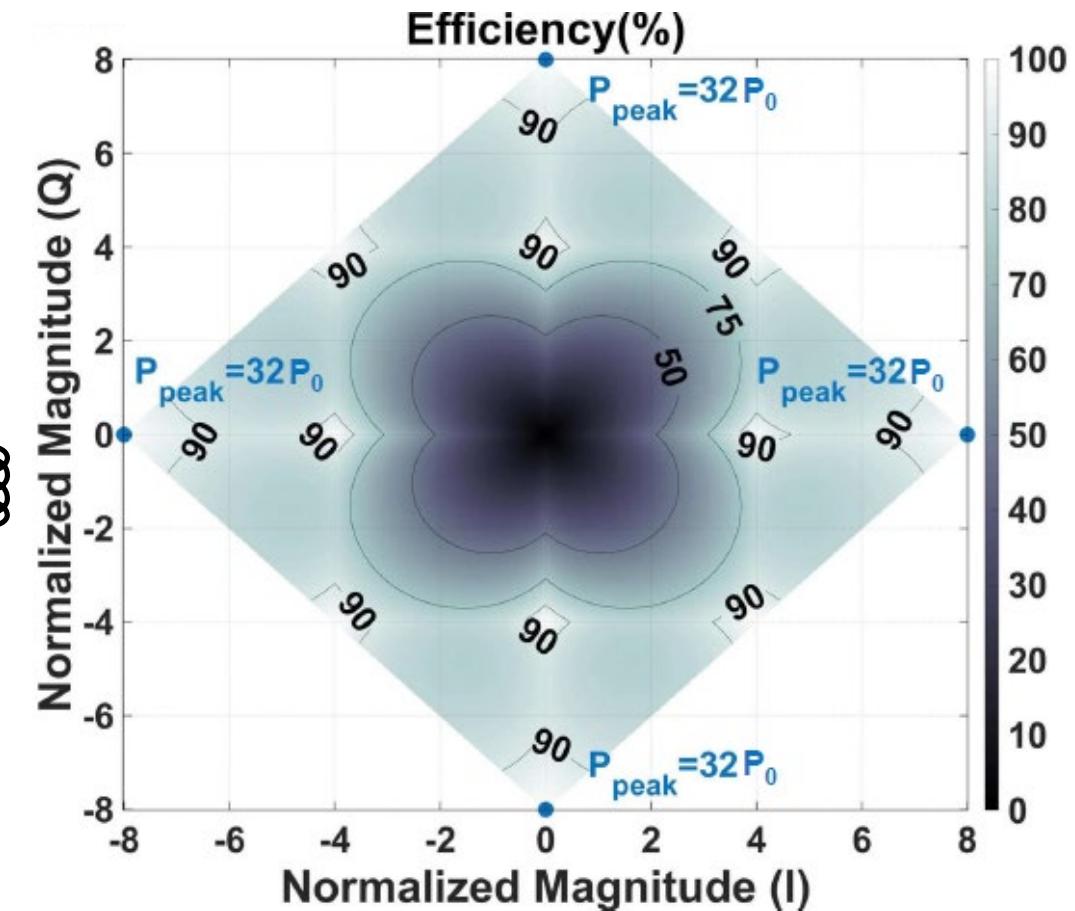
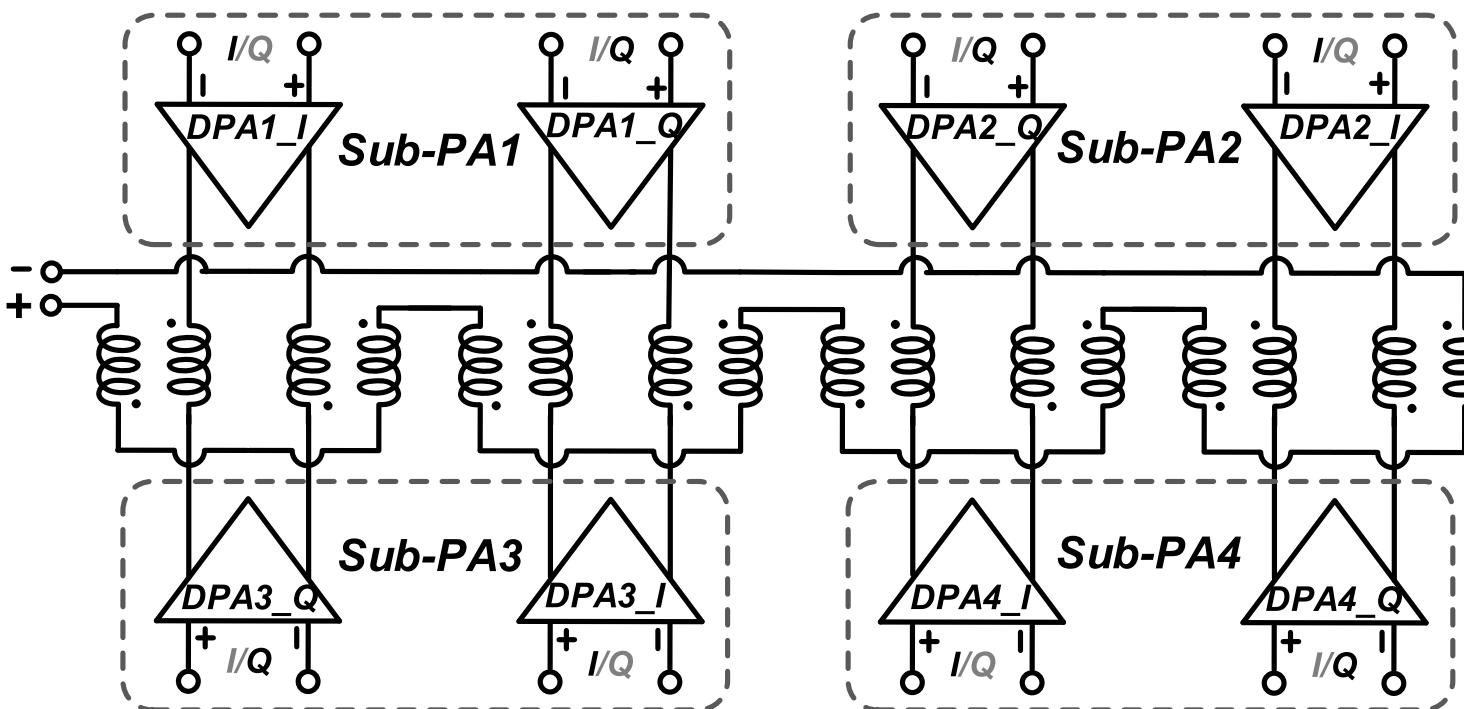


[D. Zheng, ISSCC 2020]

Pout & PAE Enhancement Techniques (4/4)

8-Way Differential Power Combined

Quadrature IQ-Reuse Cascode Doherty SCPA:



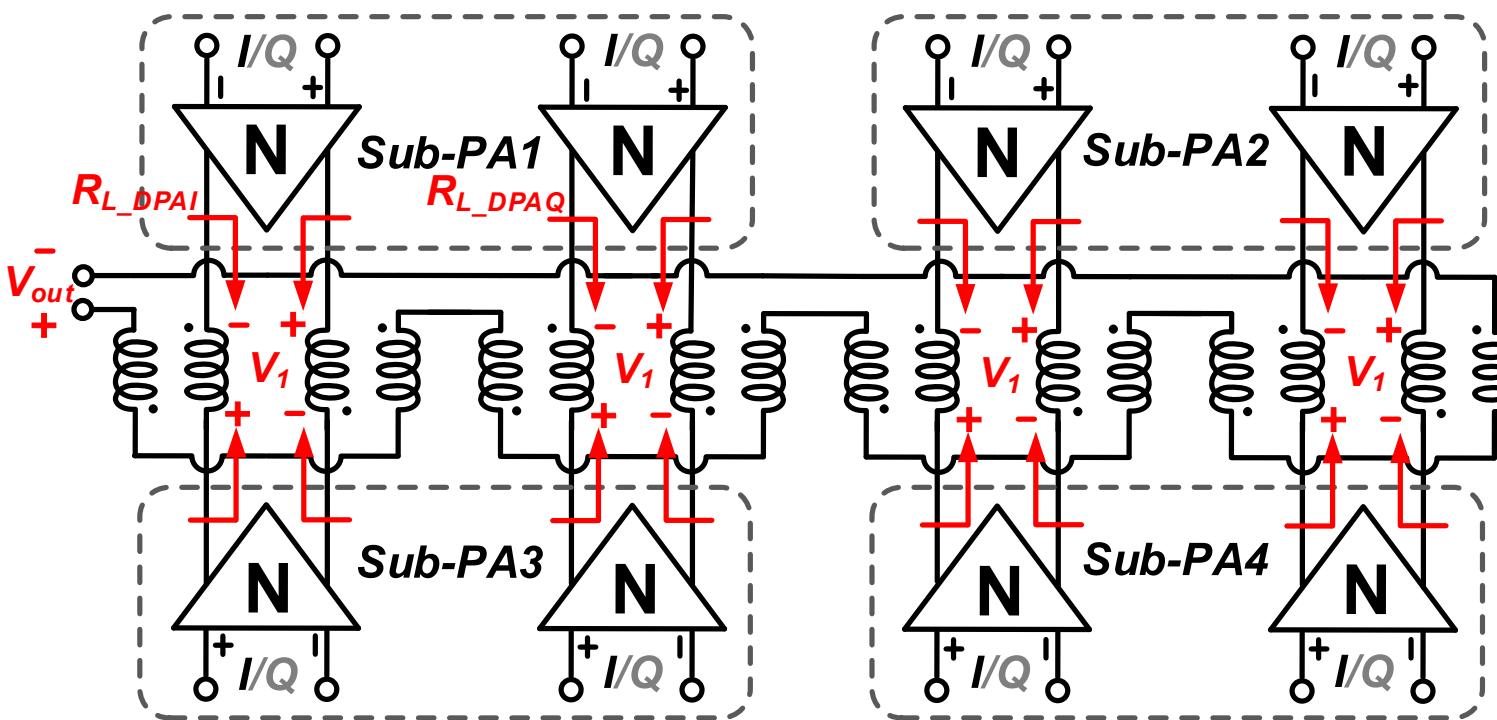
Improved η



Extremely High P_{out} ($P_{peak}=32P_0$)

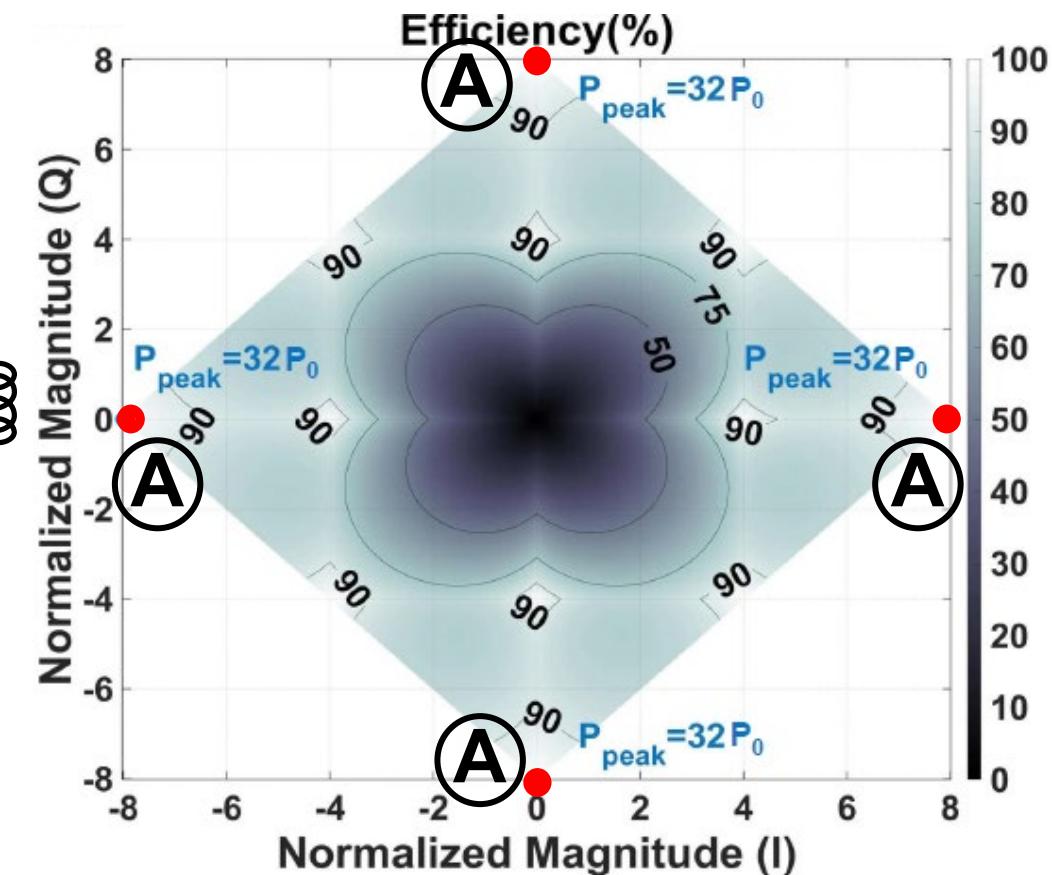
Complex-Domain Doherty Operations (1/4)

At state A (Four 0dB PBOs):



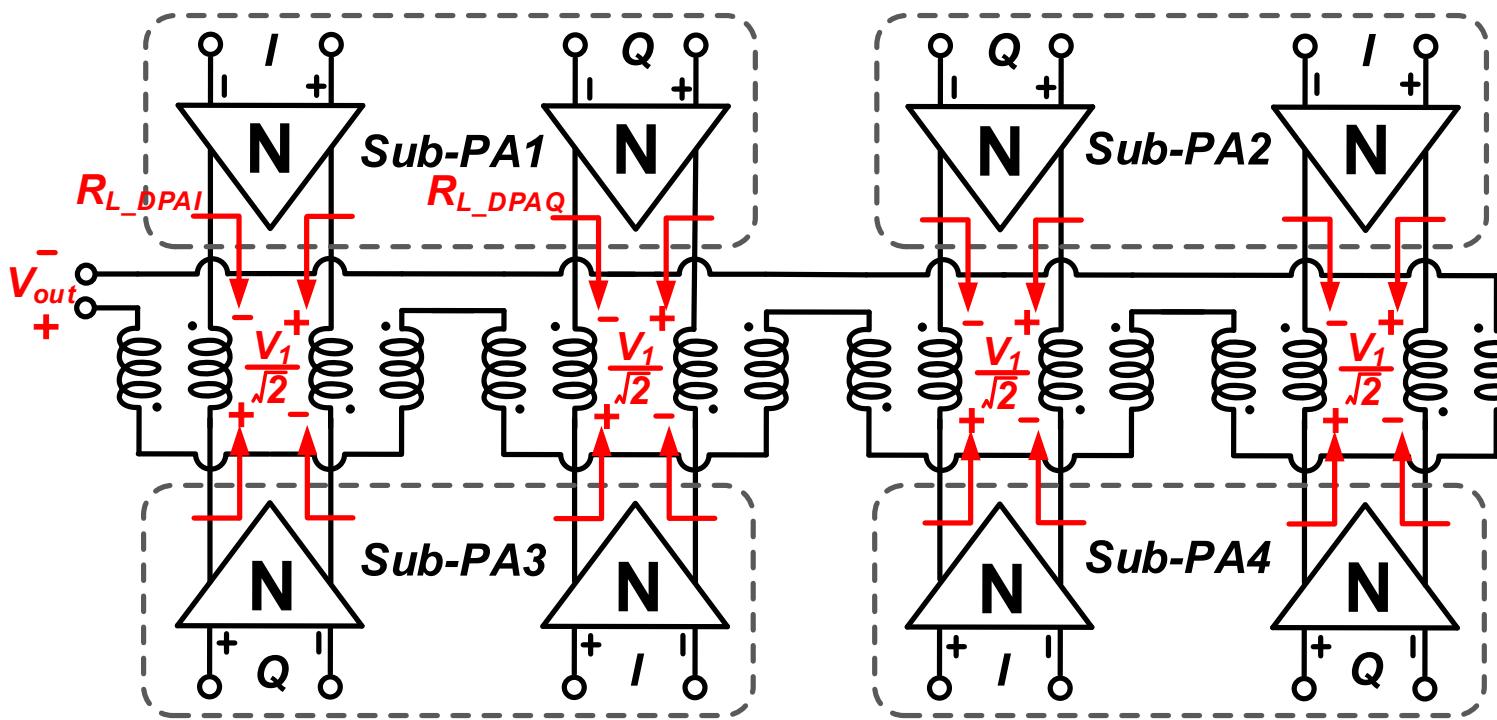
$$V_{out} = 8 \times V_1, P_{out} = V_{out}^2/R_L = P_{peak}$$

$$R_{L,DPAI} = R_{L,DPAQ} = R_L/16$$



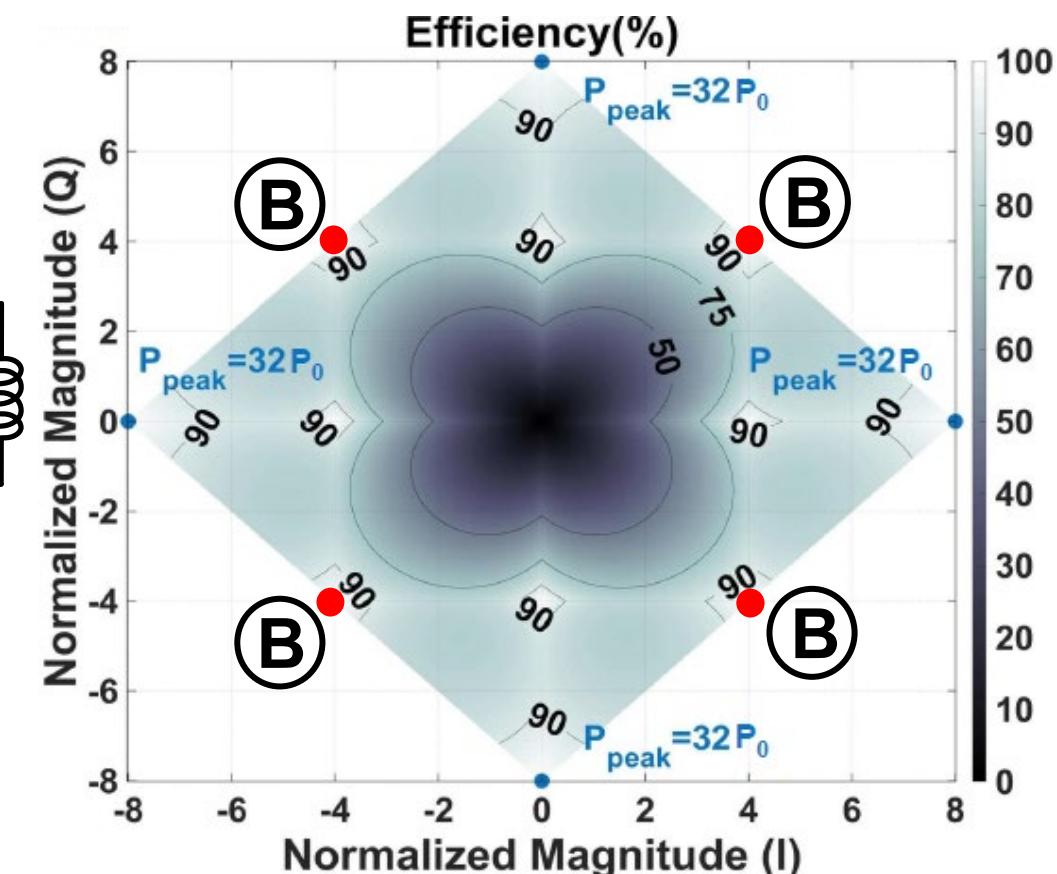
Complex-Domain Doherty Operations (2/4)

At state B (Four 3dB PBOs):



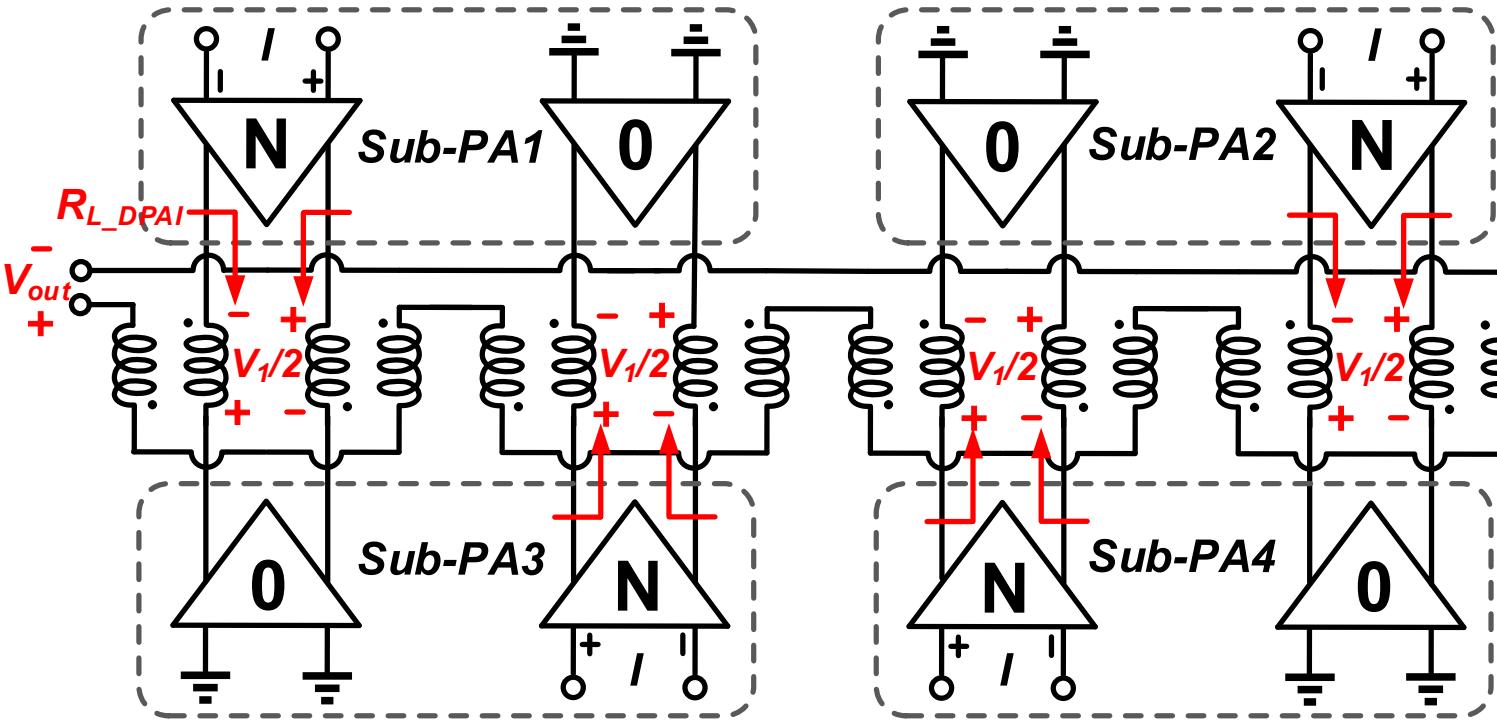
$$V_{out} = 4\sqrt{2} \times V_1, P_{out} = V_{out}^2/R_L = P_{peak}/2$$

$$R_{L_DPAI} = R_{L_DPAQ} = \sqrt{2}R_L/16$$



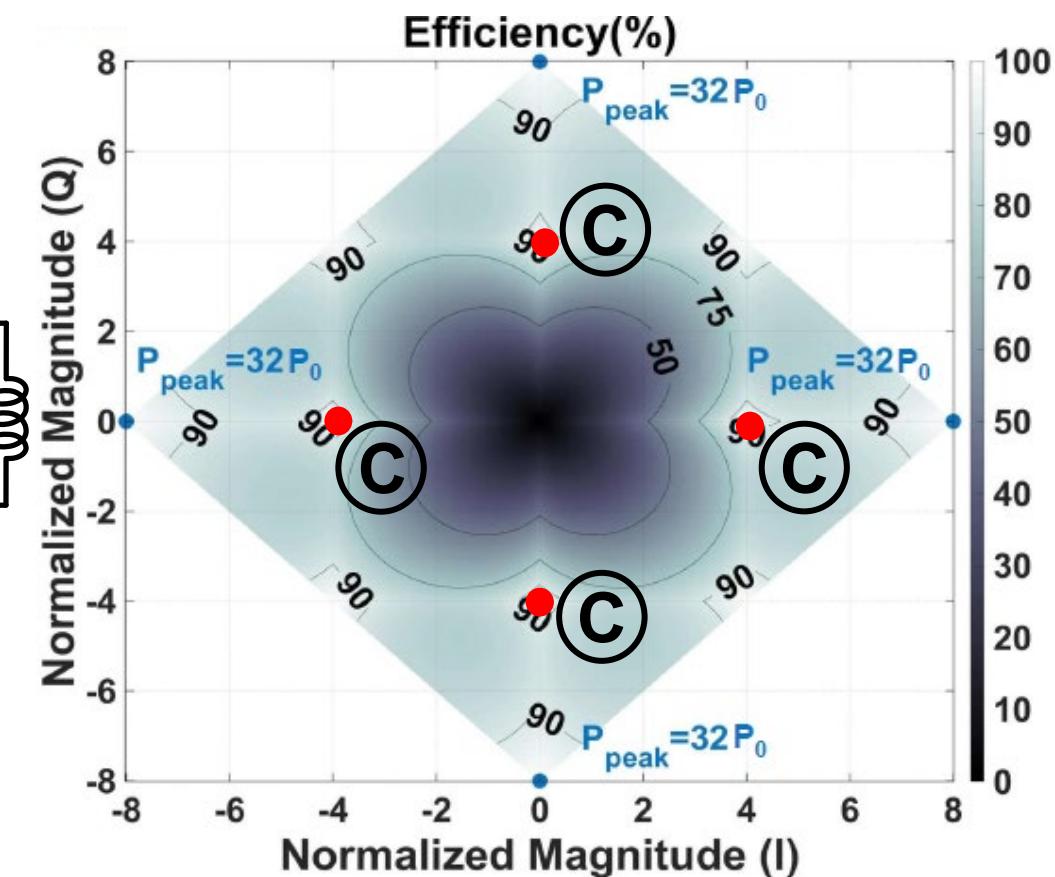
Complex-Domain Doherty Operations (3/4)

At state C (Four 6dB PBOs):

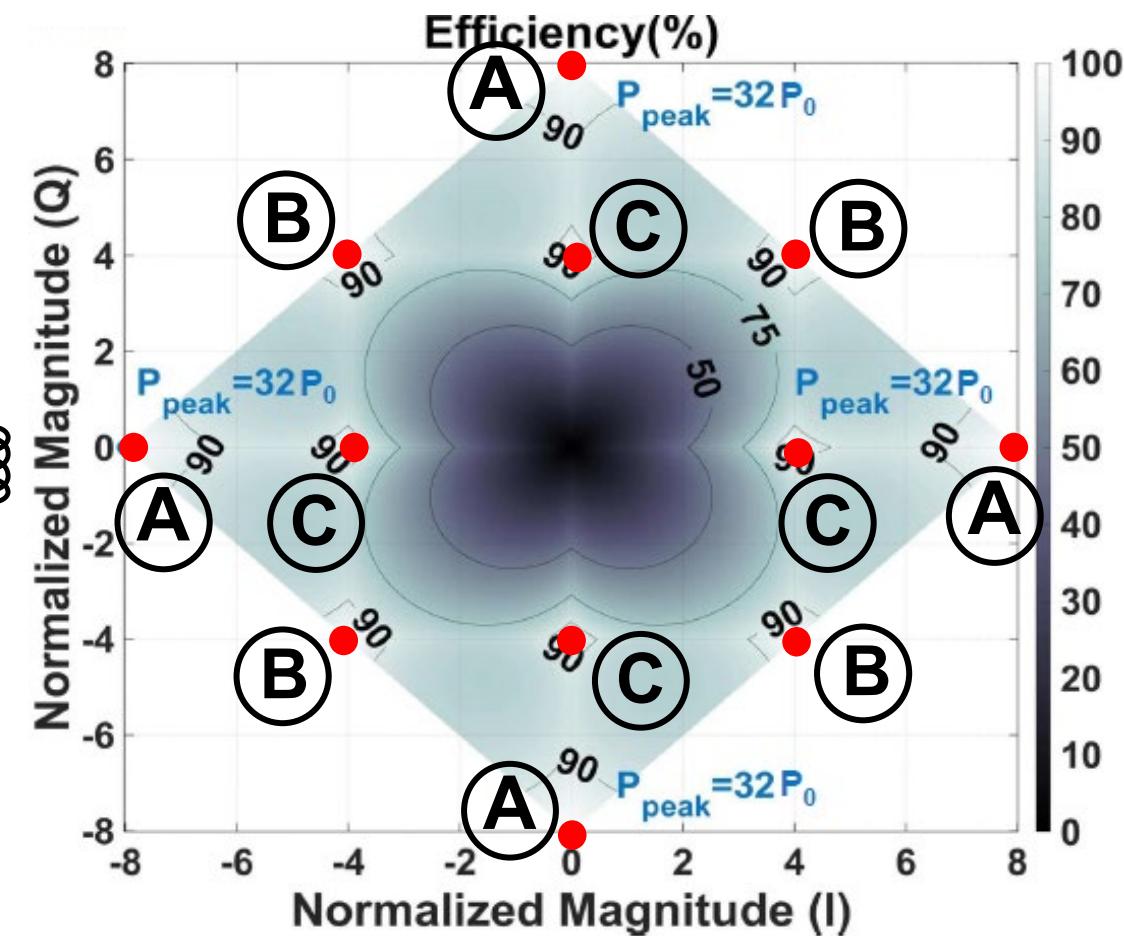
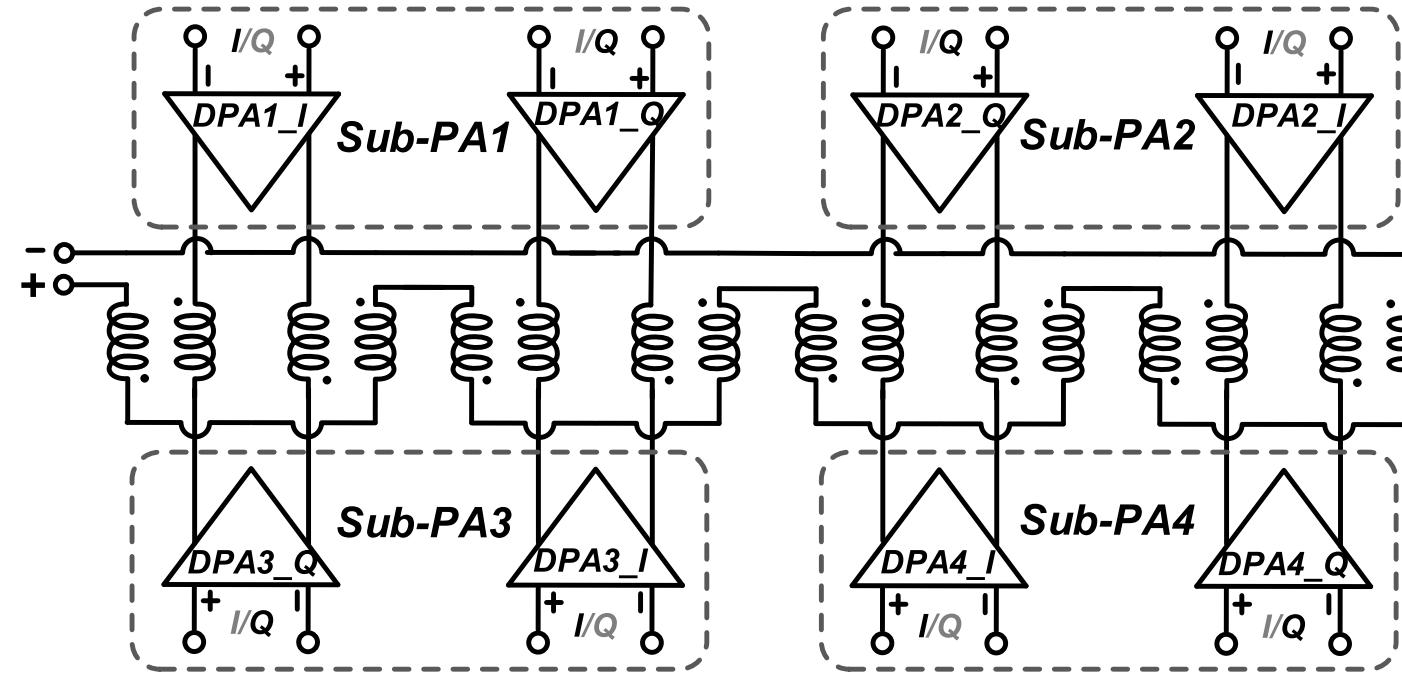


$$V_{out} = 4 \times V_1, P_{out} = V_{out}^2/R_L = P_{peak}/4$$

$$R_{L_DPAI} = R_L/8$$



Complex-Domain Doherty Operations (4/4)

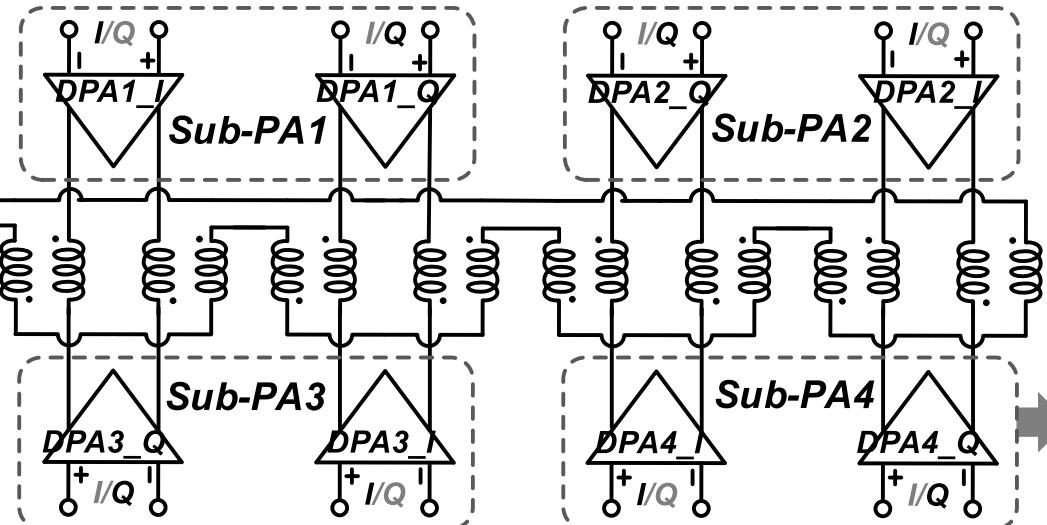


- IQ-Reuse: the same peak Pout and peak PAE as polar counterpart
- Pout increased by **32x** with cascode, IQ-reuse and 8-way differential SCT
- Doherty operations: **12 efficiency peaks** on the I/Q complex plane

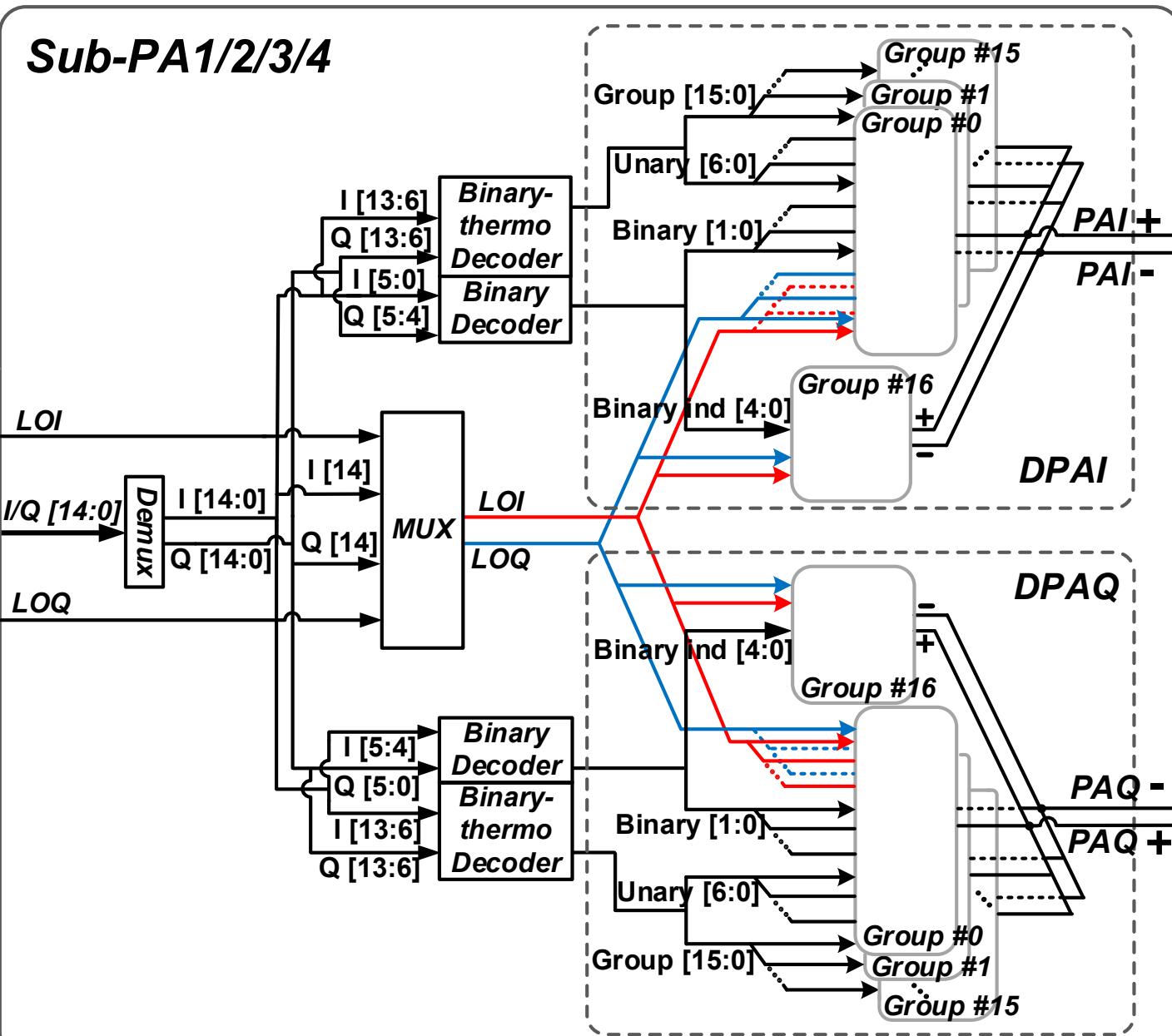
Outline

- Motivation
- Operation Principles of 8-way Differential Power Combined Quadrature DPA
- Circuit Implementation
- Measurement Results
- Conclusions

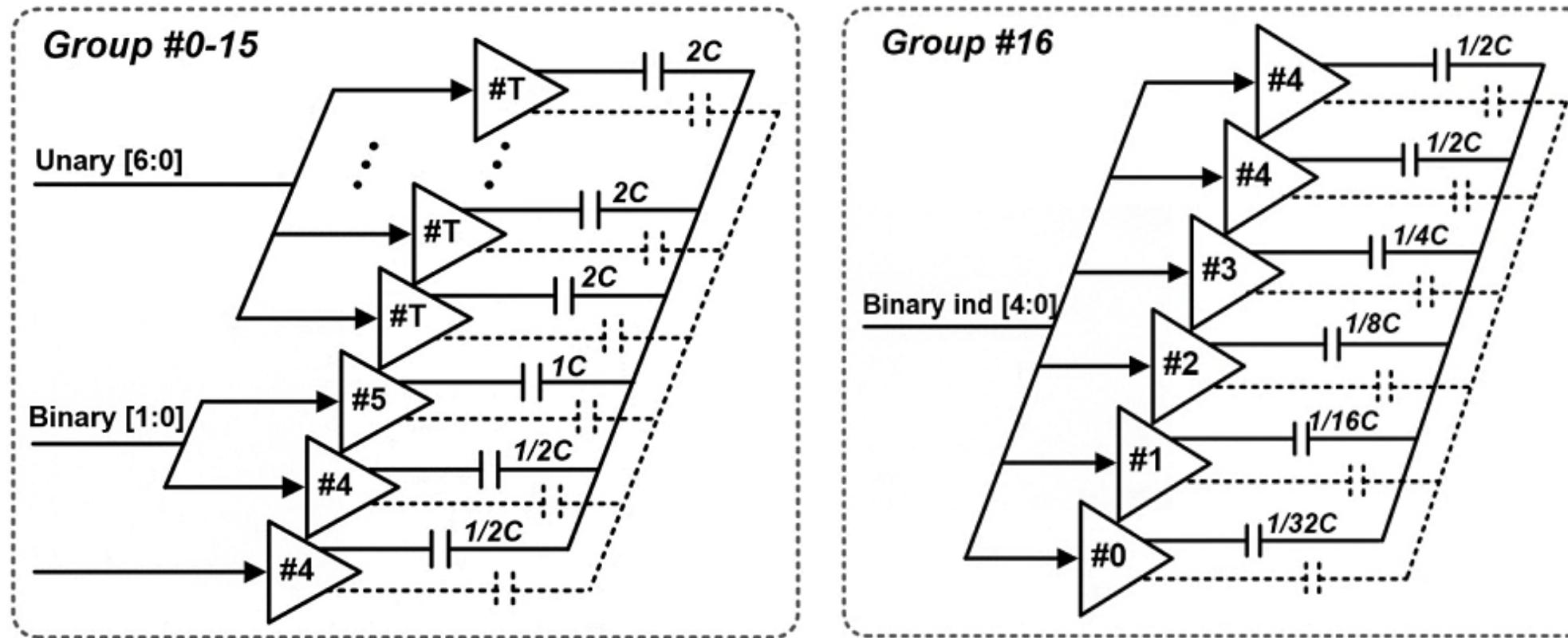
Circuit Implementation – Sub-PA Architecture



- Sub-PA1/2/3/4 are power combined with an 8-way differential SCT
- Each sub-PA consists of DPAI & DPAQ
- 15b resolution:
 - I/Q[14] are sign bits for LO selection
 - Each DPA has hybrid unary/binary-coded arrays

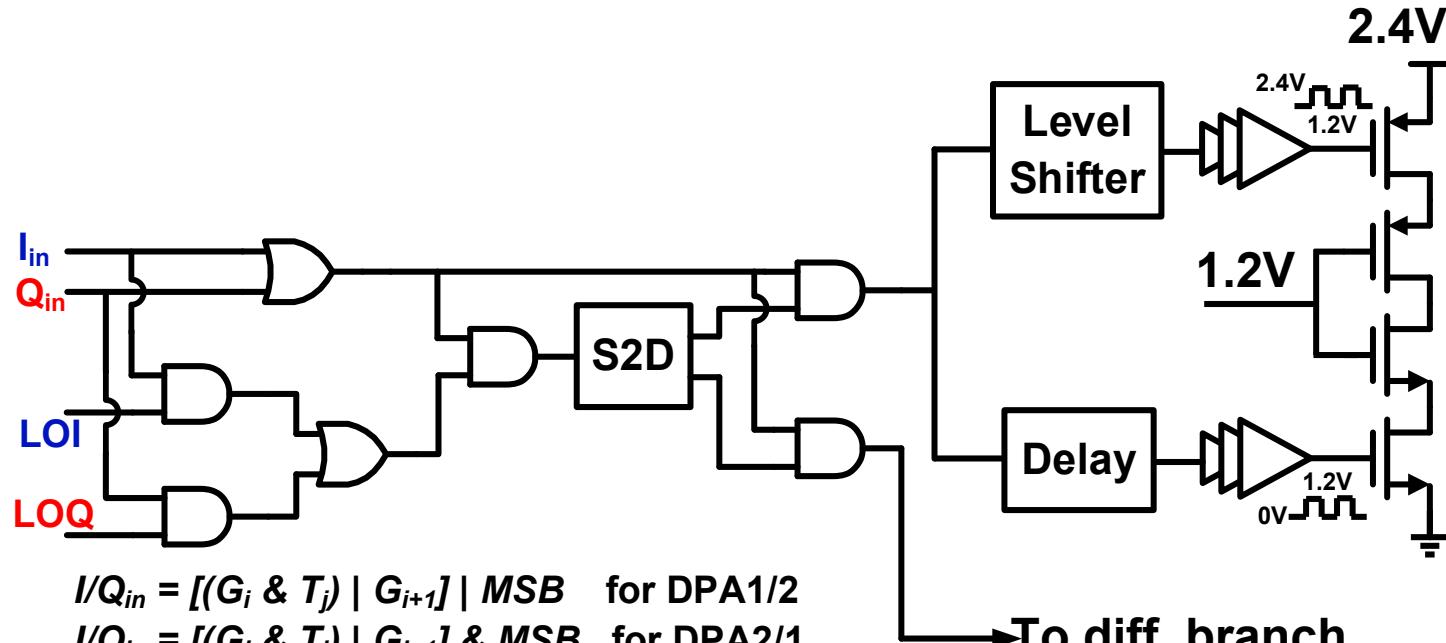


Circuit Implementation – Logic Scheme

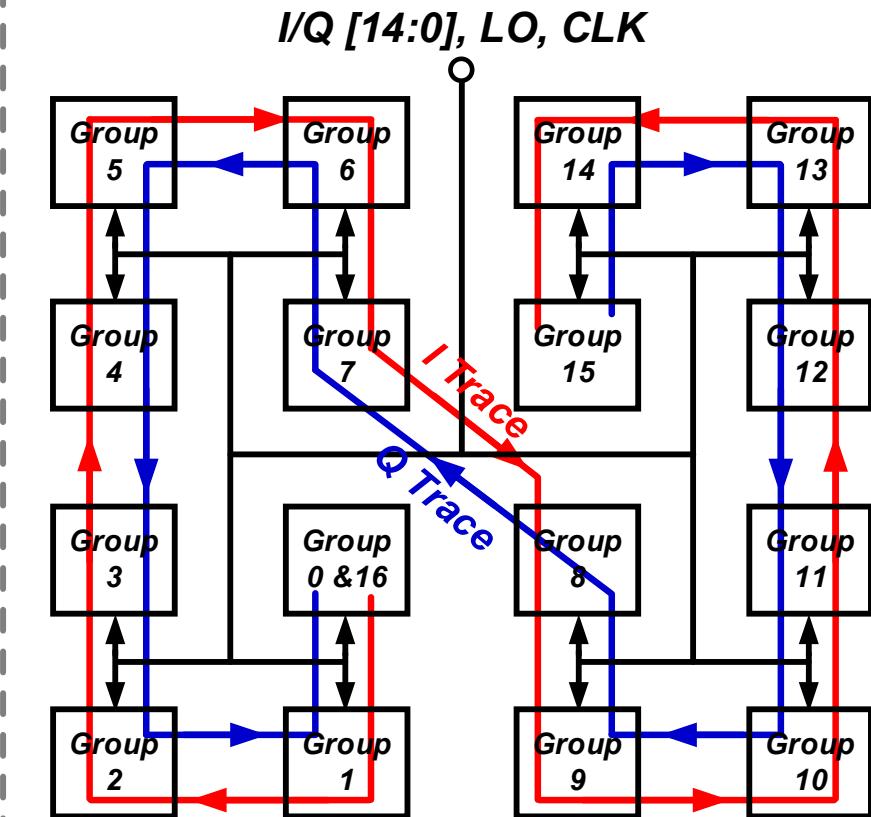


- Hybrid-coded Group #0-15: 7 unary cells (#T) and 3 binary cells (#4-5)
- Binary-coded Group #16: 4 LSB binary cells (#0-3) and 2 supplementary binary cells (#4) to avoid collision when IQ-reuse operation comes into the same group

Circuit Implementation – Unit PA & Floorplan

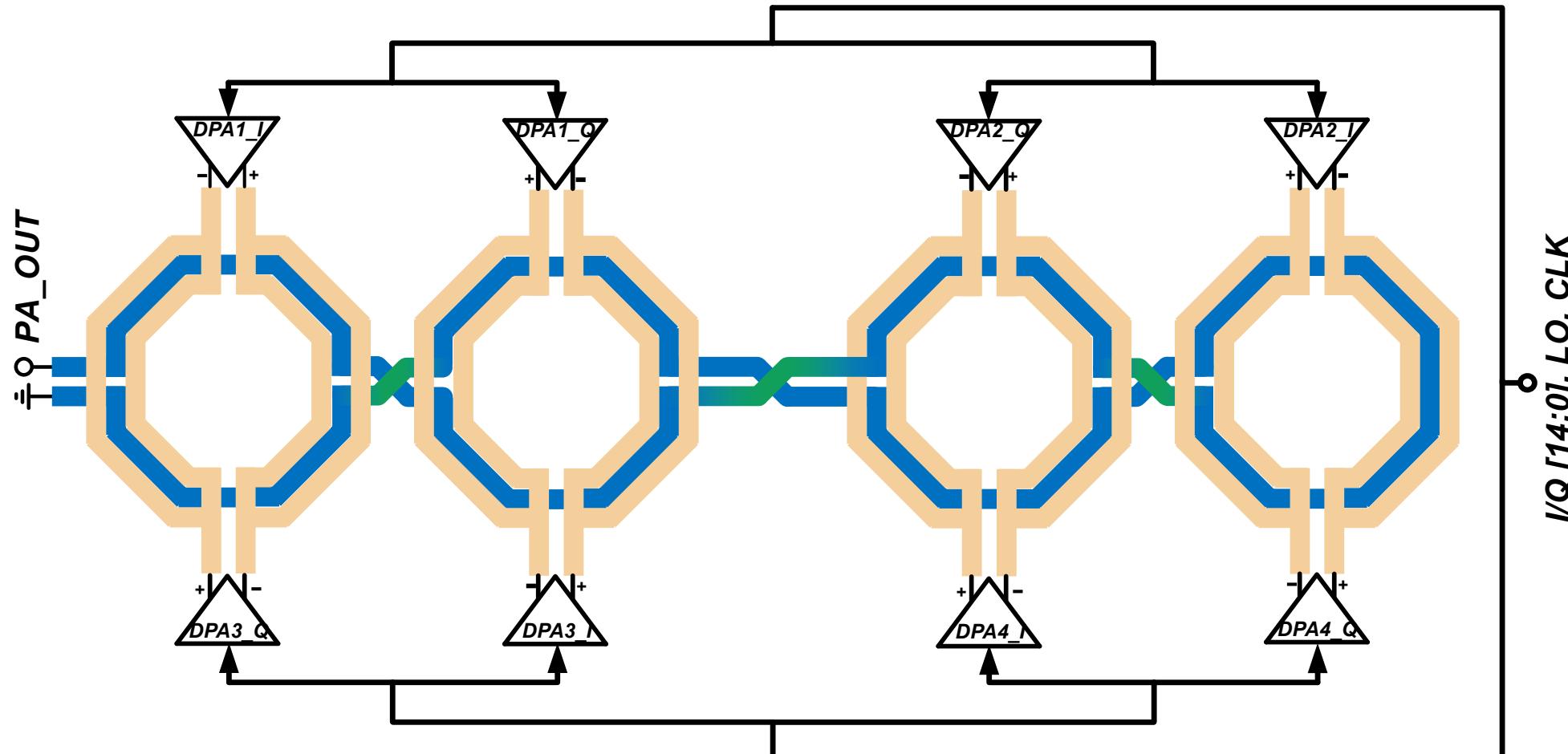


Sub-PA_I/Q Floorplan



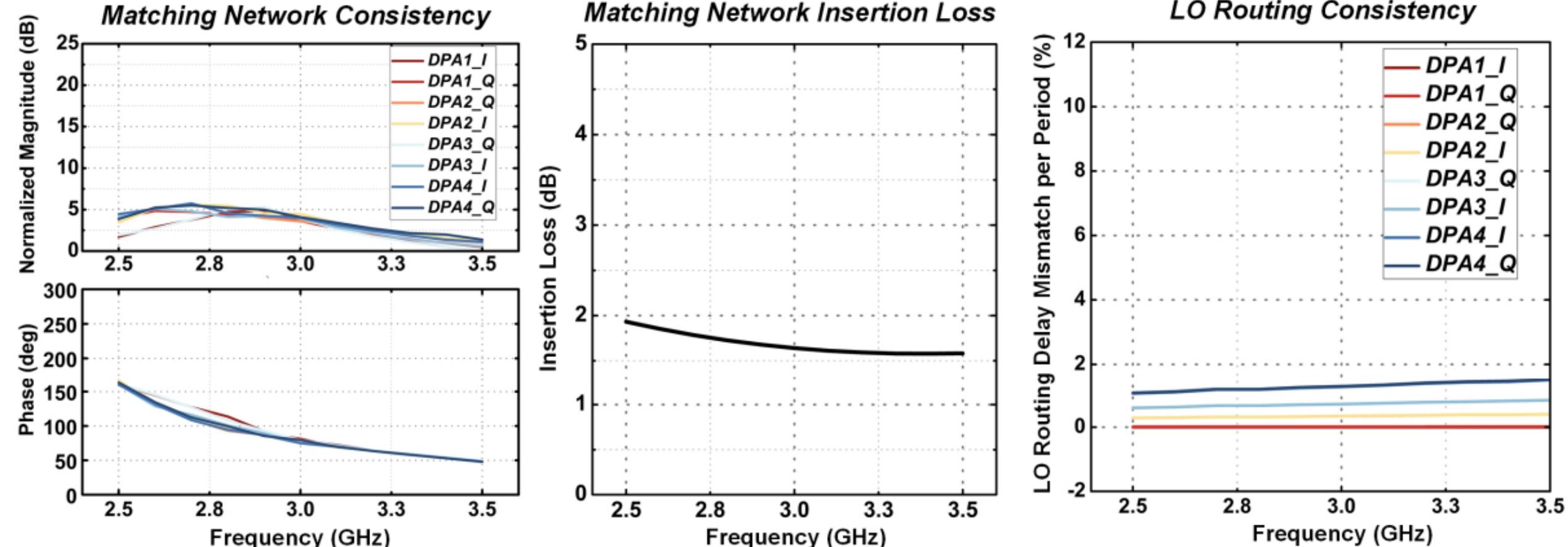
- Cascode-inverter structure for high Pout
- IQ-reuse: logic circuits to select the state (I or Q) of each unit PA
- Switching sequence traverses like snakes among Groups #0-16 to obtain center symmetry
- The I/Q traces are opposite direction to implement IQ-reuse operation

Circuit implementation – Matching Network



- Matching network consists of an 8-way differential SCT power combiner
- Each SCT connects between DPA_I and DPA_Q to avoid no-load dissipation
- Doherty operation to enhance PBO efficiency, good symmetry

Circuit implementation – Matching Network & Symmetry

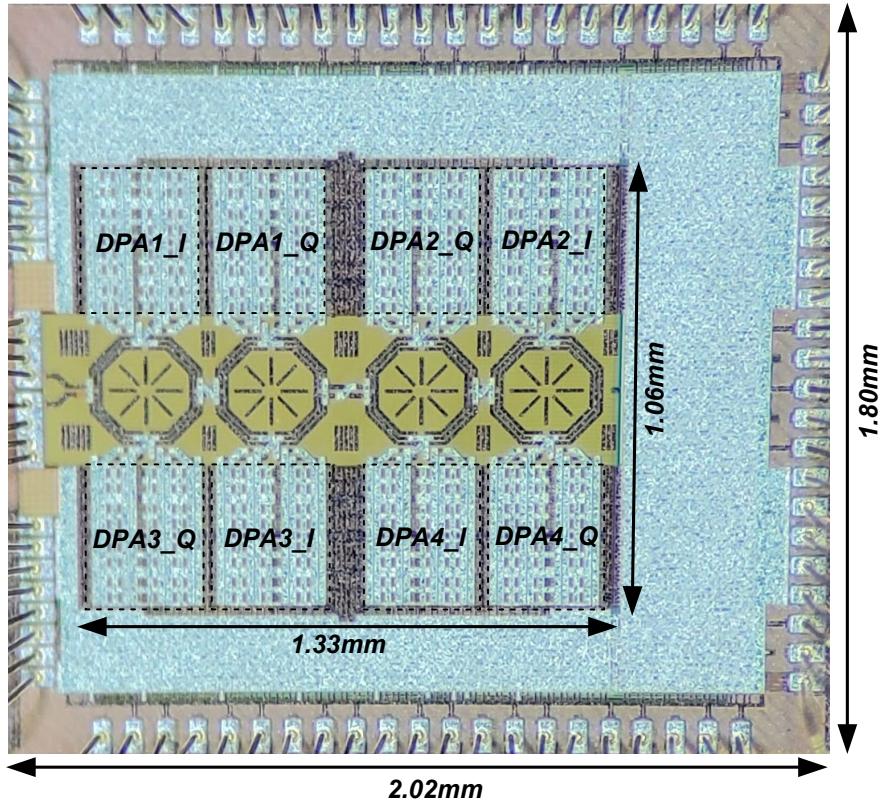


- 8-way SCT power combiner: magnitude mis. <1.2dB, phase mis. <7 degrees
- Matching network insertion loss: 1.6dB at 2.9GHz
- Simulated LO delay mismatches among DPA_I/Q of four sub-PAs are <1.5% per period over 2.5-3.5GHz

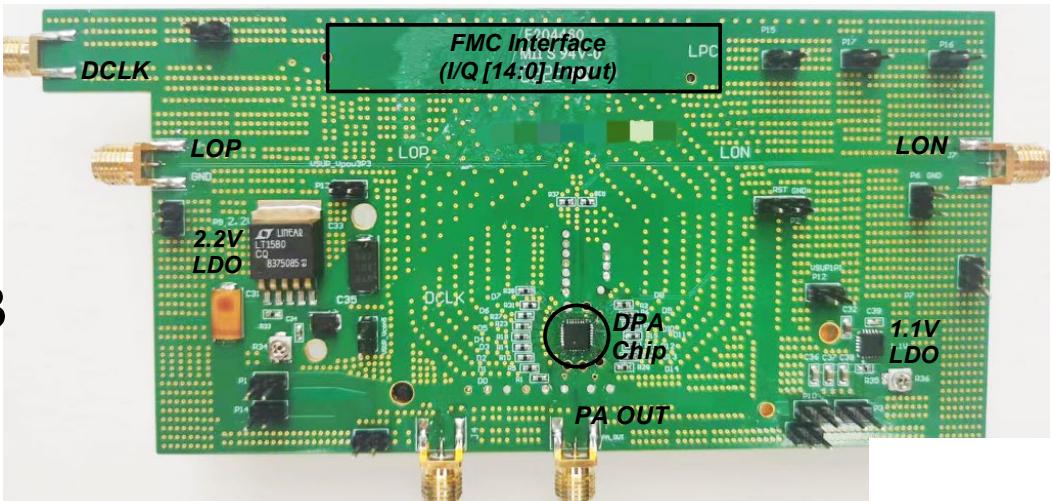
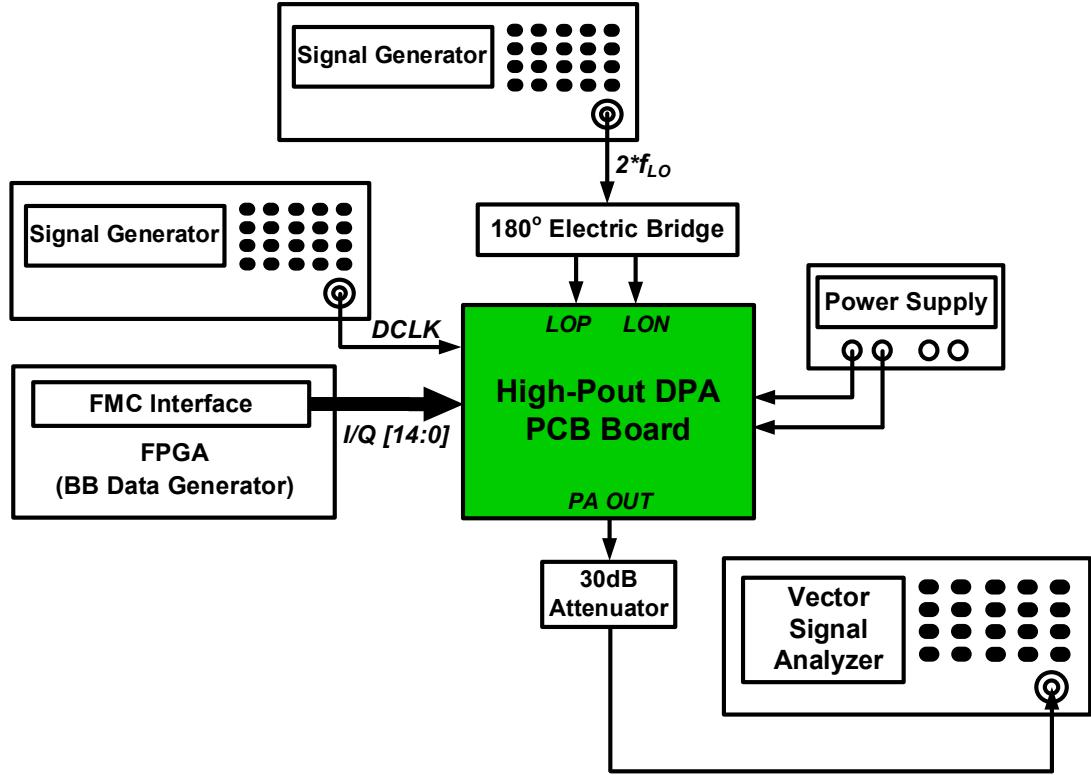
Outline

- Motivation
- Operation Principles of 8-way Differential Power Combined Quadrature DPA
- Circuit Implementation
- Measurement Results
- Conclusions

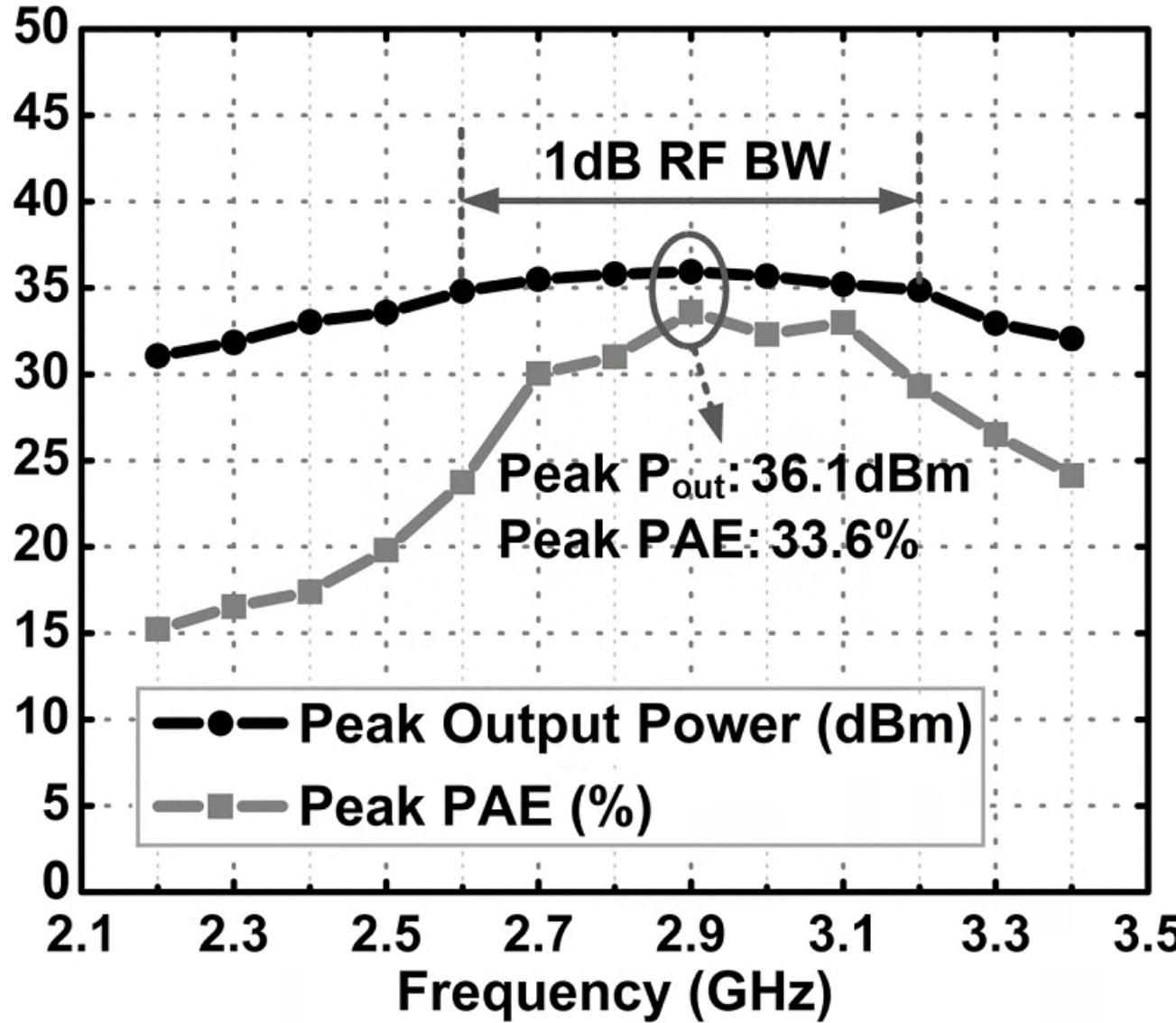
Measurement Results



- 28nm bulk CMOS
- Core area: 1.4mm²
- Dual power supplies: 2.2V & 1.1V
- 4*4mm² QFN package on FR-4 evaluation PCB
- PAE = Pout/P_{DC} (all blocks)

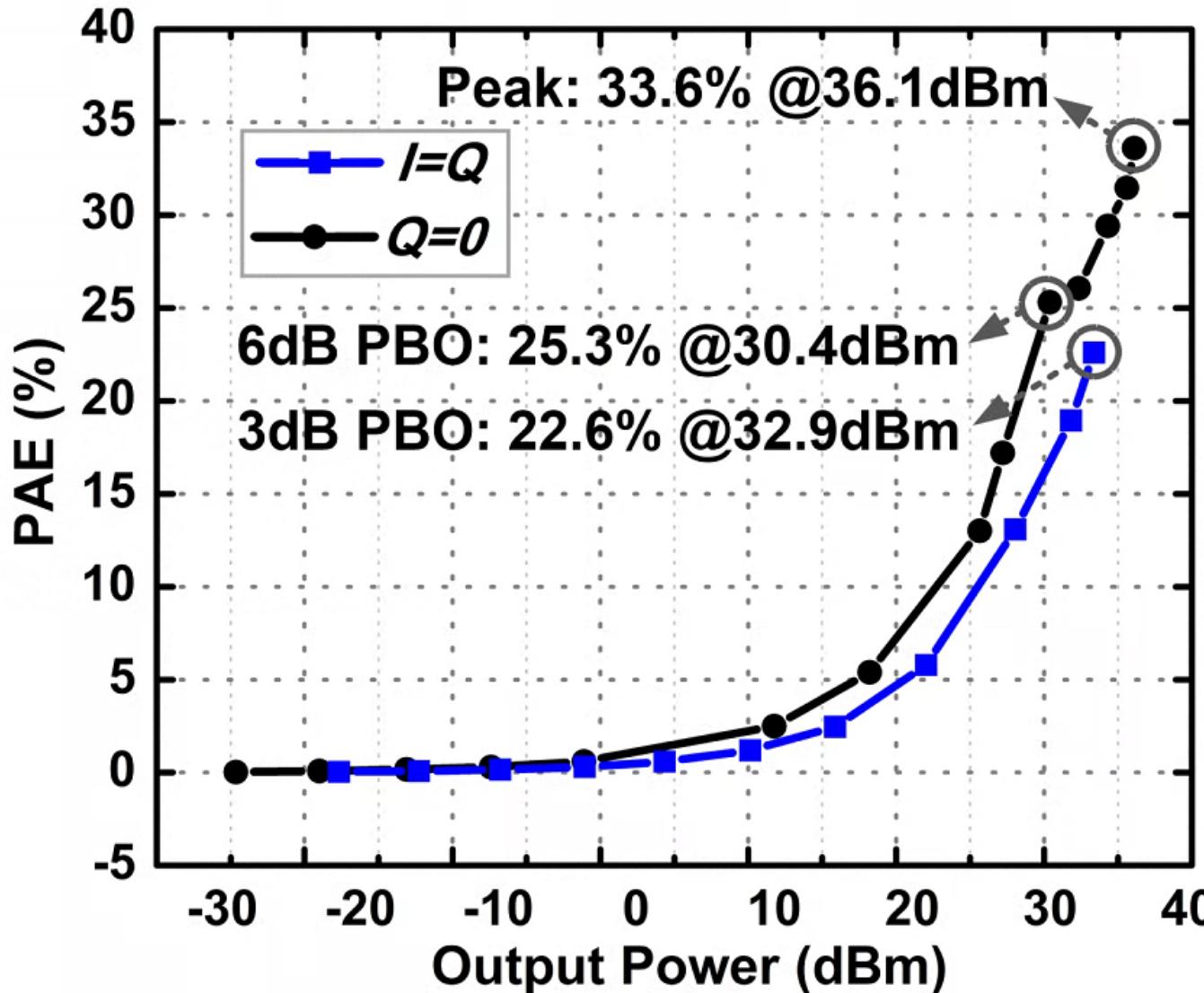


Measurement Results – CW Performance (1/2)



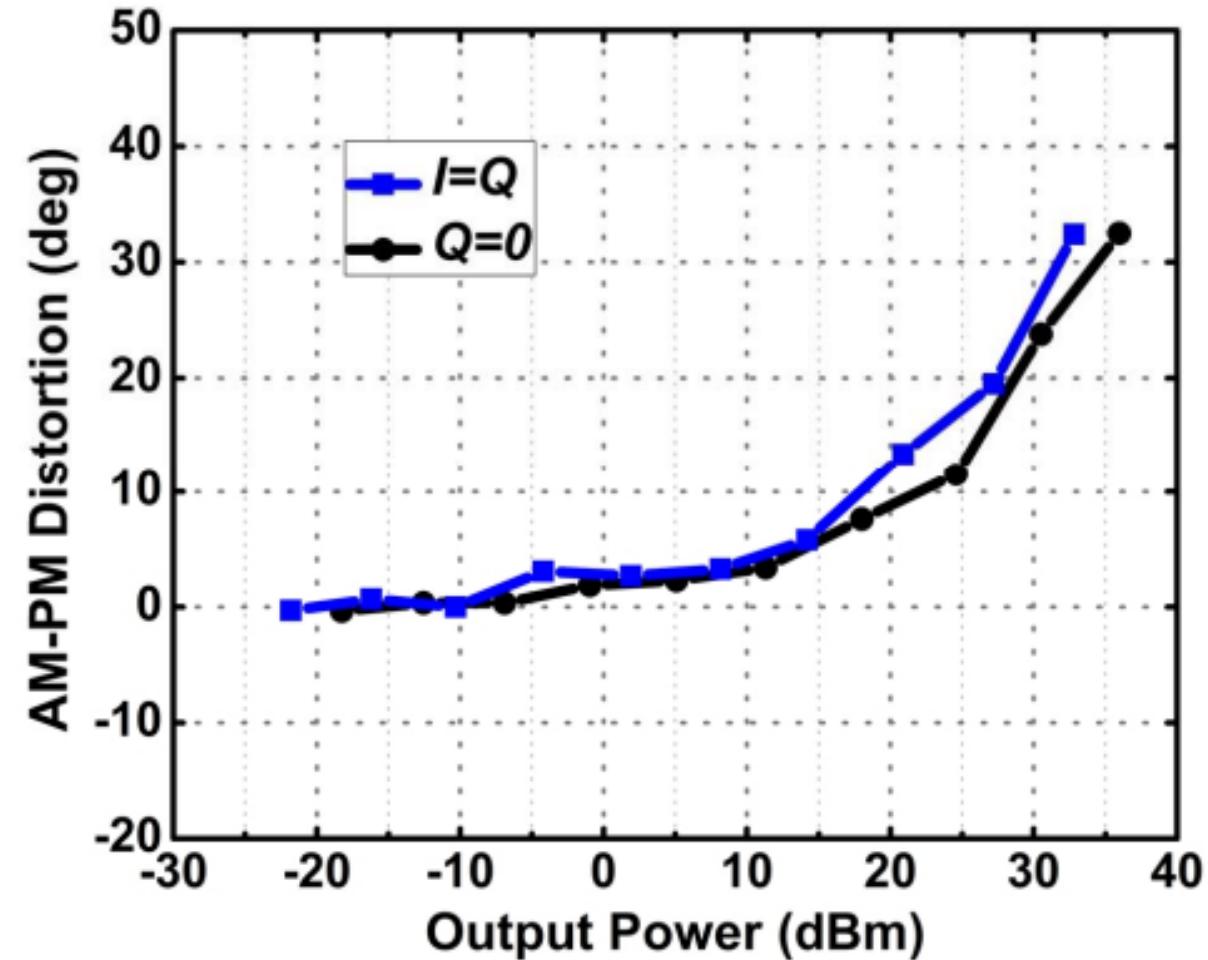
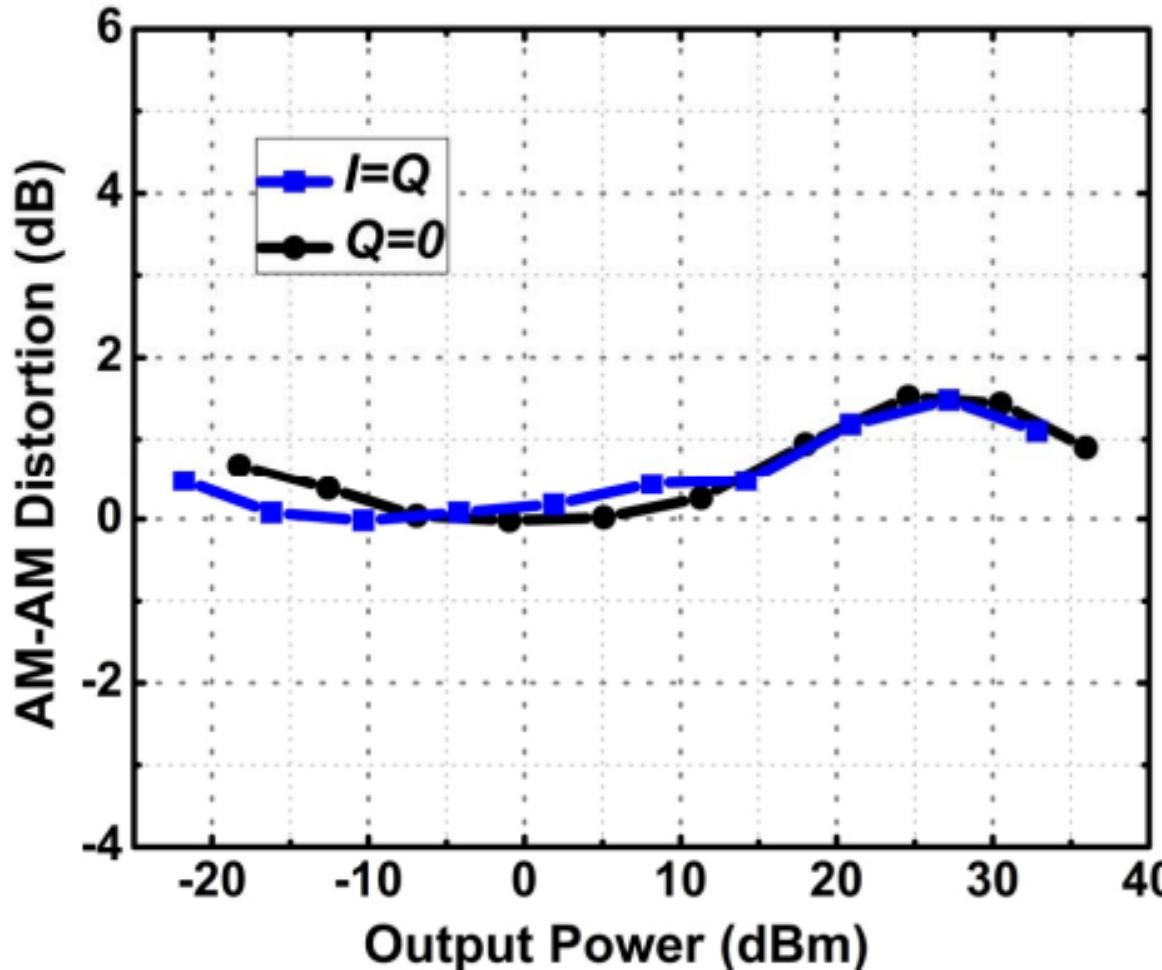
- Pout & PAE vs Frequency:
 - 36.1dBm (4.1W) peak output power with 33.6% PAE at 2.9GHz
 - 1dB RF BW of 2.6-3.2GHz
 - >30% peak PAE over 2.7-3.2GHz

Measurement Results – CW Performance (2/2)



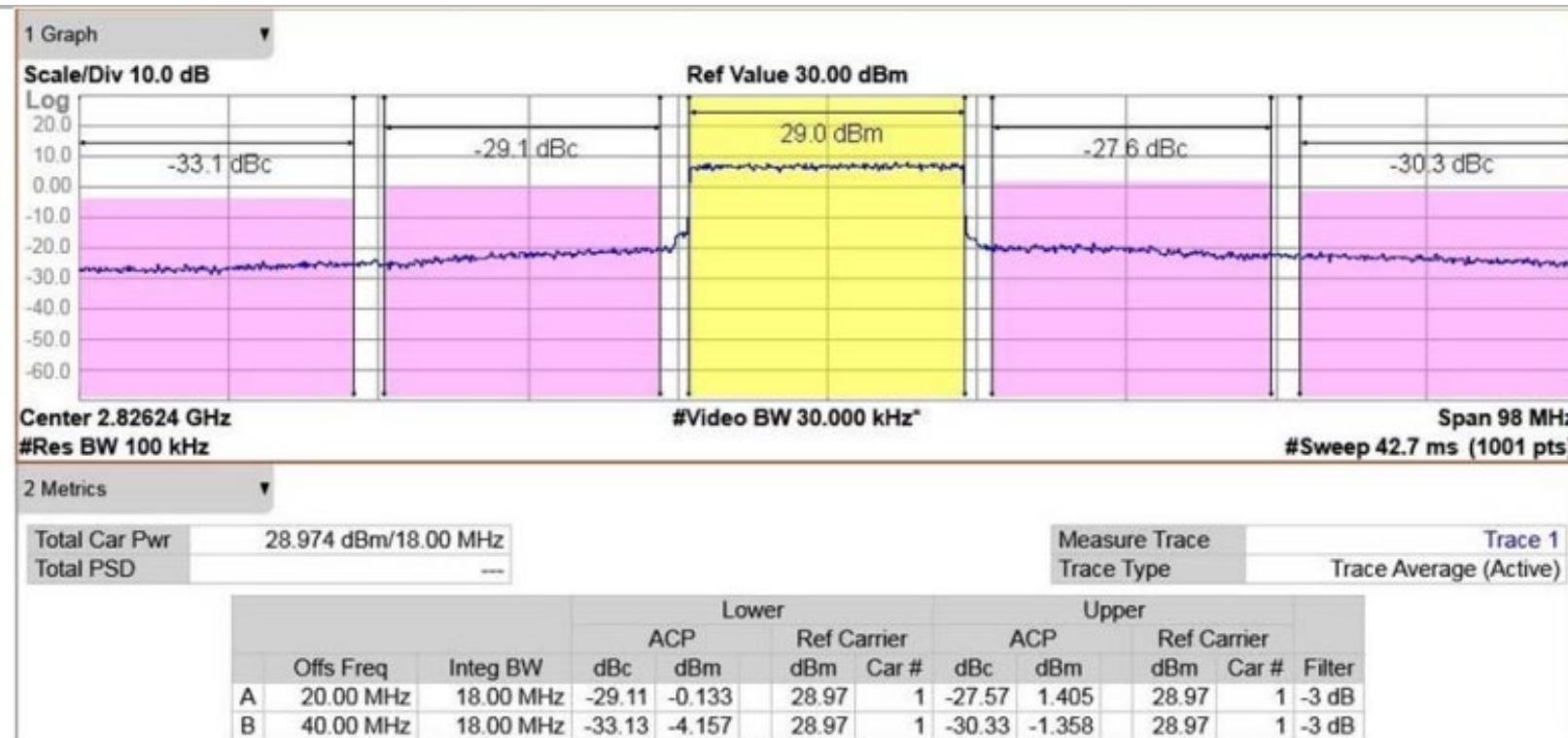
- PAE versus Pout at 2.9GHz:
 - Thanks to IQ-reuse and Doherty operations
 - 25.3% PAE at 6dB PBO
 - 22.6% PAE at 3dB PBO

Measurement Results – AM-AM & AM-PM Nonlinearity



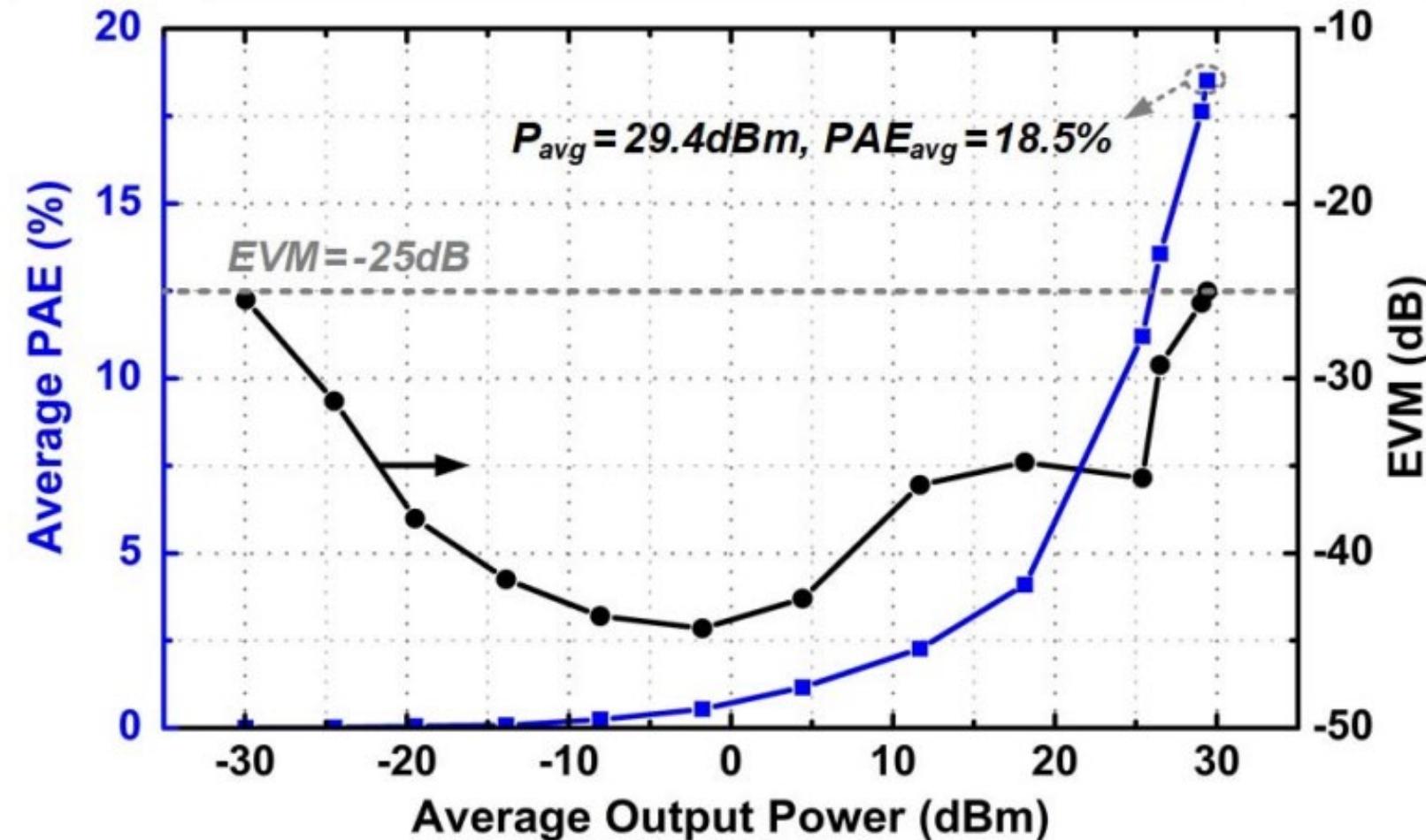
- AM-AM distortion <1.5dB, AM-PM distortion <32 degrees over 55dB output power range

Measurement Results – 20MHz 64QAM LTE Signal (1/2)



- 2-D DPD LUT to linearize AM-AM and AM-PM distortions
- 20MHz 64QAM LTE @2.83GHz:
 - Pout: 29.0dBm
 - EVM: -25.7dB

Measurement Results – 20MHz 64QAM LTE Signal (2/2)



- 29.4dBm average Pout, 18.5% average PAE at -25dB EVM limit
- ~60dB dynamic power range from -30dBm to 29.4dBm with EVM below -25dB

Outline

- Motivation
- Operation Principles of 8-way Differential Power Combined Quadrature DPA
- Circuit Implementation
- Measurement Results
- Conclusions

Comparison with Prior-Art High-Power DPAs

	This work	JSSC 2019 [3]	JSSC 2019 [4]	ISSCC 2019 [5]	JSSC 2022 [6]
Technology	28nm CMOS	65nm CMOS	28nm CMOS	65nm CMOS	40nm CMOS
Architecture	Quadrature with 8-way power combining + IQ-reuse + Doherty	Quadrature with IQ-Cell Sharing + Class-G + Merged Cell Switching	Polar/quadrature dual-mode with transformer-based load modulation	Polar with phase-interleaved multi-SHS + Class-G	Polar with reconfigurable power combining transformer
Voltage (V)	1.1/2.2	1.2/2.5	1.1/2.2	2.4/3.6	1.1/2.5
Frequency (GHz)	2.9	2.2	2.4	1.9	2
Peak Pout (dBm)	36.1	30.1	28.8 [†]	30	32.67
Peak PAE (%)	33.6	37.0	30.8 [†]	45.9 (DE)	35.5
Modulation Signal	20MHz 64QAM LTE	20MHz 64QAM Wi-Fi	20MHz 64QAM Wi-Fi	5MHz 16QAM	25MHz 256QAM
Pavg (dBm)	29.4	19.5	23.35 [†]	22.8	25.48
Average PAE (%)	18.5	14.7	23.2 [†]	31.4 (DE)	18.82
EVM (dB)	-25	-40.7	-25.4 [†]	-24.7	-32.11
Die size (mm ²)	3.6 (1.4*)	3	0.56*	7.2	2.6 (0.99*)

*Core size † Measured results in polar mode

Conclusions

- An 8-way differential power combined quadrature DPA with IQ-reuse and Doherty techniques is presented
- A symmetrical 8-way serial-combined transformer power combiner for higher Pout, efficiency enhancement and wide frequency coverage
- This quadrature DPA achieves:
 - 36.1dBm peak Pout, 33.6% peak PAE in 28nm bulk CMOS
 - 12 efficiency peaks on the I/Q complex plane
 - 29.4dBm average Pout with 18.5% average PAE for 20MHz 64QAM LTE
 - 15b resolution, ~60dB dynamic power range

Acknowledgements

- We would like to thank group members of Fudan WiCAS lab for technical discussions and supports.
- We would like to thank the State Key Laboratory of Integrated Chips and Systems at Fudan University for measurement supports.

A 19.7-to-43.8GHz Power Amplifier with Broadband Linearization Technique in 28nm Bulk CMOS

Weisen Zeng¹, Li Gao¹, Ningzheng Sun¹, Hongtao Xu²,
Quan Xue¹, Xiuyin Zhang¹

¹South China University of Technology, Guangzhou, China

²Fudan University, Shanghai, China

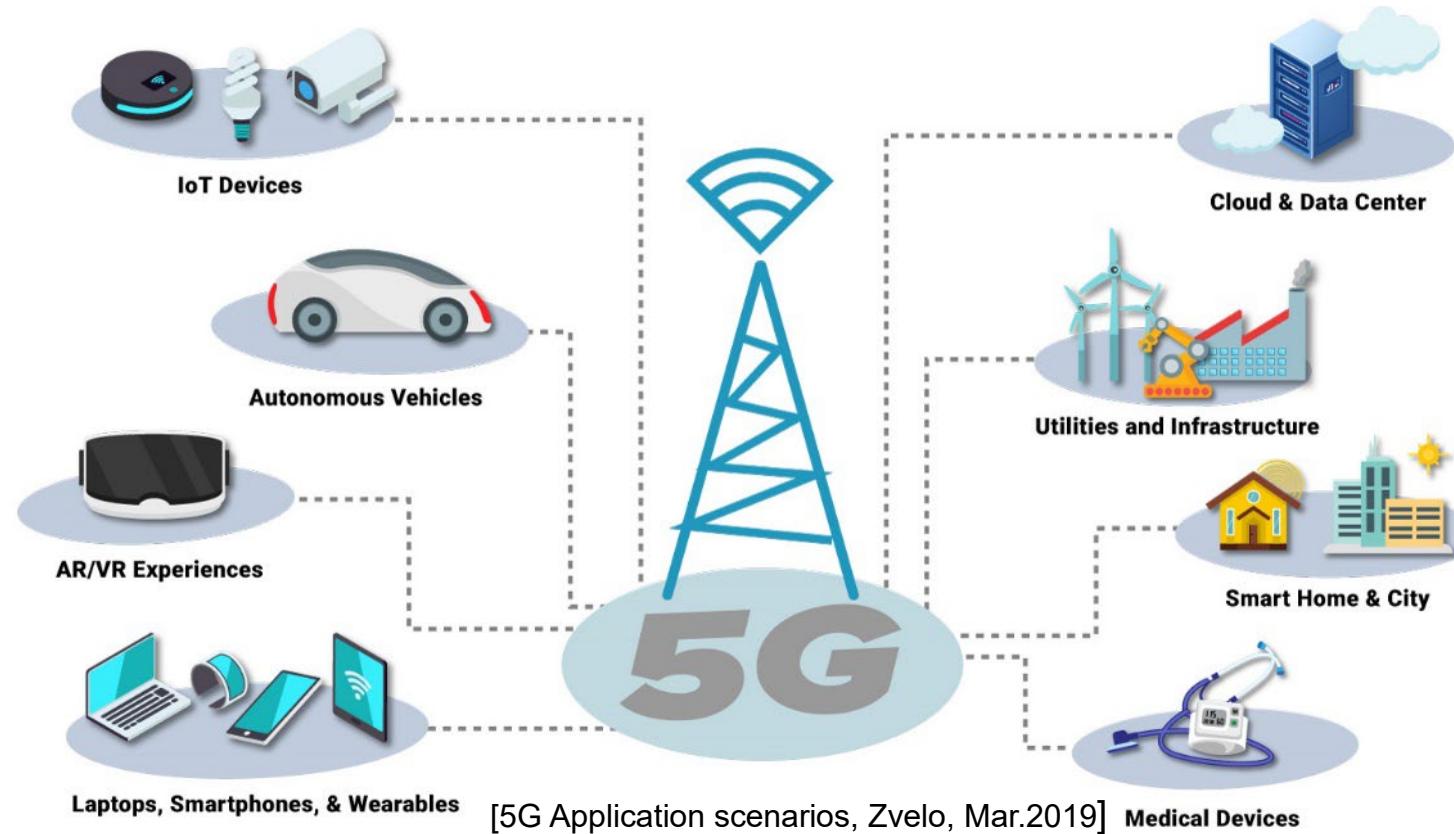


Outline

- Introduction
- ATCR-based matching technique
- Broadband Linearization technique
- Prototype Implementation
- Measurements
- Conclusion

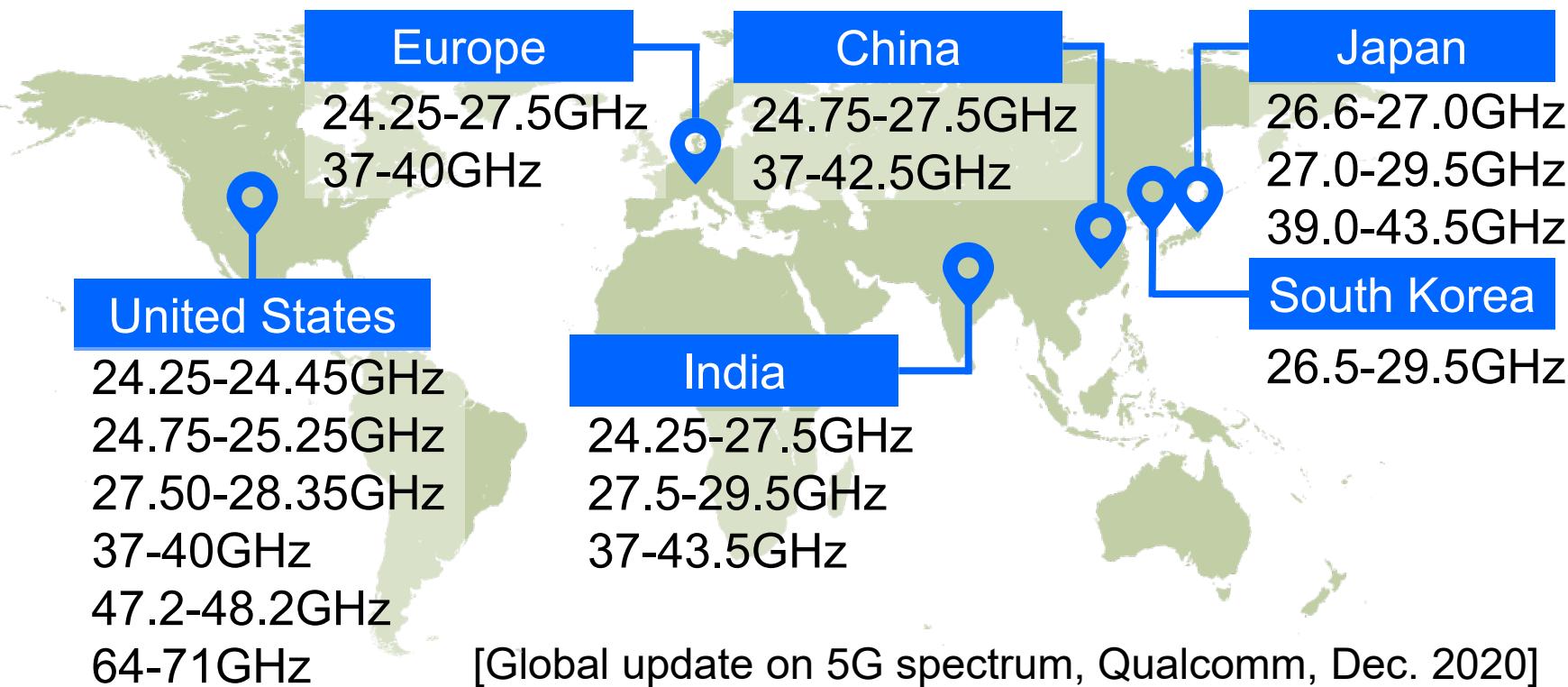
Introduction

5G Connections & Devices



- Increasing demand for mm-wave 5G for new applications
- Ultra HD video, AR/VR, Self-driving car, Wireless backhaul

Spectrum challenges of mm-wave 5G PAs

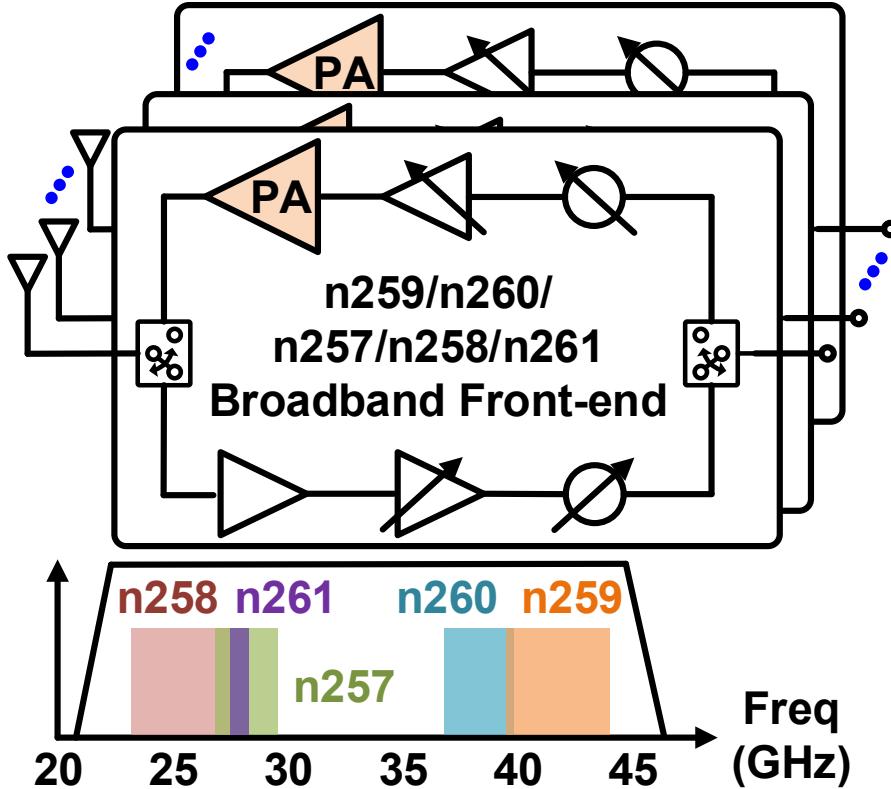


3GPP TS 38.104
operating bands in FR2

Band	Frequency
n257	26.5 – 29.5 GHz
n258	24.25 – 27.5 GHz
n259	39.5 – 43.5 GHz
n260	37–40 GHz
n261	27.5 – 28.35 GHz

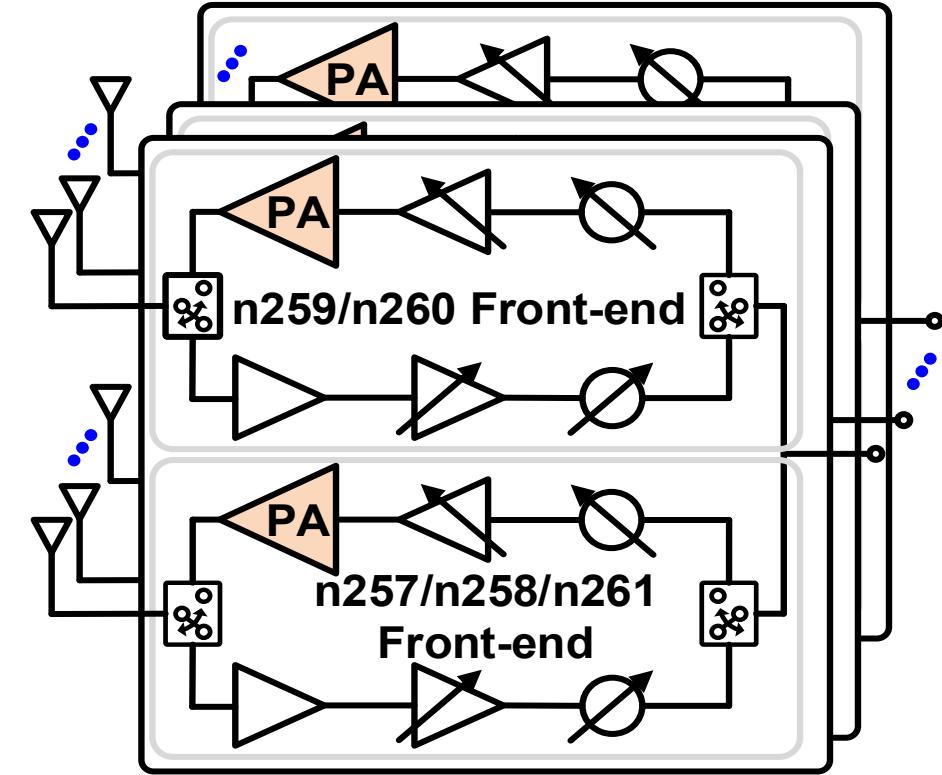
- Different countries adopt various FR2 bands for 5G networks
- Broad and discontinuous bands block international roaming

Potential solutions: broadband or multi-band PAs



Broadband system

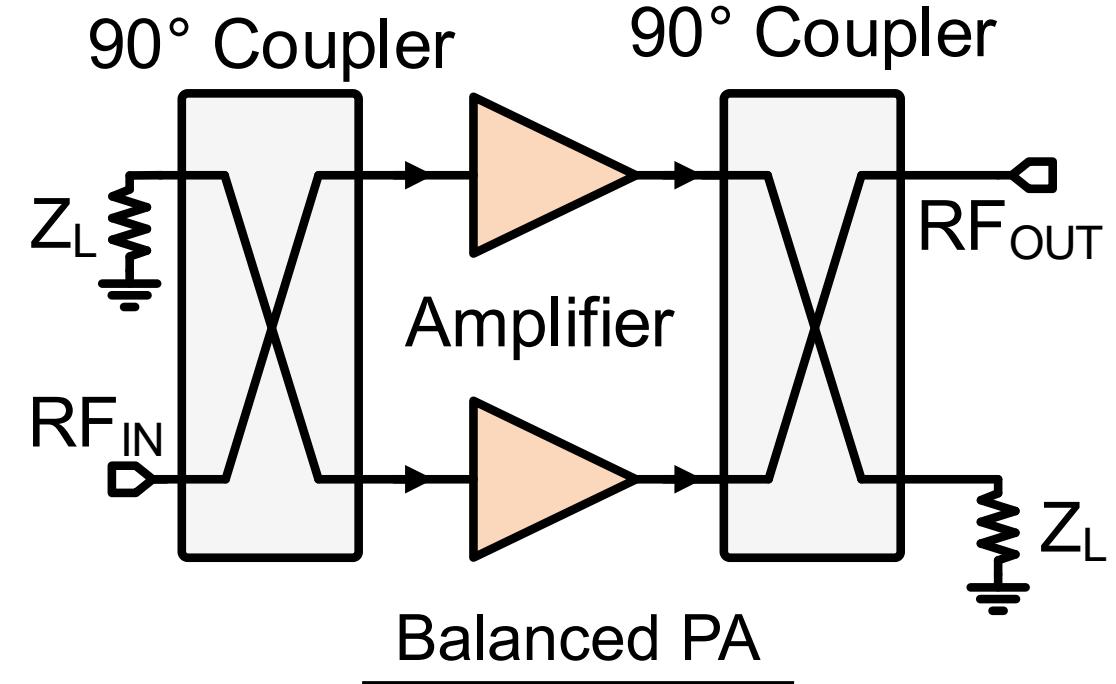
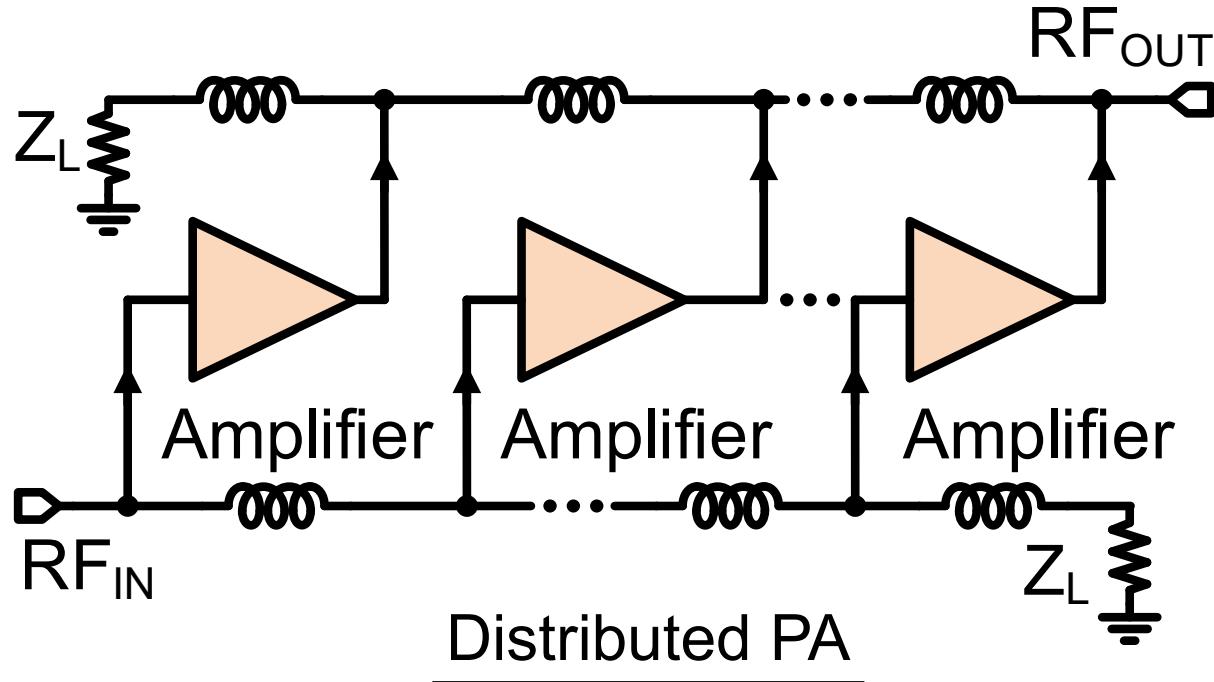
- Compact, low-cost
- Low complexity



Multi-band parallel system

- Better performance
- Bulky, high-cost

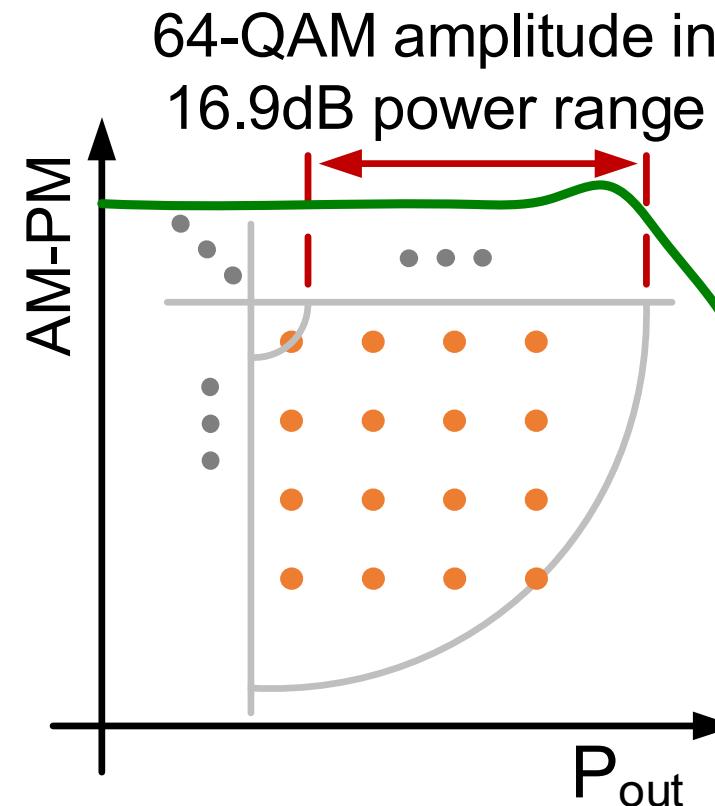
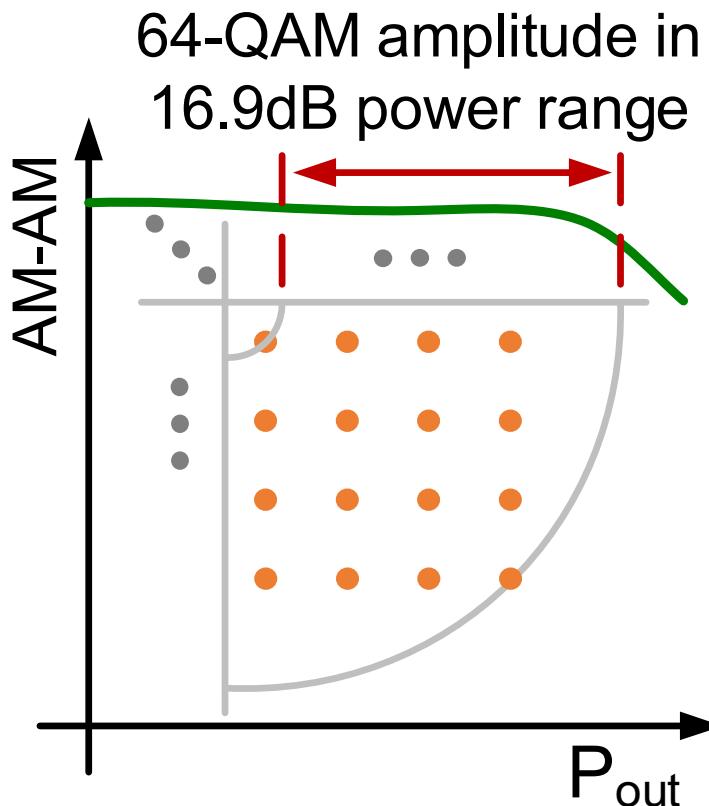
Conventional broadband techniques



😢 Large operating bandwidth amplifier with limited power efficiency

😢 Broadband 90° hybrids are bulky and lossy for on-chip implementation

Linearity challenges of mm-wave 5G PAs

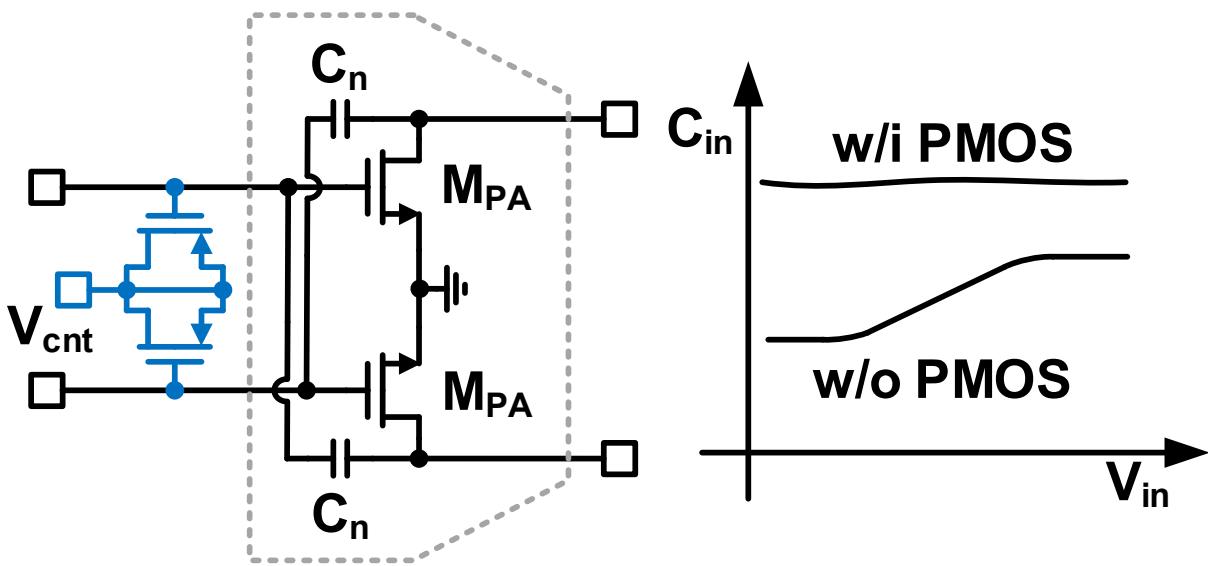


3GPP TS 38.104 EVM requirements

Band	Required EVM	
QPSK	17.5%	-15.1dB
16QAM	12.5%	-18.1dB
64QAM	8%	-21.9dB
256QAM	3.5%	-29.1dB

- High-order QAM and OFDM are used in 5G systems
- Stringent requirements on PA linearity

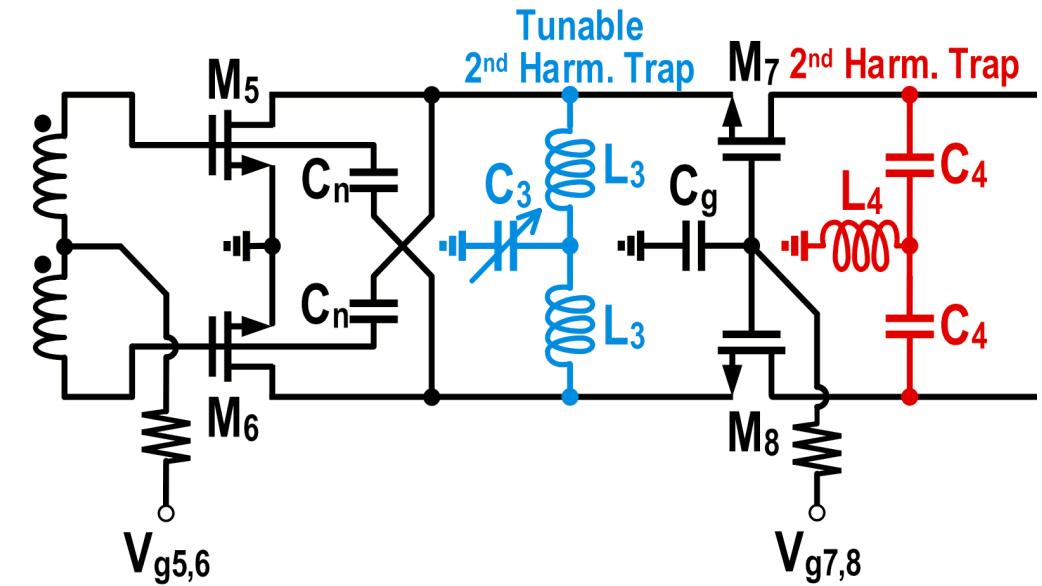
Conventional linearization techniques



[M. Vigilante *et al.*, JSSC, May 2018]

- **PMOS-based compensation**

:(Gain and efficiency reduction due to low Q value of PMOS-based capacitance



[Y. Yi *et al.*, JSSC, Sept. 2022]

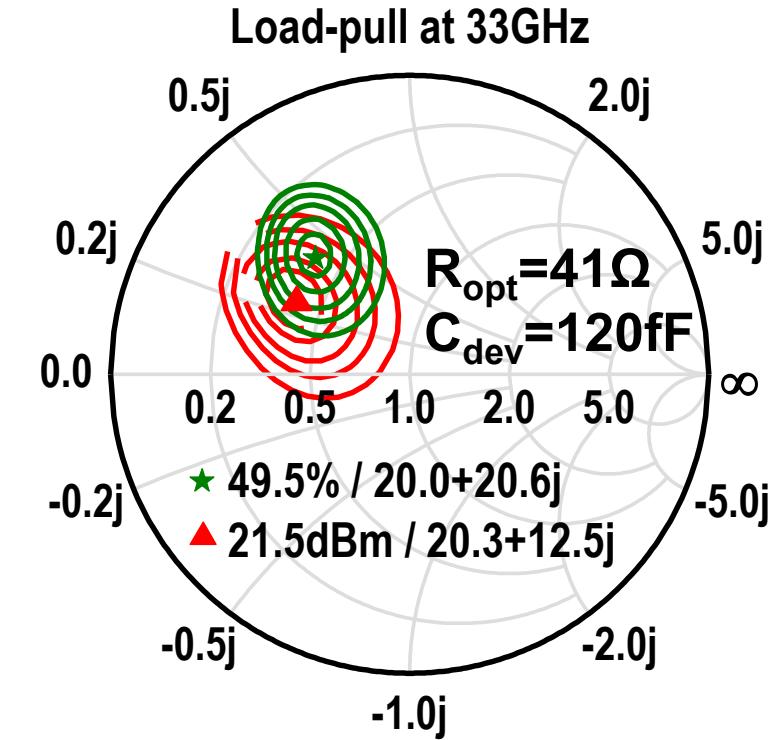
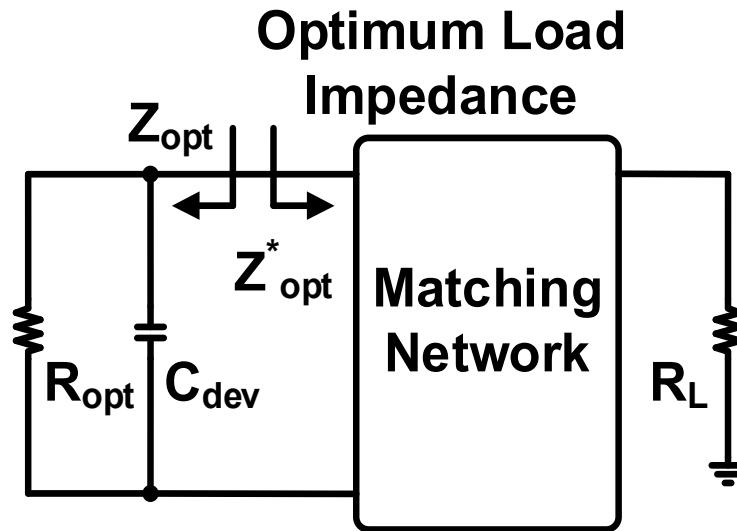
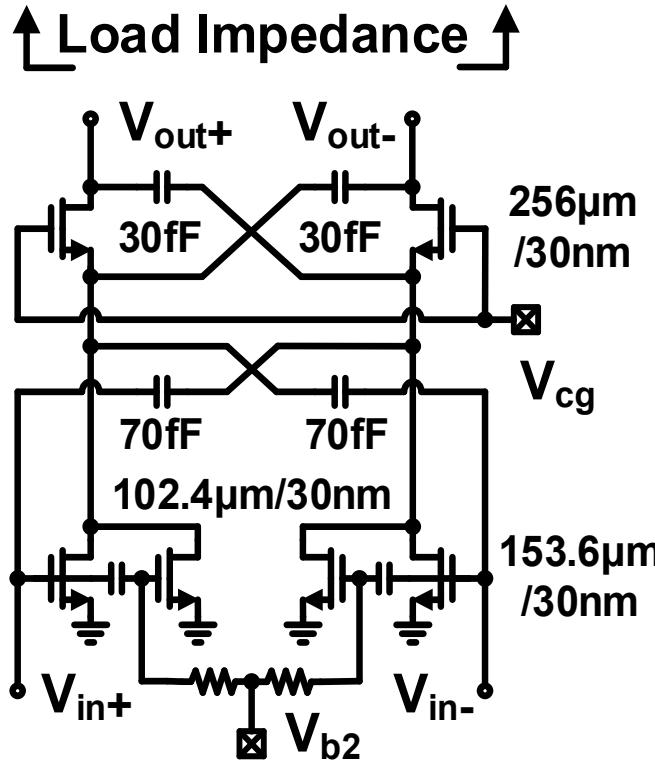
- **2nd Harmonic Trap**

:(Narrowband, not suitable for broadband

Outline

- Introduction
- ATCR-based matching technique
- Broadband Linearization technique
- Prototype Implementation
- Measurements
- Conclusion

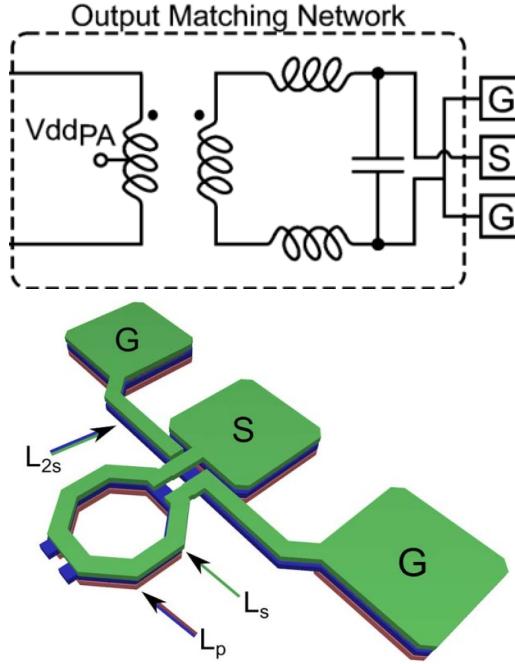
Maximize the Pout and PAE of broadband PA



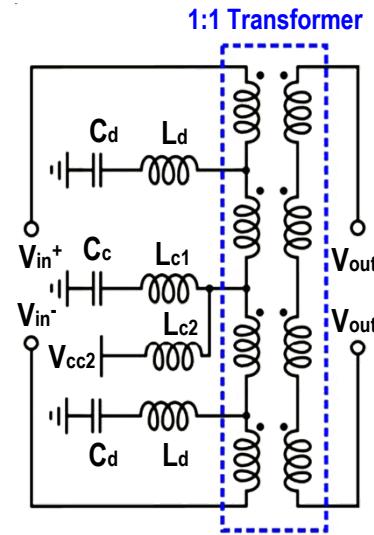
- Using load pull for optimum load impedance
- The R_{opt} and C_{dev} can be assumed as frequency independent
- Matching network transforms optimum impedance to the load

[S. Cripps, RF Power Amplifiers for Wireless Communications 2nd ed]

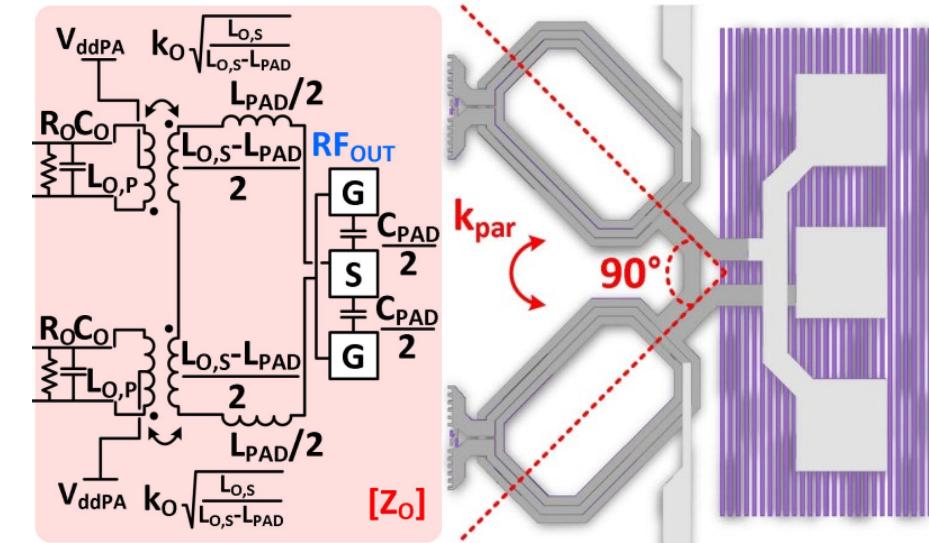
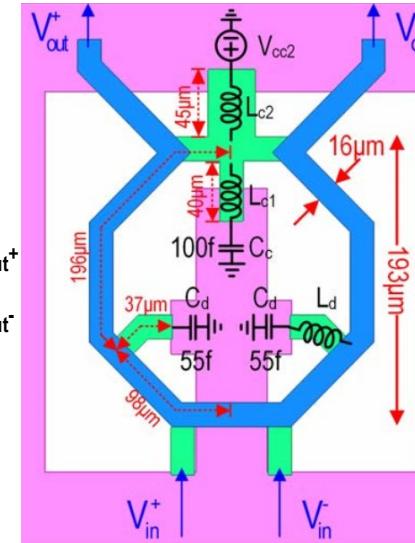
Transformer-based broadband matching technique



[M. Bassi *et al.*, JSSC, July 2015]



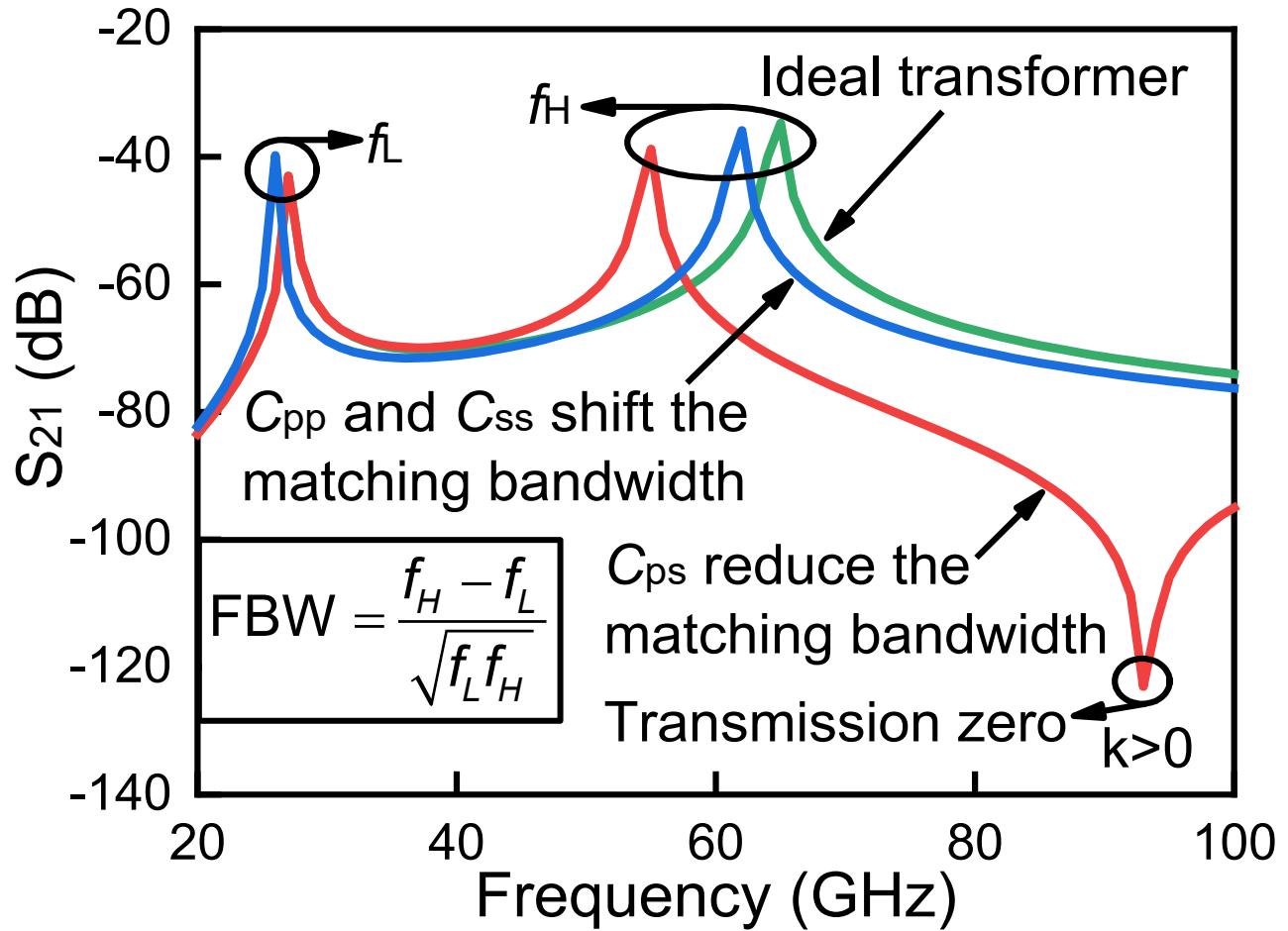
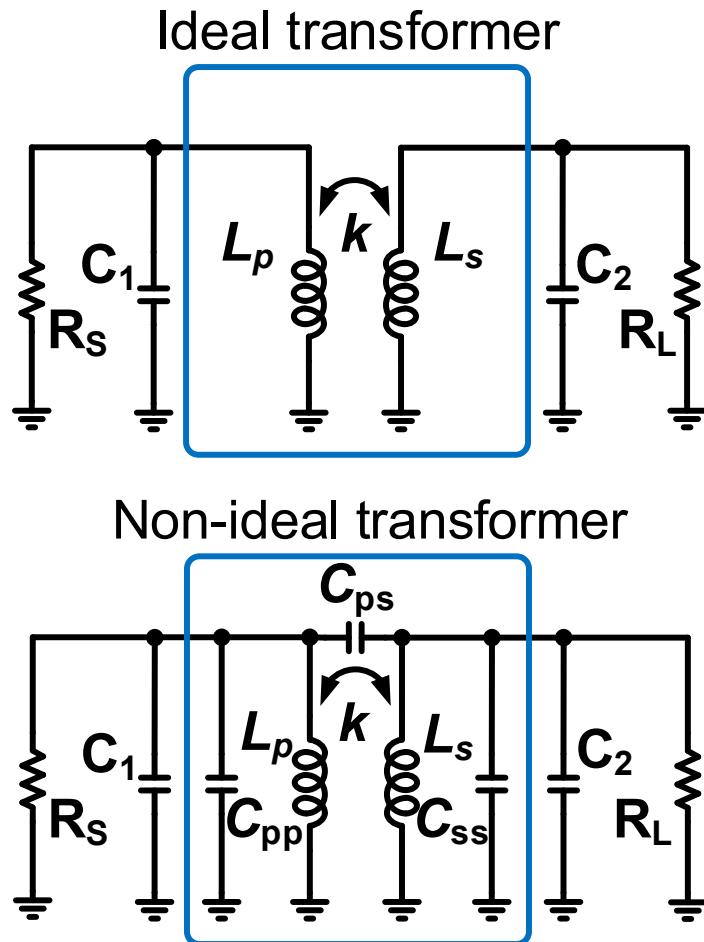
[T. Li *et al.*, ISSCC 2018]



[M. Vigilante *et al.*, JSSC, May 2018]

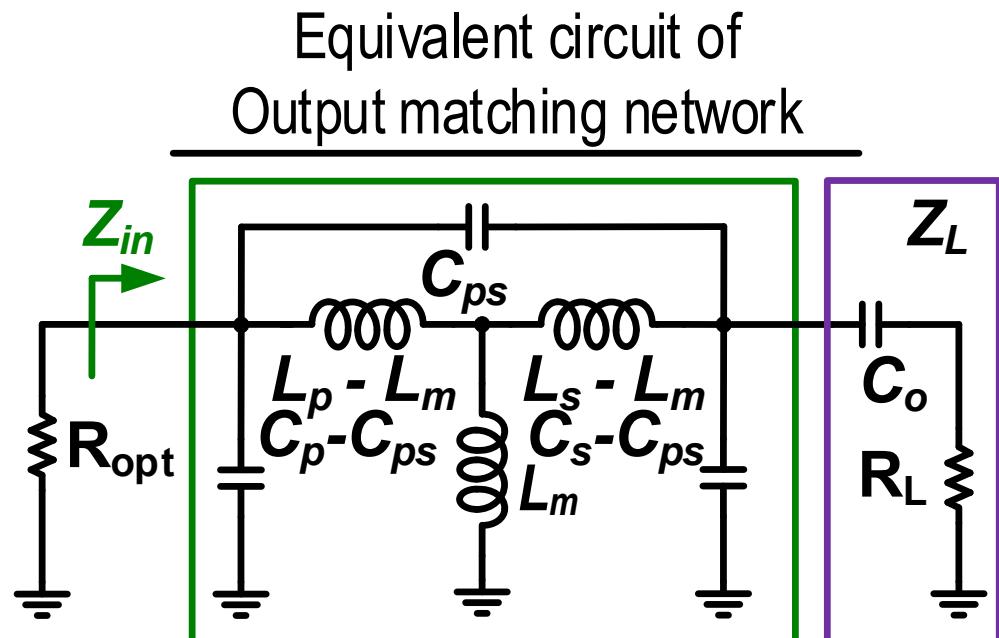
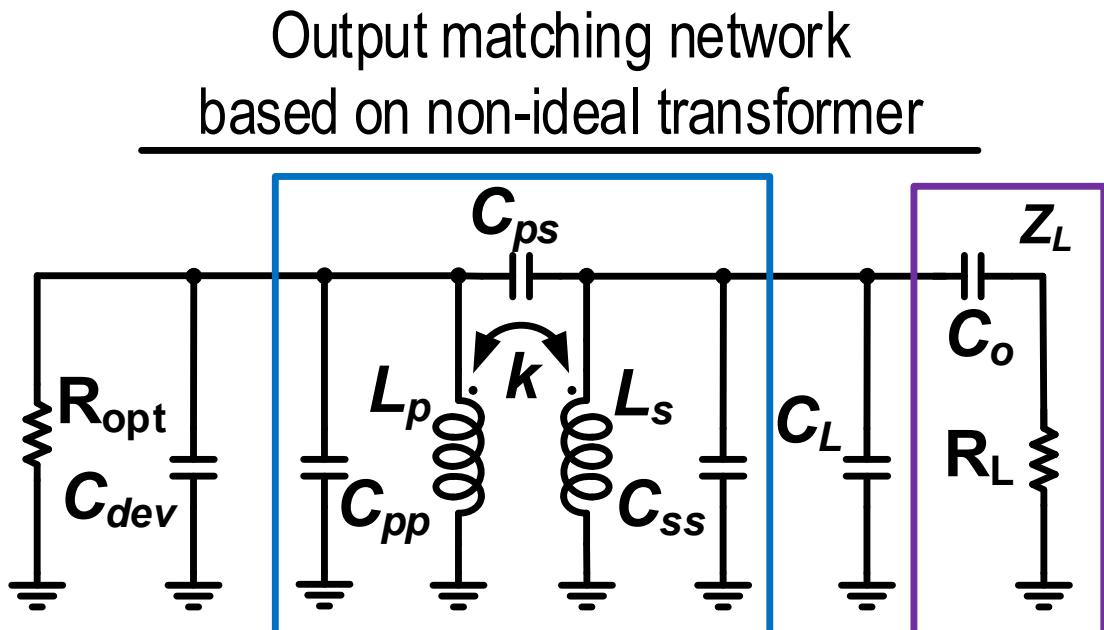
- Widely used in mm-wave broadband PAs
- Simple lumped element model is often helpful in primary design

Parasitic effect impact on transformer



■ Parasitic effect reduces matching bandwidth of transformer

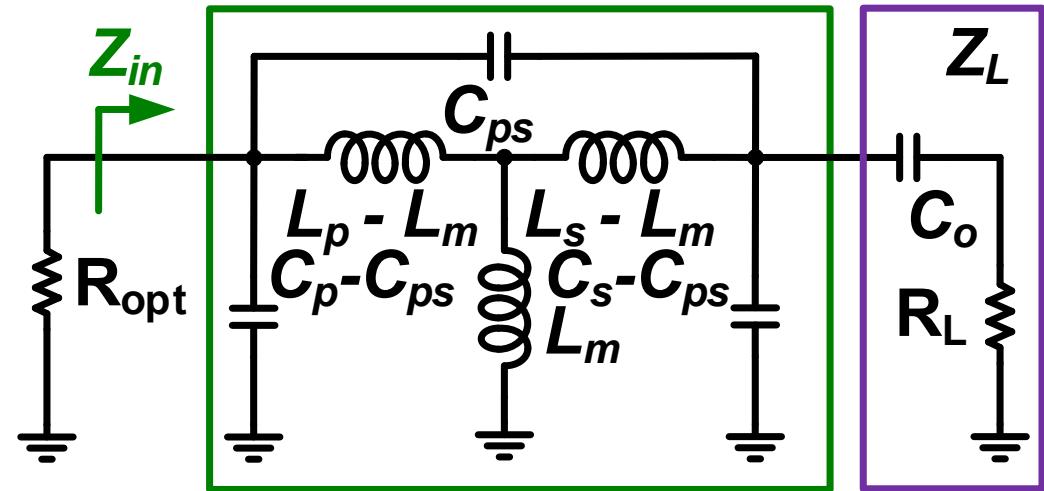
ATCR-based matching technique



- Capacitive load is used to further broaden the matching bandwidth
- Both magnetic coupling and electric coupling are considered
- C_{dev} , C_L , C_{pp} and C_{ss} can be absorbed into ATCR equivalent circuit

ATCR-based matching technique

ATCR-based Output
matching network



Y matrix can be derived as

$$[Y] = \begin{bmatrix} j\omega C_p + \frac{1}{j\omega L_p(1-k^2)} & -j\omega C_{ps} + \frac{1}{j\omega L_m(1-1/k^2)} \\ -j\omega C_{ps} + \frac{1}{j\omega L_m(1-1/k^2)} & j\omega C_s + \frac{1}{j\omega L_s(1-k^2)} \end{bmatrix}$$

Resonant frequency and transmission zero

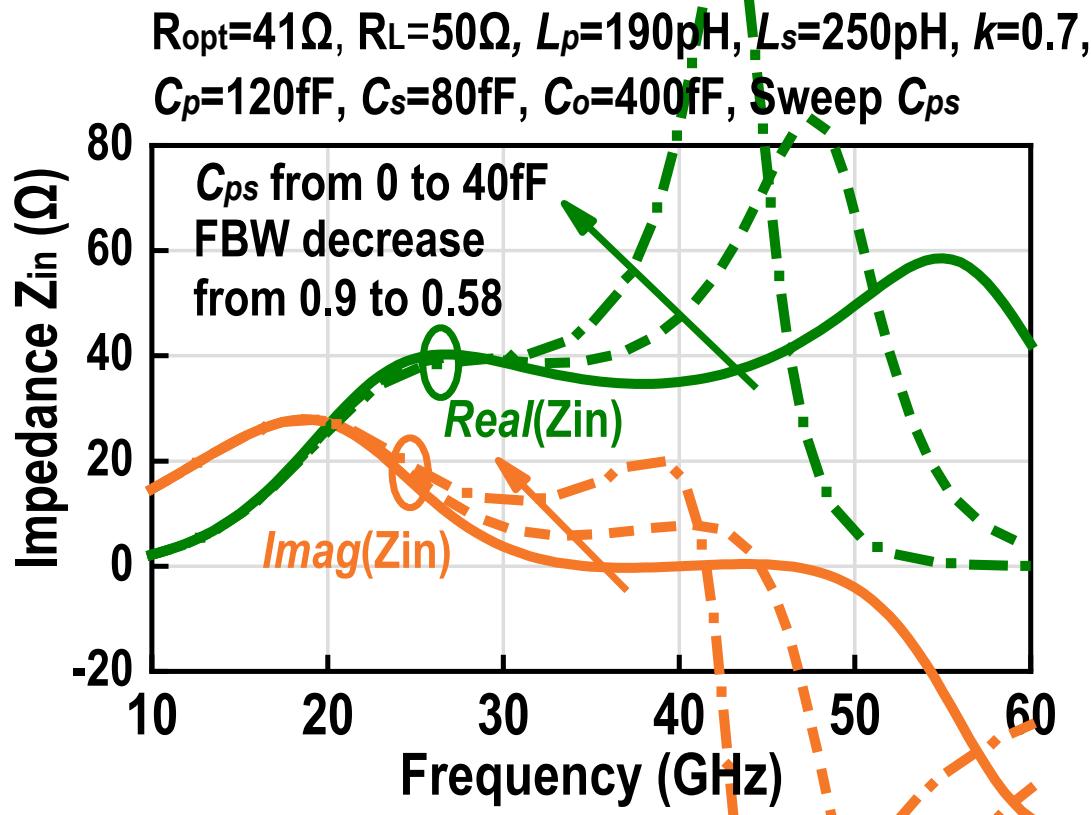
$$\Psi_A = 2(L_p C_p L_s C_s - L_m^2 C_p C_s - L_p L_s C_{ps}^2 + L_m^2 C_{ps}^2)$$

$$\Psi_B = (L_p C_p + L_s C_s - 2L_m C_{ps}), \quad \Psi_c = \sqrt{\Psi_B^2 - 2\Psi_A}$$

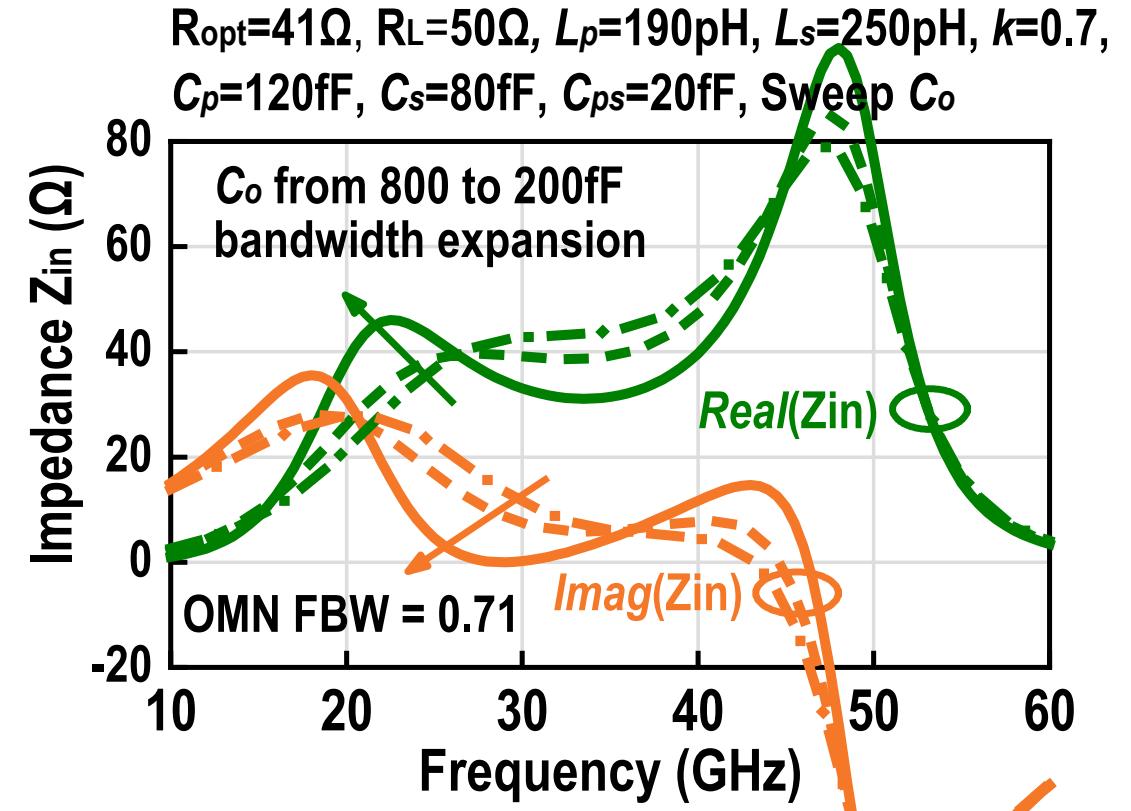
$$\omega_{p1} = \sqrt{\frac{\Psi_B - \Psi_c}{\Psi_A}}, \quad \omega_{p2} = \sqrt{\frac{\Psi_B + \Psi_c}{\Psi_A}}, \quad \omega_z = \sqrt{\frac{k^2}{L_m C_{ps}(1-k^2)}}$$

■ Two resonant frequency and one transmission zero can be calculated

ATCR-based matching technique



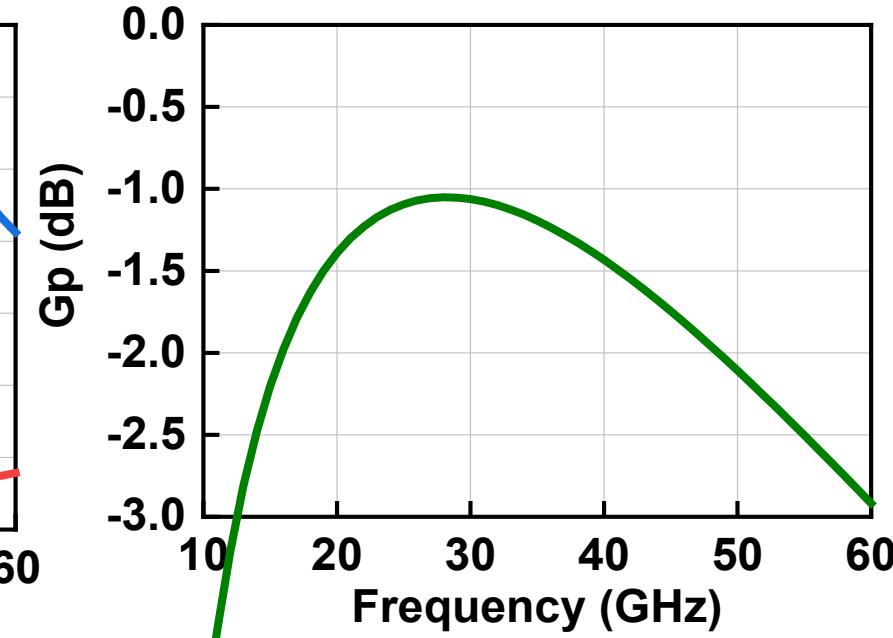
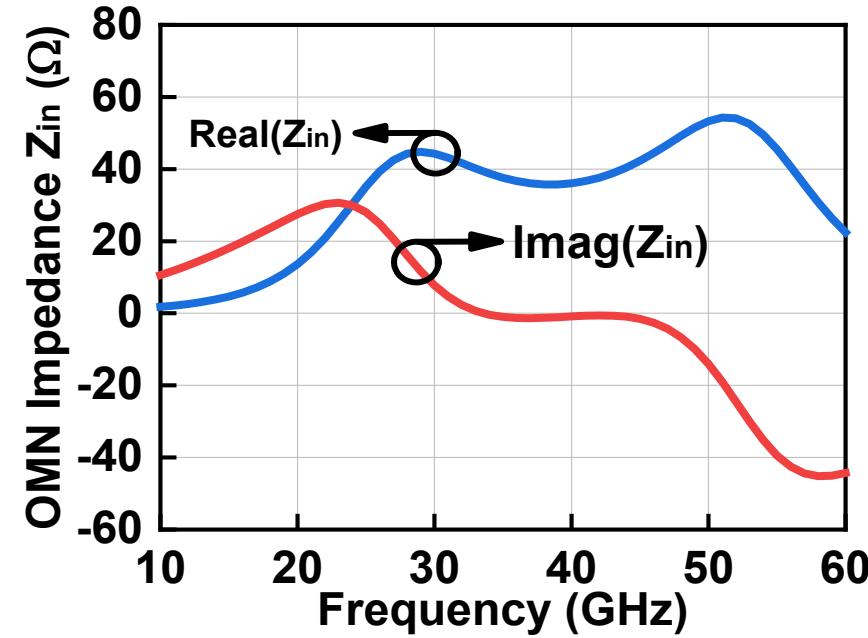
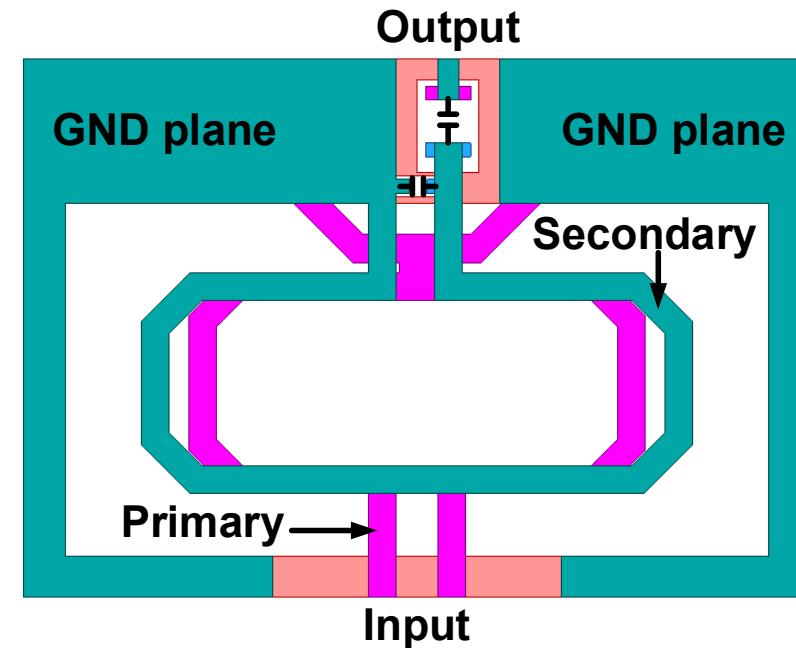
$$Z_{in} = \frac{Y_{22}Z_L + 1}{(Y_{11}Y_{22} - Y_{12}Y_{21})Z_L + Y_{11}}$$



$$FBW = \frac{\omega_{p2} - \omega_{p1}}{\sqrt{\omega_{p2}\omega_{p1}}} = \sqrt{\frac{(L_pC_p + L_sC_s - 2L_mC_{ps})}{\sqrt{(L_pL_s - L_m^2)(C_pC_s - C_{ps}^2)}}} - 2$$

■ FBW can be broadened by adjusting transformer(L_p, L_s, k) and C_o

ATCR-based matching technique

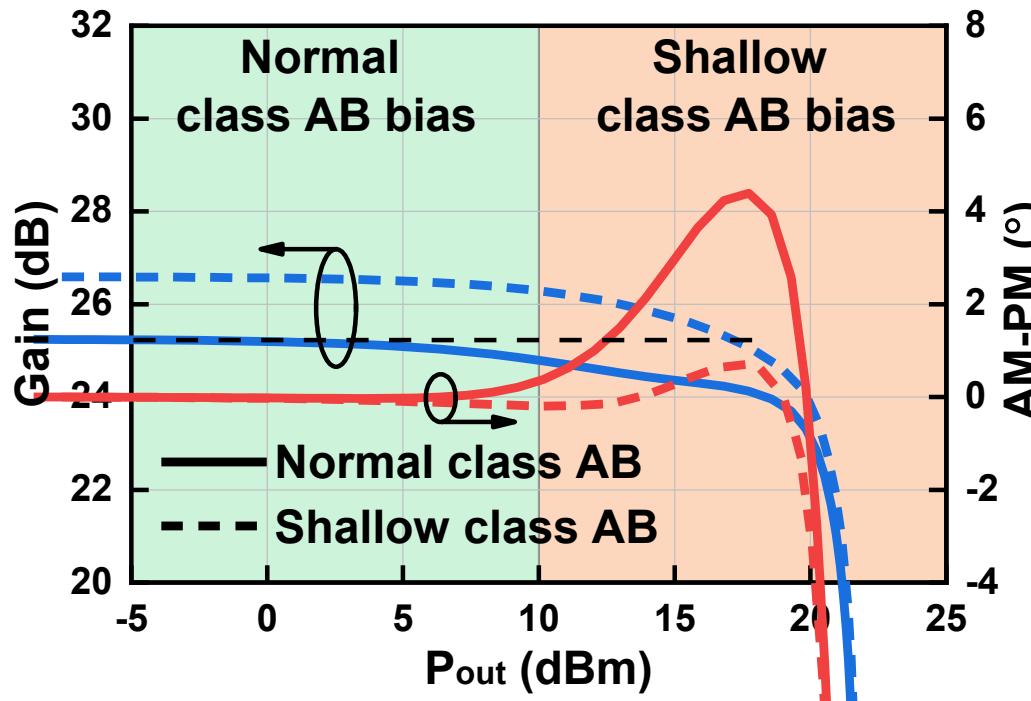
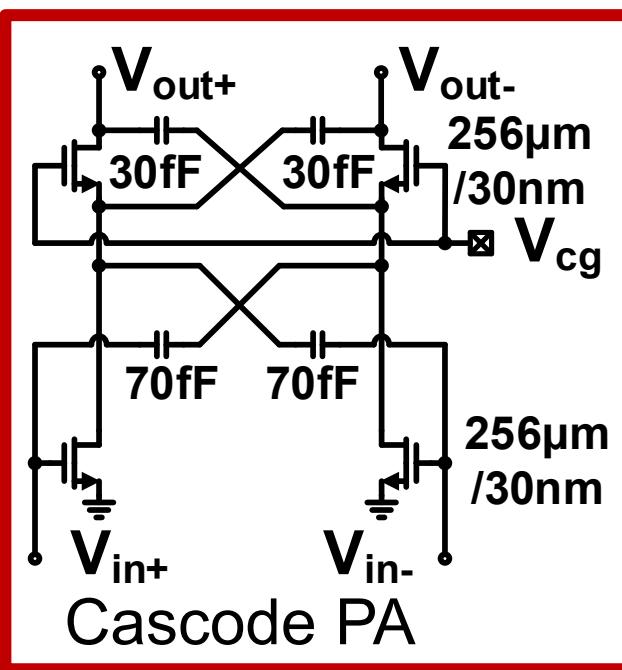


- 3D EM simulation results of the output matching network
- Well matching and low loss within a broadband

Outline

- Introduction
- ATCR-based Matching Technique
- **Broadband Linearization Technique**
- Prototype Implementation
- Measurements
- Conclusion

Broadband Linearization Technique

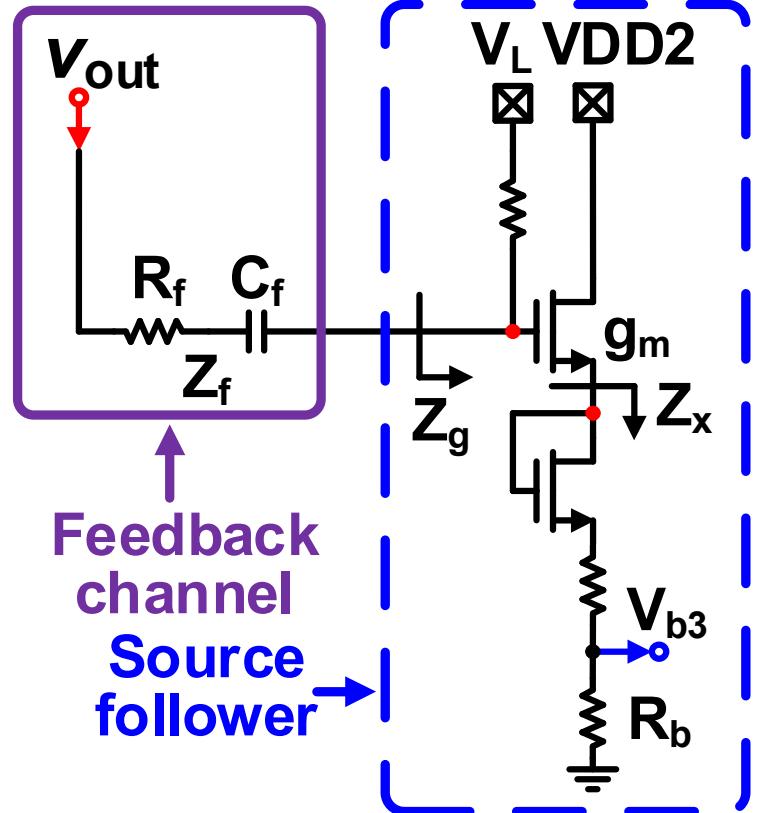


- Normal class AB bias
 - Better AM-AM and $P_{1\text{dB}}$
 - Poor AM-PM and gain
- Shallow class AB bias
 - Better AM-PM and gain
 - Poor AM-AM and $P_{1\text{dB}}$

- Use normal class AB bias in low power region to maintain high gain
- Use shallow class AB bias in high power region to improve AM-AM and AM-PM
- Higher gain and $P_{1\text{dB}}$ with smaller AM-AM and AM-PM distortion

Adaptive feedback linearizer

Adaptive feedback linearizer (AFL)



Static bias voltage

$$V_{bias} = \frac{R_b}{R_b + Z_x} \frac{g_m Z_x}{1 + g_m Z_x} V_L$$

AC component: canceled in differential circuits

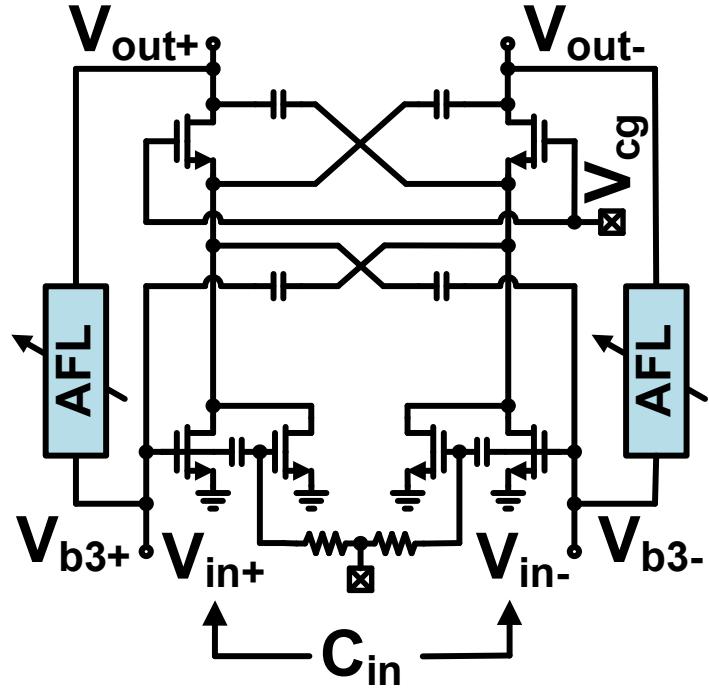
$$V_{ac} = \frac{R_b}{R_b + Z_x} \frac{g_m Z_x}{1 + g_m Z_x} \frac{Z_g}{Z_g + Z_f} V_{out}$$

DC component: dynamic bias voltage

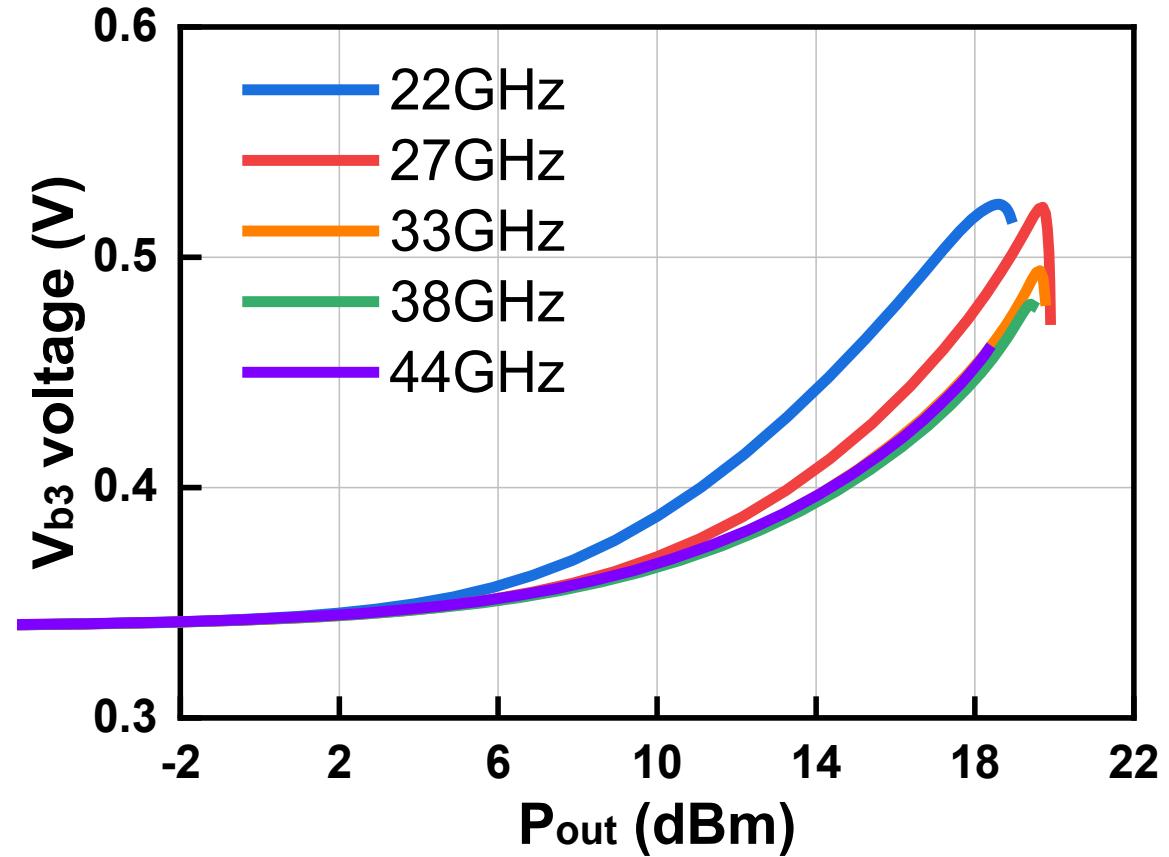
$$V_{b3} = \frac{R_b}{R_b + Z_x} \frac{g_m Z_x}{1 + g_m Z_x} \left(V_L + \frac{Z_g}{Z_g + Z_f} V_{out_rms} \right)$$

Adaptive feedback linearizer

multi-gated connection
for dynamic bias



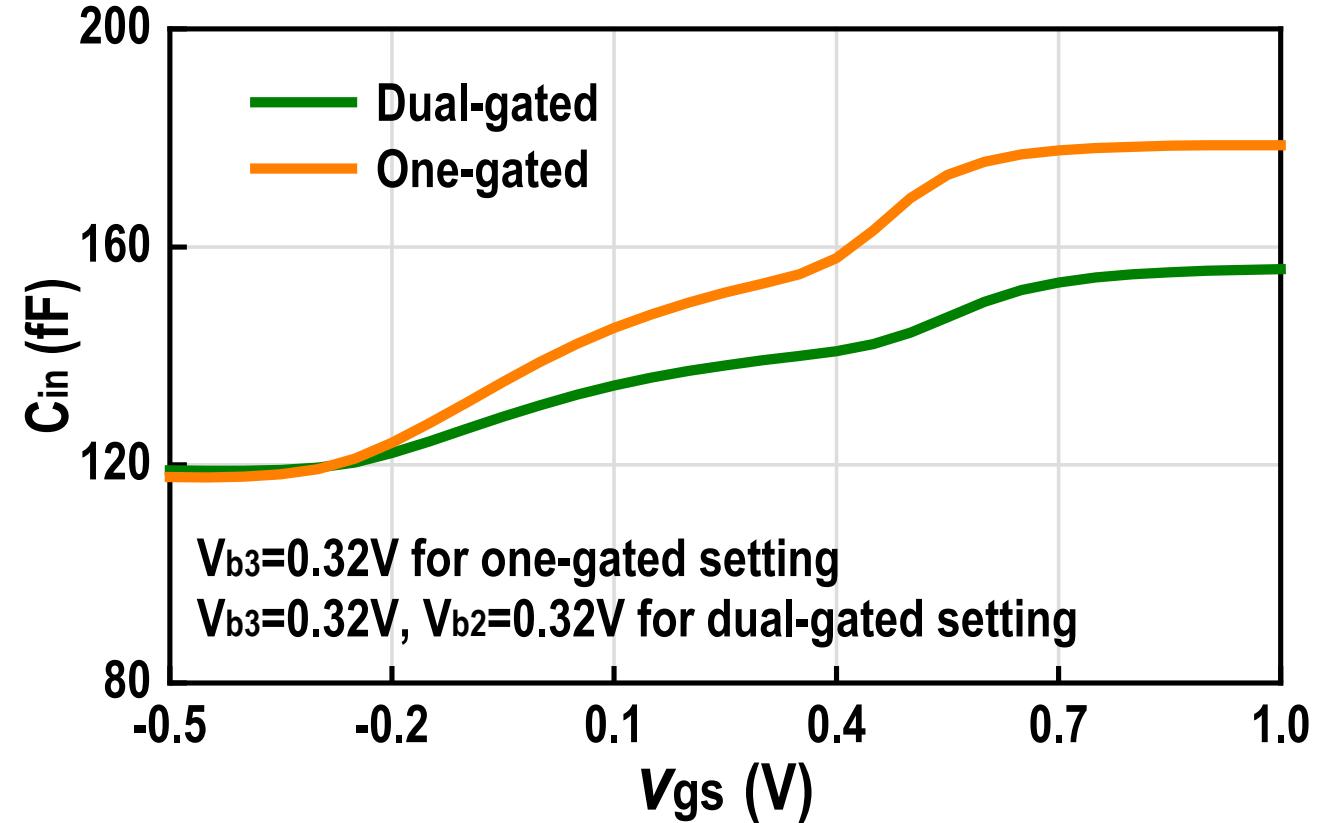
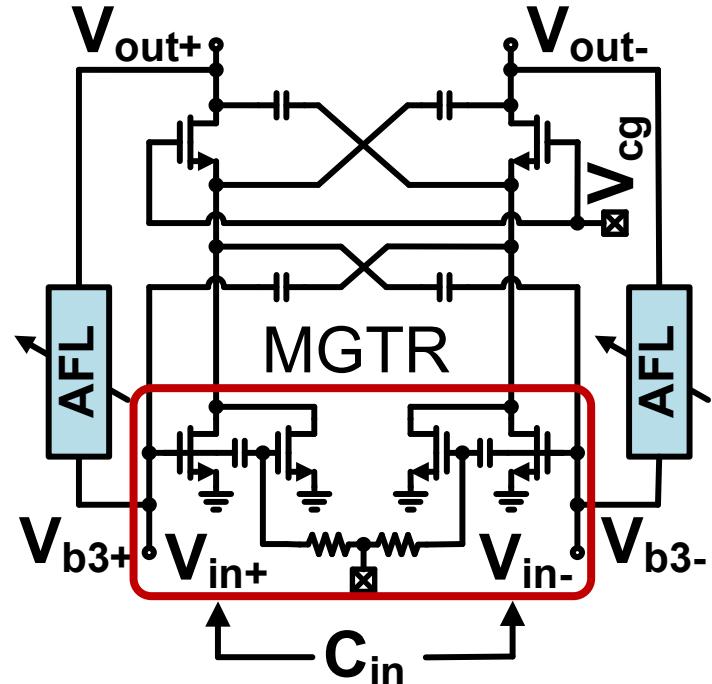
- Work in broadband
- Provide a bias voltage



- Consume very small power
- Not affect the output matching

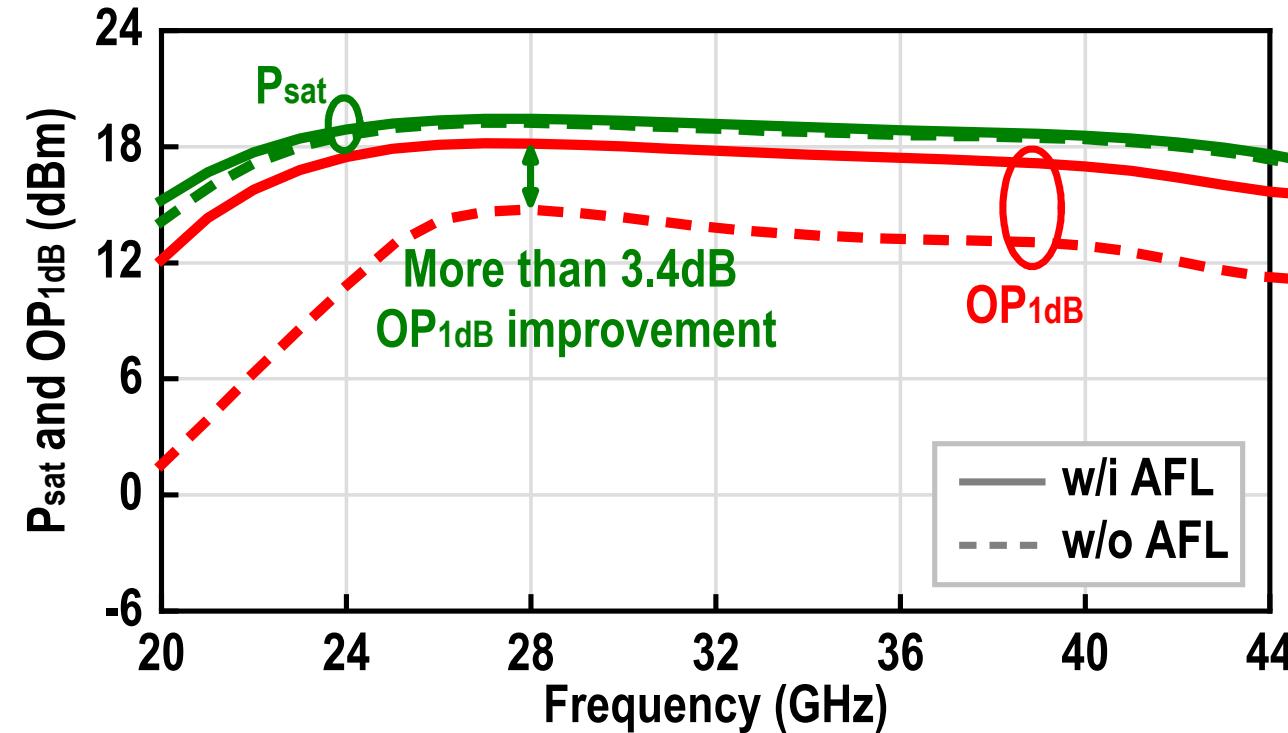
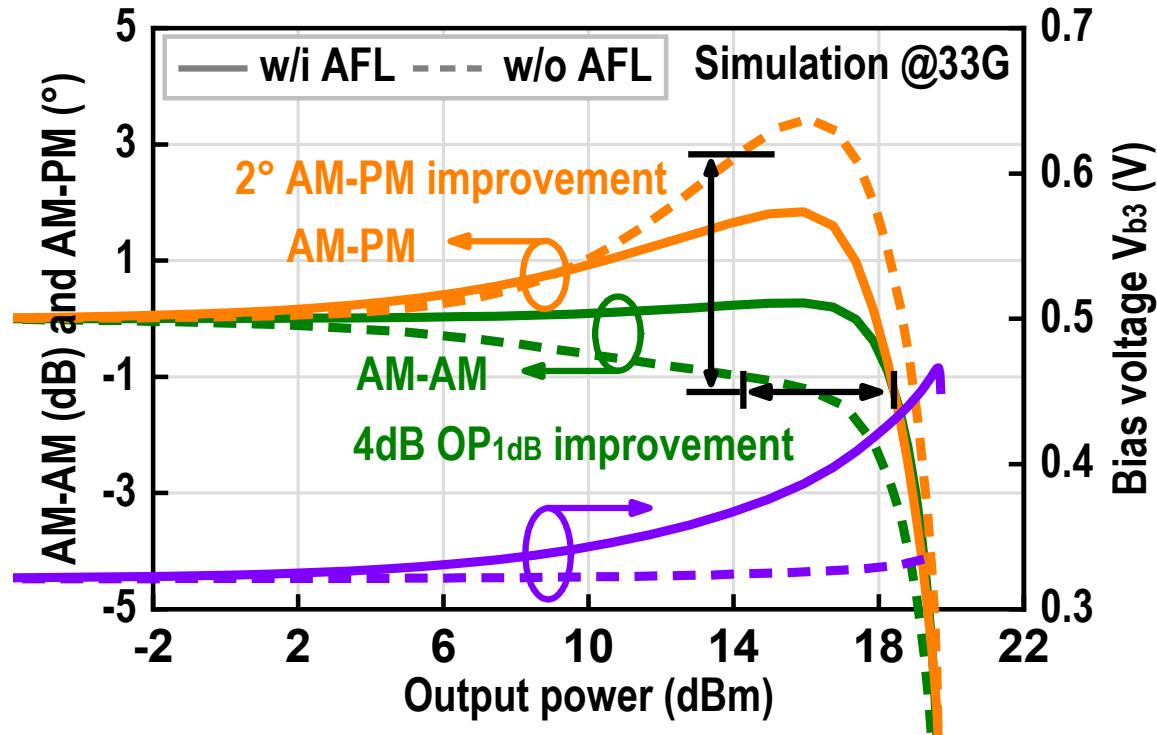
Multi-gated connection

multi-gated connection
for dynamic bias



- Smaller input equivalent capacitance variation range
- Multi-gated connection helps to improve AM-PM distortion

Benefits of broadband linearization technique

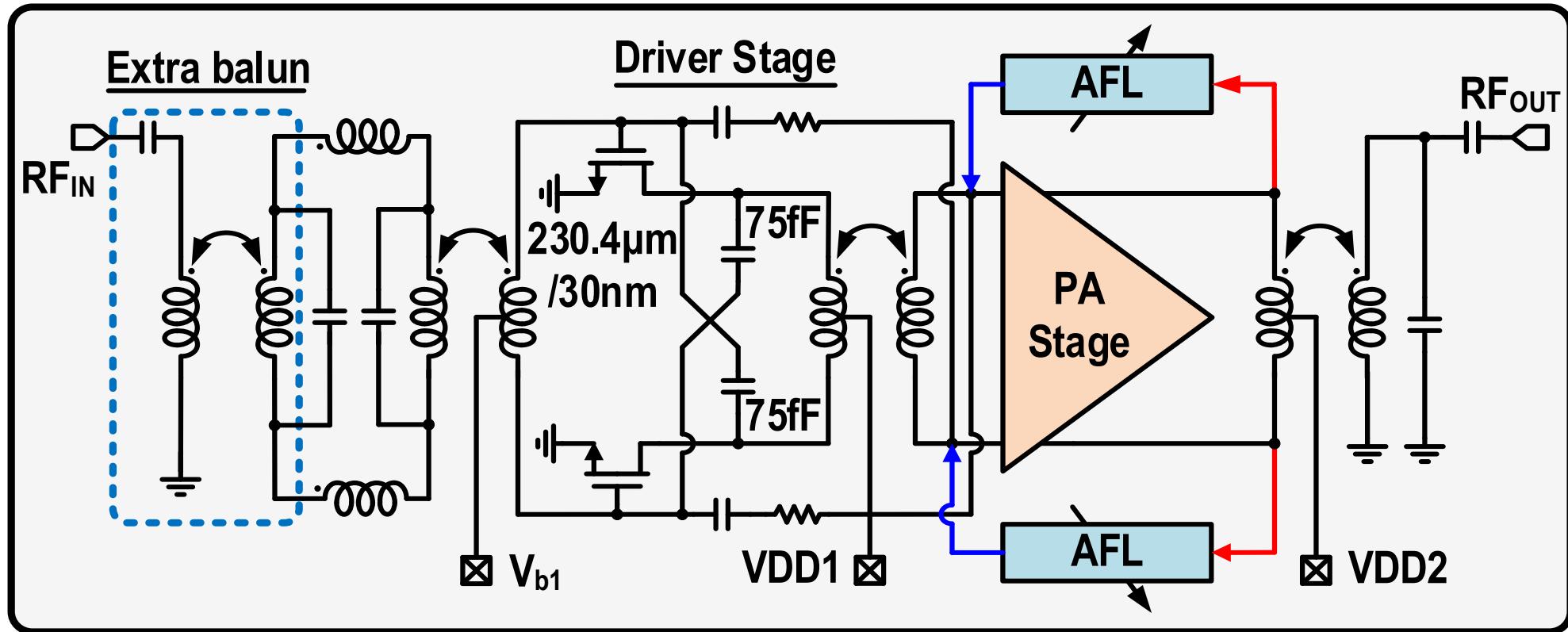


- AM-AM and AM-PM are reduced by using AFL and MGTR techniques
- OP_{1dB} and AM-PM is improved by 4dB and 2° respectively at 33GHz
- OP_{1dB} is improved by more than 3.4dB over 20-44GHz

Outline

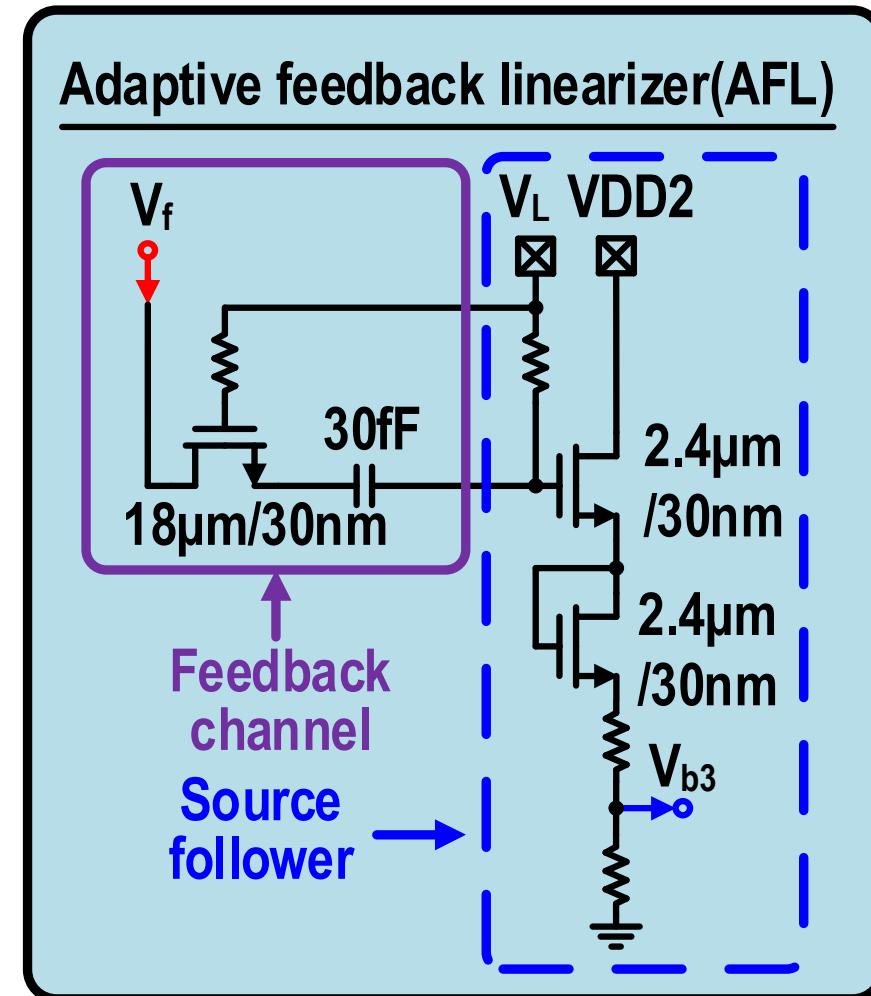
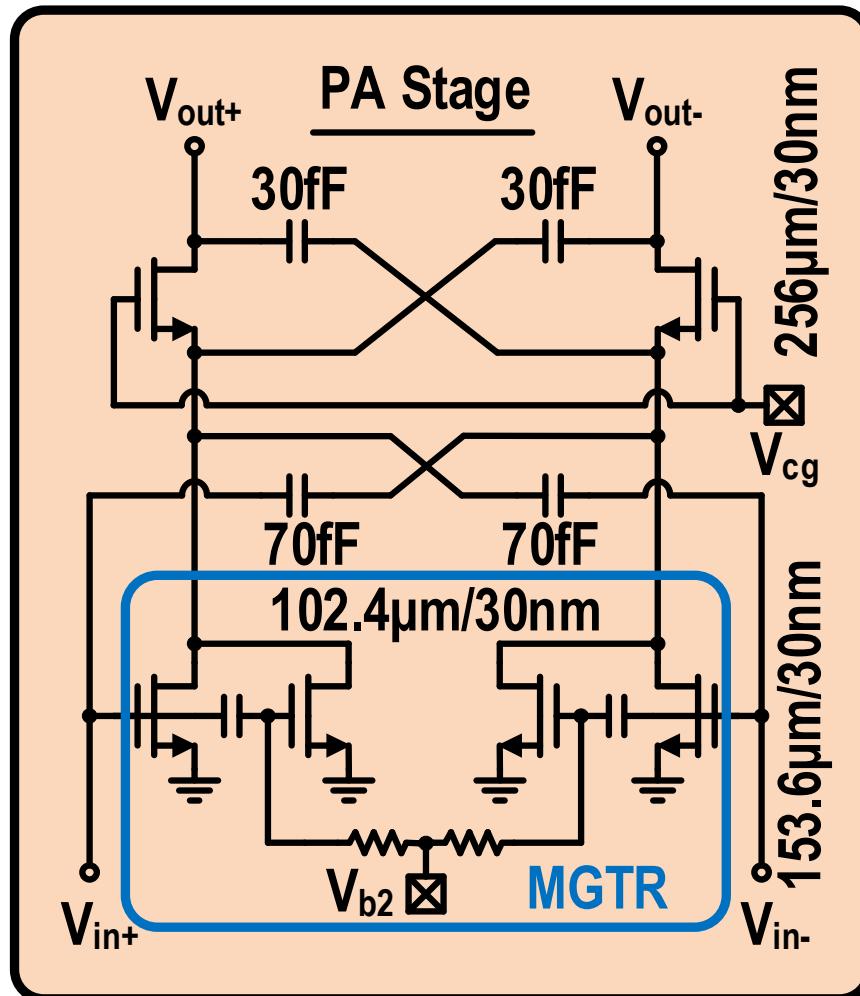
- Introduction
- ATCR-based Matching Technique
- Broadband Linearization Technique
- Prototype Implementation
- Measurements
- Conclusion

Prototype Implementation: Schematic



- PA stage with 1.8V and driver stage with 0.9V supply voltage
- RC series feedback is used in driver stage for flat gain
- Extra balun at input for single end measurement purpose

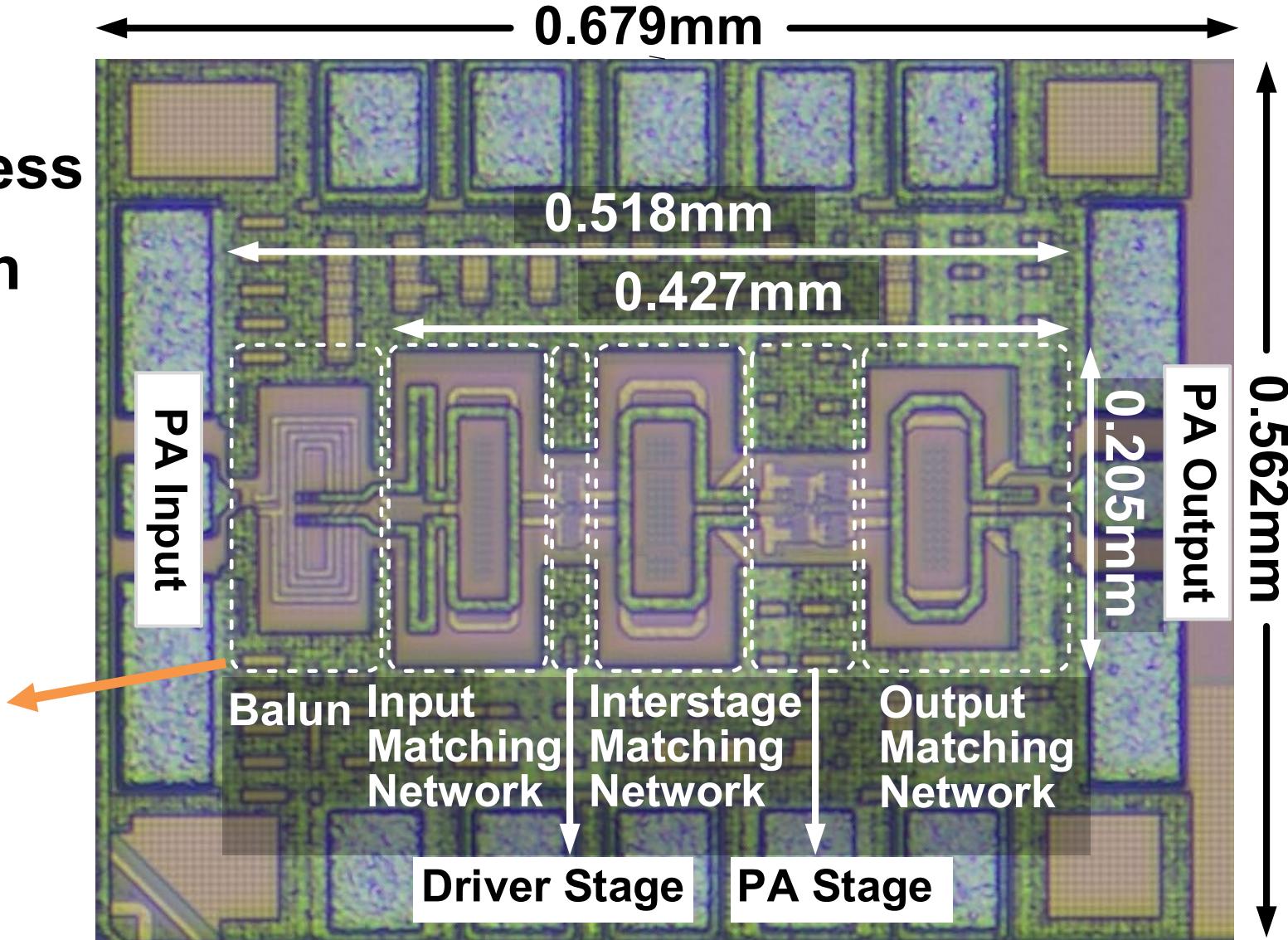
Prototype Implementation: Schematic



■ Details of PA stage and AFL implementation

Prototype Implementation: Chip microphotograph

- 28-nm bulk CMOS process
- 0.106mm² core area with extra balun
- 0.088mm² core area without extra balun



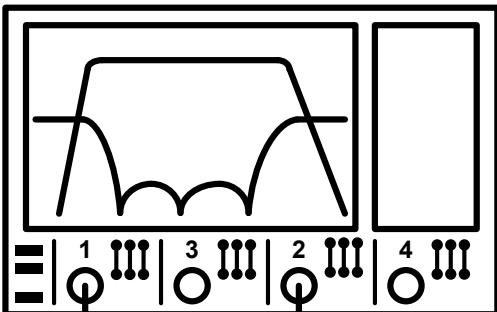
Outline

- Introduction
- ATCR-based Matching Technique
- Broadband Linearization Technique
- Prototype Implementation
- Measurements
- Conclusion

Measurement setup

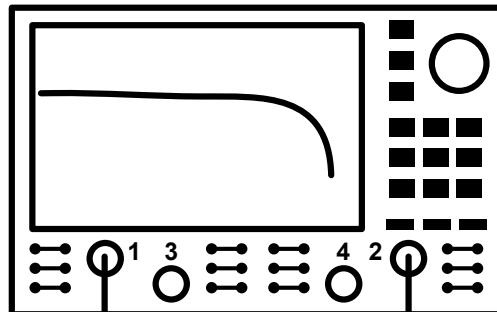
S-parameter

Rohde & Schwarz ZNA67



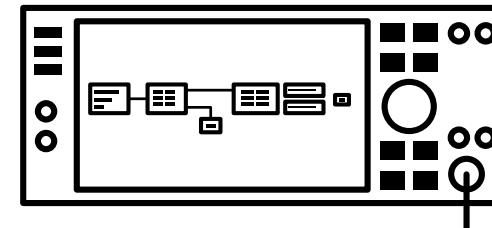
AM-PM

Keysight PNA-X N5244B

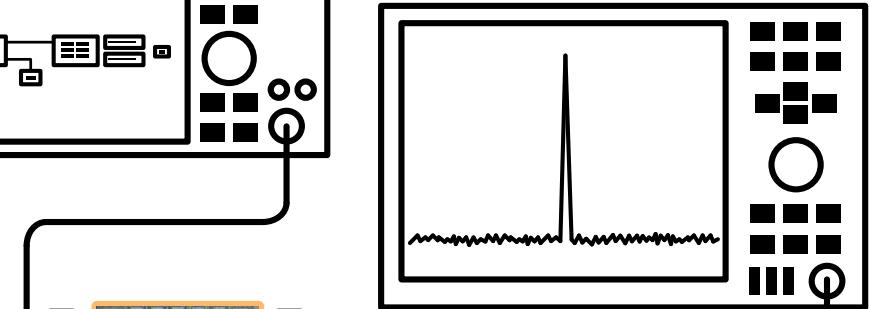


Large-signal and 5G NR signal

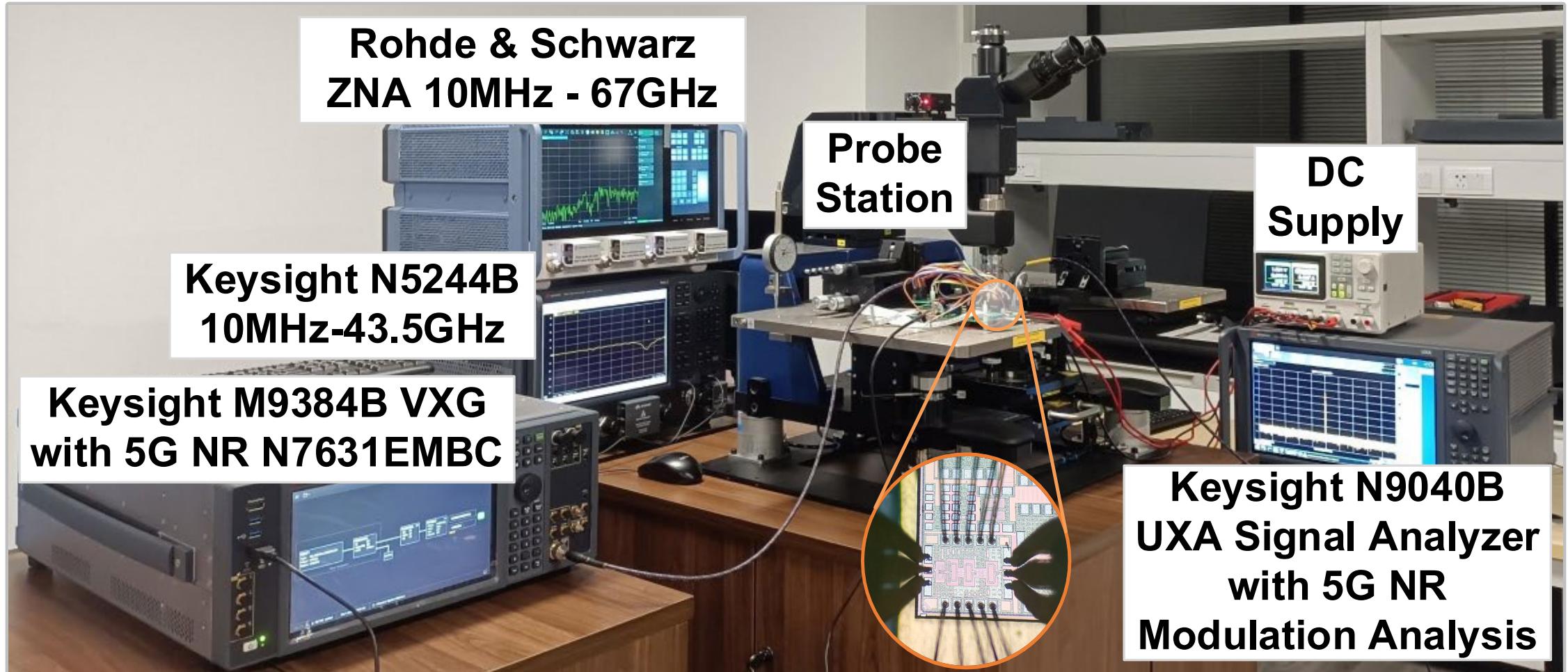
Keysight VXG M9384B
with 5G NR N7631EMBC



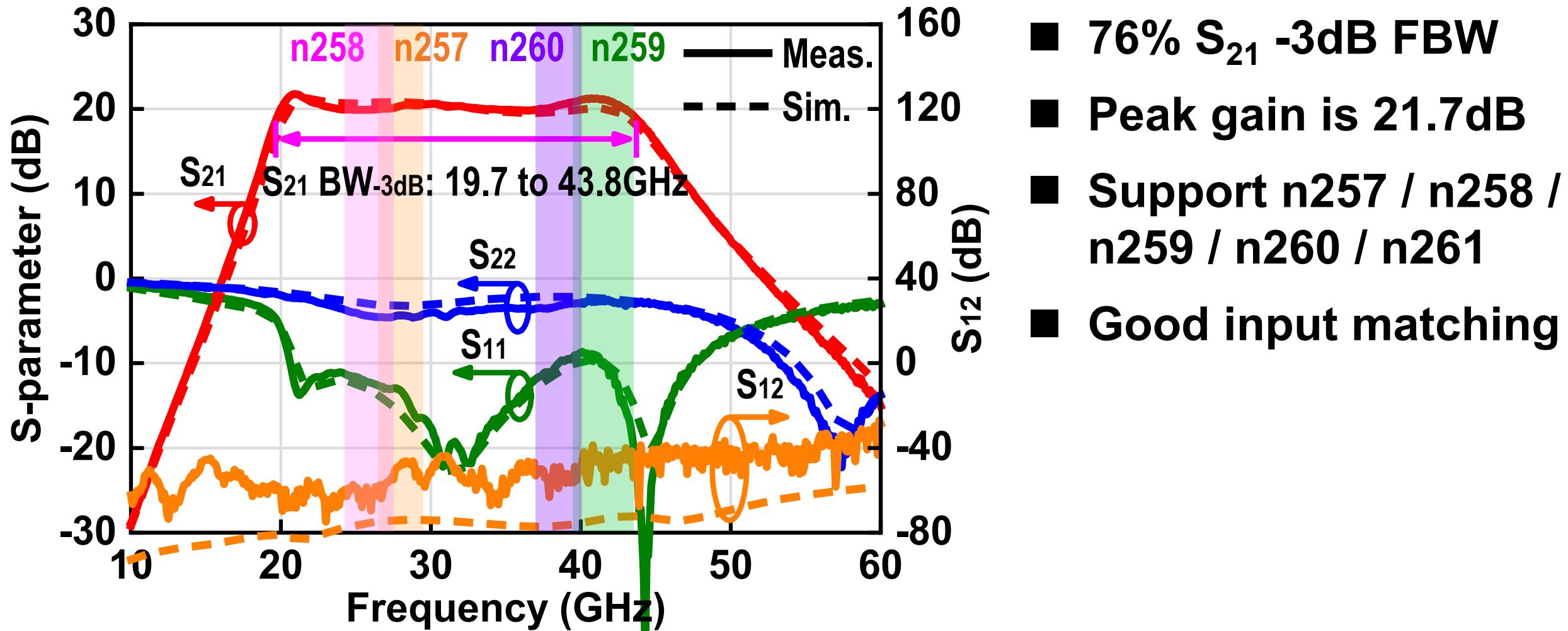
Keysight UXA N9040B
Signal Analyzer with 5G
NR Modulation Analysis



Measurement setup



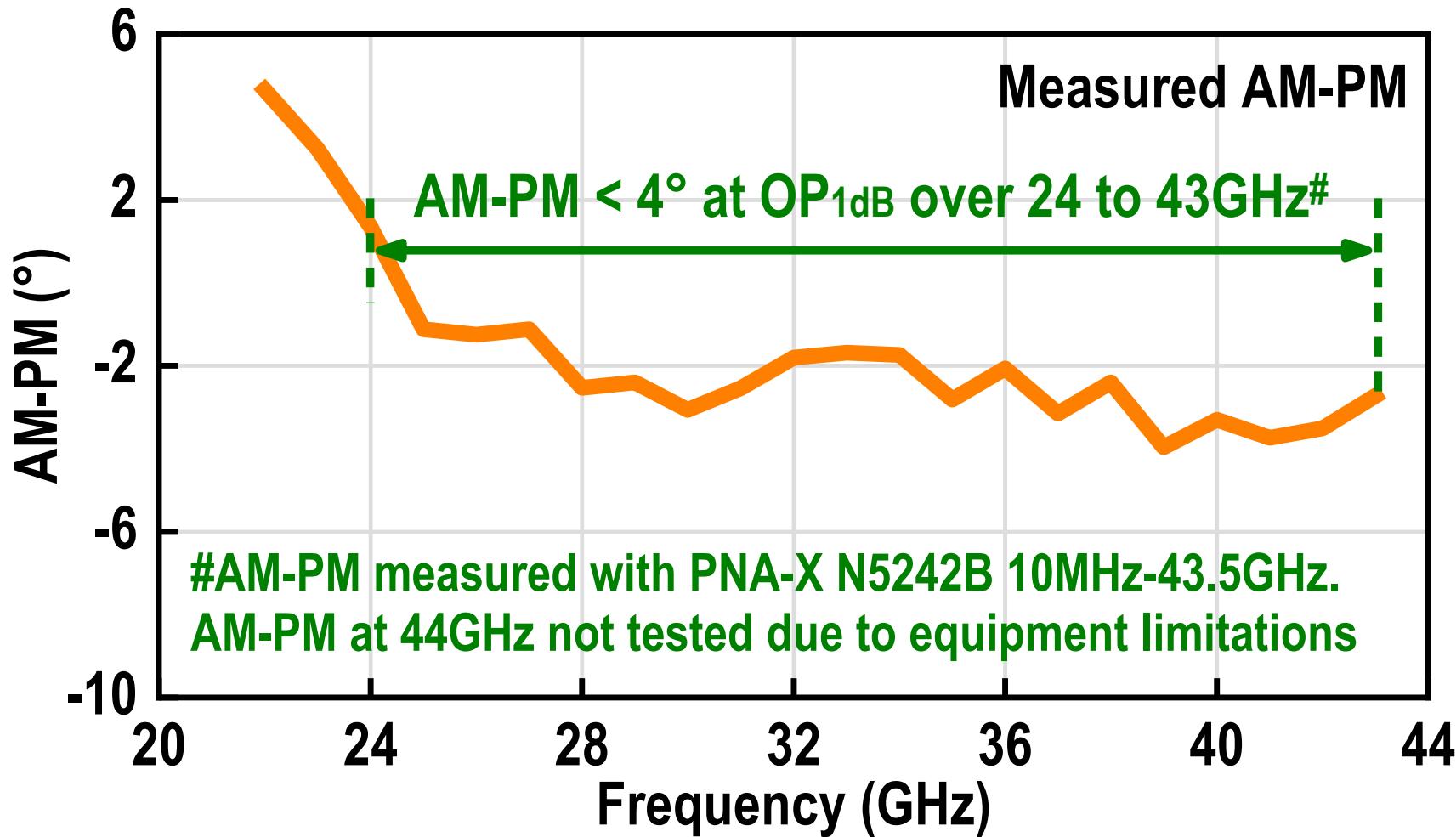
S-parameter measurement results



- 76% S_{21} -3dB FBW
- Peak gain is 21.7dB
- Support n257 / n258 / n259 / n260 / n261
- Good input matching

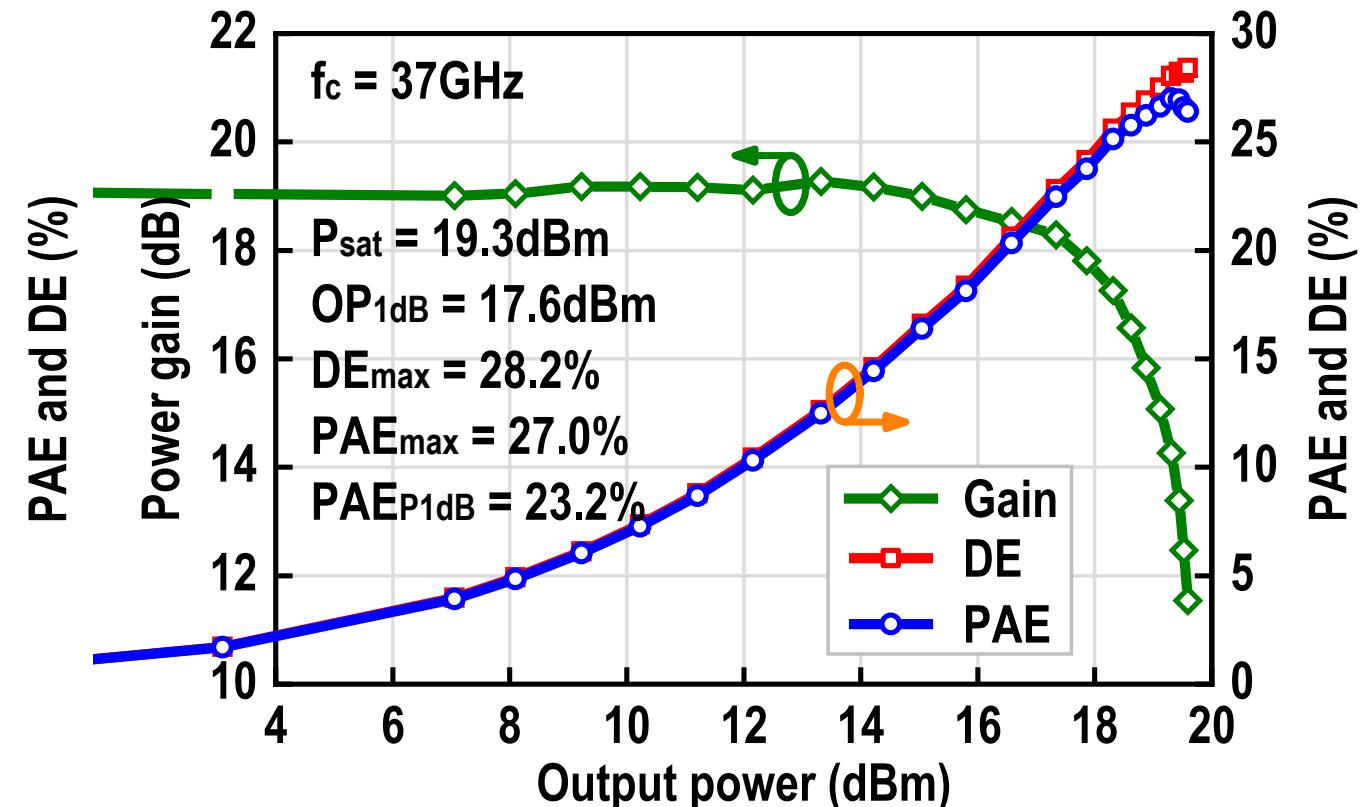
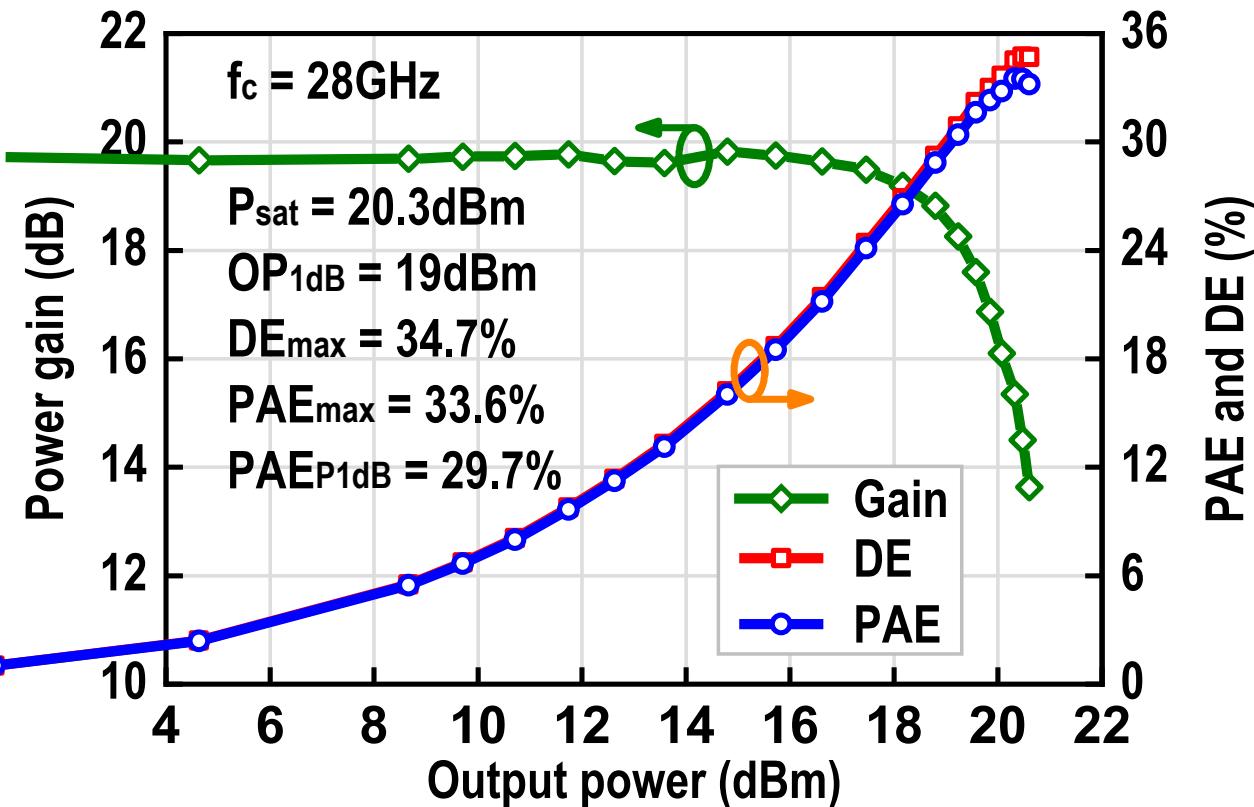
■ The measured results are consistent with the simulated one

AM-PM measurement result



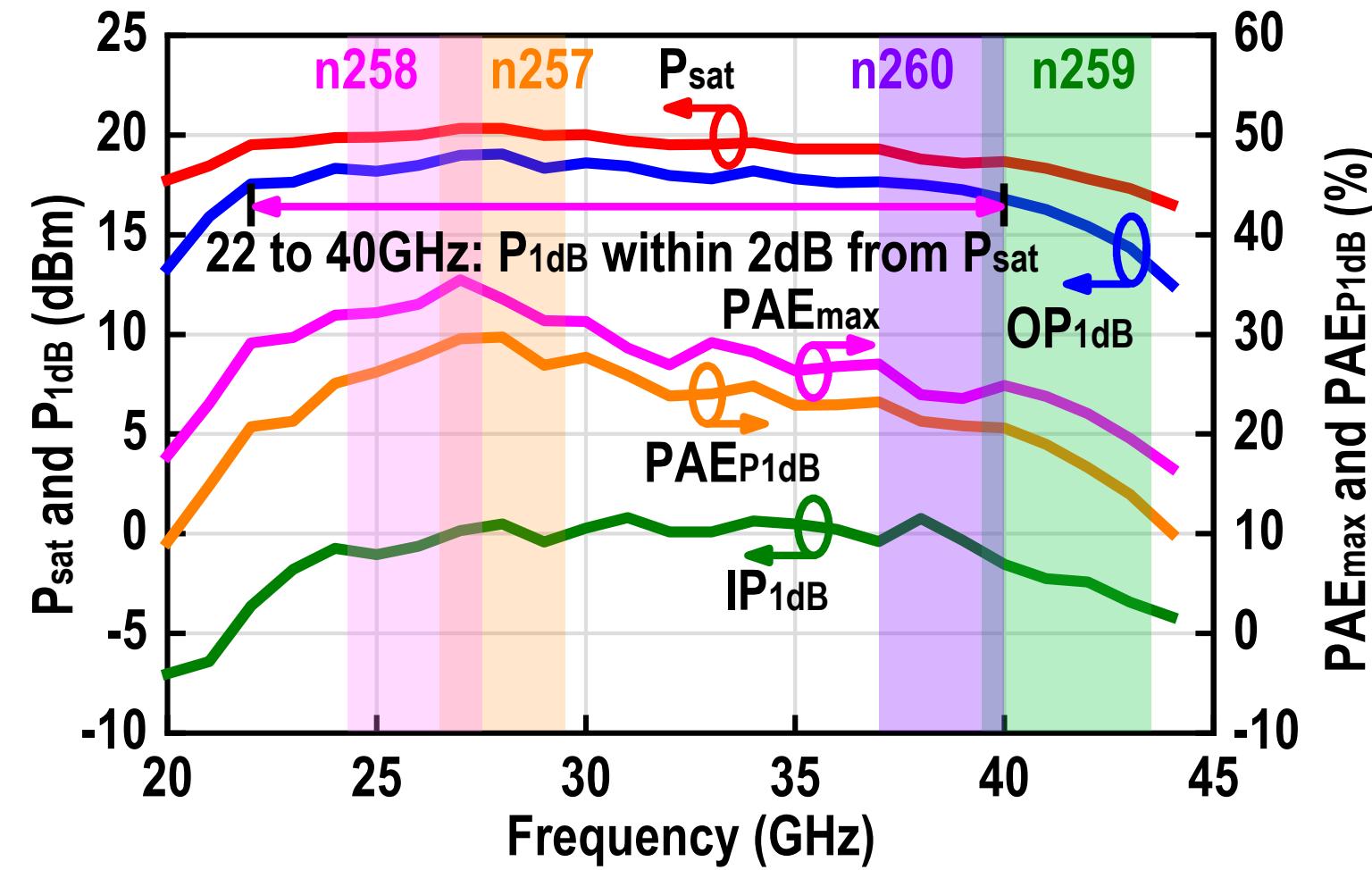
- Measured AM-PM<4° at OP_{1dB} over 24 to 43GHz

Large-signal CW measurement results



- Measured P_{sat} , $\text{OP}_{1\text{dB}}$, DE_{max} , PAE_{max} , PAE_{P1dB} at 28GHz and 37GHz

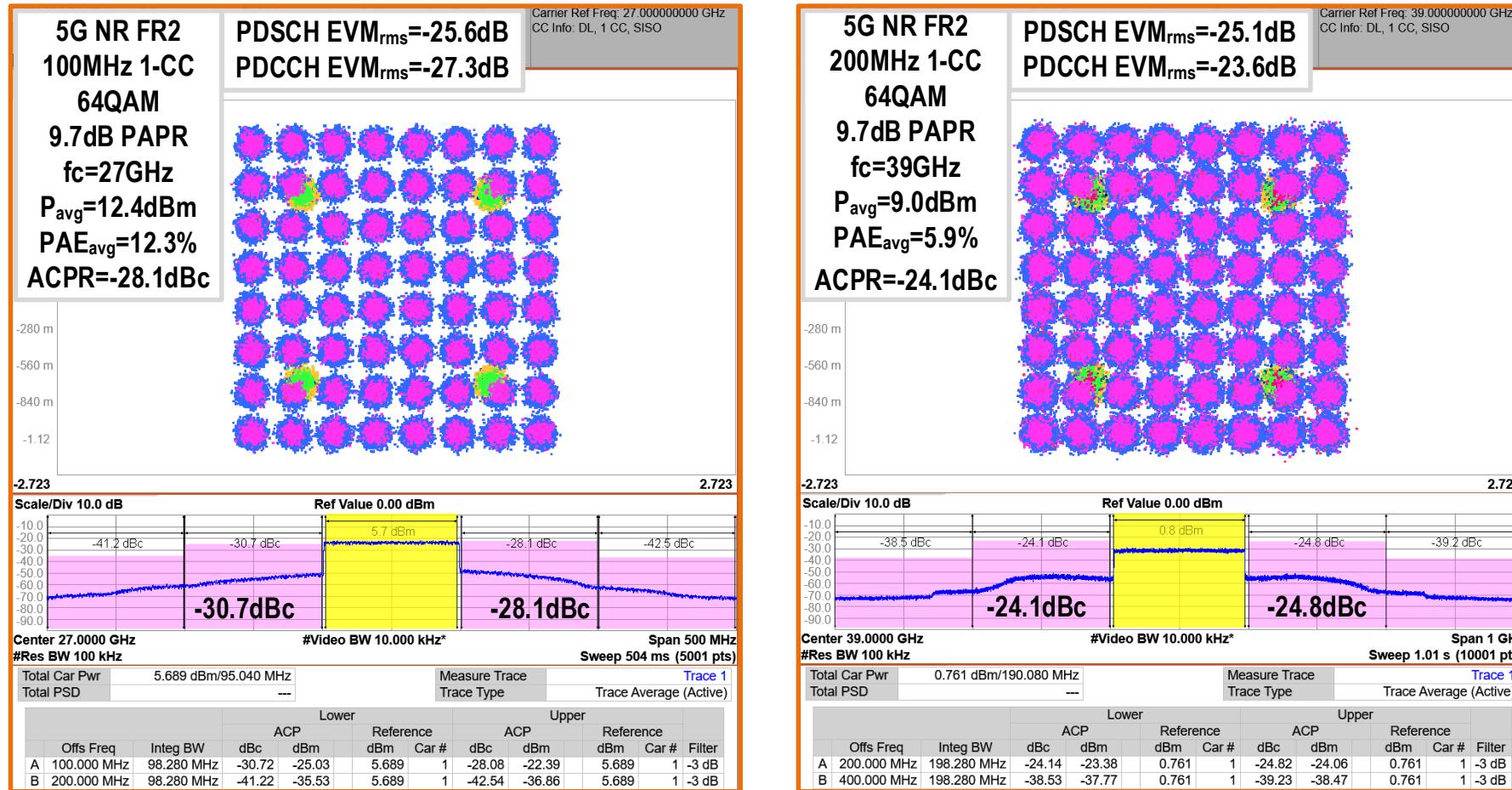
Large-signal CW measurement results



From 22 to 40GHz

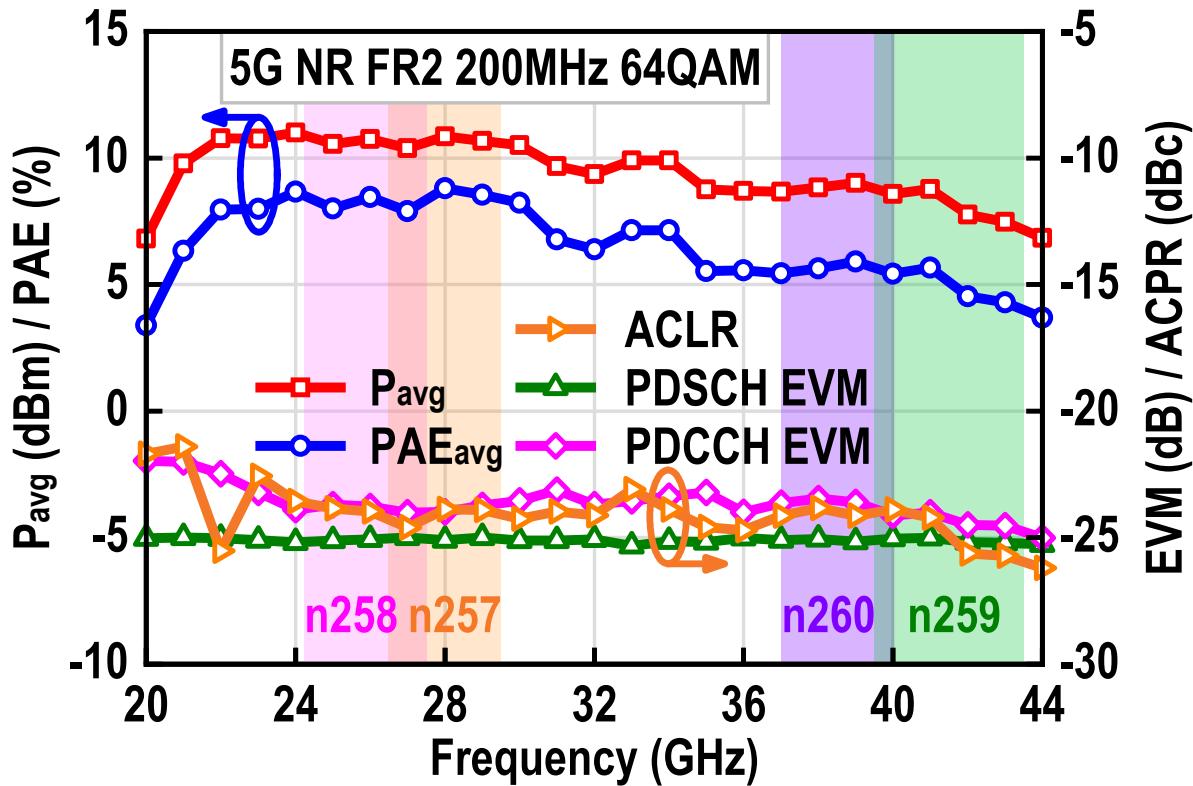
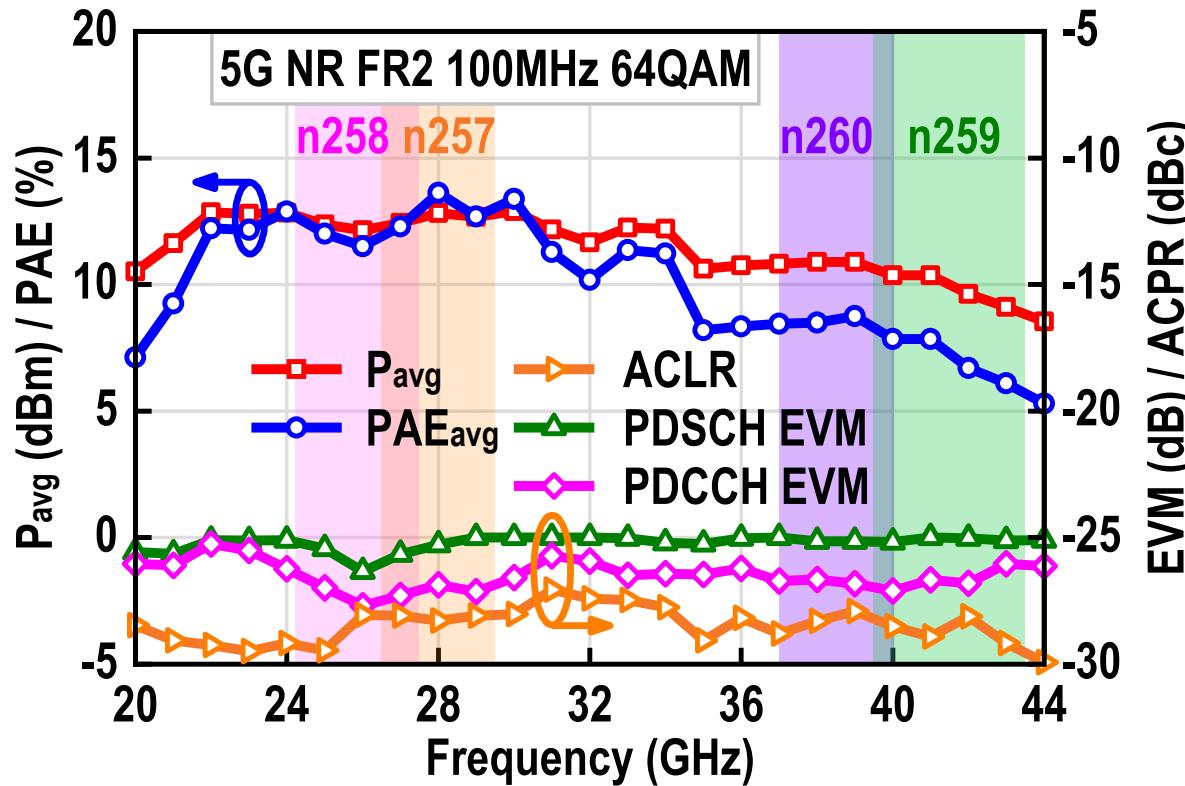
- P_{sat} : 18.7-20.3dBm
- $\text{OP}_{1\text{dB}}$: 16.8 to 19dBm (within 2dB from P_{sat})
- PAE_{max} : 24.9-35.5%
- $\text{PAE}_{P_{1\text{dB}}}$: 20.6-29.7%

Modulation measurement results



■ Measured constellation and ACPR with 5G NR FR2 100/200MHz
64QAM without DPD (9.7dB PAPR at 0.01% CCDF)

Modulation measurement results

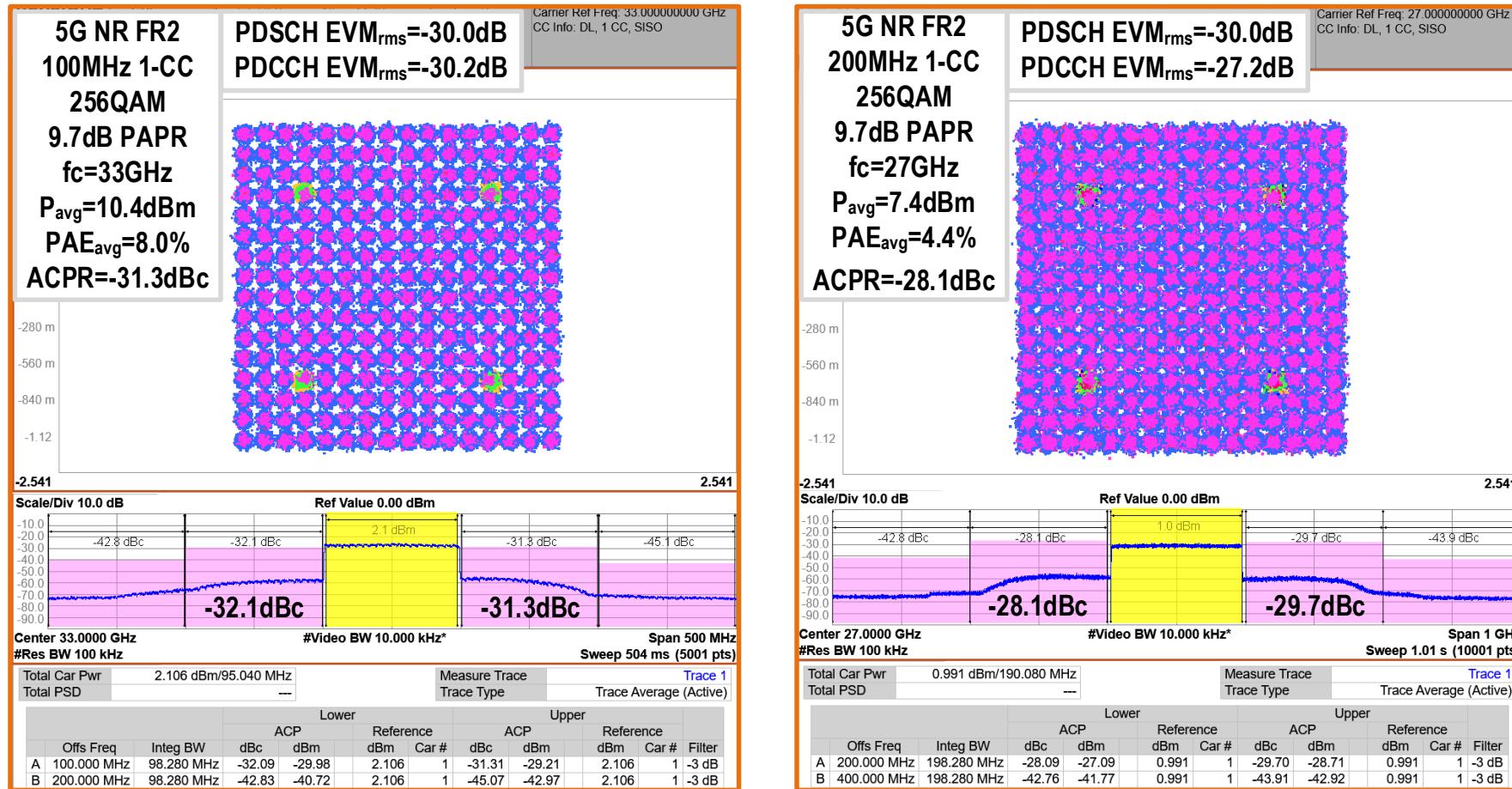


From 22 to 44GHz

- P_{avg} : 8.5-12.8dBm
- PAE_{avg} : 5.3-13.6%

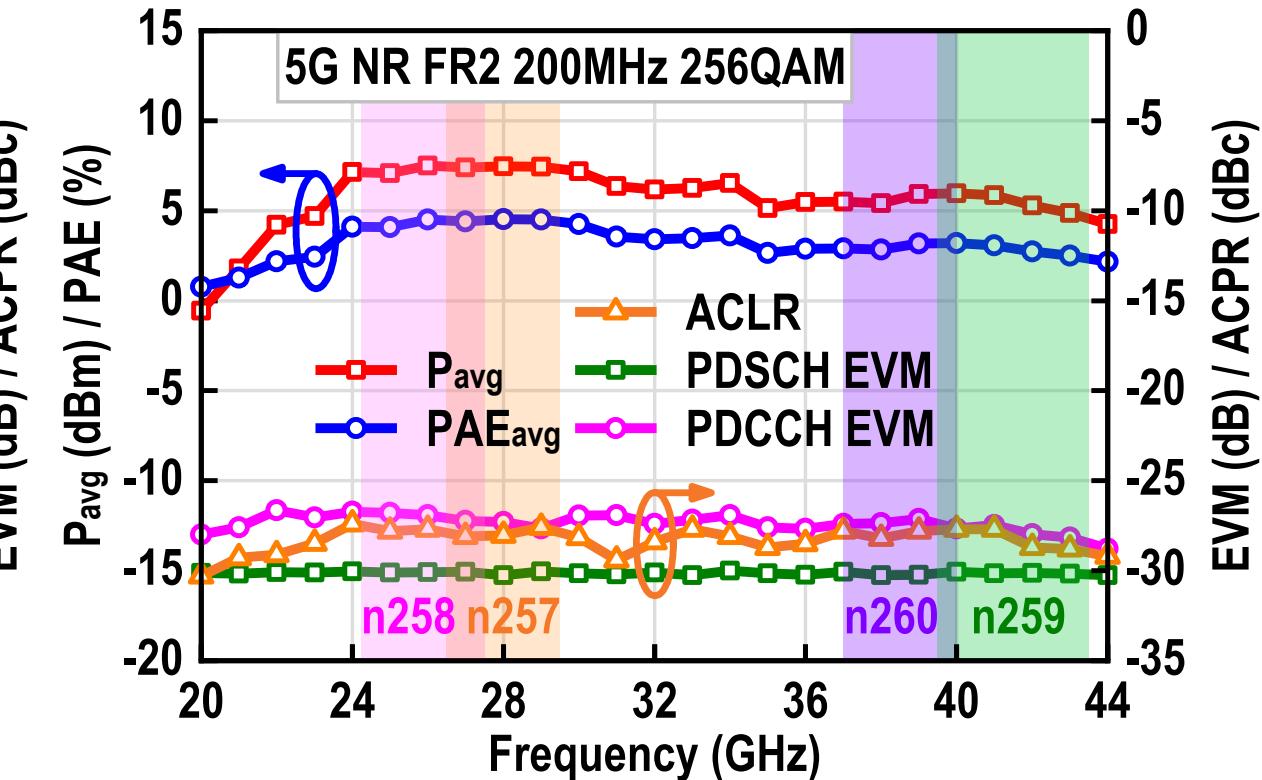
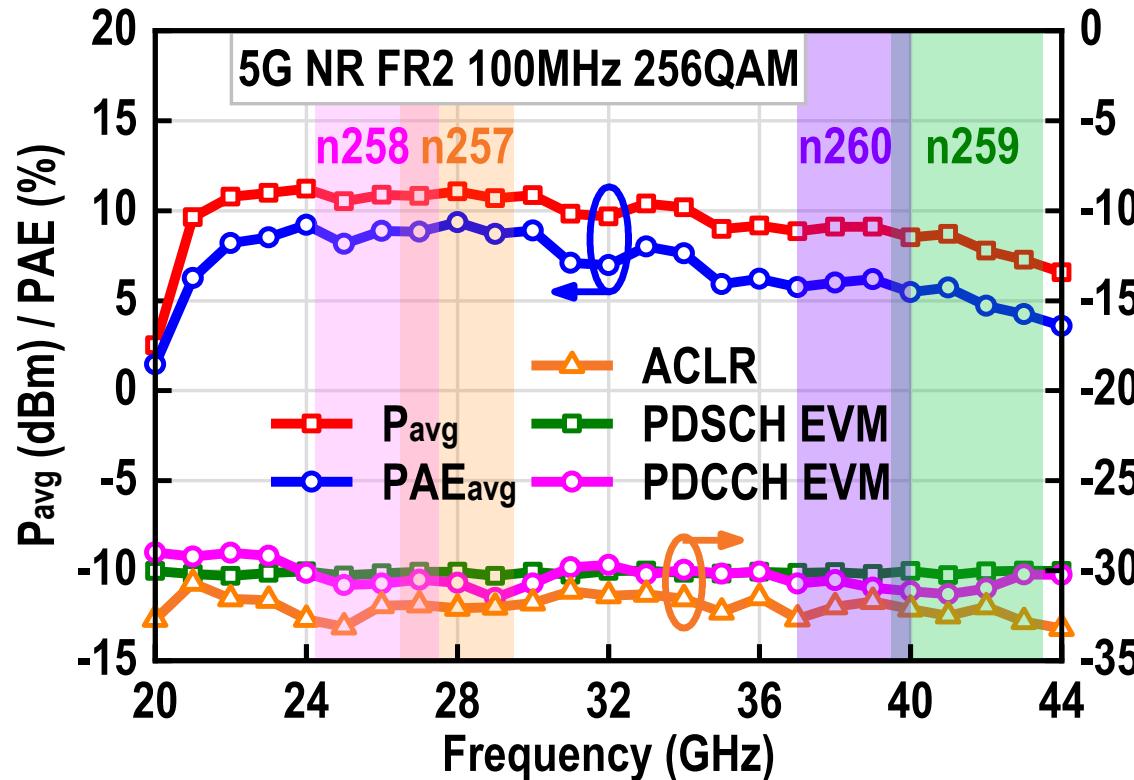
- P_{avg} : 6.8-11dBm
- PAE_{avg} : 3.7-8.8%

Modulation measurement results



■ Measured constellation and ACPR with 5G NR FR2 100/200MHz
256QAM without DPD (9.7dB PAPR at 0.01% CCDF)

Modulation measurement results



From 22 to 44GHz

- P_{avg} : 6.7-11.1 dBm
- PAE_{avg} : 3.6-9.7%

- P_{avg} : 4.2-7.5 dBm
- PAE_{avg} : 2.2-4.5%

Summary and comparisons

	This work			[5] Vigilante, JSSC'18	[2] Shakib, ISSCC'16	[1] Wang, ISSCC'20			[8] Garay, ISSCC'21	[6] Huang, ISSCC'21	[7] Hu, ISSCC'17	[3] Shakib, ISSCC'17
Technology	28nm CMOS			28nm CMOS	28nm CMOS	45nm SOI CMOS			45nm SOI CMOS	45nm SOI CMOS	0.13um SiGe	40nm CMOS
Architecture	Two-stage PA with feedback linearizer			Transformer-based High Order Network	Two-stage PA	Compensated Distributed Balun			Dual-Driver PA Core	Continuous Coupler Doherty	Multiband Analog Doherty	dual-resonance transformer
Supply(V)	1.8V(PA) 0.9V(Driver)			0.9	1.0	2			1.9	2V(PA) 1V(Driver)	1.5	1.1
Gain(dB)	20.5			20.8	15.7	20.5			20.4	16@32.5GHz*	18.2	22.4
5G Band Support	n257/n258/ n259/n260/n261			n259/n260	n257/n261	n257/n258#/ 259#/n260/n261			n257/n258/ n261	n257/n259/ n260/n261	n257/n258/ n260#/n261	n257/n261
S ₂₁ BW _{-3dB} (GHz)	19.7 to 43.8 (76%)			29 to 57 (65%)	27.5 to 31 (12%)*	25.8 to 43.4 (51%)			23.5 to 34 (37%)††	26 to 60 (79%)-	23.3 to 39.7 (52%)	26 to 32 (21%)*
Freq(GHz)	25	28	37	40	30	40	50	30	24	28	37.5	40
P _{sat} (dBm)	19.8	20.3	19.3	18.7	16.6	15.9	15.1	14	20	20.4	20	17.9
P _{1dB} (dBm)	18.2	19.0	17.6	16.8	13.4	11.1	10.9	13.2	19.6	19.1	18.9	15.7
PAE _{max} (%)	32.2	33.6	27.0	24.9	24.2	18.4	14.9	35.5	38.9	45.0	38.7	35.0
PAE _{P1dB} (%)	26.2	29.7	23.2	20.6	12.6	7.5	7.0	34.3	38.9	42.5	37.7	30.4

‡w/o extra balun, *graphically estimated, #partial support, ††OP1dB BW_{-1dB}, - P_{sat} BW_{-3dB}, †last stage collector efficiency

■ Performance summary and comparisons of small signal and large signal

Summary and comparisons

	This work				[5] Vigilante, JSSC'18	[2] Shakib, ISSCC'16	[1] Wang, ISSCC'20				[8] Garay, ISSCC'21	[6] Huang, ISSCC'21	[7] Hu, ISSCC'17	[3] Shakib, ISSCC'17						
Technology	28nm CMOS				28nm CMOS		28nm CMOS	45nm SOI CMOS				45nm SOI CMOS				0.13um SiGe	40nm CMOS			
Architecture	Two-stage PA with feedback linearizer				Transformer-based High Order Network		Two-stage PA	Compensated Distributed Balun				Dual-Driver PA Core	Continuous Coupler Doherty				Multiband Analog Doherty	dual-resonance transformer		
Supply(V)	1.8V(PA) 0.9V(Driver)				0.9		1.0	2				1.9	2V(PA) 1V(Driver)				1.5	1.1		
Modulation scheme	5G NR FR2 64-QAM 1-CC OFDM				64-QAM		64-QAM OFDM	5G NR FR2 64-QAM 2-CC OFDM				5G NR FR2 64-QAM	5G NR FR2 64-QAM				64QAM	64-QAM 1-CC OFDM		
PAPR (dB)	9.7				8.3		9.6	11.78				9.64	9.64				6	9.7		
Symbol rate (Sym/s)	200M				500M		250M	800M				200M	200M				500M	100M		
Freq(GHz)	25	28	37	40	28	32	34	30	24	28	37	42	28	29	40	50	28	37	39	27
EVM(dB)	-25.1	-25.1	-25.1	-25.0	-25.0	-25.0	-25.0	-25.0	-25.1	-25.1	-25.1	-25.1	-25.0	-25.0	-25.3	-25.2	-27	-30.3	-28.7	-25.0
ACPR(dBc)	-23.9	-23.9	-24.1	-23.9	-37.6	-34.2	-30.2	-26.4	-25.2	-25.6	-27.9	-26.4	-26.6	N.A.	-25.4	-26.1	-28.4	-28.2	-29.8	N.A.
P _{avg} (dBm)	10.6	10.9	8.7	8.6	6.8	8.1	8.9	4.2	10.9	11.3	10.2	8.4	10.7	7.8*	8.9	7.4	9.2	9.5	9.3	6.4*
PAE _{avg} (%)	8.0	8.8	5.4	5.4	2.9	3.9	4.4	9	14.2	16.6	13.6	10.3	15.5	7*	10.5	7.8	18.5 [†]	19.2 [†]	17.2 [†]	10*
Core Area(mm ²)	0.106/0.088 [‡]				0.16		0.16	0.21				0.21	0.62				1.76(pad)		0.23	

‡w/o extra balun, *graphically estimated, #partial support, ††OP1dB BW_{-1dB}, - P_{sat} BW_{-3dB}, †last stage collector efficiency

Performance summary and comparisons of modulation signal

Outline

- Introduction
- ATCR-based Matching Technique
- Broadband Linearization Technique
- Prototype Implementation
- Measurements
- Conclusion

Conclusion

- ATCR-based matching methodology for broadband mm-wave PAs
- Broadband linearization technique for AM-AM and AM-PM distortion
- 76% fractional bandwidth(exceeding one octave) with flat gain
- Support 5G NR and beyond signal over 19.7 to 43.8GHz (5G bands of n257/n258/n259/n260/n261)

Acknowledgement

The authors thank the support of the National Natural Science Foundation of China under Grant 61725102, the Key Research and Development Program of Guangzhou under Grant 202103020002, and the Guangdong Basic and Applied Basic Research Foundation under Grant 2019B1515120024.

THANK YOU FOR YOUR ATTENTION!

A 4.8dB NF, 70-to-86GHz Deep-Noise-Canceling LNA Using Asymmetric Compensation Transformer and 4-to-1 Hybrid-Phase Combiner in 40nm CMOS

Changxuan Han*, Jie Zhou*, Zhixian Deng, Yiyang Shu,
and Xun Luo

University of Electronic Science and Technology of China



Outline

- **Introduction and Motivation**
- **Deep-Noise-Canceling LNA Architecture**
- **Asymmetric CG Based Noise-Canceling**
- **Resistive Feedback Noise-Canceling**
- **LNA Implementation**
- **Measurement and Comparison**
- **Conclusion**

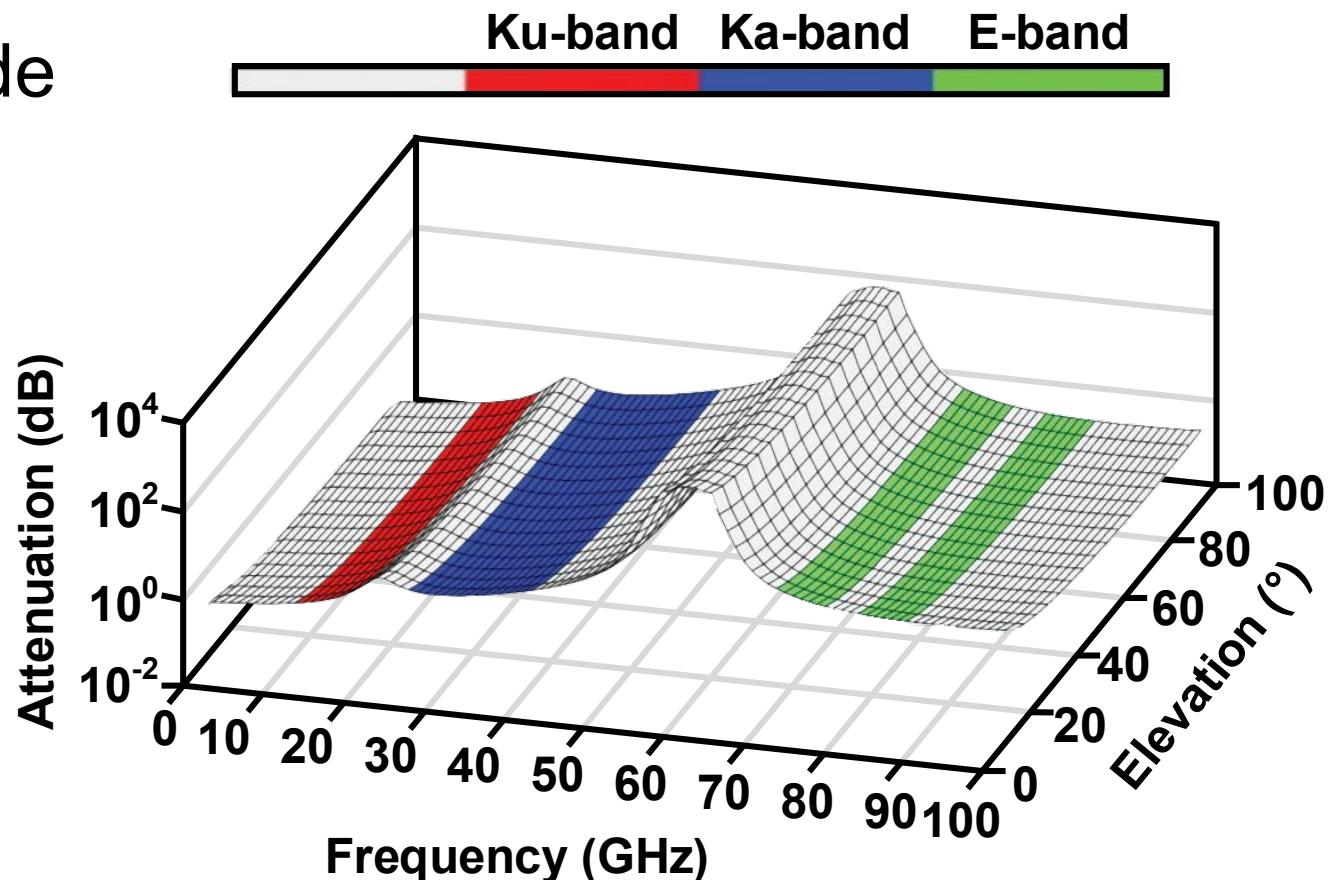
Outline

- **Introduction and Motivation**
- Deep-Noise-Canceling LNA Architecture
- Asymmetric CG Based Noise-Canceling
- Resistive Feedback Noise-Canceling
- LNA Implementation
- Measurement and Comparison
- Conclusion

Introduction and Motivation

■ Increasing demand of mm-wave communication

- high data-rates desire wide channel bandwidth
- Low atmospheric attenuation in E-band
- Application on cellular backhaul networks and satellite communication

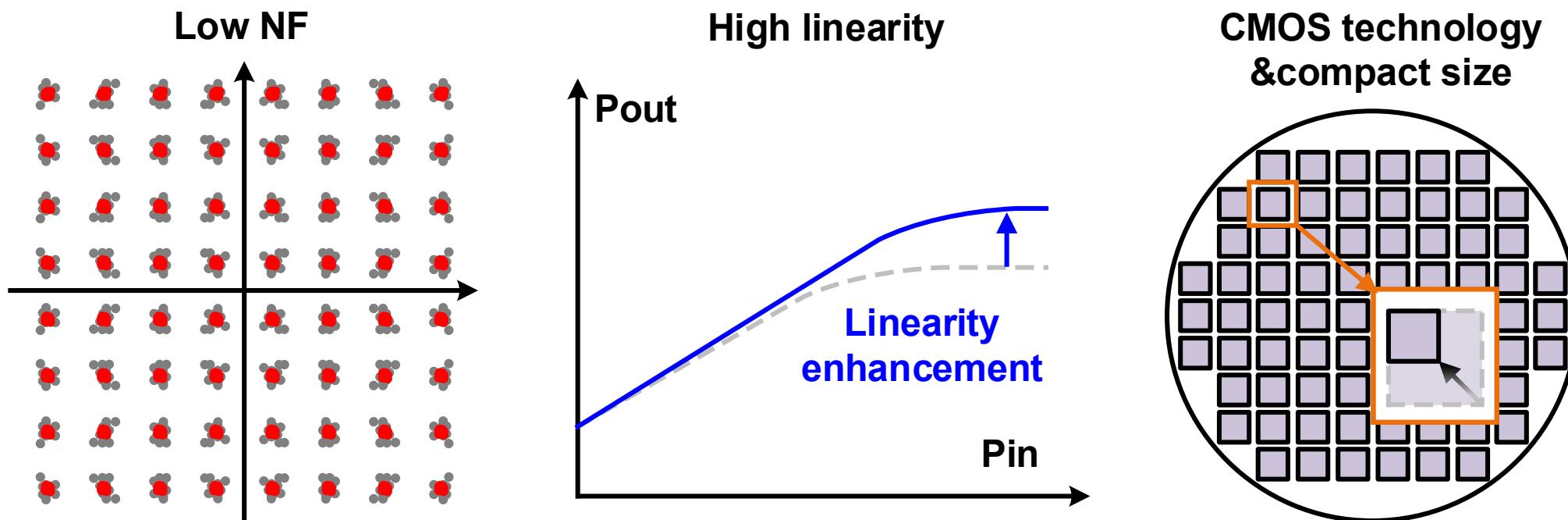


[P. Harati, et al., Microwave Magazine'17]

Introduction and Motivation

■ Design challenges for mm-wave LNA

- Low NF, high linearity and low cost



Introduction and Motivation

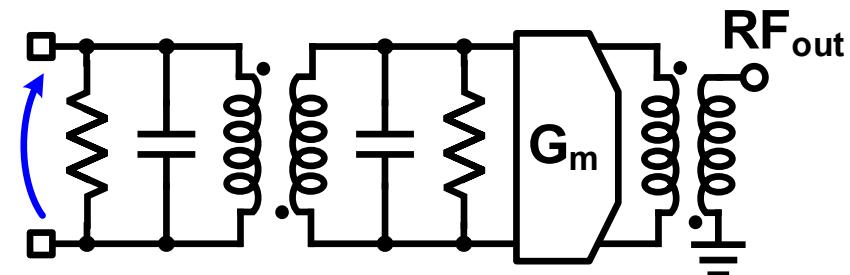
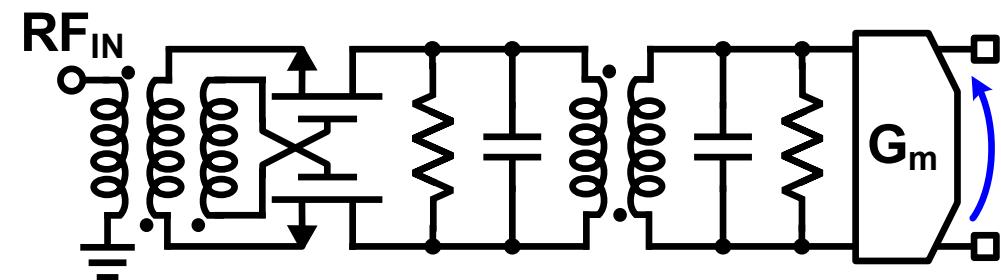
■ Transformer based g_m -boosting LNA

😊 High gain and broadband

😊 Compact size

😢 CG input leads to high NF

😢 Low linearity and high P_{dc}

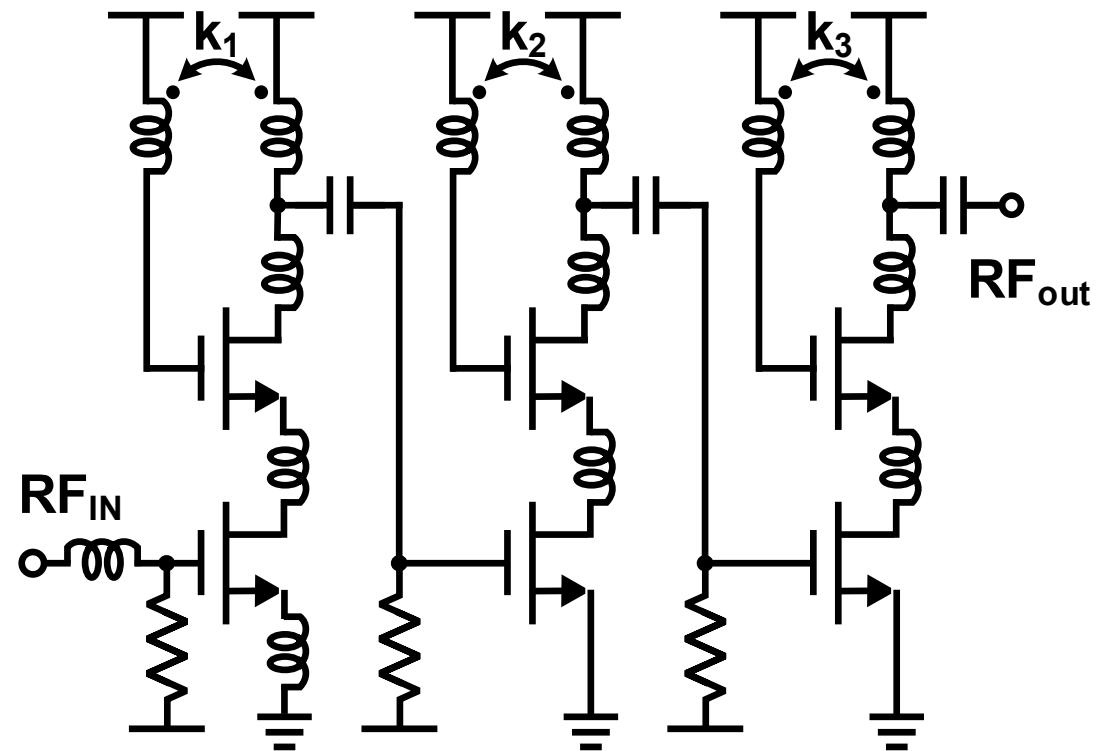


[M. Vigilante, et al., ISSCC'16]

Introduction and Motivation

■ Cascode LNA with g_m -boosting

- 😊 High gain with low P_{dc}
- 😊 Low noise figure
- 😢 Low linearity
- 😢 Large chip size

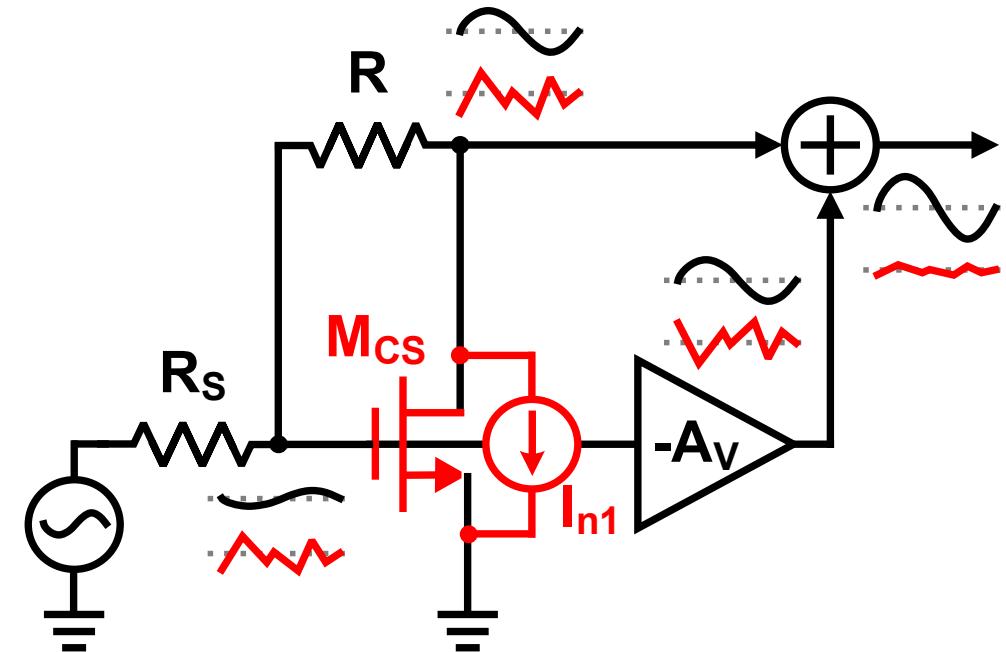


[L. Gao, et al., TMTT'20]

Introduction and Motivation

■ Resistive feedback noise-canceling LNA topology

- 😊 Noise of M_{CS} is canceled
- 😢 Adder is difficult to implement at high frequency
- 😢 Parasitics degrade noise cancellation

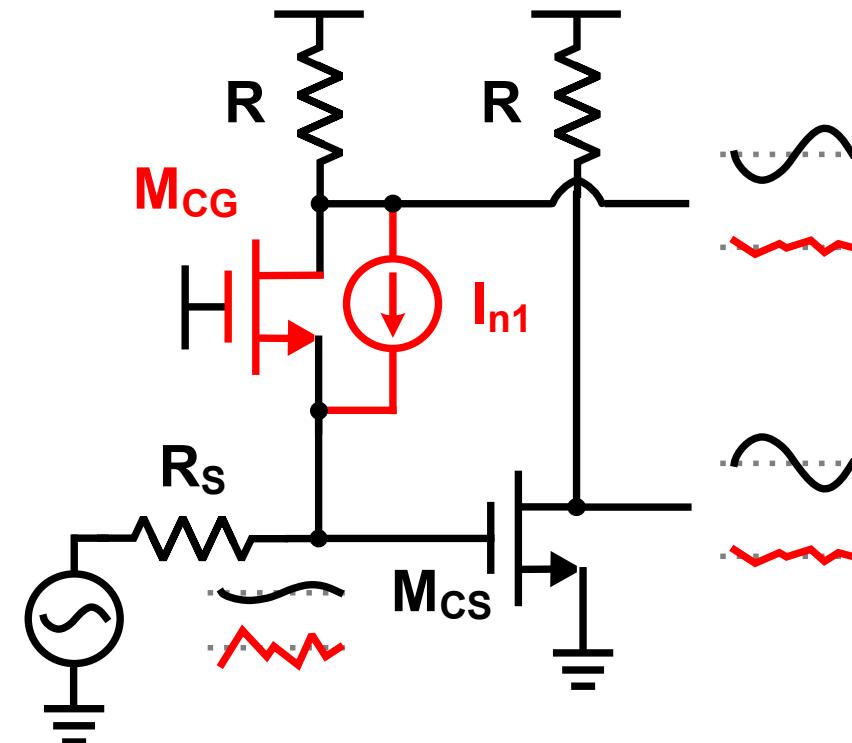


[F. Bruccoleri, et al., JSSC'04]

Introduction and Motivation

■ CG based noise-canceling LNA topology

- 😊 Noise of M_{CG} is canceled
- 😊 Differential output with high linearity
- 😢 Low Single stage gain
- 😢 Resistive load limits high frequency operation

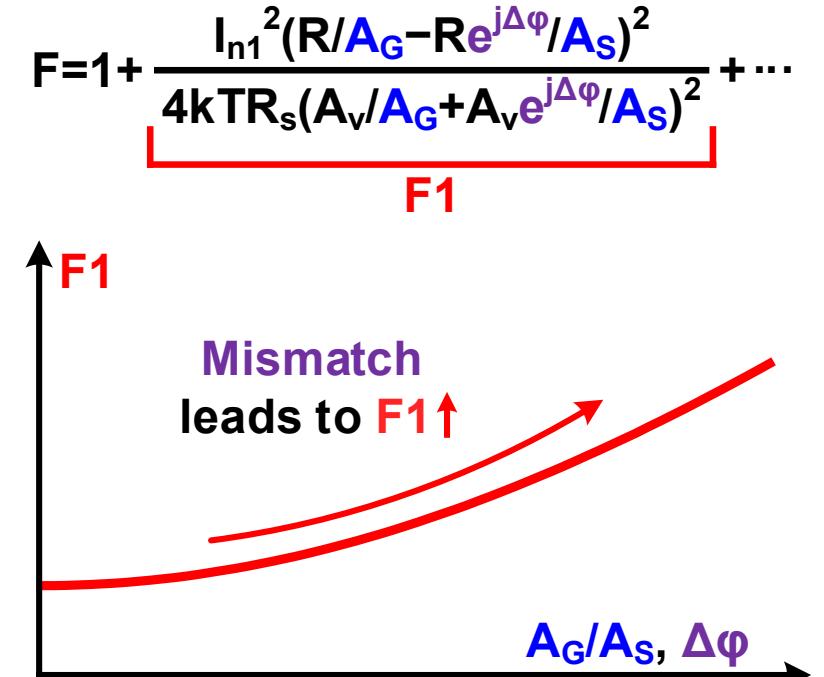
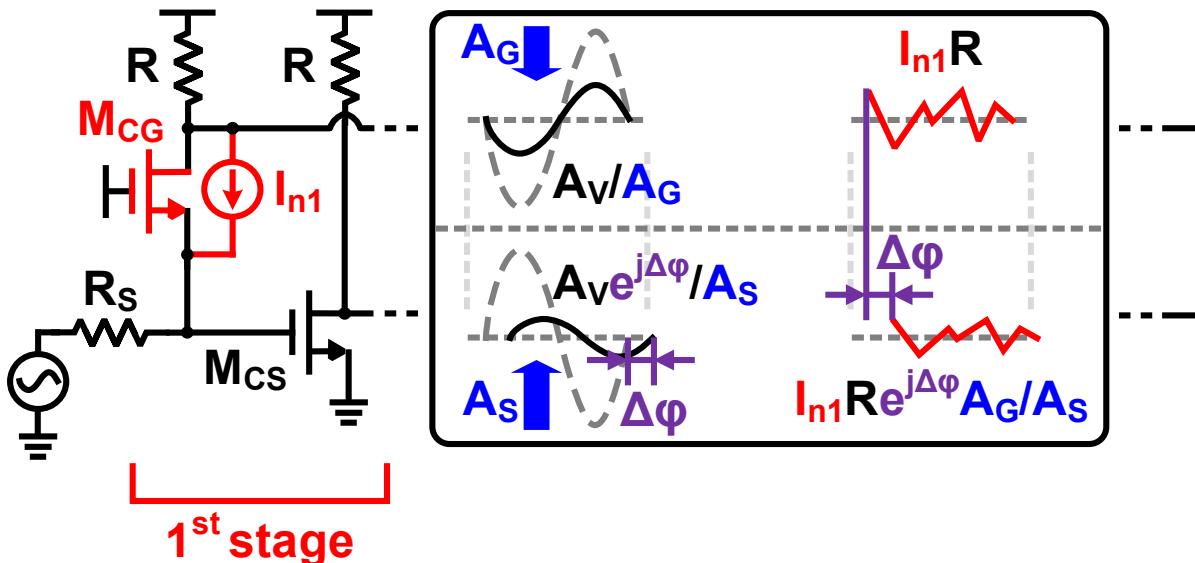


[S. Blaakmeer, et al., JSSC'08]

Introduction and Motivation

■ Limitation of the noise-canceling LNA topology

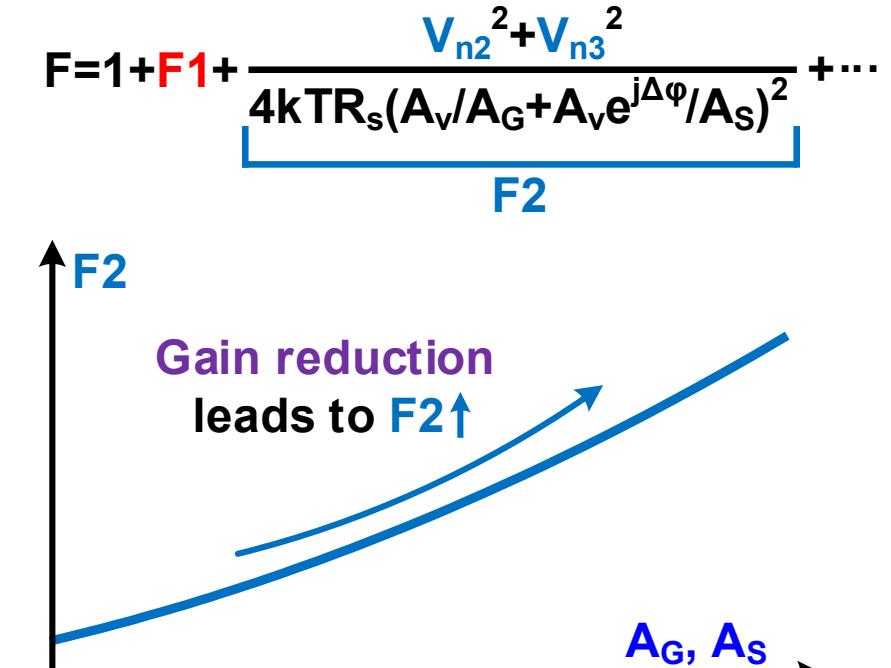
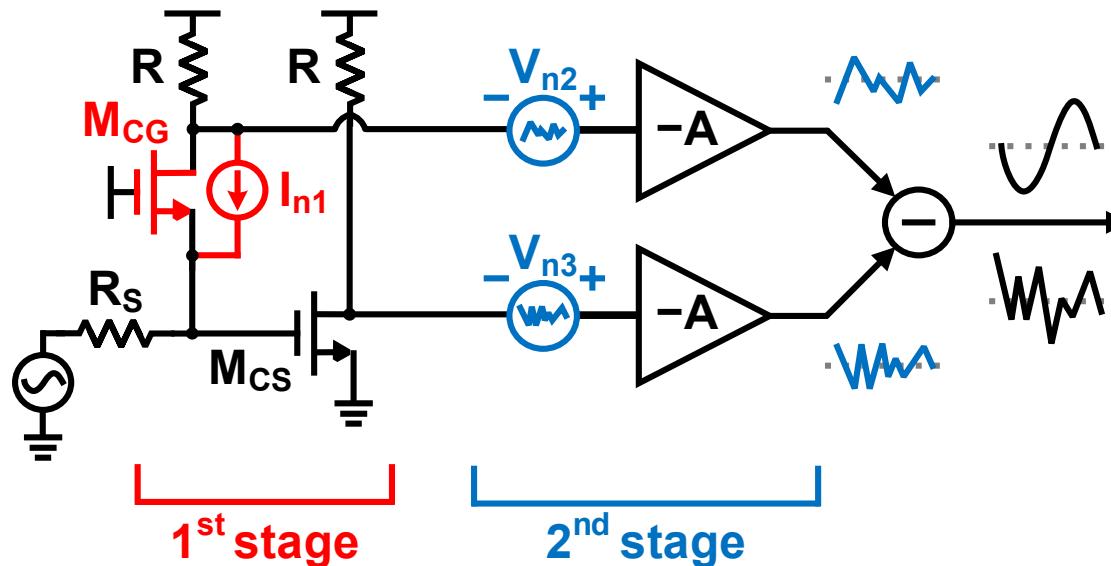
- Amplitude and phase imbalances are generated by the parasitics
- Noise cancellation is degraded



Introduction and Motivation

■ Limitation of the noise-canceling LNA topology

- Parasitics reduce the gain of the 1st stage
- 2nd stage noise contribution increases

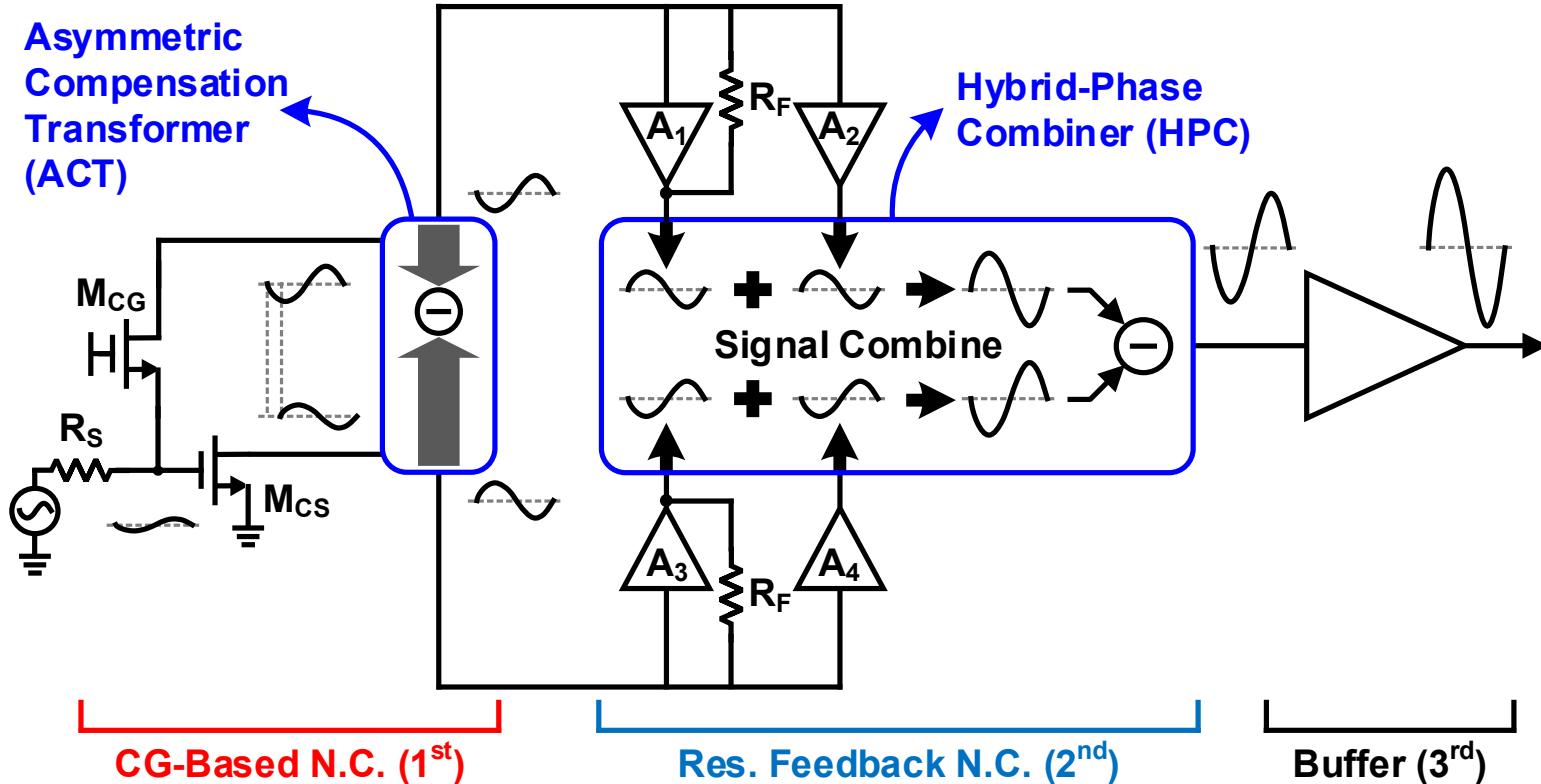


Outline

- Introduction and Motivation
- Deep-Noise-Canceling LNA Architecture
- Asymmetric CG Based Noise-Canceling
- Resistive Feedback Noise-Canceling
- LNA Implementation
- Measurement and Comparison
- Conclusion

Deep-Noise-Canceling LNA Architecture

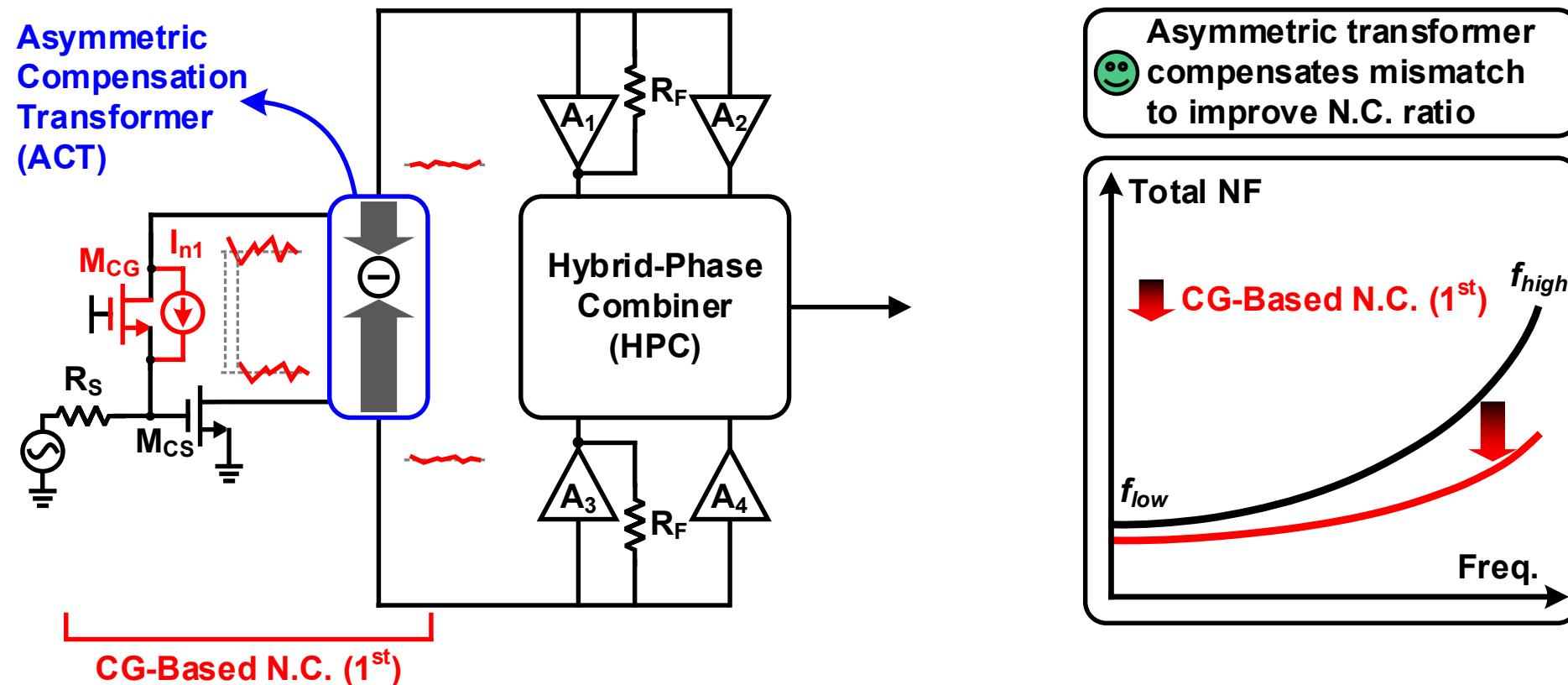
■ Proposed deep-noise-canceling LNA



- CG based noise-canceling stage using ACT
- Resistive feedback noise-canceling stage with 4-to-1 HPC

Deep-Noise-Canceling LNA Architecture

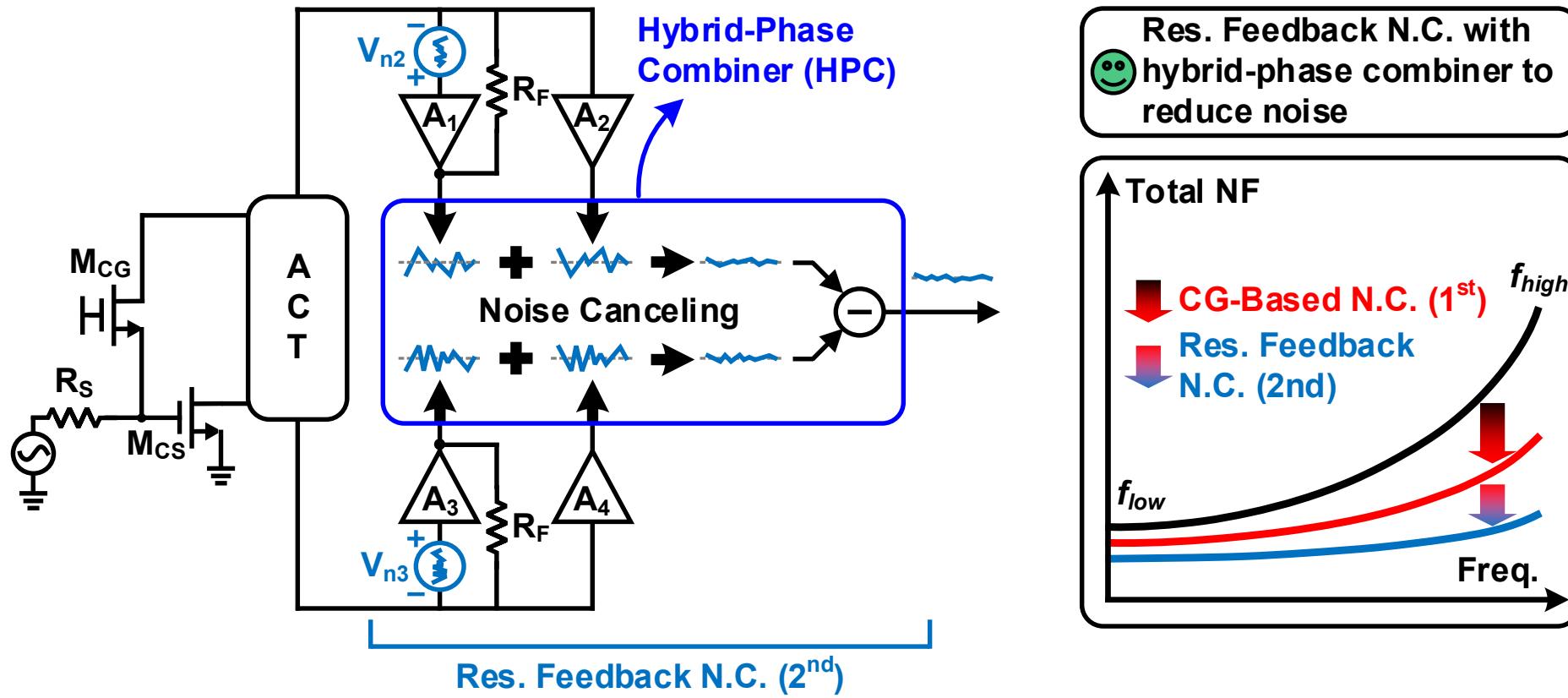
■ CG based noise-canceling using ACT



- Noise of M_{CG} can be fully canceled with the ACT compensation

Deep-Noise-Canceling LNA Architecture

■ Resistive feedback noise-canceling stage with HPC



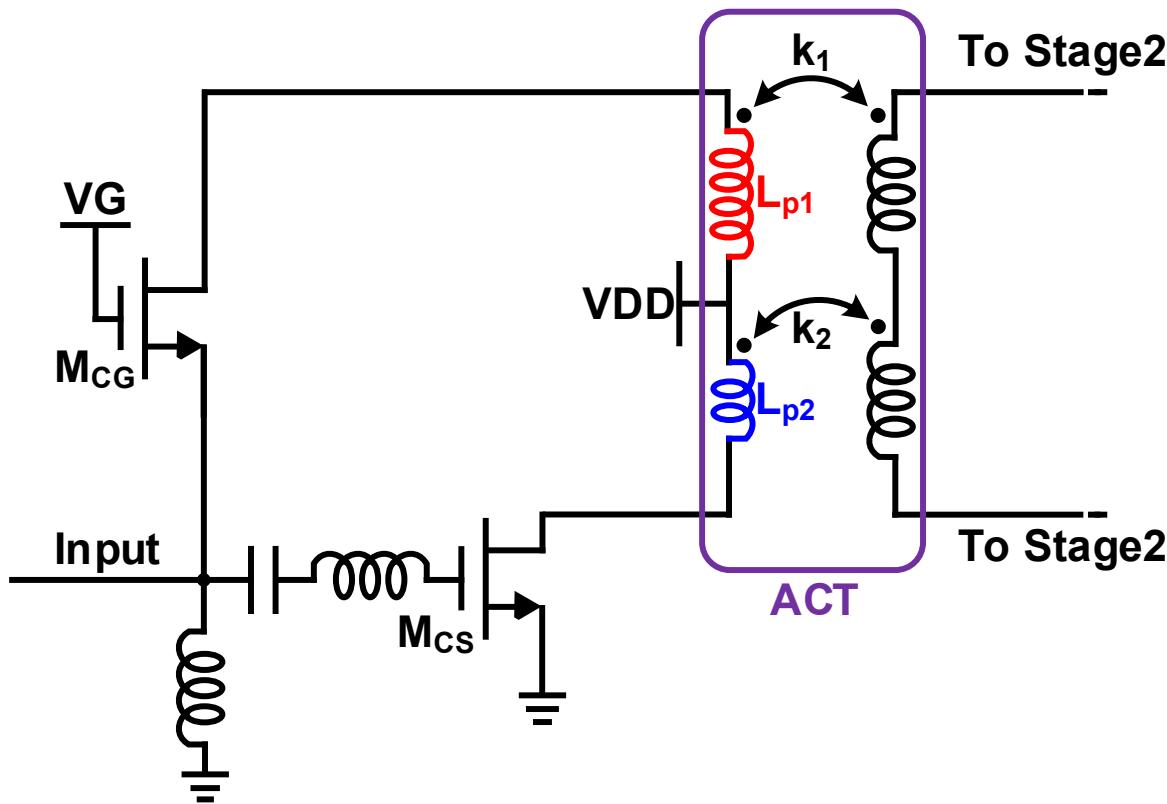
- V_{n2} & V_{n3} can be canceled by the HPC

Outline

- Introduction and Motivation
- Deep-Noise-Canceling LNA Architecture
- **Asymmetric CG Based Noise-Canceling**
- Resistive Feedback Noise-Canceling
- LNA Implementation
- Measurement and Comparison
- Conclusion

Asymmetric CG Based Noise-Canceling

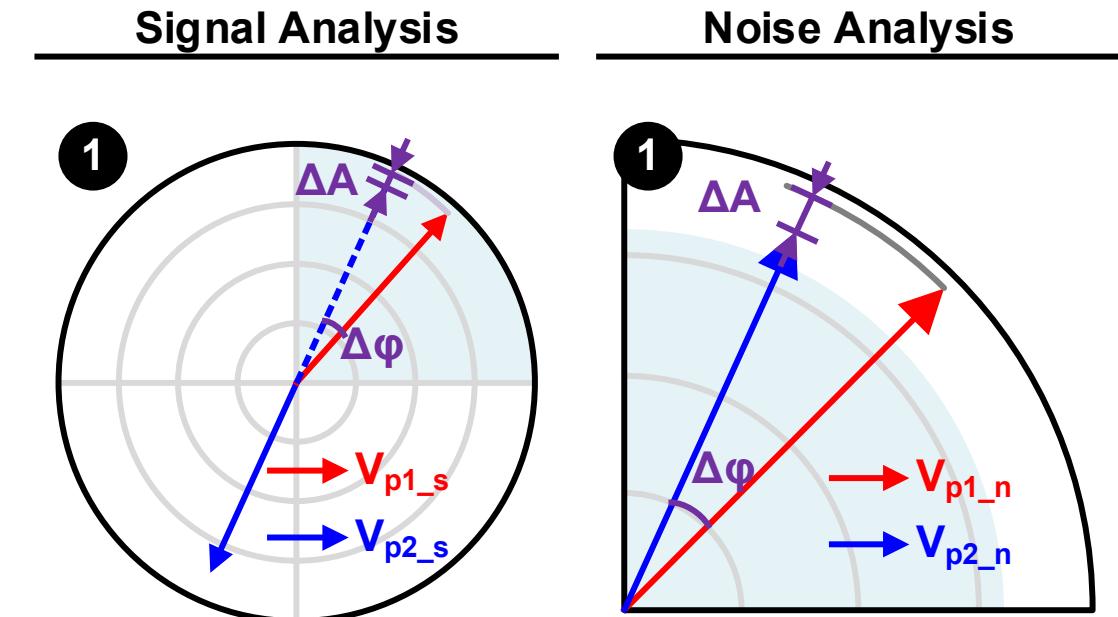
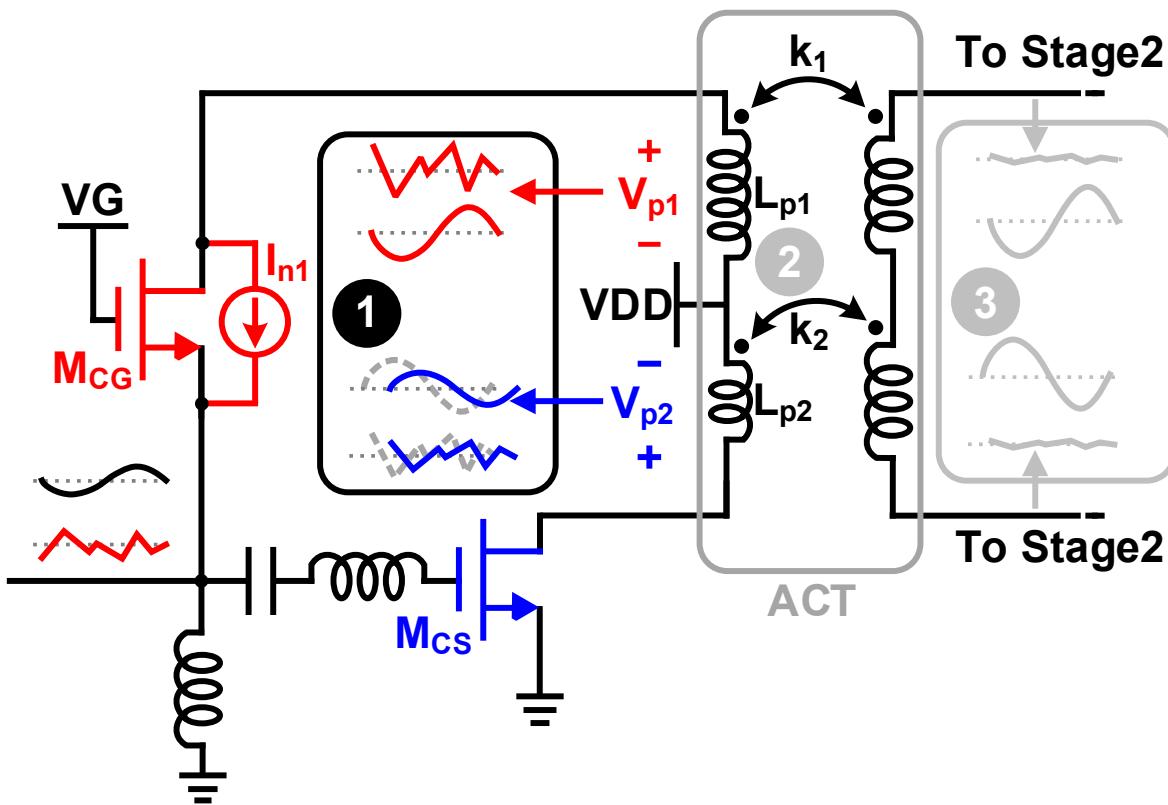
■ Architecture



- CG-CS noise-canceling stage
- ACT is introduced to combine the signal in CG and CS paths
- Asymmetric center-tap on ACT
 - Divide L_{P1} and L_{P2}
 - Compensate the amplitude and phase mismatch

Asymmetric CG Based Noise-Canceling

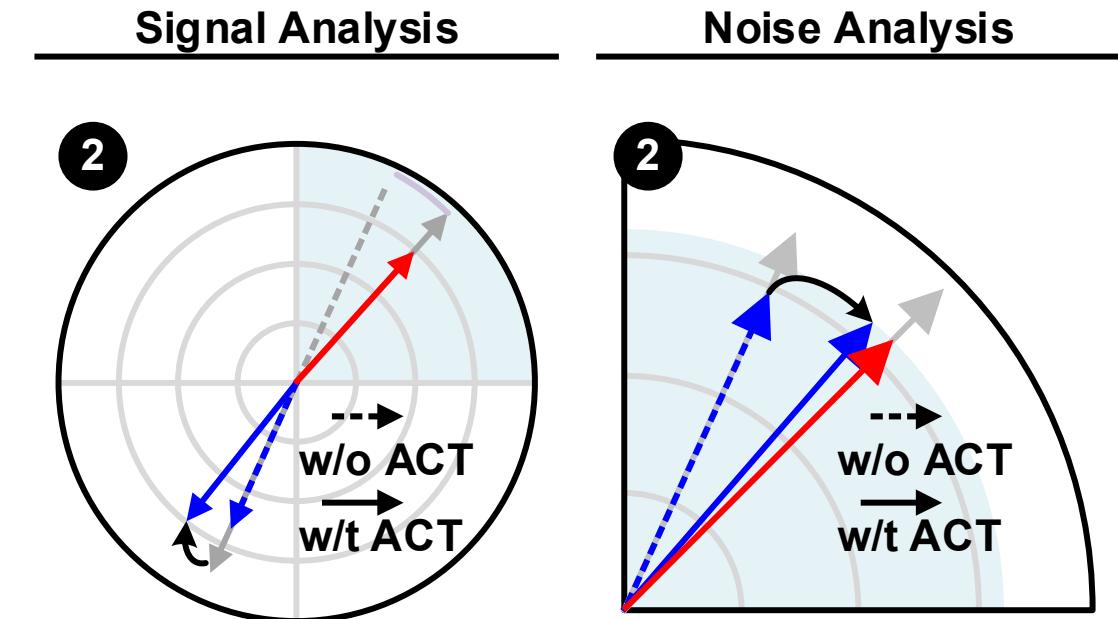
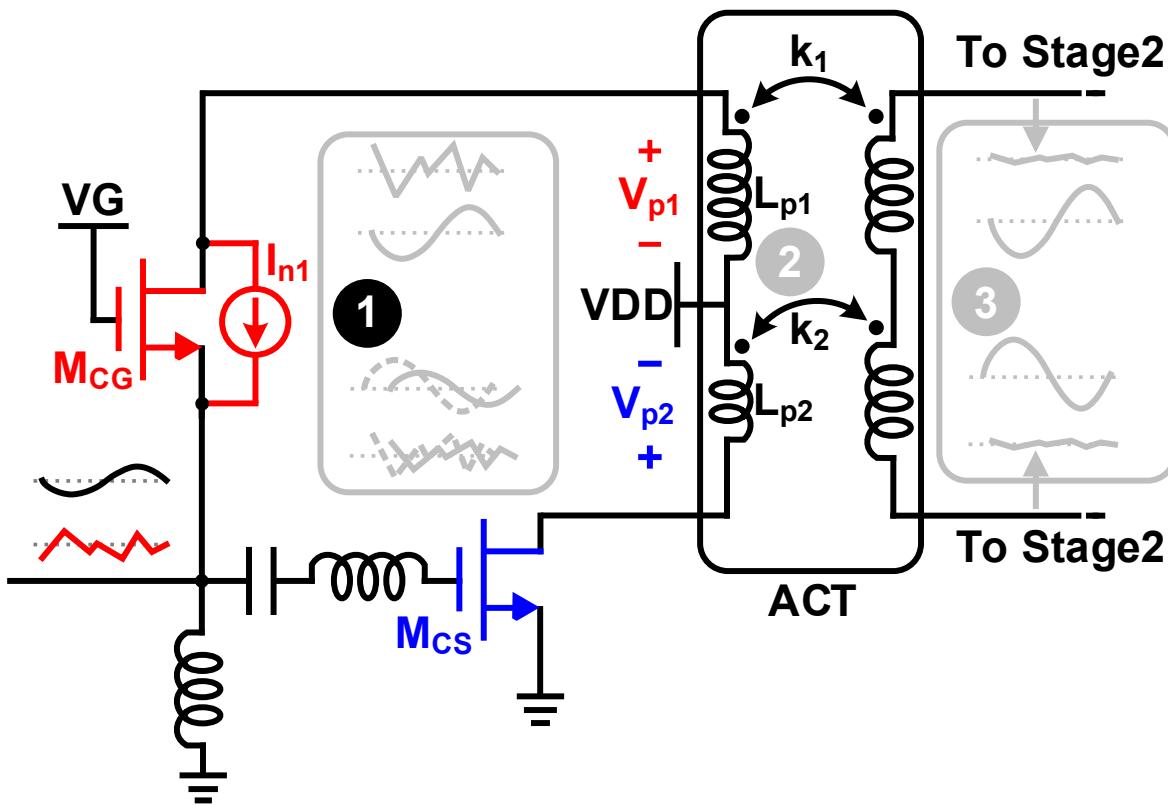
■ Signal and noise analysis



- Amplitude/phase mismatches exist between the CG and CS paths

Asymmetric CG Based Noise-Canceling

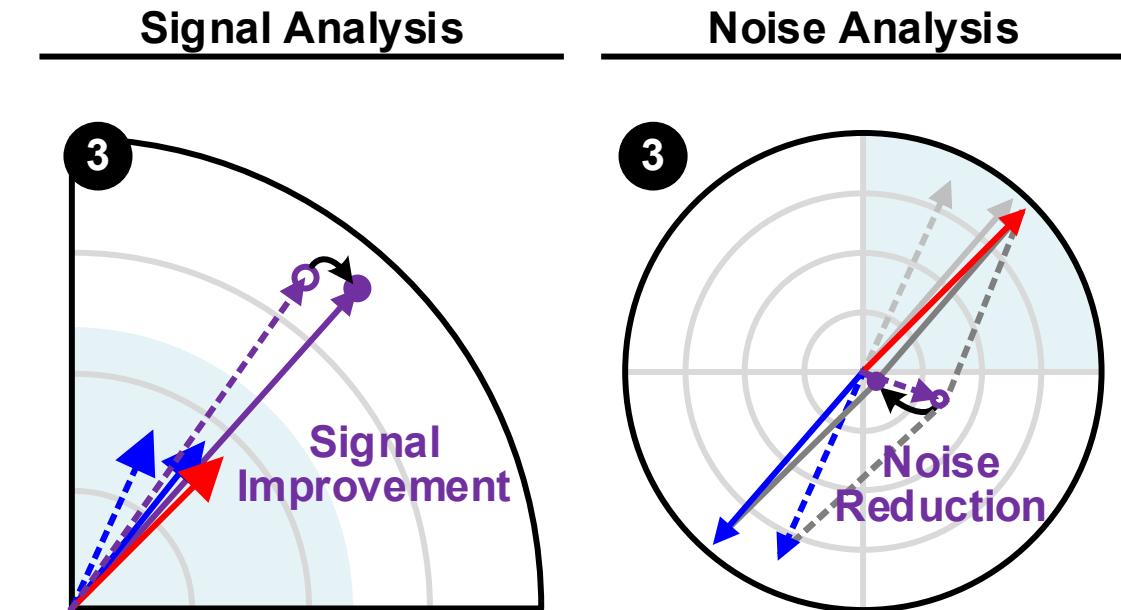
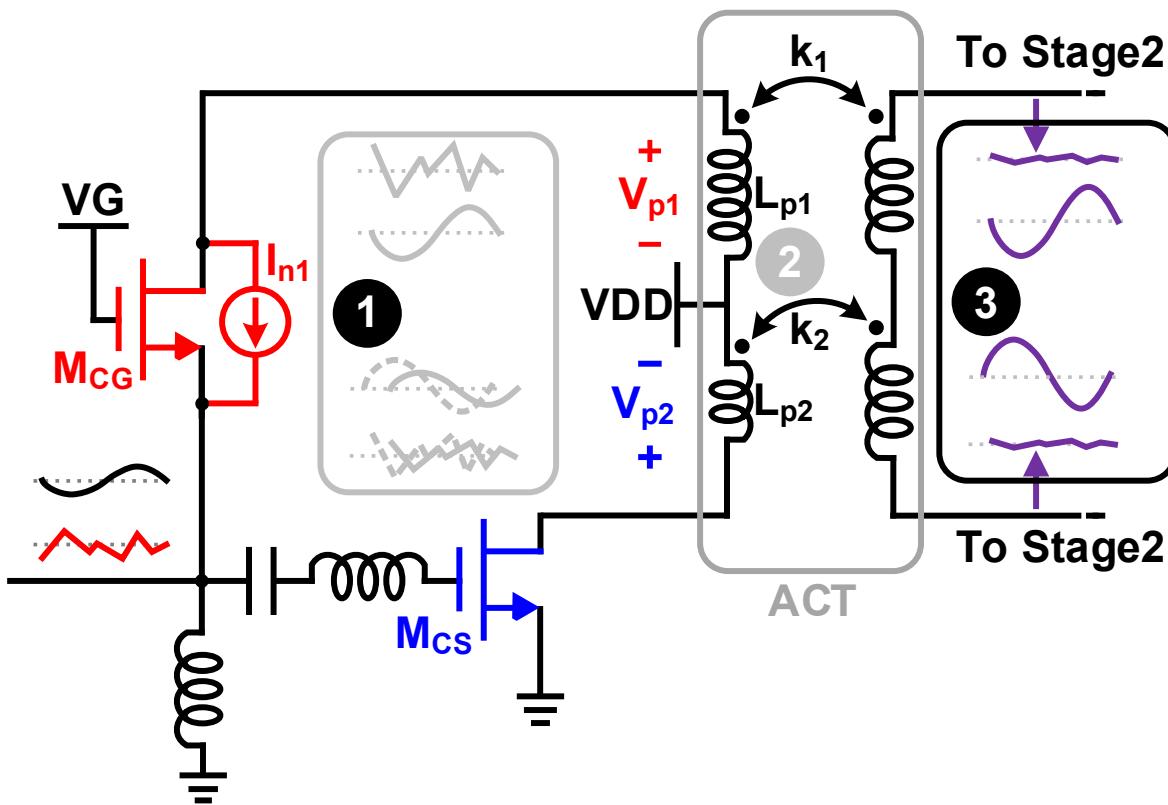
■ ACT operation



- Different values of L_{p1} & L_{p2} introduce the amp./phase compensation

Asymmetric CG Based Noise-Canceling

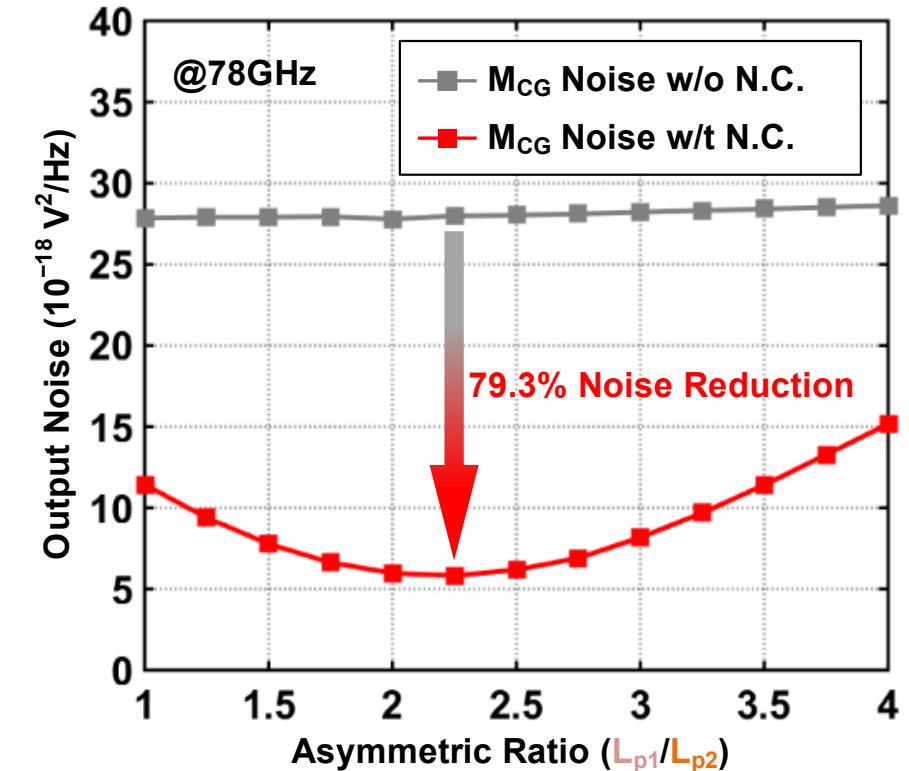
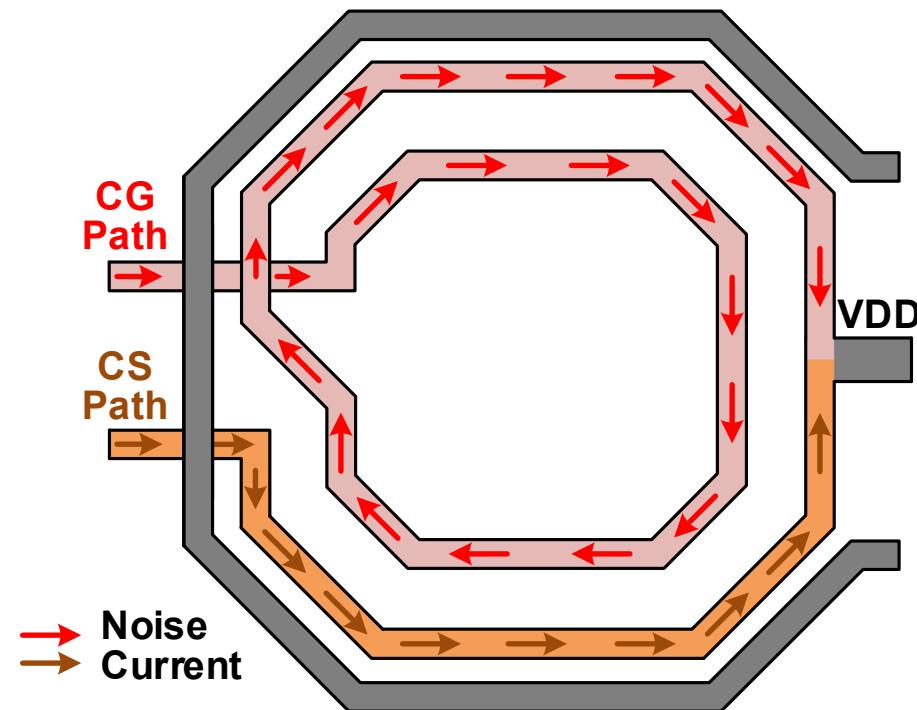
■ Signal and noise output



- Signal combination and noise reduction

Asymmetric CG Based Noise-Canceling

■ ACT Implementation



- Asymmetric center-tap divides the L_{p1} and L_{p2}
- Optimized value of L_{p1}/L_{p2} enhances the noise canceling

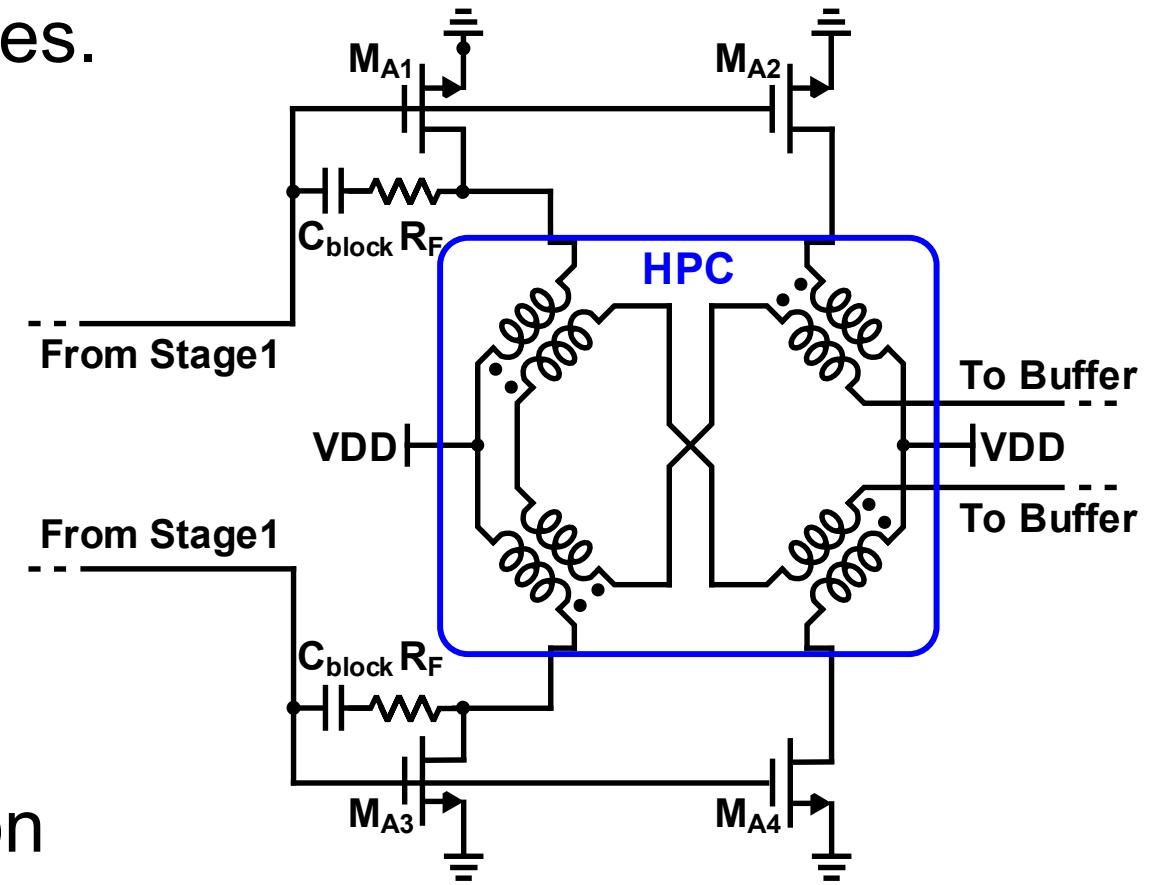
Outline

- Introduction and Motivation
- Deep-Noise-Canceling LNA Architecture
- Asymmetric CG Based Noise-Canceling
- Resistive Feedback Noise-Canceling
- LNA Implementation
- Measurement and Comparison
- Conclusion

Resistive Feedback Noise-Canceling

■ Resistive feedback noise-canceling topology

- Differential signal inputs to two res. feedback noise-canceling paths
- In-phase synthesis is desired for noise cancellation
- Anti-phase synthesis is desired for signal combination
- HPC achieves the above function



Resistive Feedback Noise-Canceling

■ Signal analysis

- Output signals of 4 transistor:

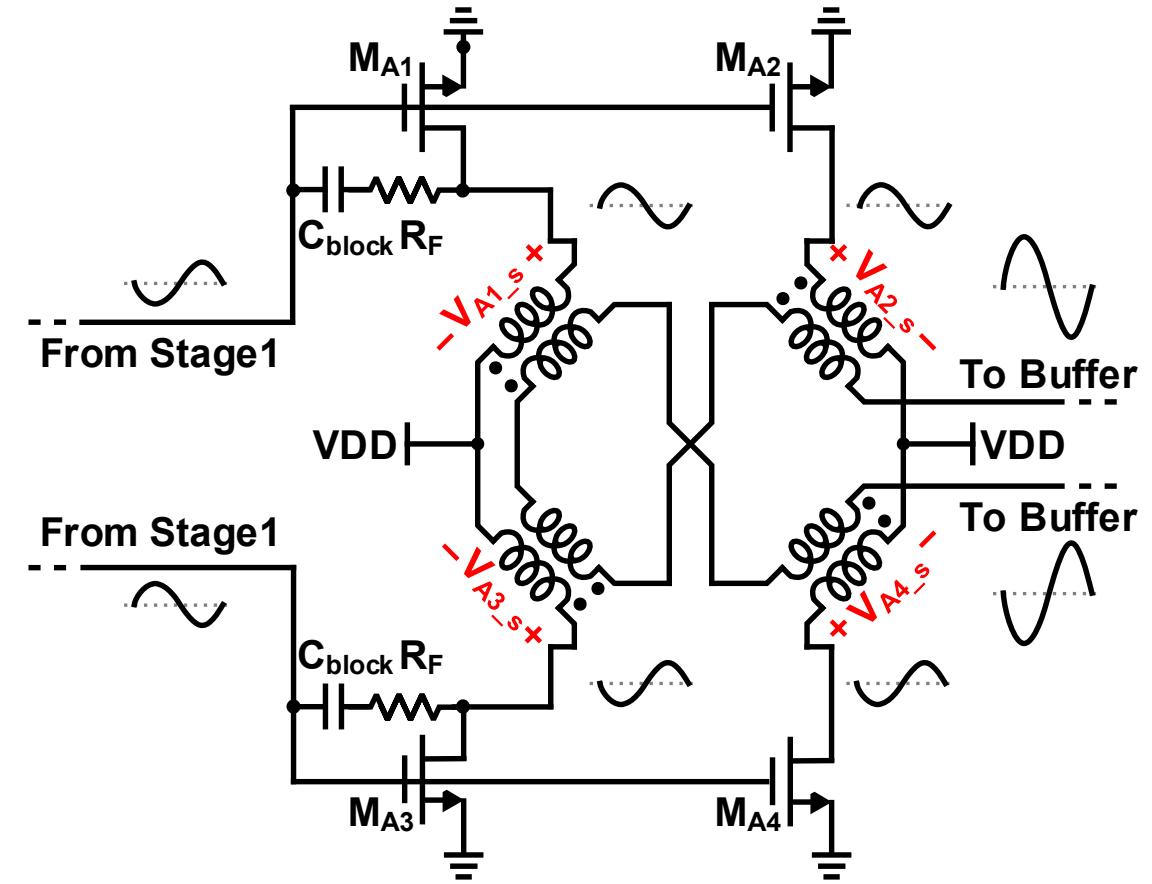
$$\rightarrow V_{A1_s} = V_{A2_s} = V_s$$

$$\rightarrow V_{A3_s} = V_{A4_s} = -V_s$$

- HPC achieves:

$$\begin{aligned} V_{out_s} &= V_{A1_s} + V_{A2_s} - (V_{A3_s} + V_{A4_s}) \\ &= 4V_s \end{aligned}$$

- Output signals are combined



Resistive Feedback Noise-Canceling

■ Noise analysis

- Output signals of 4 transistor:

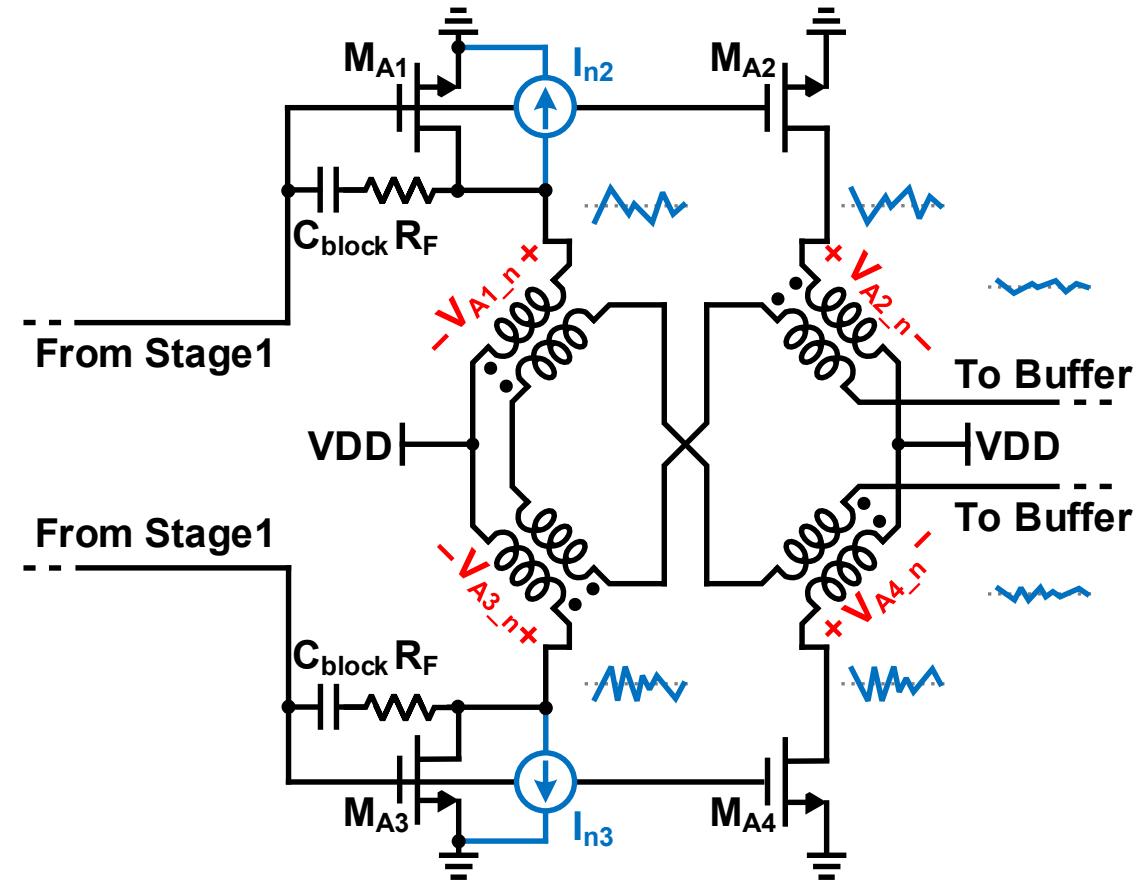
$$\rightarrow V_{A1_n} = -V_{A2_n} = V_{n2}$$

$$\rightarrow V_{A3_n} = -V_{A4_n} = V_{n3}$$

- HPC achieves:

$$V_{out_n} = V_{A1_n} + V_{A2_n} - (V_{A3_n} + V_{A4_n}) \\ = 0$$

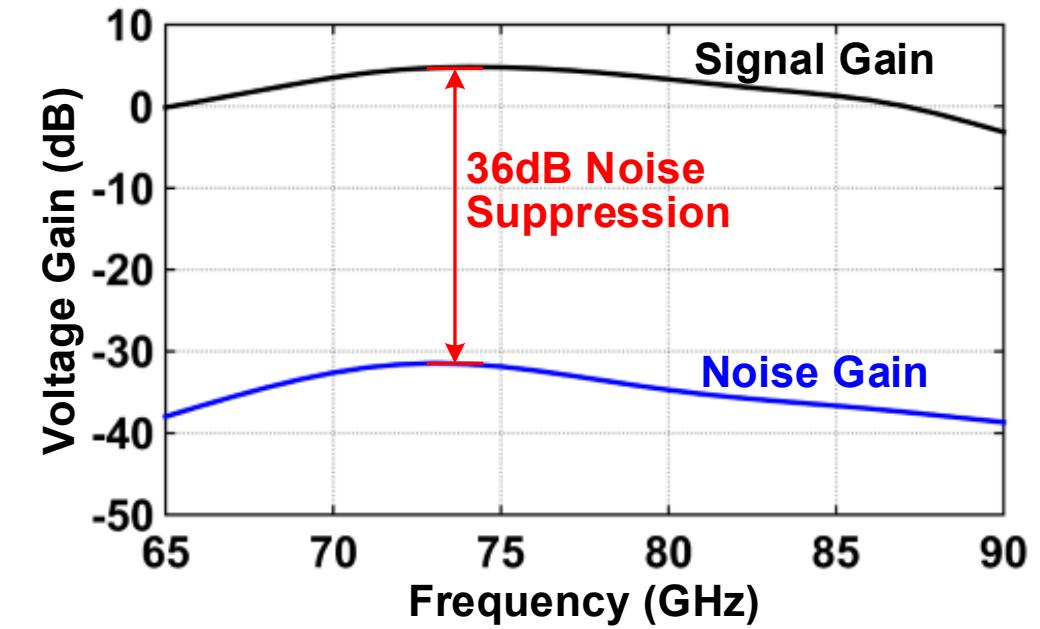
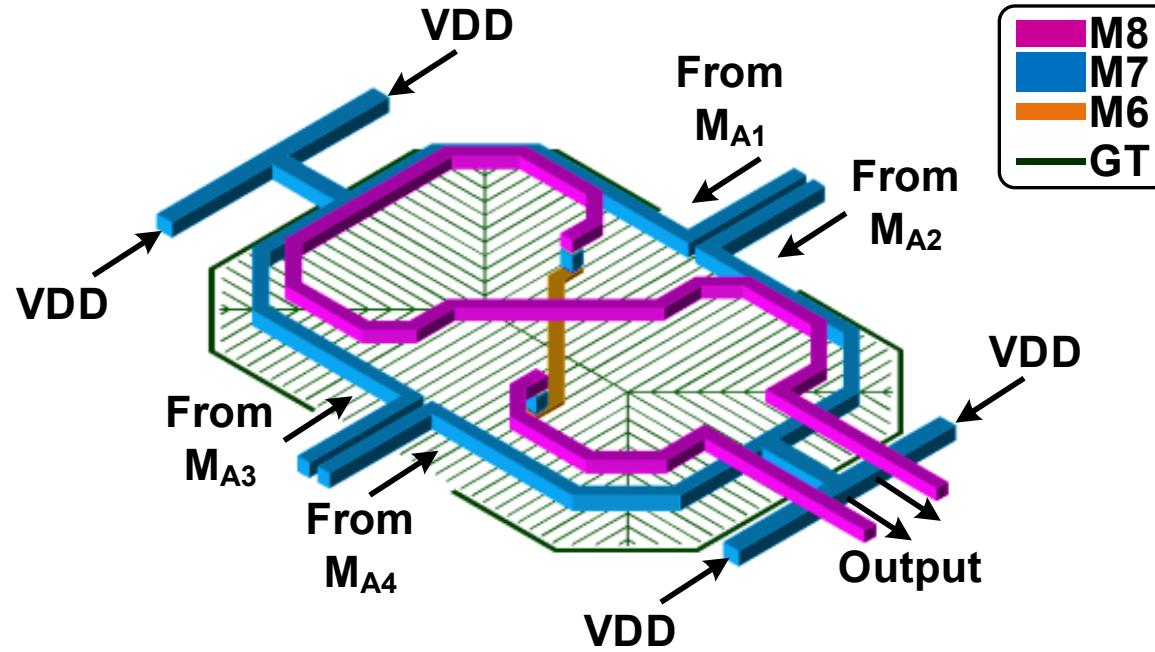
- Output noise are canceled



Resistive Feedback Noise-Canceling

■ HPC Implementation

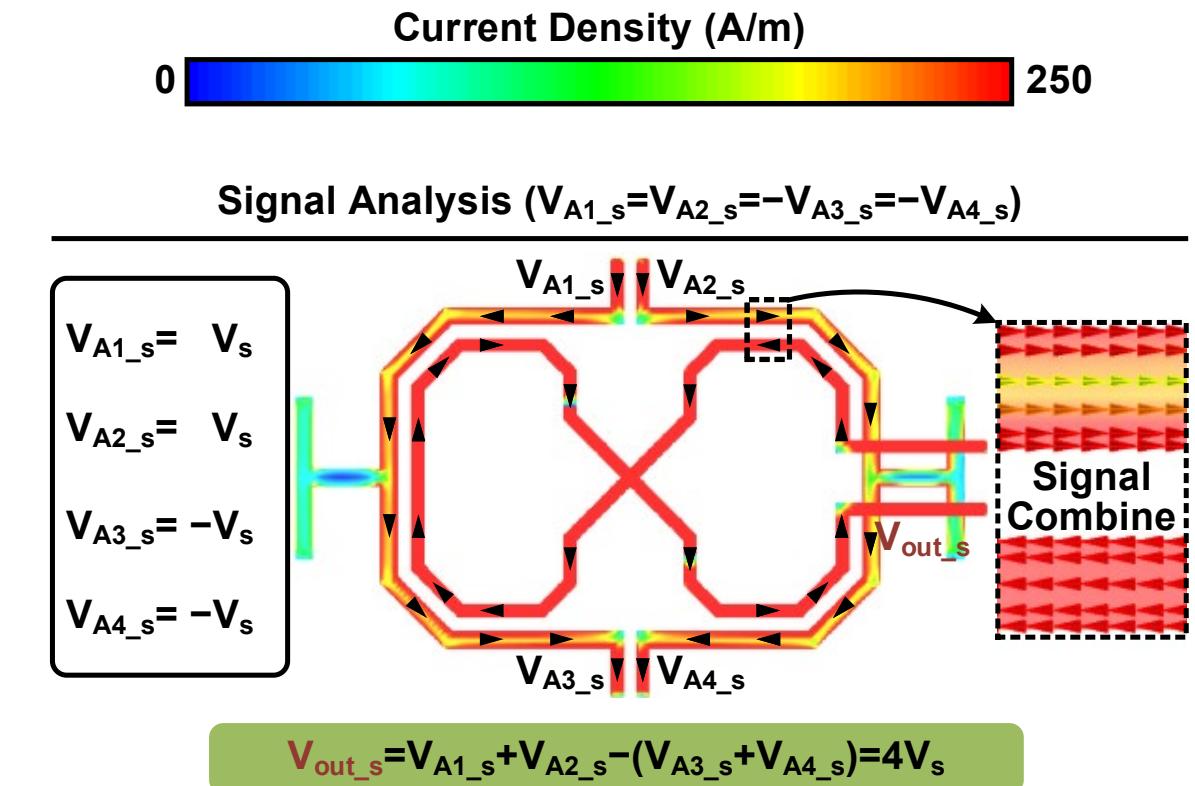
- Primary coil has two pairs of input ports on the opposite sides
- A crossover in secondary coil achieves in-/anti-phase synthesis



Resistive Feedback Noise-Canceling

■ Current density of the 4-to-1 HPC

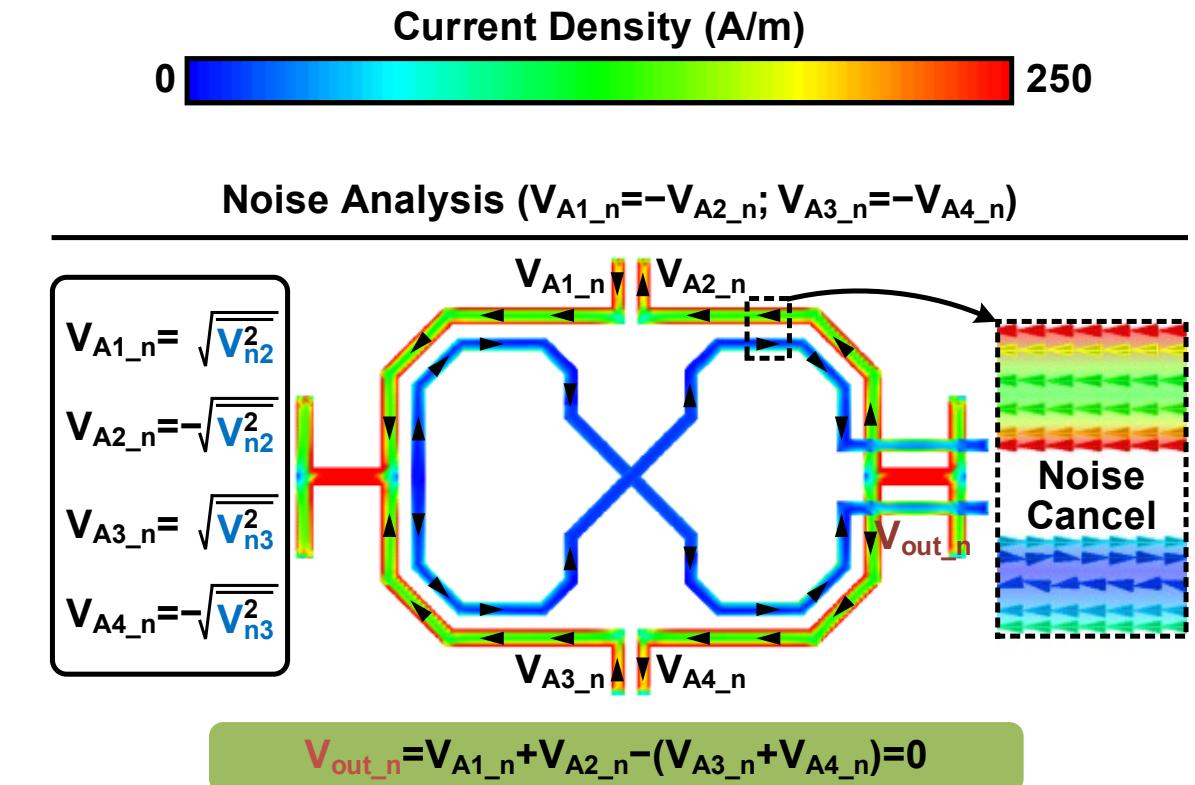
- Signal Input condition:
 $\rightarrow V_{A1_s} = V_{A2_s} = -V_{A3_s} = -V_{A4_s}$
- Induced current in secondary coil is in the same direction
- Signal can be enhanced at output terminal



Resistive Feedback Noise-Canceling

■ Current density of the 4-to-1 HPC

- Signal Input condition:
 $\rightarrow V_{A1_n} = -V_{A2_n}; V_{A3_n} = -V_{A4_n}$
- Induced current is canceled in secondary coil
- Noise can be canceled at output terminal

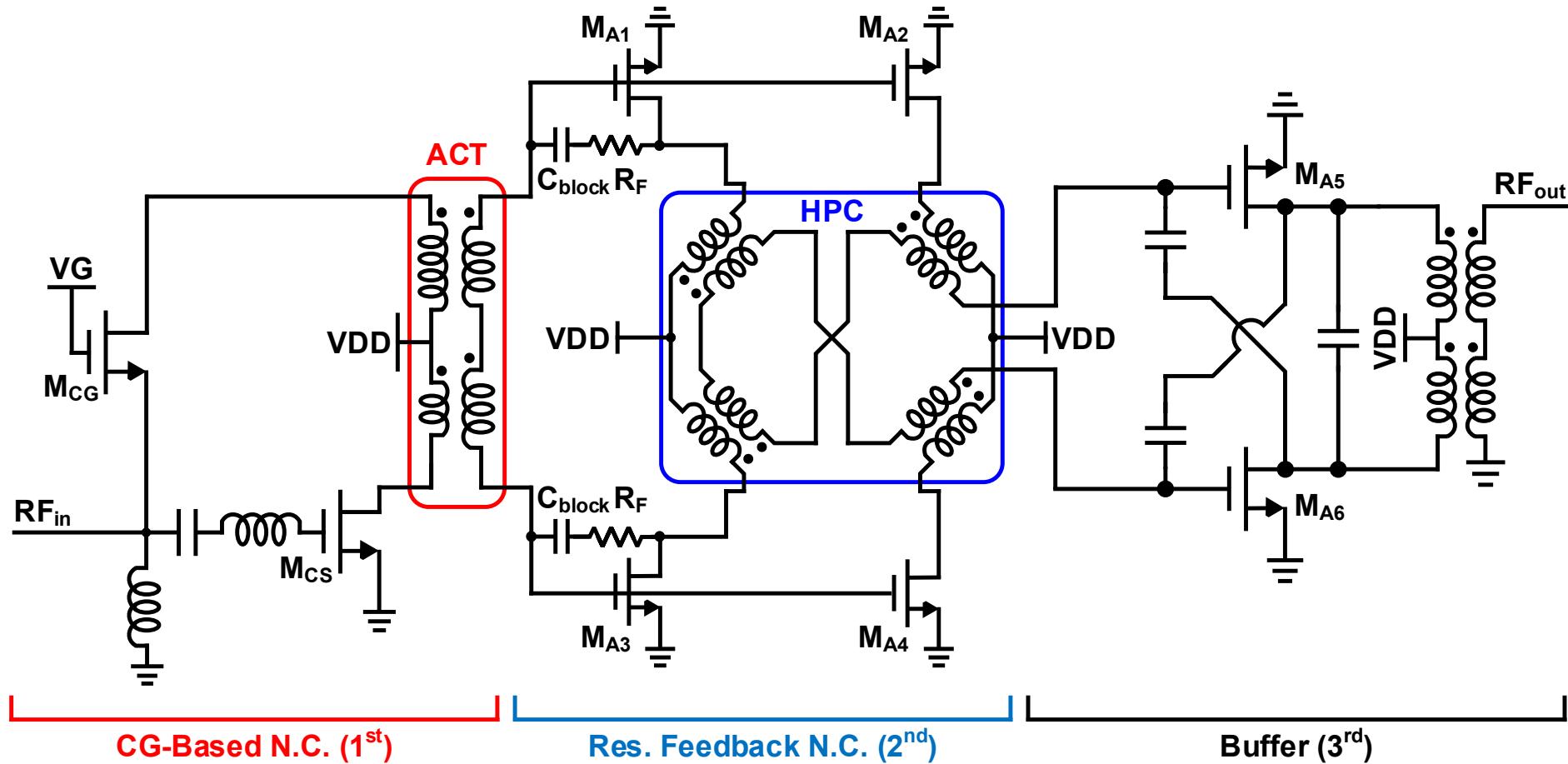


Outline

- Introduction and Motivation
- Deep-Noise-Canceling LNA Architecture
- Asymmetric CG Based Noise-Canceling
- Resistive Feedback Noise-Canceling
- **LNA Implementation**
- Measurement and Comparison
- Conclusion

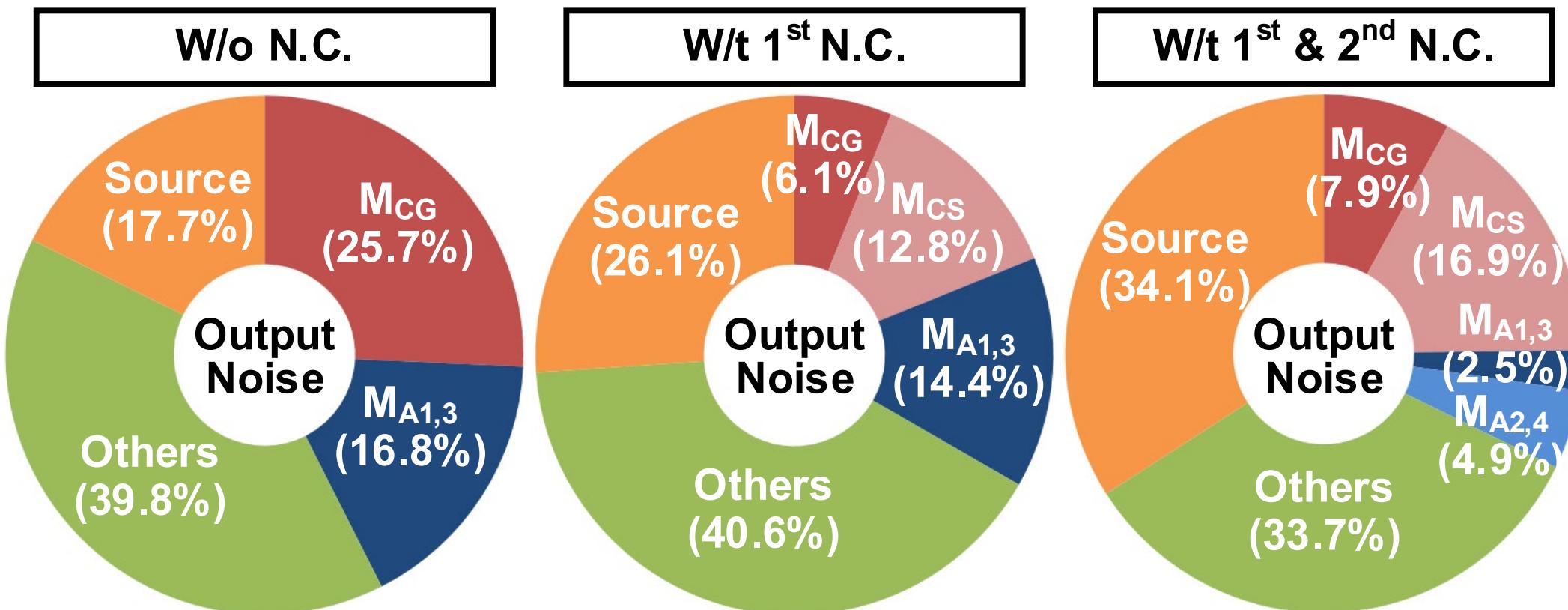
LNA Implementation

■ Schematic of the deep-noise-canceling LNA



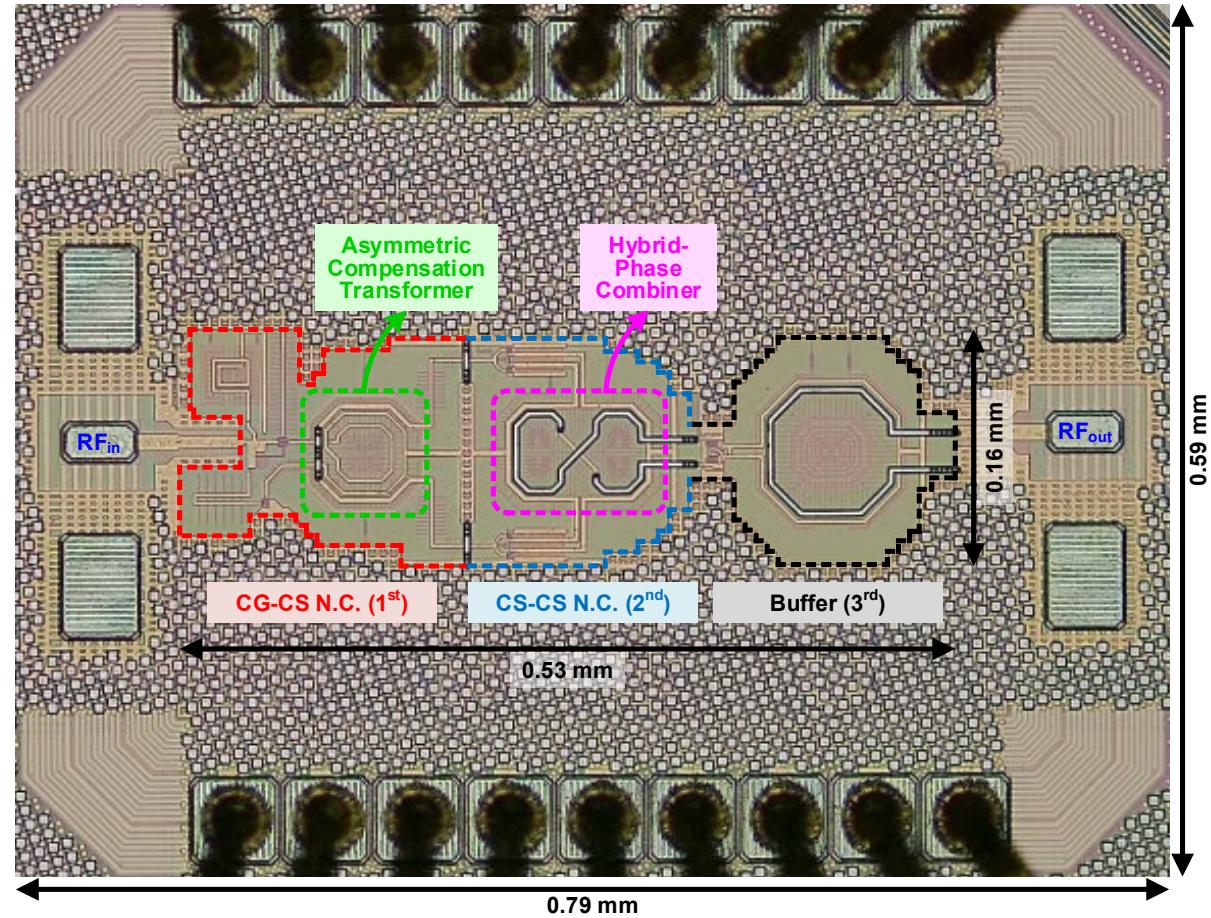
LNA Implementation

■ Noise contribution



Chip Micrograph

- Conventional 40nm CMOS
- Chip size: 0.79mm by 0.59mm
- Core size: 0.53mm by 0.16mm
- Supply: 1.1V



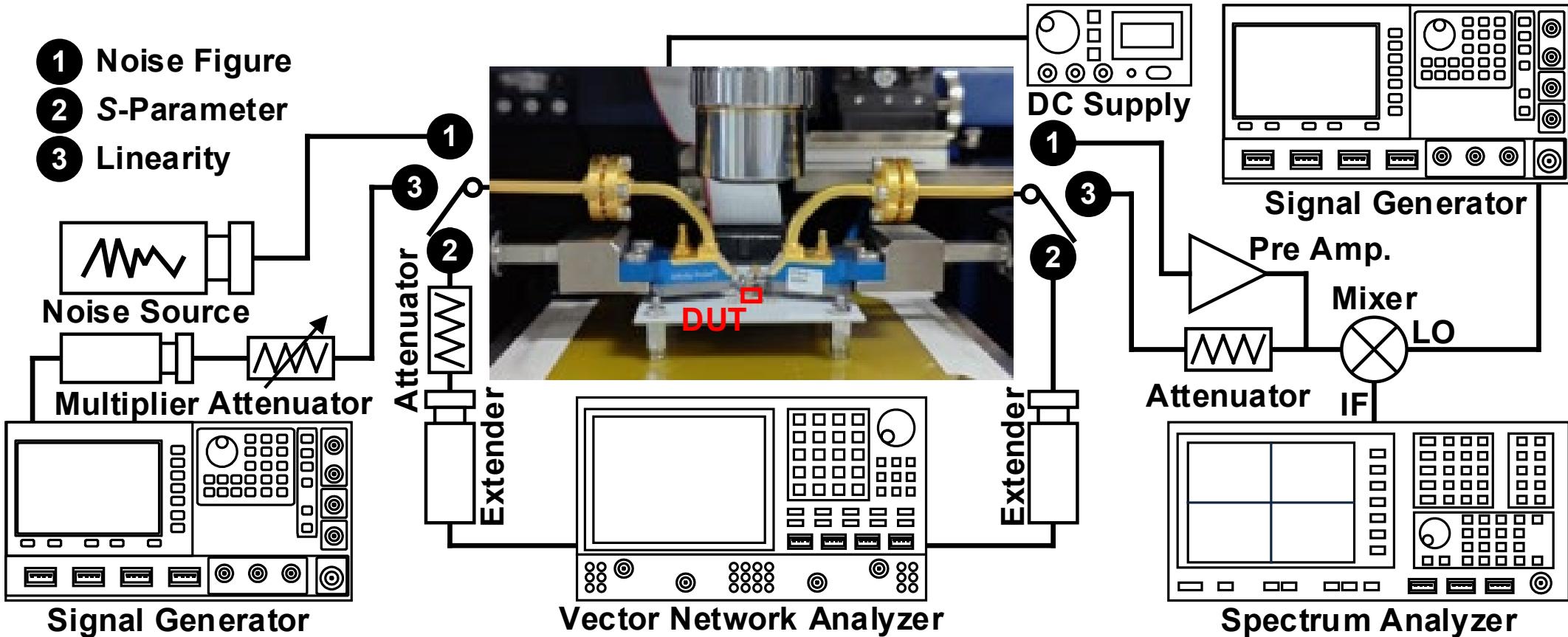
25.3: A 4.8dB NF, 70-to-86GHz Deep-Noise-Canceling LNA Using Asymmetric Compensation Transformer and 4-to-1 Hybrid-Phase Combiner in 40nm CMOS

Outline

- Introduction and Motivation
- Deep-Noise-Canceling LNA Architecture
- Asymmetric CG Based Noise-Canceling
- Resistive Feedback Noise-Canceling
- LNA Implementation
- Measurement and Comparison
- Conclusion

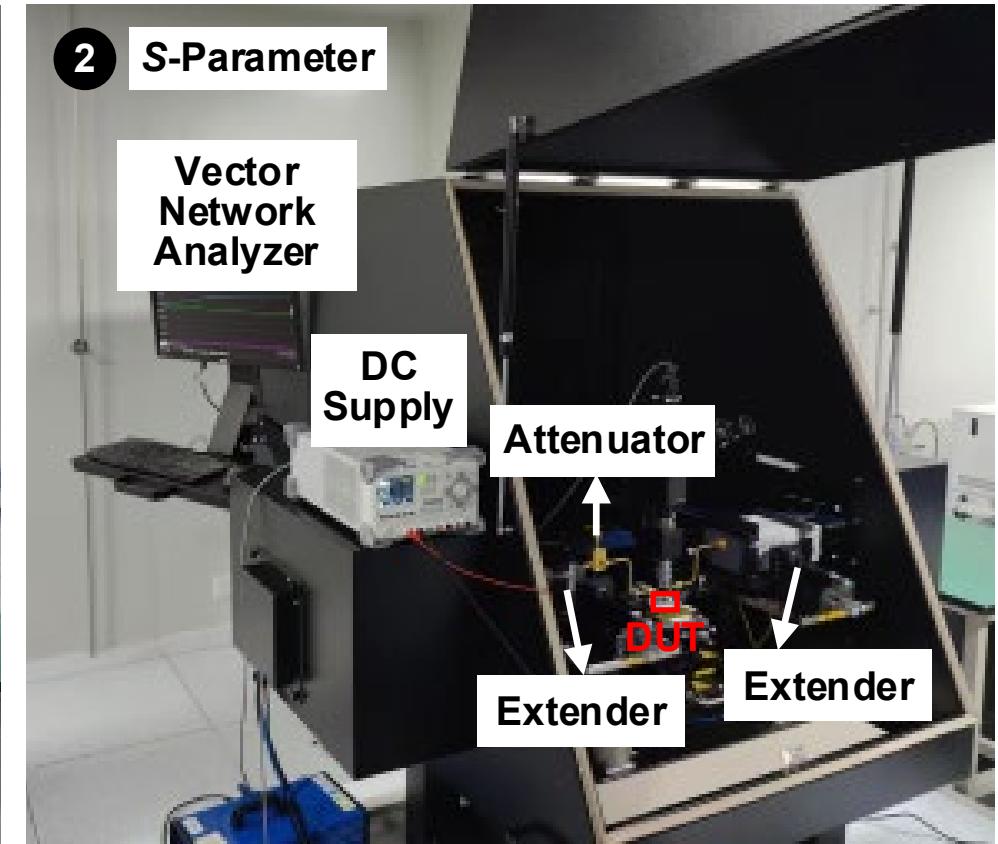
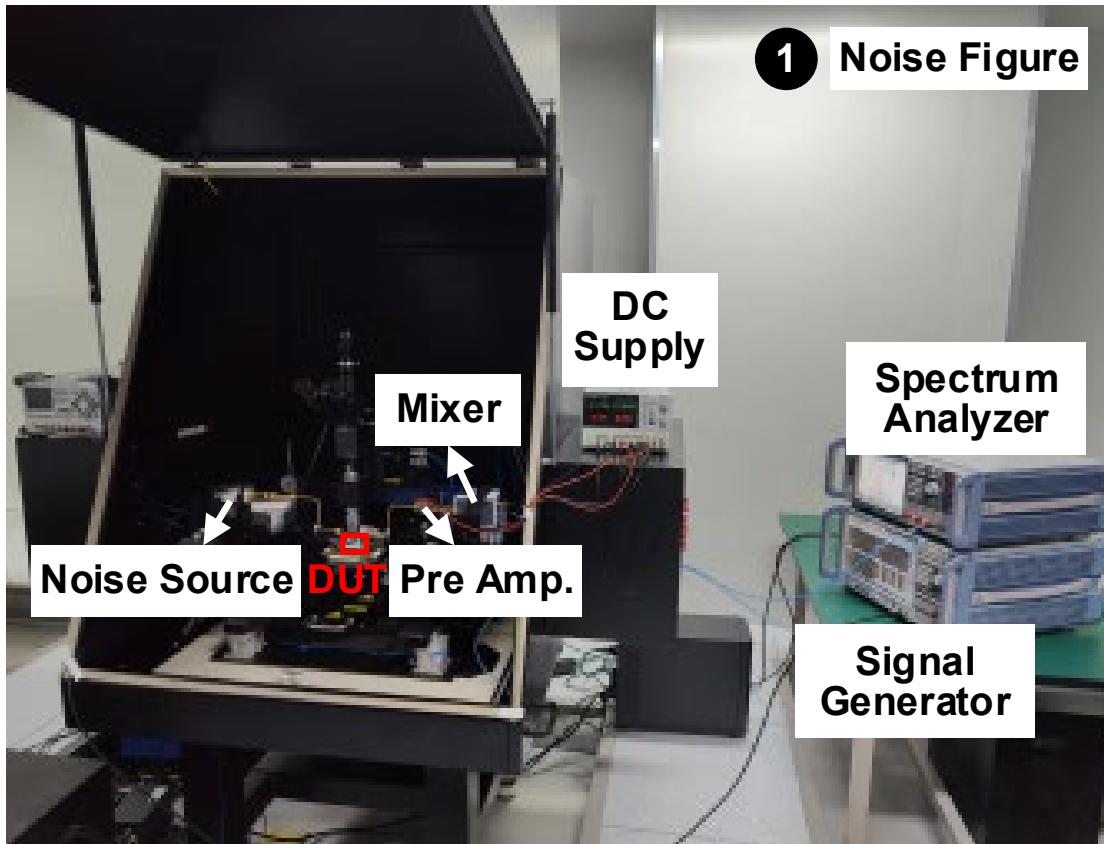
Measurement

■ Measurement setup



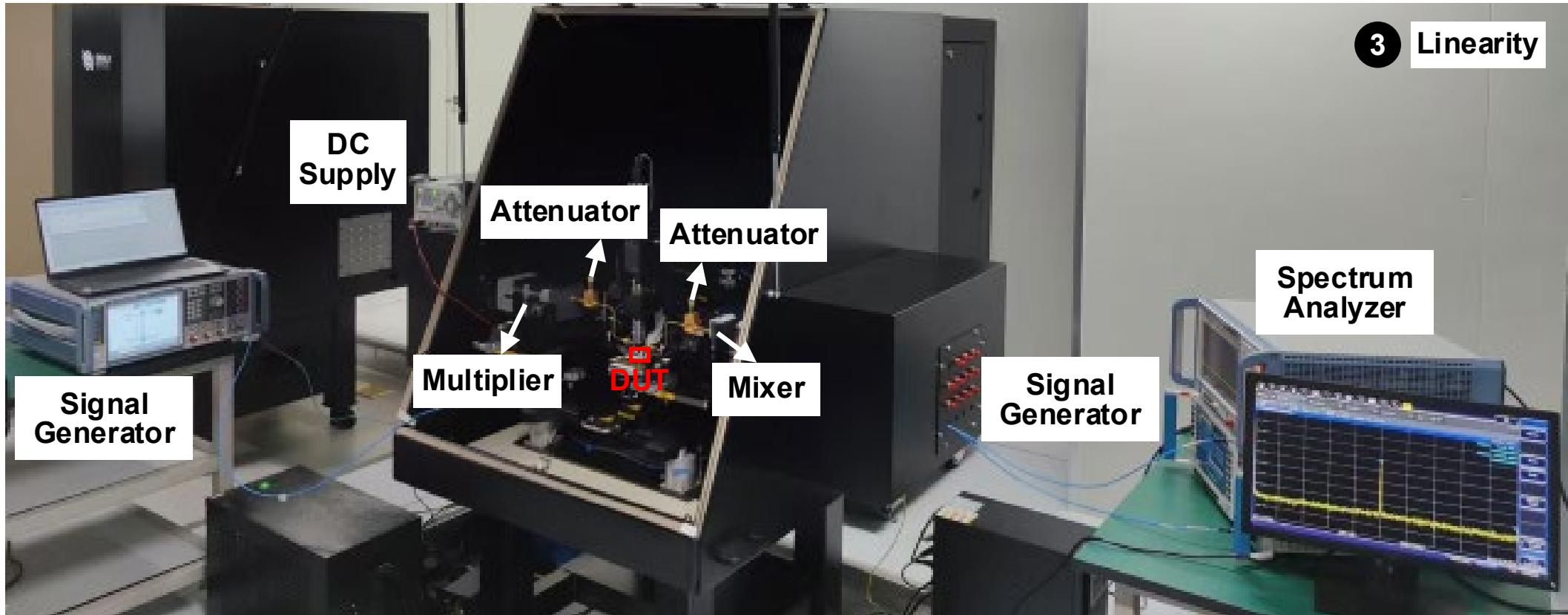
Measurement

■ Noise figure and S-parameter measurement setup



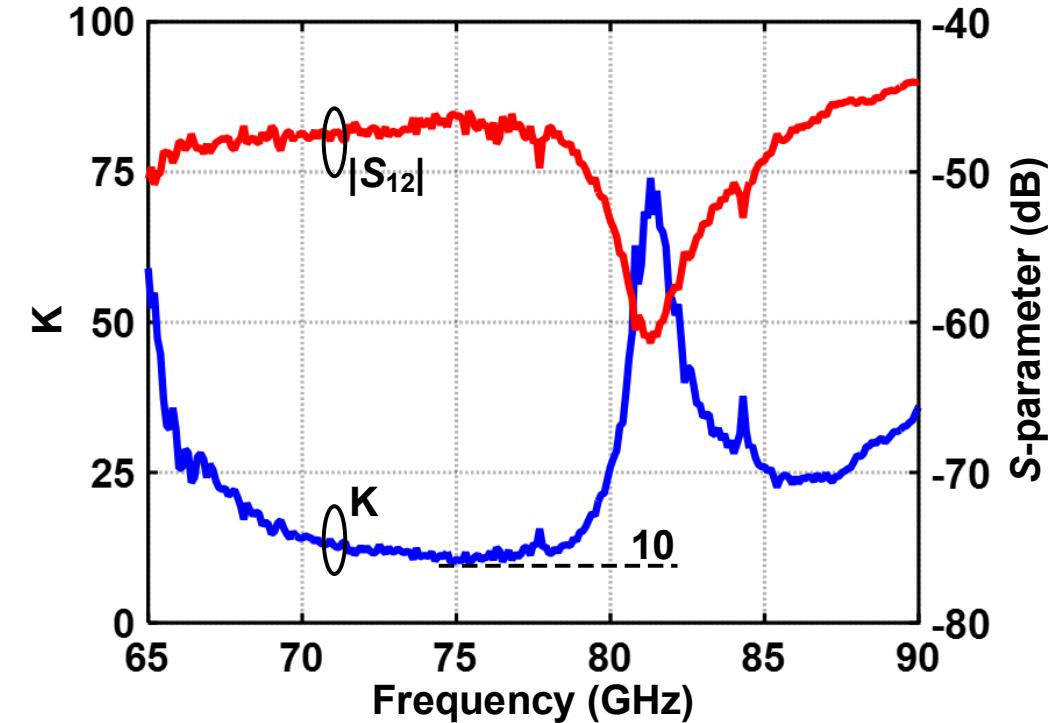
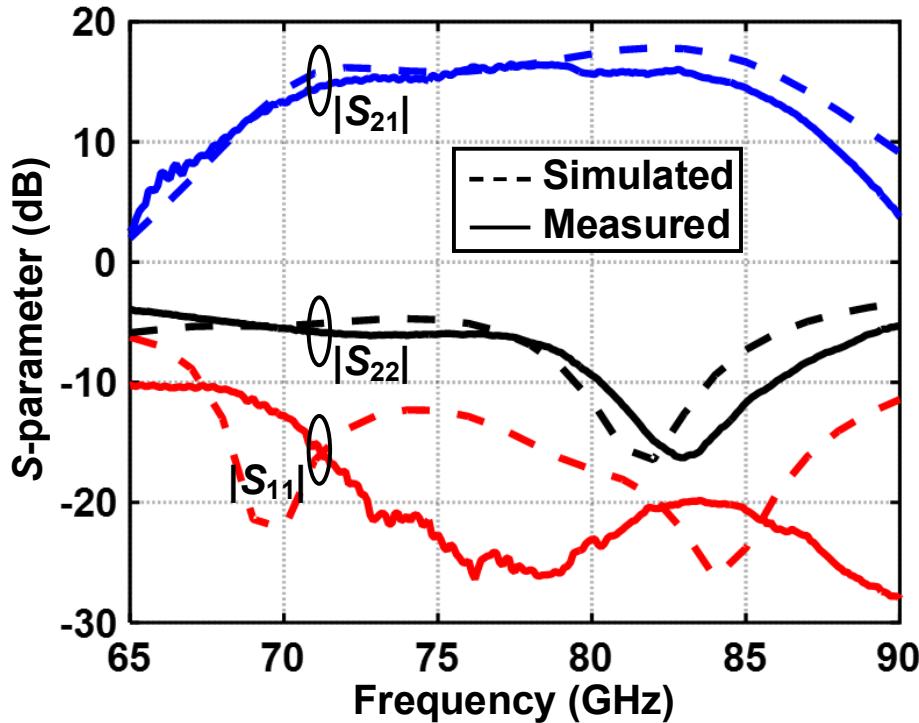
Measurement

■ Linearity measurement setup



Measurement

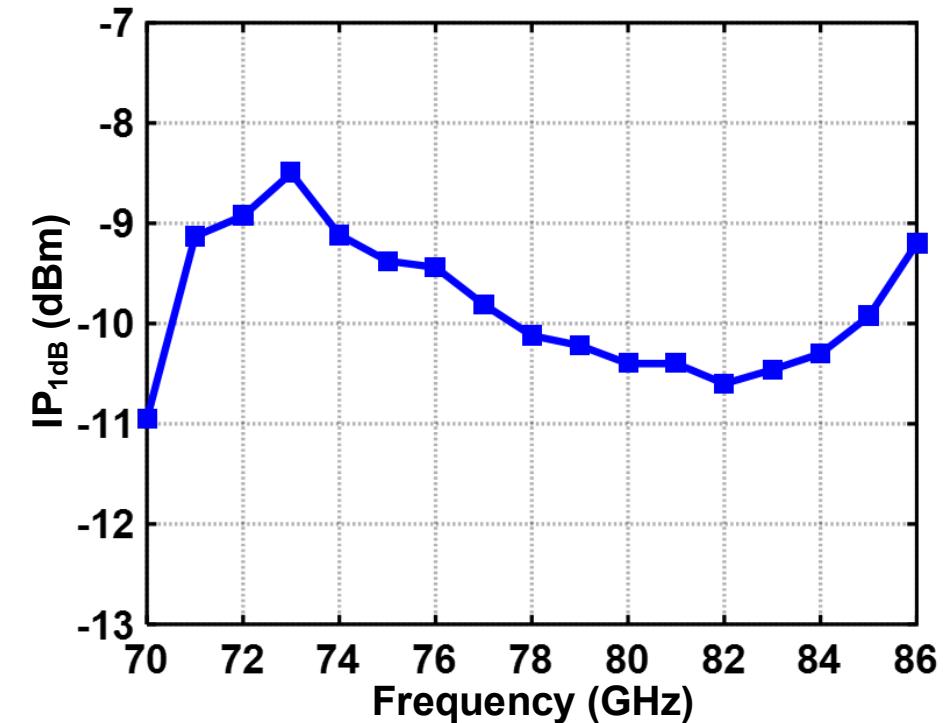
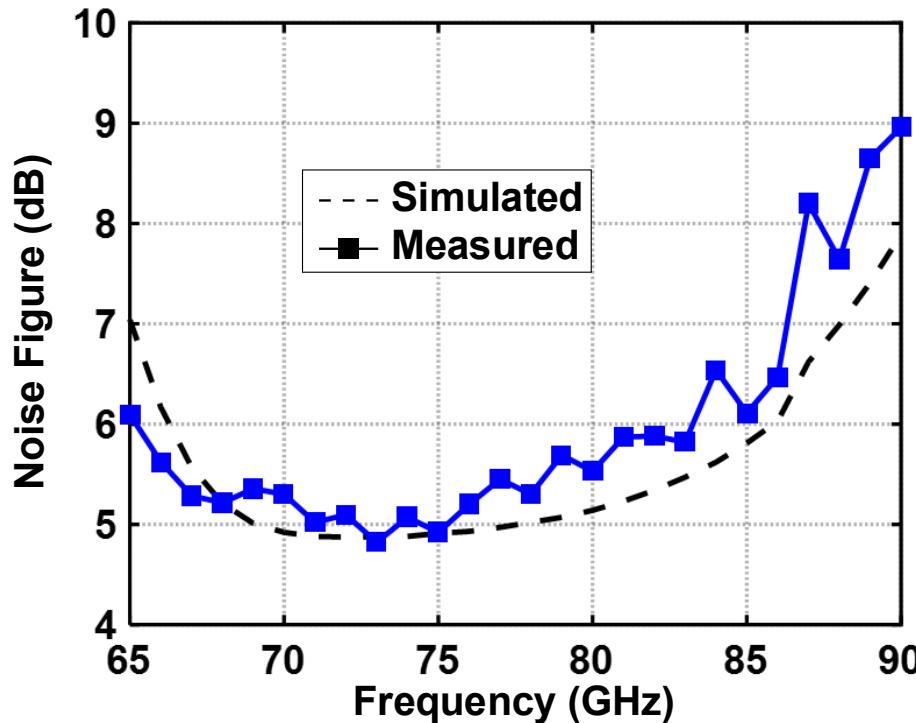
S-parameter measurements



- Peak small-signal gain: 16.5dB at 77.4GHz
- 3dB bandwidth: 70 to 86GHz

Measurement

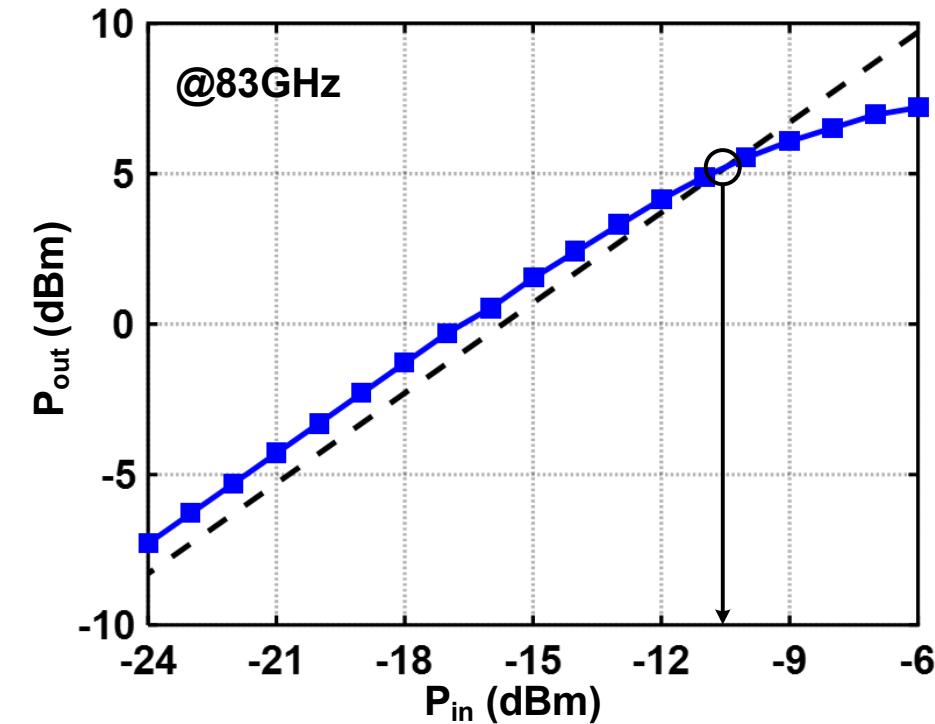
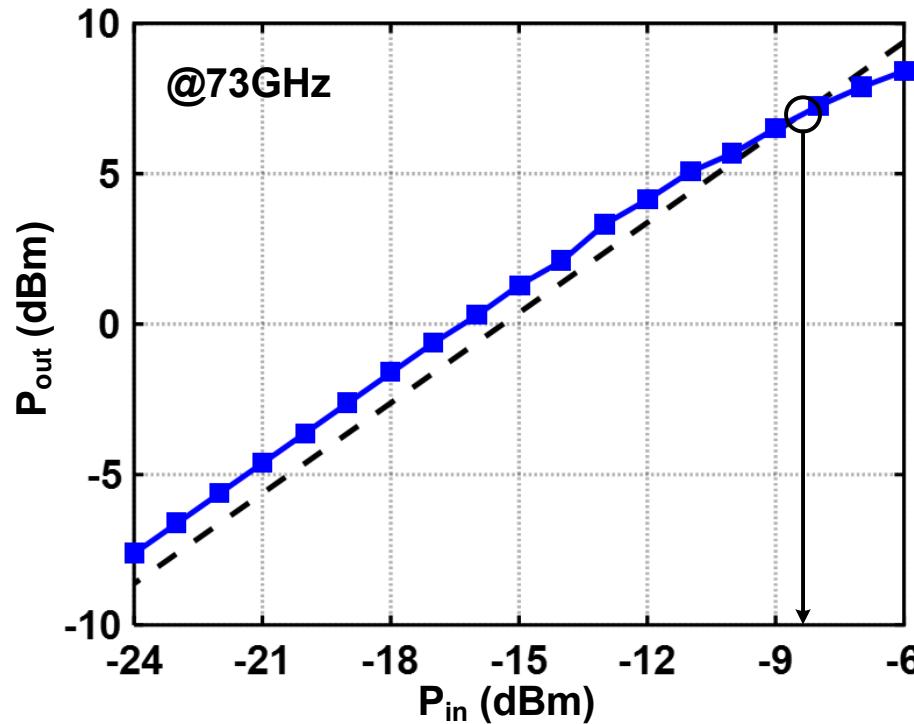
■ Noise figure and IP_{1dB} measurements



- Minimal NF: 4.8dB at 73GHz
- Input P_{1dB} : -10.9 to -8.5dBm from 70 to 86 GHz

Measurement

■ Large-signal CW performance at 73 and 83 GHz



- IP_{1dB} : -8.5dBm at 73GHz
- IP_{1dB} : -10.5dBm at 83GHz

Comparison

Ref.	This work	ISSCC2020 [2]	JSSC2017 [5]	ISSCC2016 [3]	TMTT2020 [6]
Architecture	Two-stage deep noise canceling with hybrid transformers	On-antenna noise canceling and G_m -boosting	Pole-converging with transformer feedback	Transformer-based G_m -boosted CG	Inductively degenerated cascode with gain-boosting
Technology	40nm CMOS	45nm CMOS SOI	65nm CMOS	28nm CMOS	22nm CMOS FD-SOI
Frequency (GHz)	70–86	73–88	63–93	68.1–96.4	70.5–83.5
Gain (dB)	16.5	16.8	18.5	29.6	24
NF (dB)	4.8–6.5	4.8–6.1	5.5–7.9	6.4–8.2	4.6
IP _{1dB} (dBm)	-8.5	-7.4*	-15	-28.1	-26.8
IIP ₃ (dBm)	1.1*	2.2	-5.4*	-18.5*	-17.2*
Supply (V)	1.1	N.A.	1.8	0.9	1.6
DC Power (mW)	25	46	27	31.3	16
Core Size (mm ²)	0.08	0.63	0.06	0.255	0.35
FoM ₁	6.0	3.0	-0.2	-8.4	-12.9
FoM ₂	28.0	7.0	24.2	3.5	-3.8

*The values are estimated from IIP₃≈IP_{1dB}+9.6dB.

$$FoM_1 = 20 \log_{10} \left(\frac{BW[\text{GHz}] \cdot Gain[\text{abs}] \cdot IP_{1dB}[\text{mW}]}{P_{DC}[\text{mW}] \cdot (F_{min}-1)} \right)$$

$$FoM_2 = 20 \log_{10} \left(\frac{BW[\text{GHz}] \cdot Gain[\text{abs}] \cdot IP_{1dB}[\text{mW}]}{P_{DC}[\text{mW}] \cdot (F_{min}-1) \cdot Size[\text{mm}^2]} \right)$$

Comparison

Ref.	This work	ISSCC2020 [2]	JSSC2017 [5]	ISSCC2016 [3]	TMTT2020 [6]
Architecture	Two-stage deep noise canceling with hybrid transformers	On-antenna noise canceling and G_m -boosting	Pole-converging with transformer feedback	Transformer-based G_m -boosted CG	Inductively degenerated cascode with gain-boosting
Technology	40nm CMOS	45nm CMOS SOI	65nm CMOS	28nm CMOS	22nm CMOS FD-SOI
Frequency (GHz)	70–86	73–88	63–93	68.1–96.4	70.5–83.5
Gain (dB)	16.5	16.8	18.5	29.6	24
NF (dB)	4.8–6.5	4.8–6.1	5.5–7.9	6.4–8.2	4.6
IP_{1dB} (dBm)	-8.5	-7.4*	-15	-28.1	-26.8
IIP3 (dBm)	1.1*	2.2	-5.4*	-18.5*	-17.2*
Supply (V)	1.1	N.A.	1.8	0.9	1.6
DC Power (mW)	25	46	27	31.3	16
Core Size (mm^2)	0.08	0.63	0.06	0.255	0.35
FoM_1	6.0	3.0	-0.2	-8.4	-12.9
FoM_2	28.0	7.0	24.2	3.5	-3.8

*The values are estimated from $IIP3 \approx IP_{1dB} + 9.6 \text{ dB}$.

$$FoM_1 = 20 \log_{10} \left(\frac{BW[\text{GHz}] \cdot Gain[\text{abs}] \cdot IP_{1dB}[\text{mW}]}{P_{DC}[\text{mW}] \cdot (F_{min}-1)} \right)$$

$$FoM_2 = 20 \log_{10} \left(\frac{BW[\text{GHz}] \cdot Gain[\text{abs}] \cdot IP_{1dB}[\text{mW}]}{P_{DC}[\text{mW}] \cdot (F_{min}-1) \cdot Size[\text{mm}^2]} \right)$$

Outline

- Introduction and Motivation
- Deep-Noise-Canceling LNA Architecture
- Asymmetric CG Based Noise-Canceling
- Resistive Feedback Noise-Canceling
- LNA Implementation
- Measurement and Comparison
- Conclusion

Conclusion

- **Deep-Noise-Canceling LNA** Architecture for lower NF, higher linearity and compact size
- **Asymmetric compensation transformer (ACT)** for CG based noise-canceling enhancement
- **Hybrid-phase combiner (HPC)** is utilized for resistive feedback noise-canceling design and decreases 2nd stage noise contribution
- Deep-noise-canceling LNA achieves **low noise and high linearity** with compact size

Acknowledgement

The authors thank the support of National Key R&D Program of China under Grant 2021YFE0205600, the National Natural Science Foundation of China under Grant 61934001, 62161160310.

Thank You

25.4: A 4b RFDAC at 8GS/s for FMCW Chirps with 4GHz Bandwidth in 10 μ s

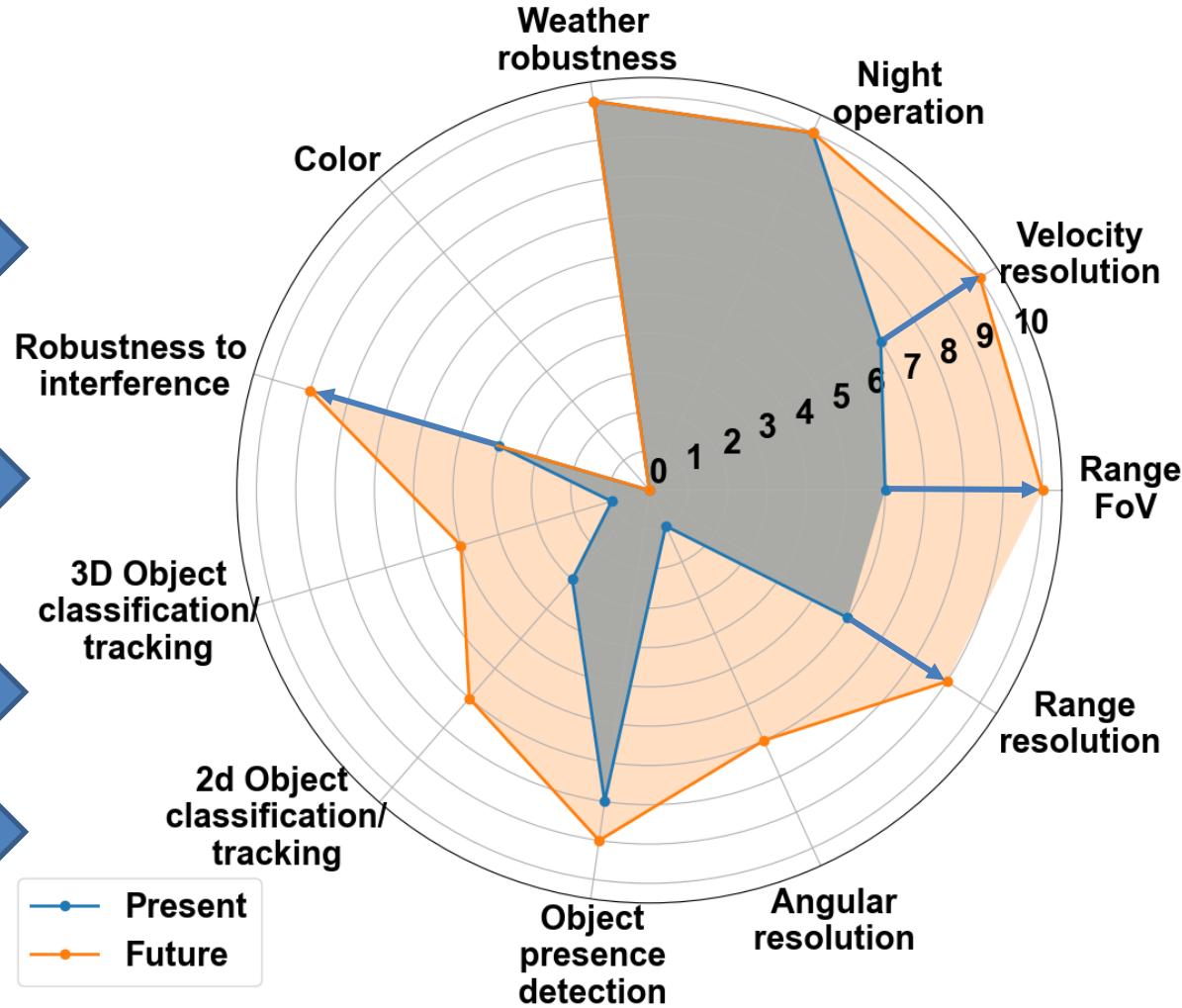
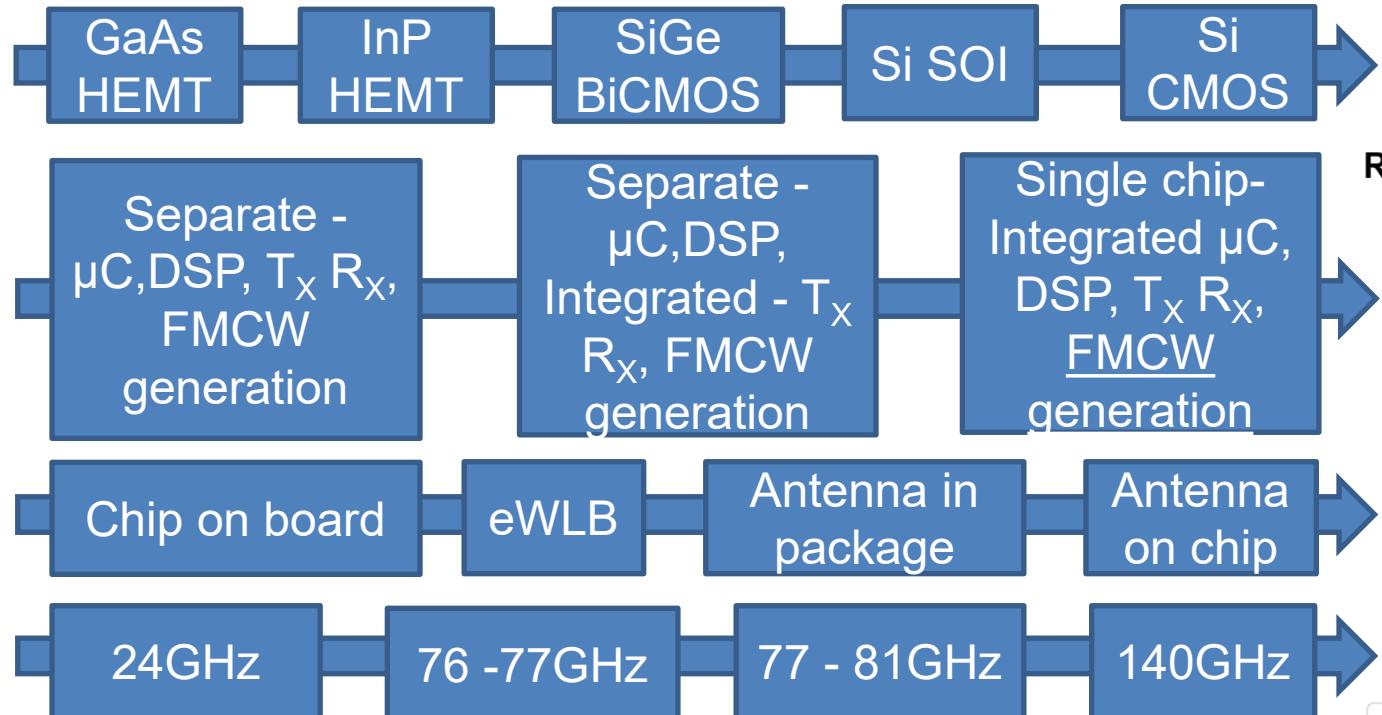
Soumya Krishnapuram Sireesh^{1,2}, Sanaz Hadipour Abkenar^{1,2},
Niels Christoffers¹, Christoph Wagner¹, Thorsten Brandt¹,
Andreas Stelzer²



¹Infineon Technologies, Linz, Austria
²Johannes Kepler University, Linz, Austria

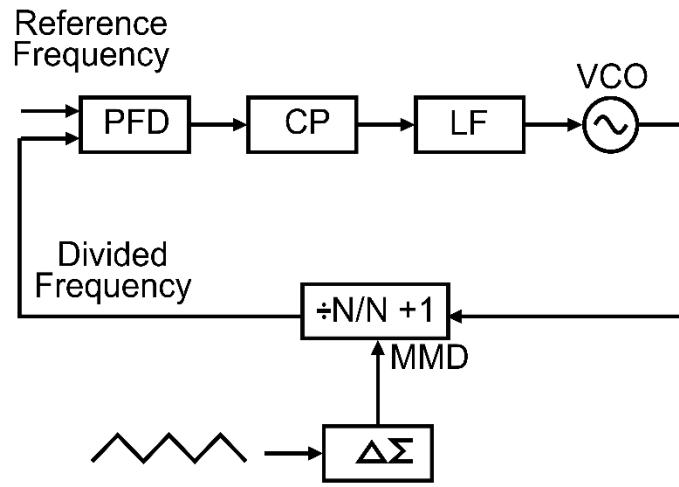


Automotive Radar – Technology trend

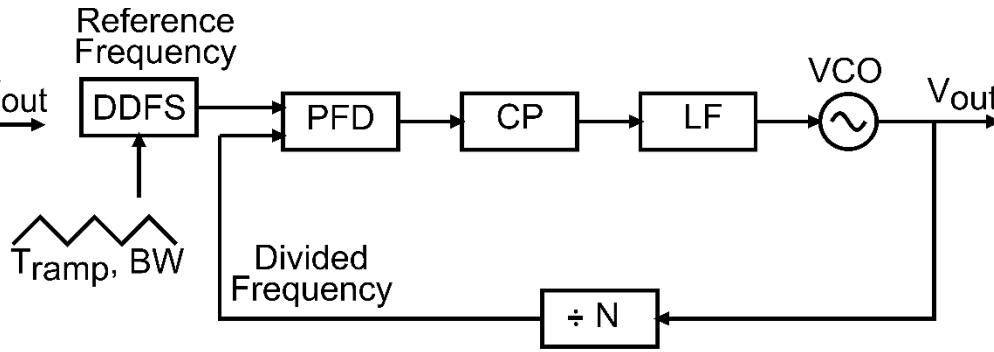


Source : IDTechEX Research

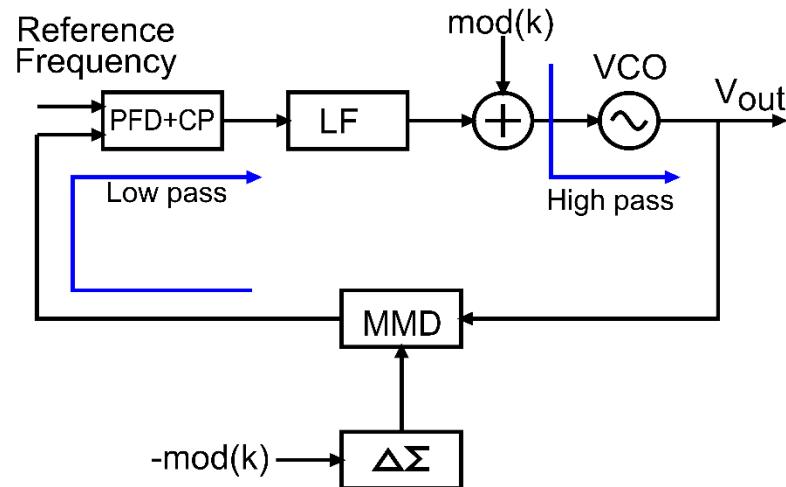
Frequency Modulator Architectures



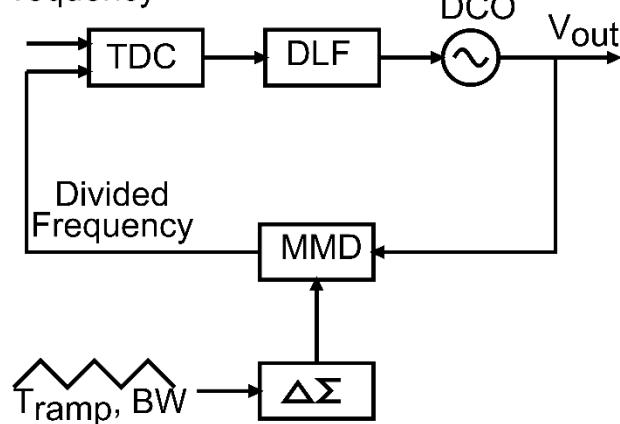
Frac – N PLL



DDFS – Integer N PLL[3]



PLL – TPM



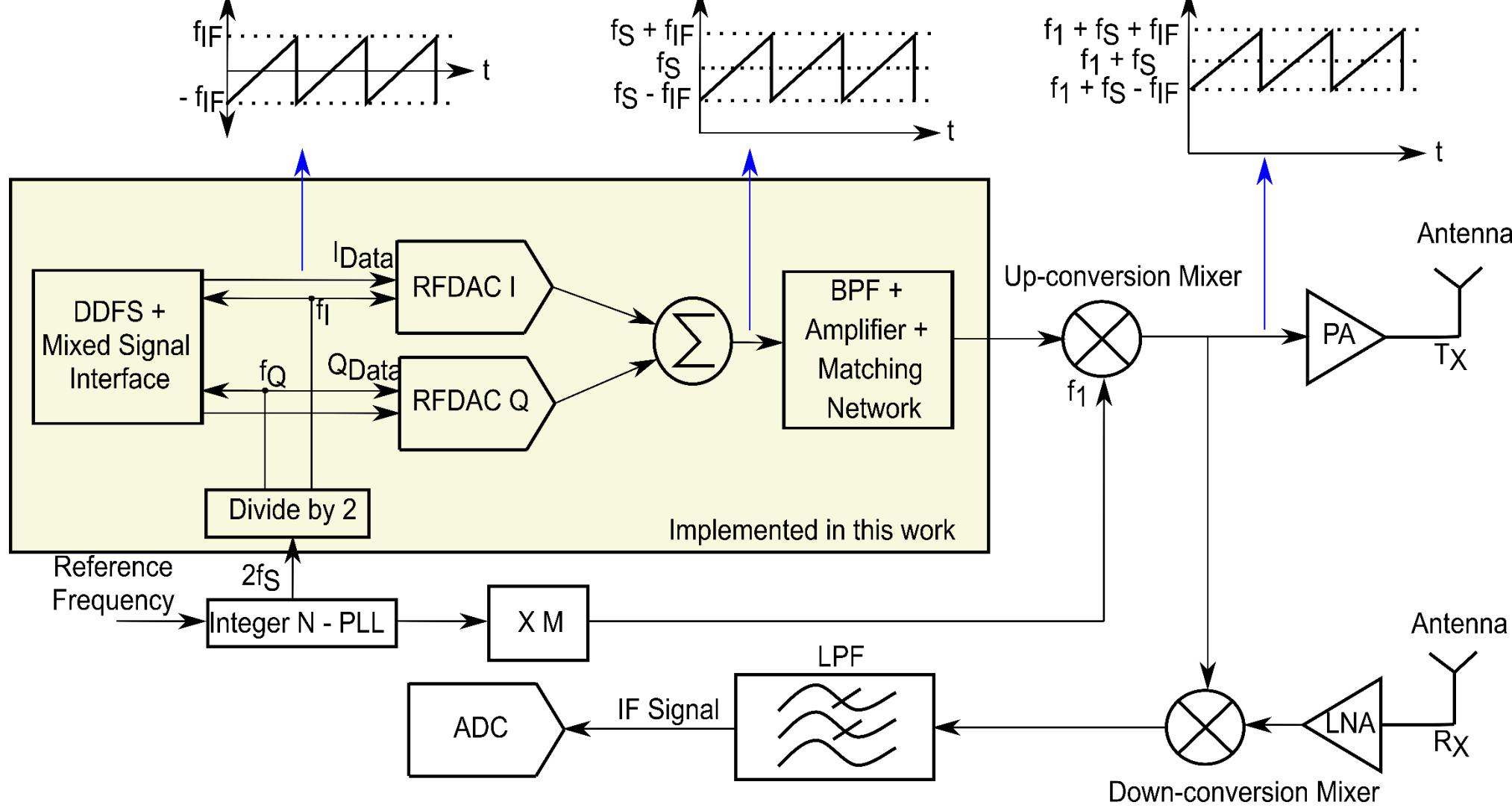
Digital PLL

- PLL's trade between loop bandwidth and modulation bandwidth to satisfy phase noise requirements
- 2-point modulation to decouple loop bandwidth and modulation bandwidth with predistortion and calibration[4]
- ADPLL [1,2] catch up with low supply voltage and digital technology trend

Outline

- **RFDAC Based FMCW Transceiver**
- **Circuit Implementation**
- **Measurement Results**
 - Spectral Characterization
 - Transient Behavior
- **Conclusion**

RFDAC Based FMCW Transceiver

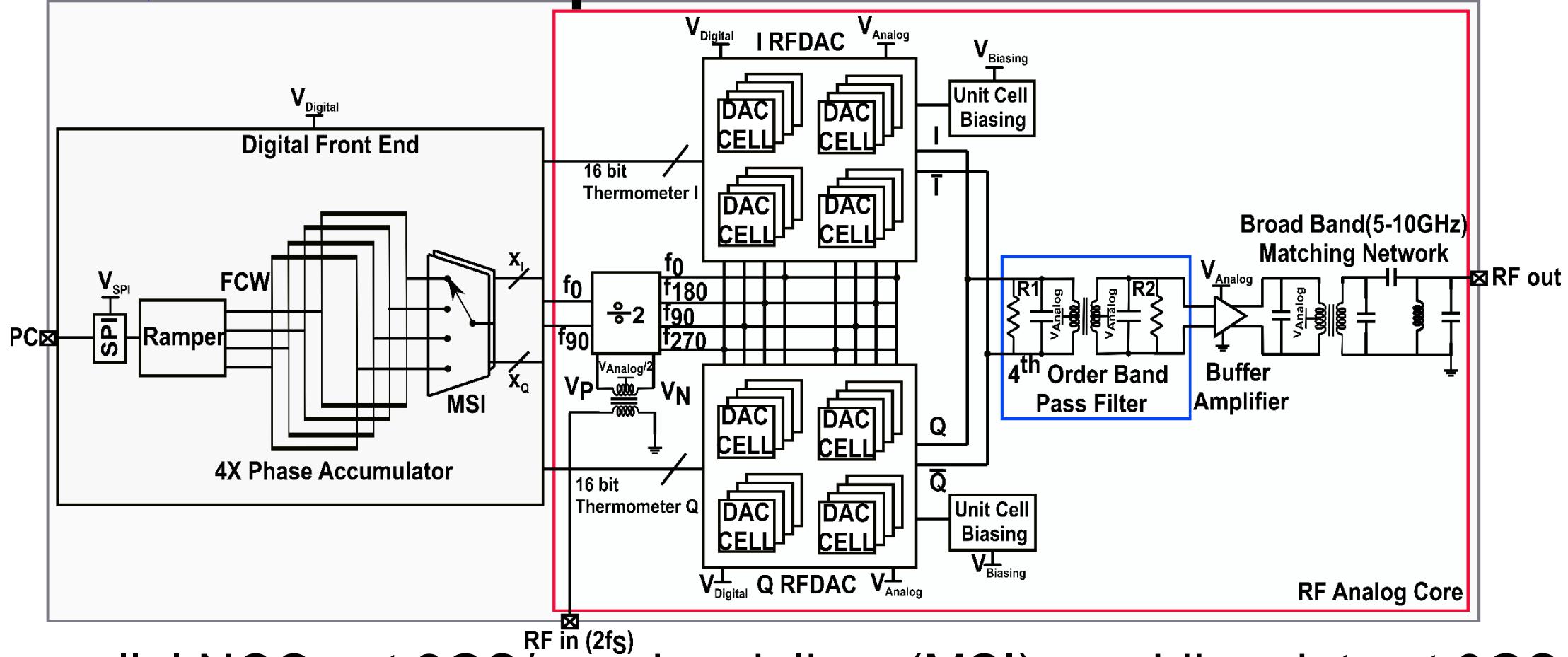


- Accurate frequency modulated IQ data from -3GHz to 1GHz by DDFS
- 4 bit RFDAC at 8GHz to accomodate 4GHz ramp bandwidth

Key Features of the Implemented Approach

- Integer-N-PLL
 - Less complex design
 - Loop bandwidth can be chosen for optimum phase noise performance
 - Gain of the VCO can be kept low
- RF-DAC & DDFS
 - Frequency ramps with 4GHz bandwidth in configurable time
 - Fast and identical frequency ramps with perfect accuracy
 - Settling time is negligible in sub – ns range
 - Slow ramps and fast ramps depend on the data from the digital front-end and not on the responsiveness of PLL
 - Scales with technology

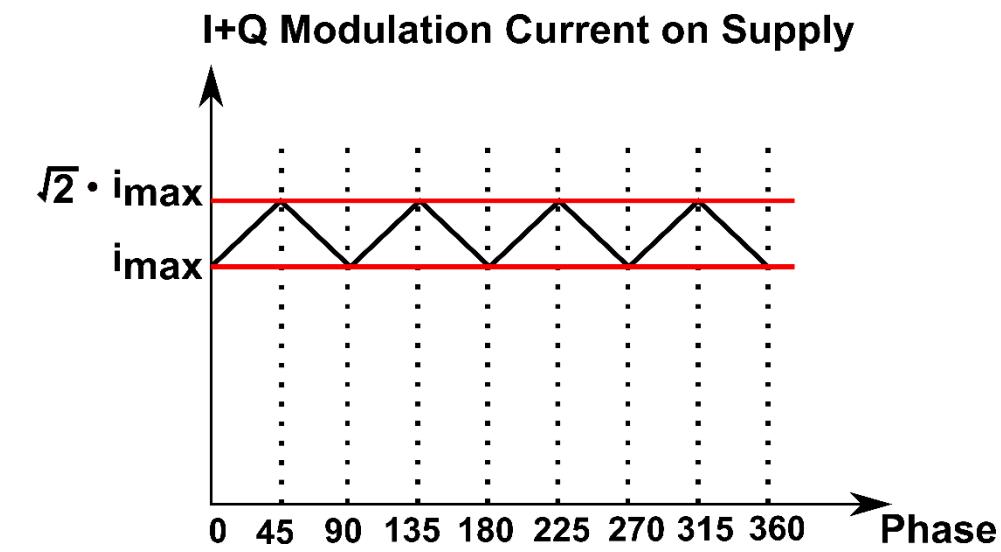
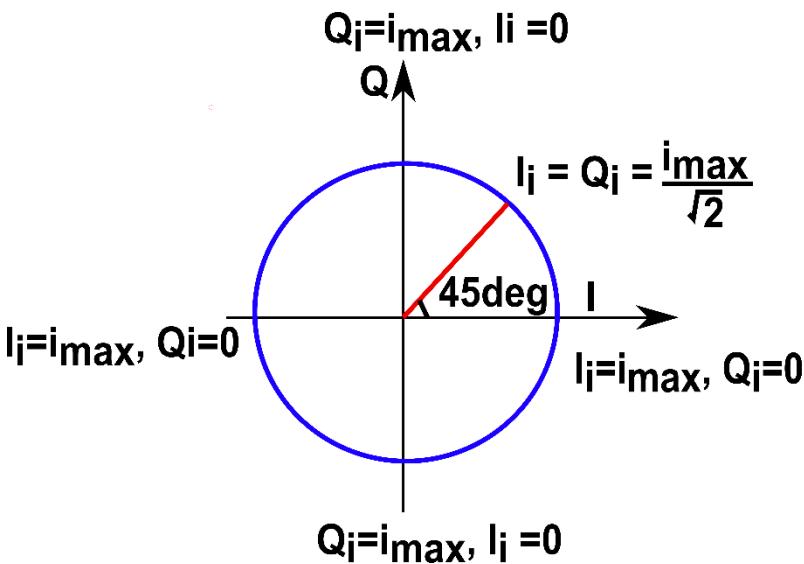
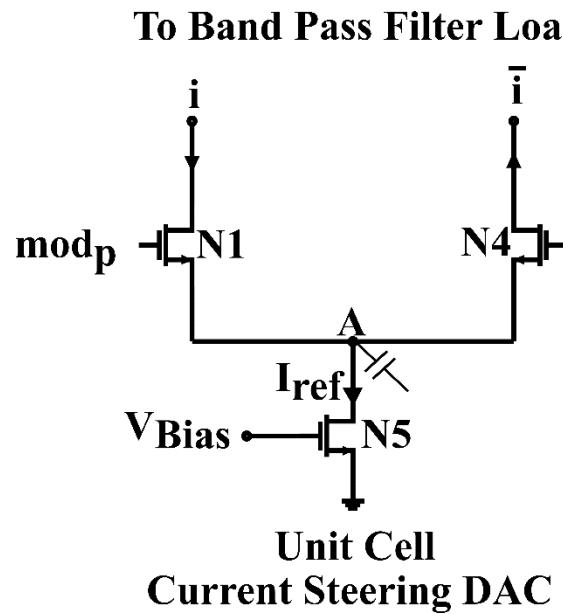
Implemented Work



- 4 parallel NCOs at 2GS/s and serialiser (MSI) providing data at 8GS/s
- On-chip divide by 2 frequency divider & IQ generation
- 4 x 4 current steering DAC cells including data retiming and modulation
- 4th order 50% fractional bandwidth BPF load

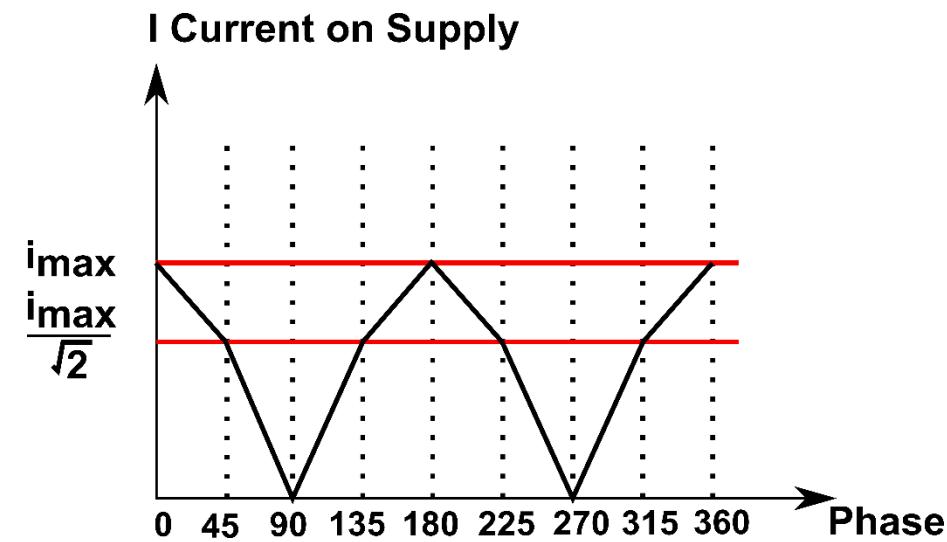
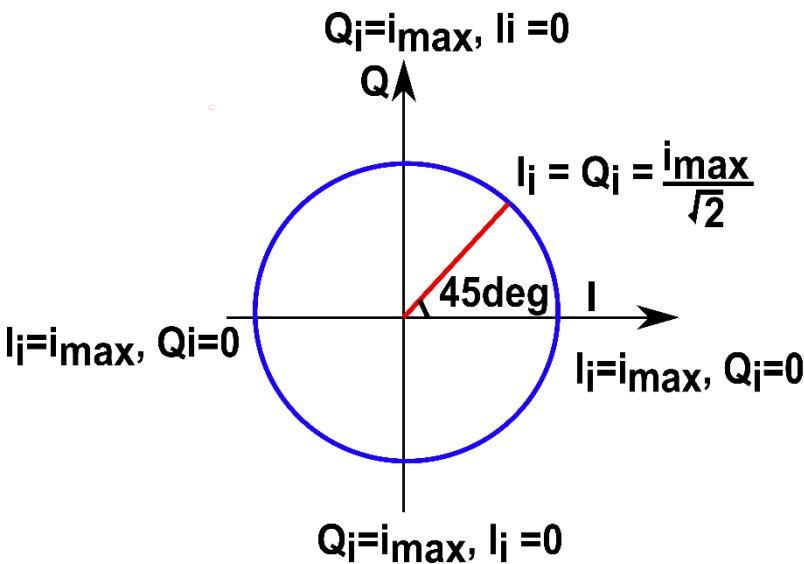
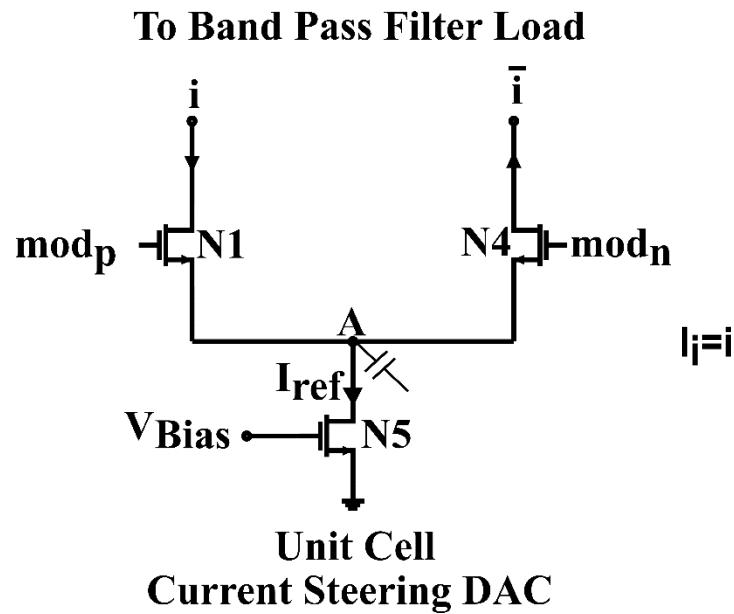
25.4: A 4b RFDAC at 8GS/s for FMCW Chirps with 4GHz Bandwidth in 10μs

Current Steering Unit Cell



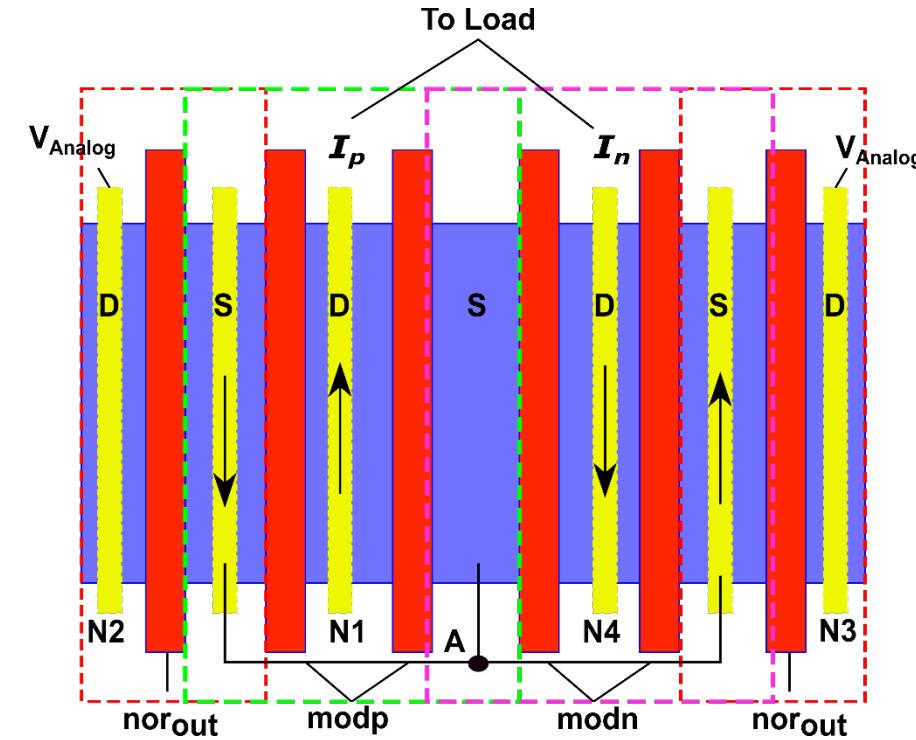
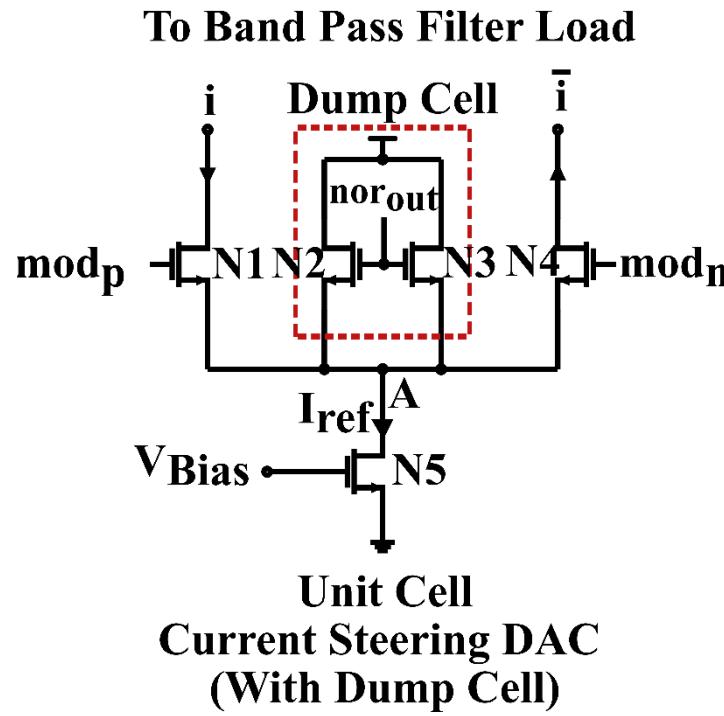
- In shown configuration, the total current drawn from supply by I and Q array varies from $2^N \cdot I_{ref}$ to $\sqrt{2} \cdot 2^N \cdot I_{ref}$ for every base band cycle 4 times
- Thus, supply is prone to exhibit ripple frequencies at $4f_{IF}$ i.e., up to 12GHz

Current Steering Unit Cell



- The parasitic node capacitance on node 'A' is prone to charging via N1 and N4 and discharging via N5 giving rise to $2f_{IF}$ voltage variation on node A

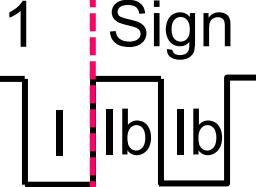
Current Steering Unit Cell and Layout

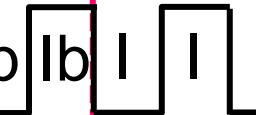


- Dump cell to counter supply-current variations and the tail node ripple
- Dump cell is ‘ON’ when there is no data
- Width of N2/N3 is half of N1/N4 for charge balancing

Modulation of Data with Clock

Given digital I data and CLK_i ,

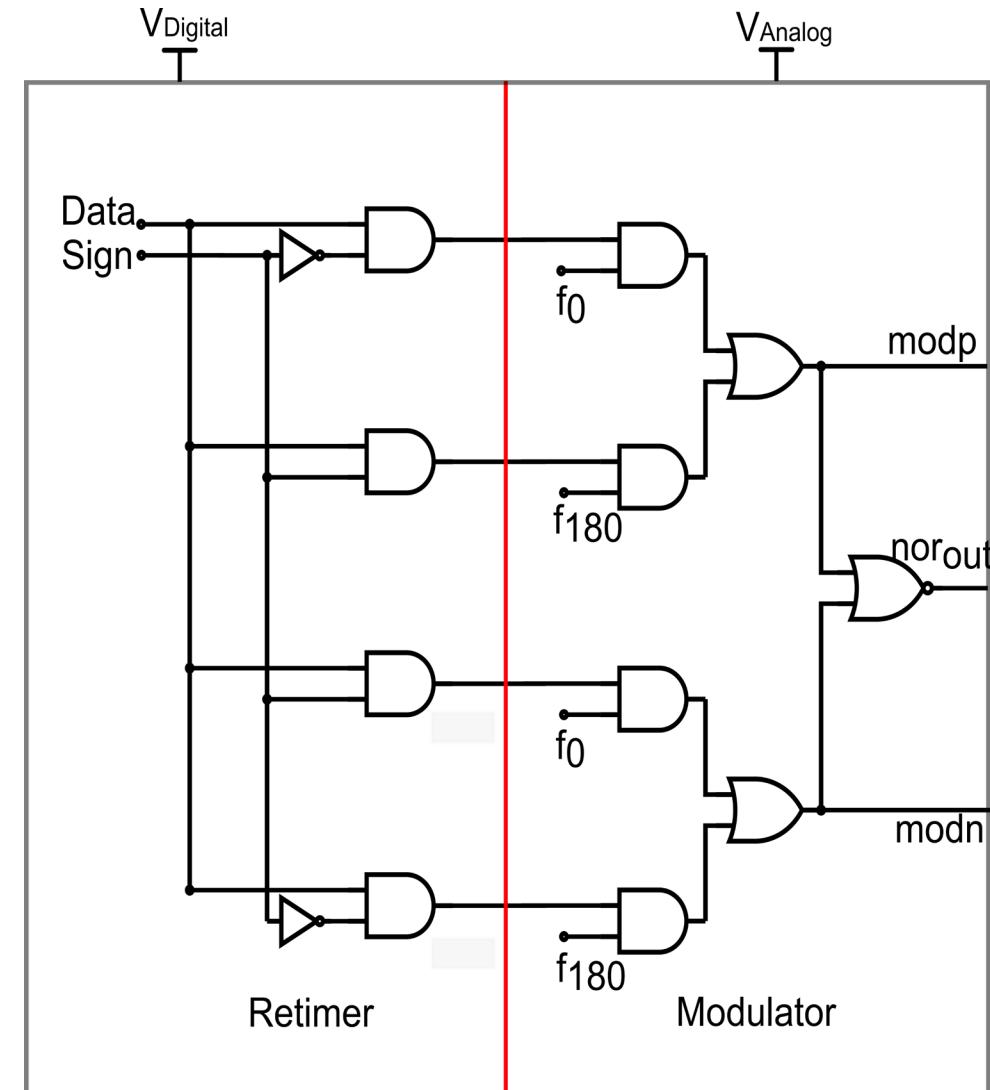
Sign bit = 1 Sign bit = 0
 CLK_i  = modp

\overline{CLK}_i  = modn

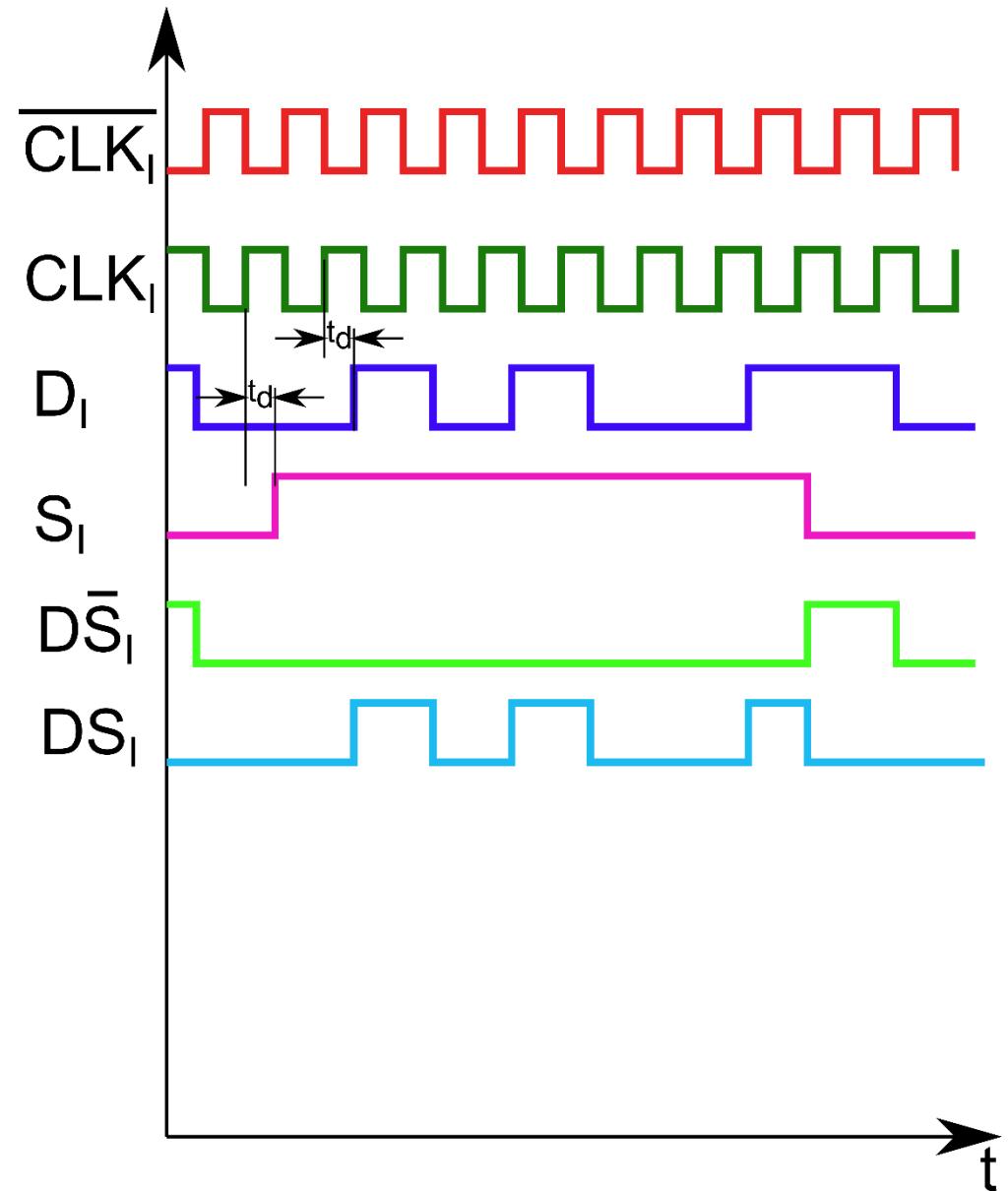
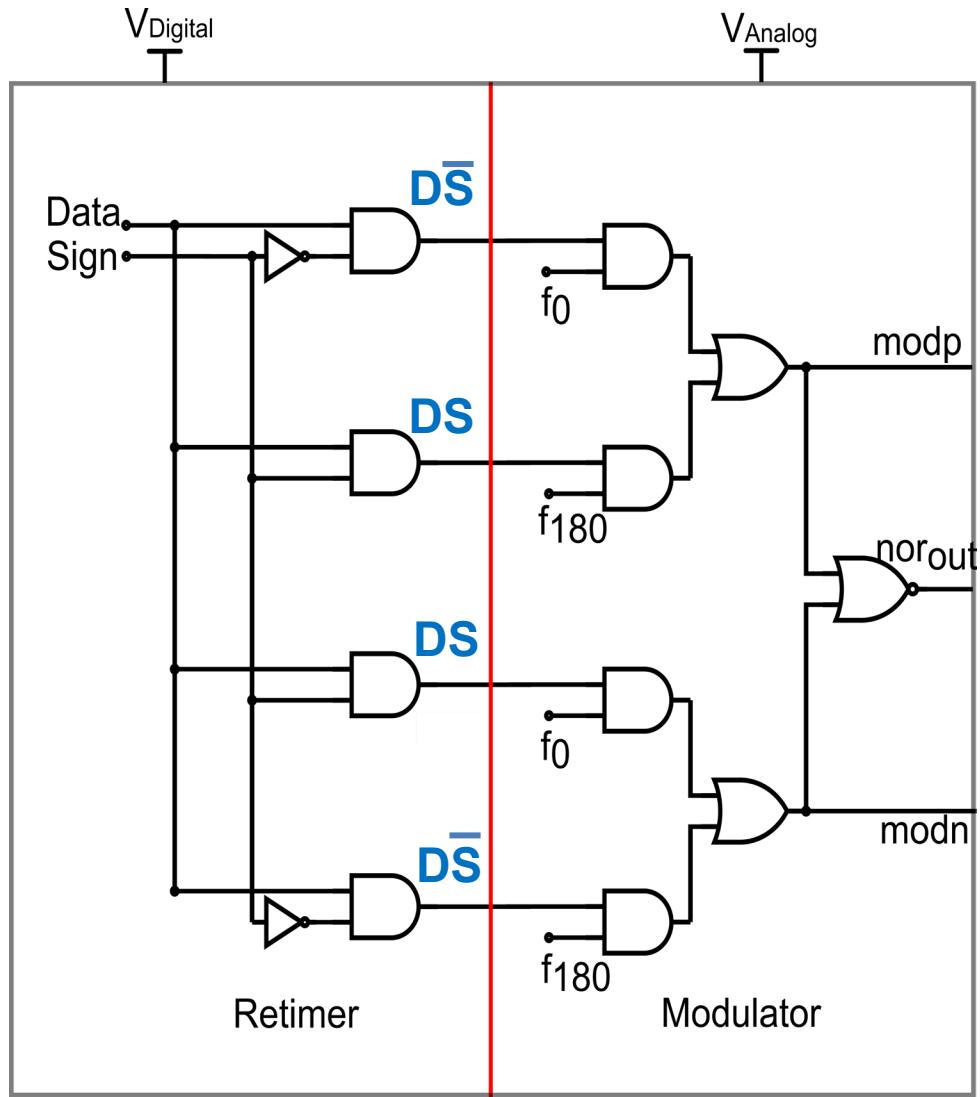
Hence,

$$modp = CLK_i \cdot D \cdot \bar{S} + \overline{CLK}_i \cdot D \cdot S$$

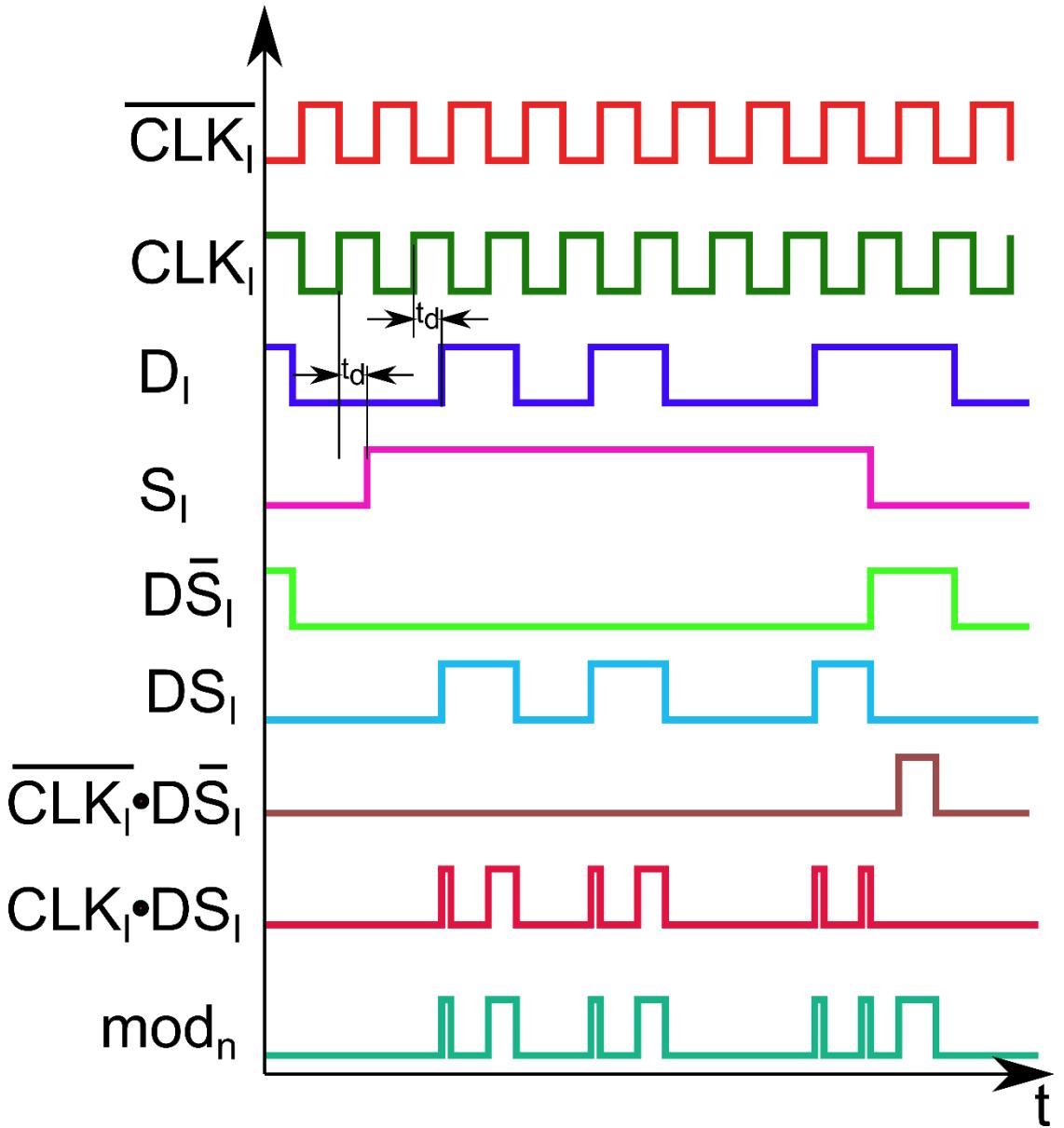
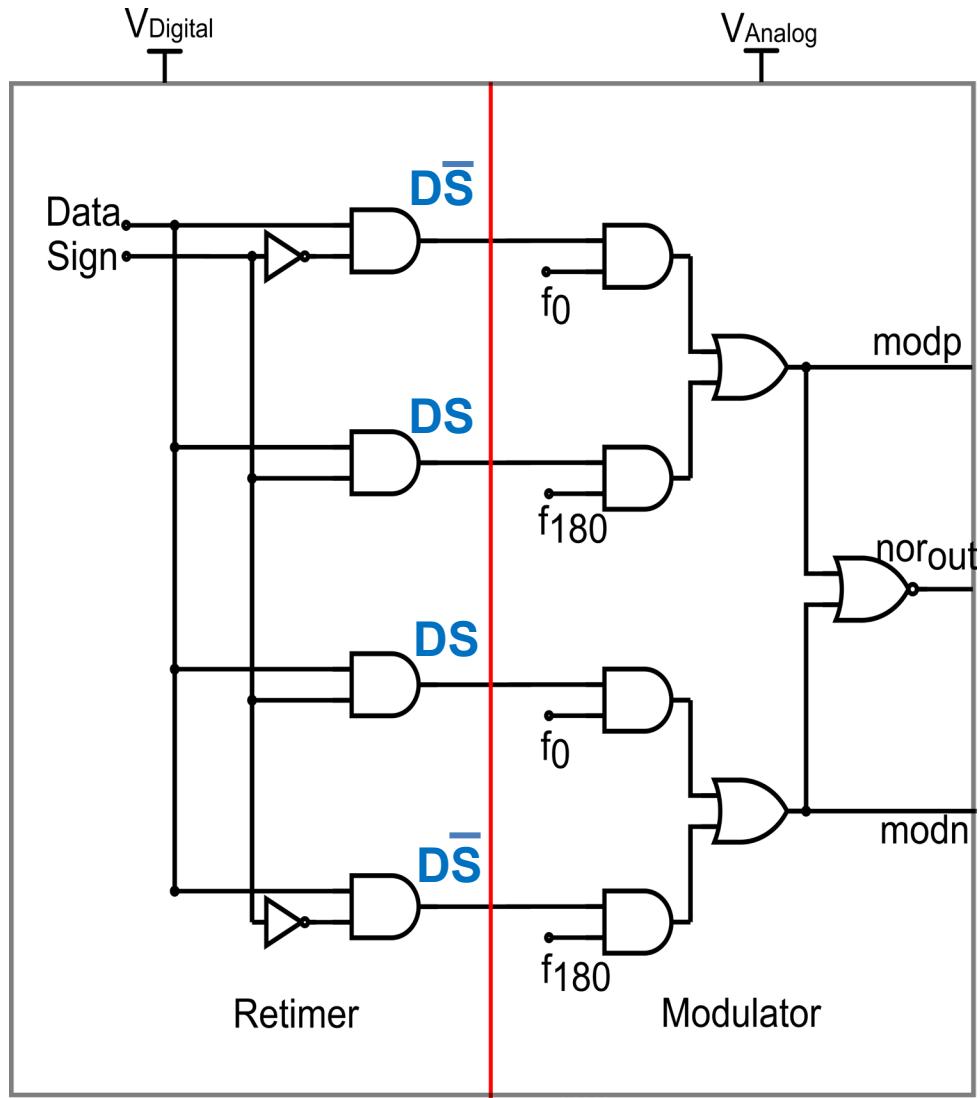
$$modn = \overline{CLK}_i \cdot D \cdot \bar{S} + CLK_i \cdot D \cdot S$$



Modulation of Data with Clock

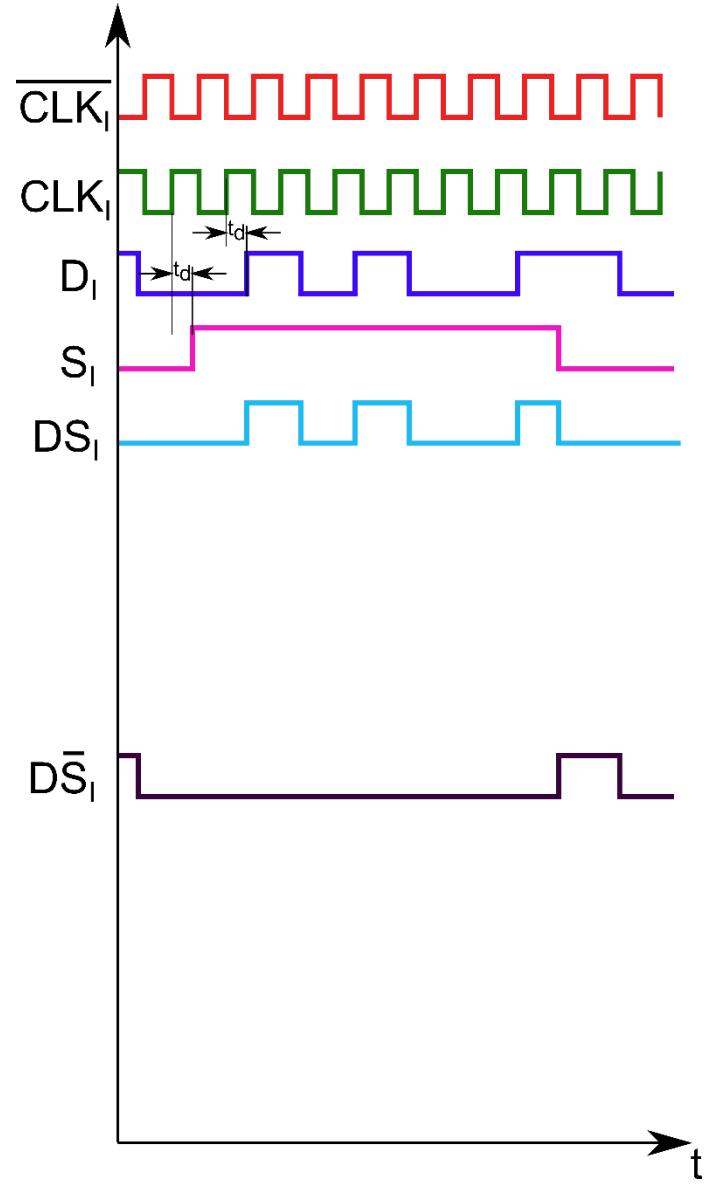
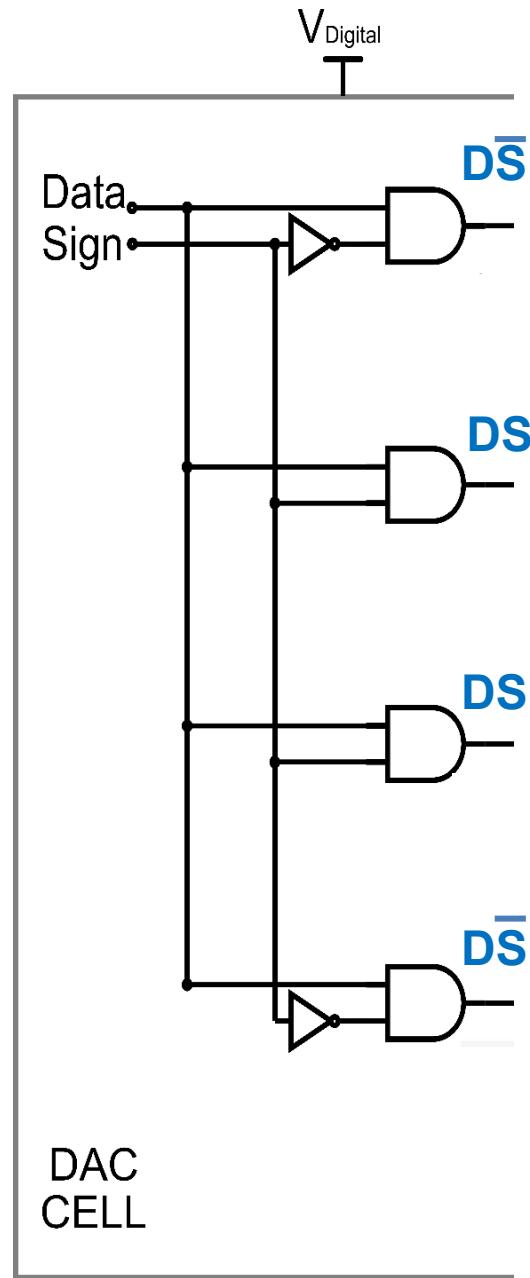


Modulation of Data with Clock

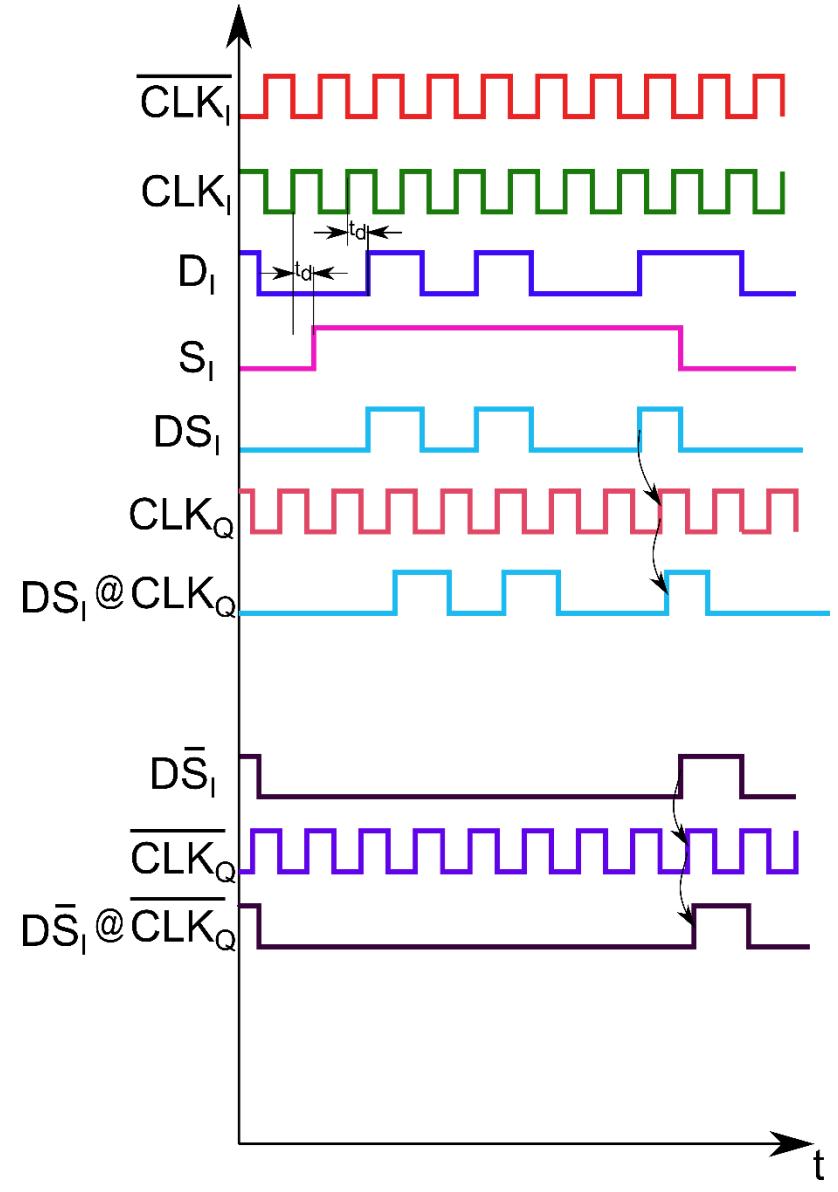
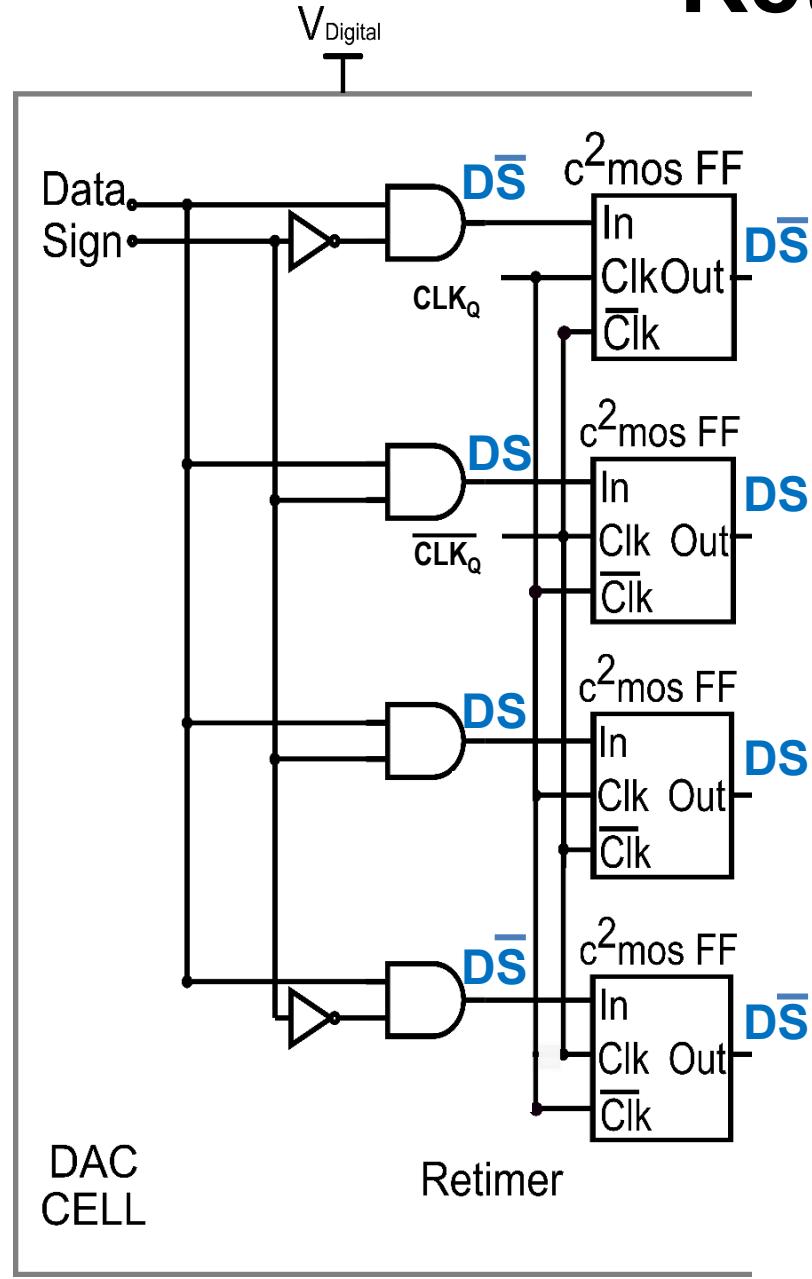


25.4: A 4b RFDAC at 8GS/s for FMCW Chirps with 4GHz Bandwidth in 10 μ s

Retimer and Modulator

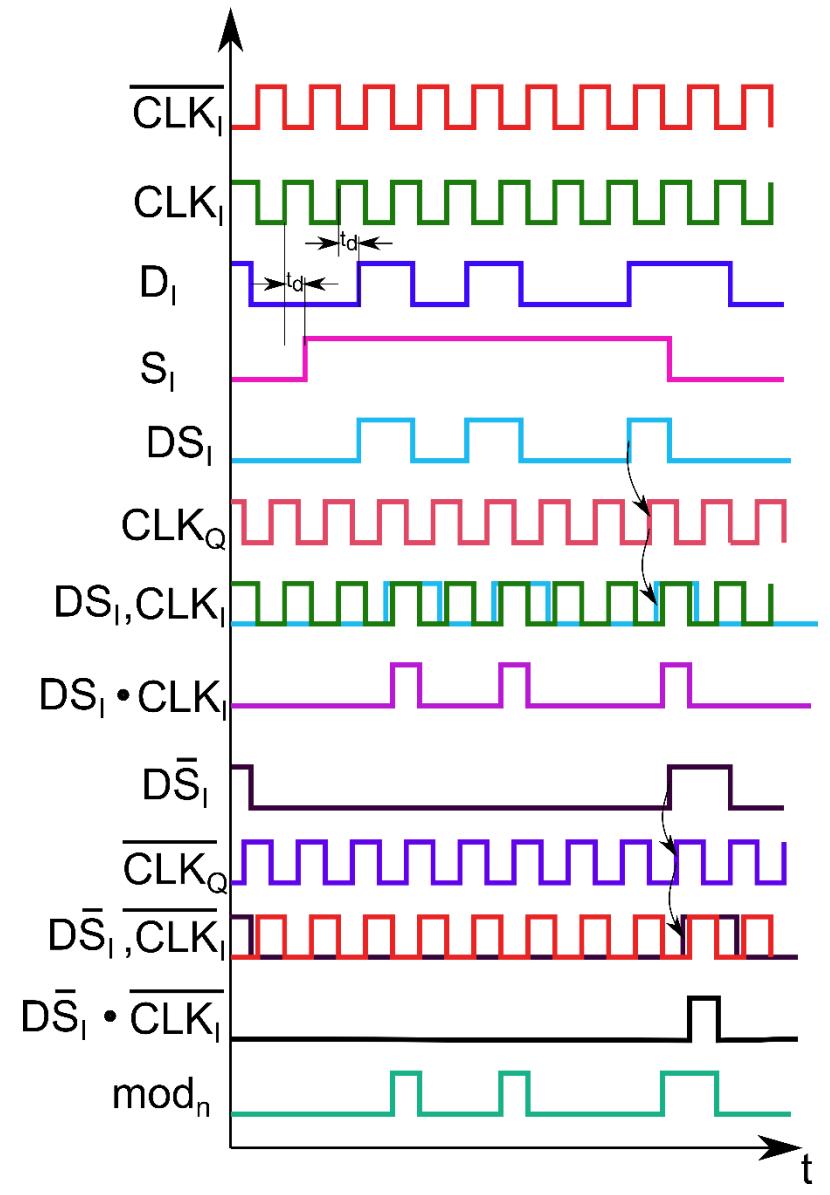
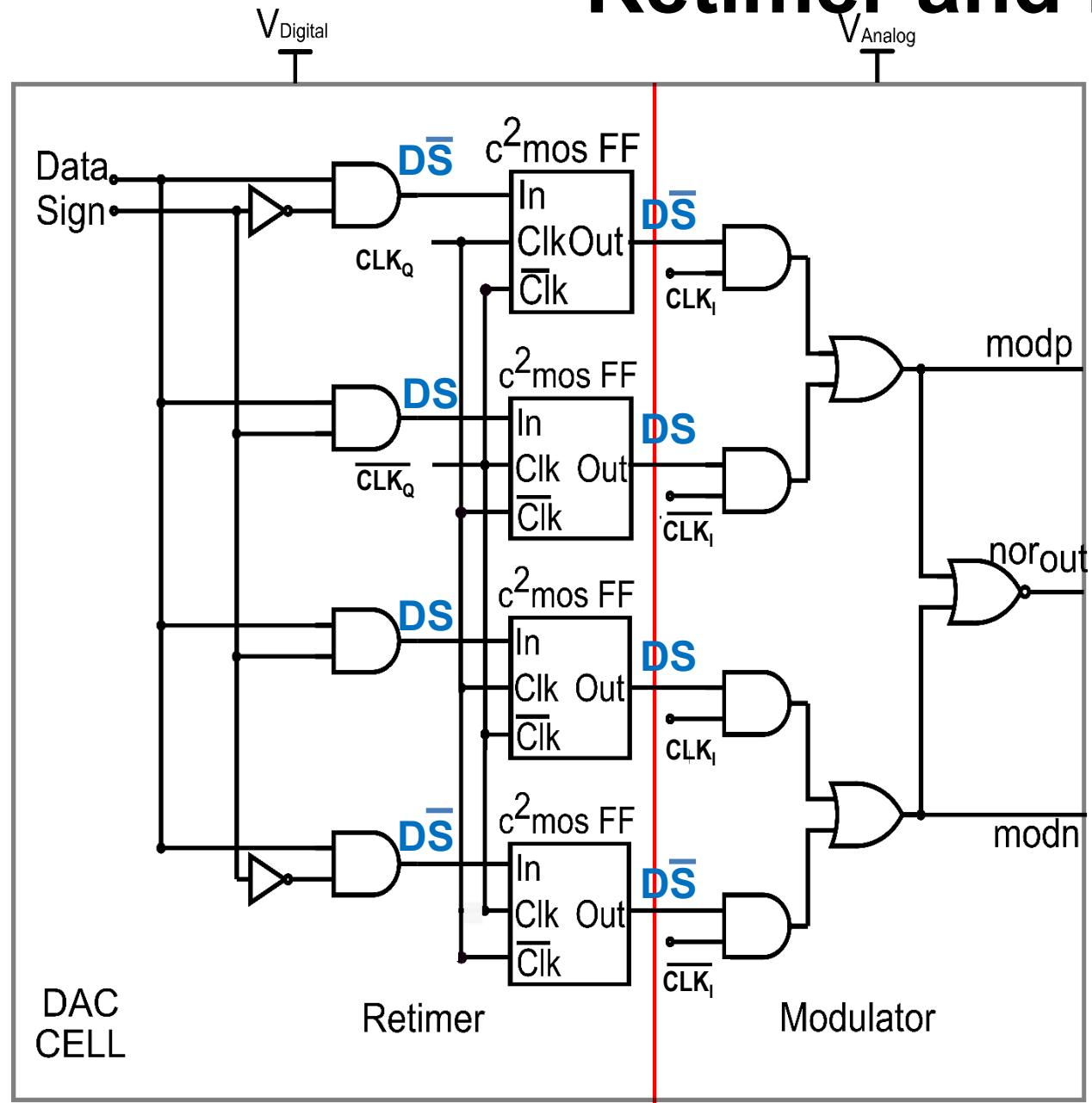


Retimer and Modulator

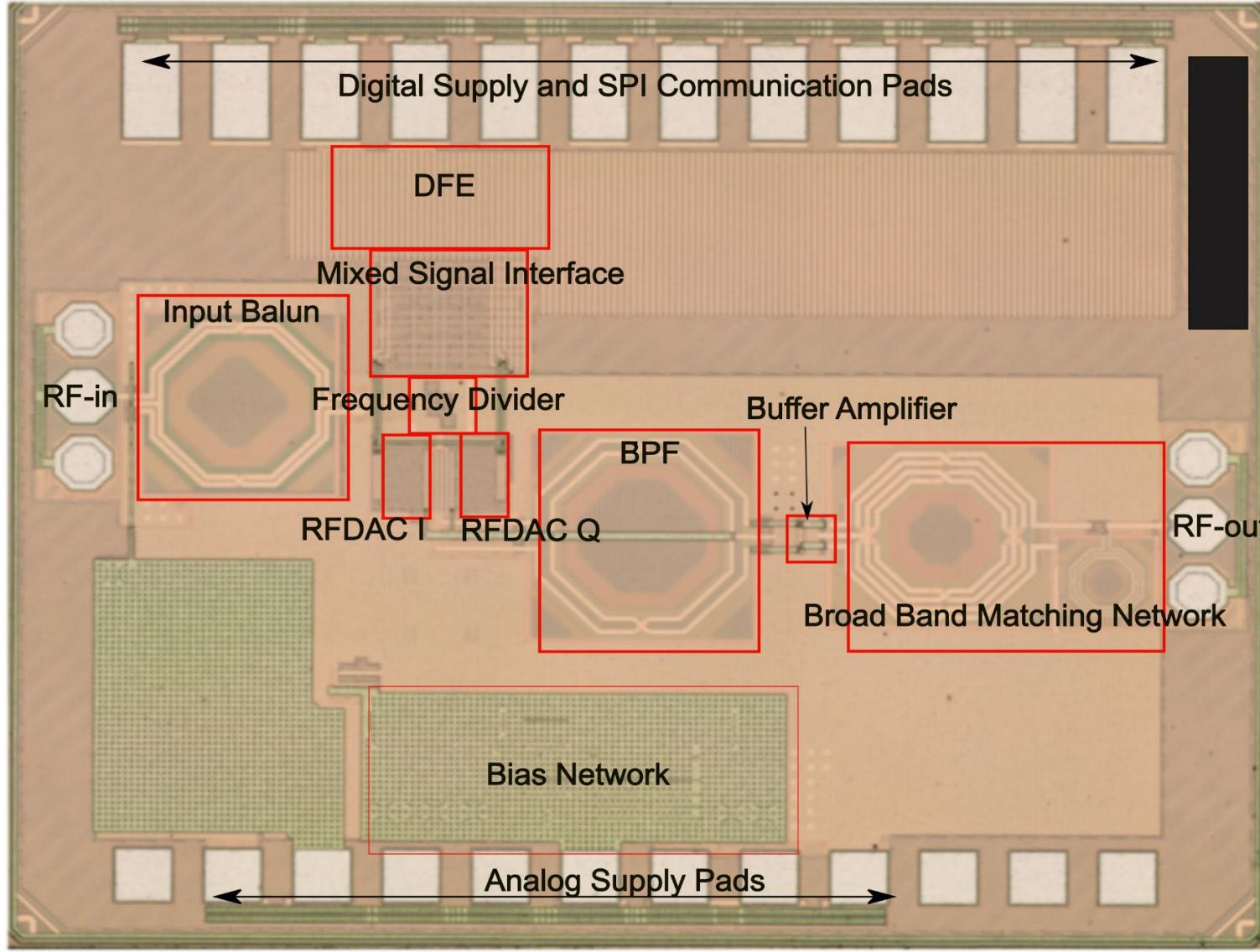


25.4: A 4b RFDAC at 8GS/s for FMCW Chirps with 4GHz Bandwidth in 10μs

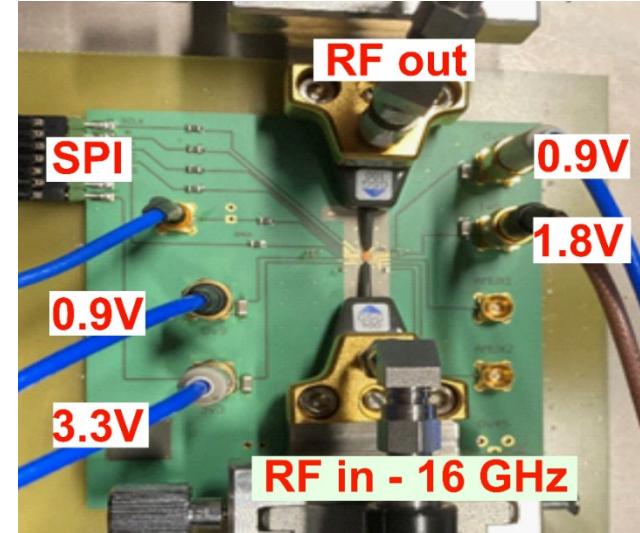
Retimer and Modulator



Die Micrograph and Measurement Setup



1.44mm×1.76mm

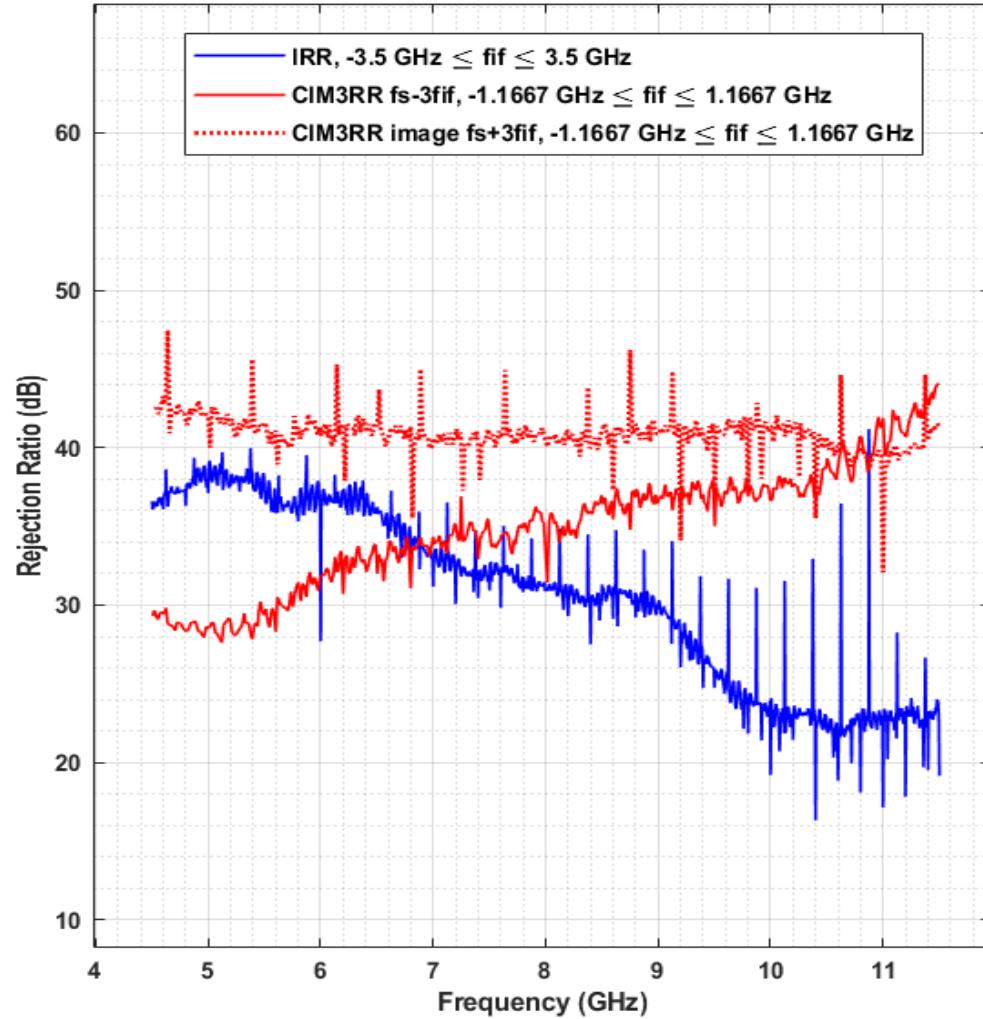
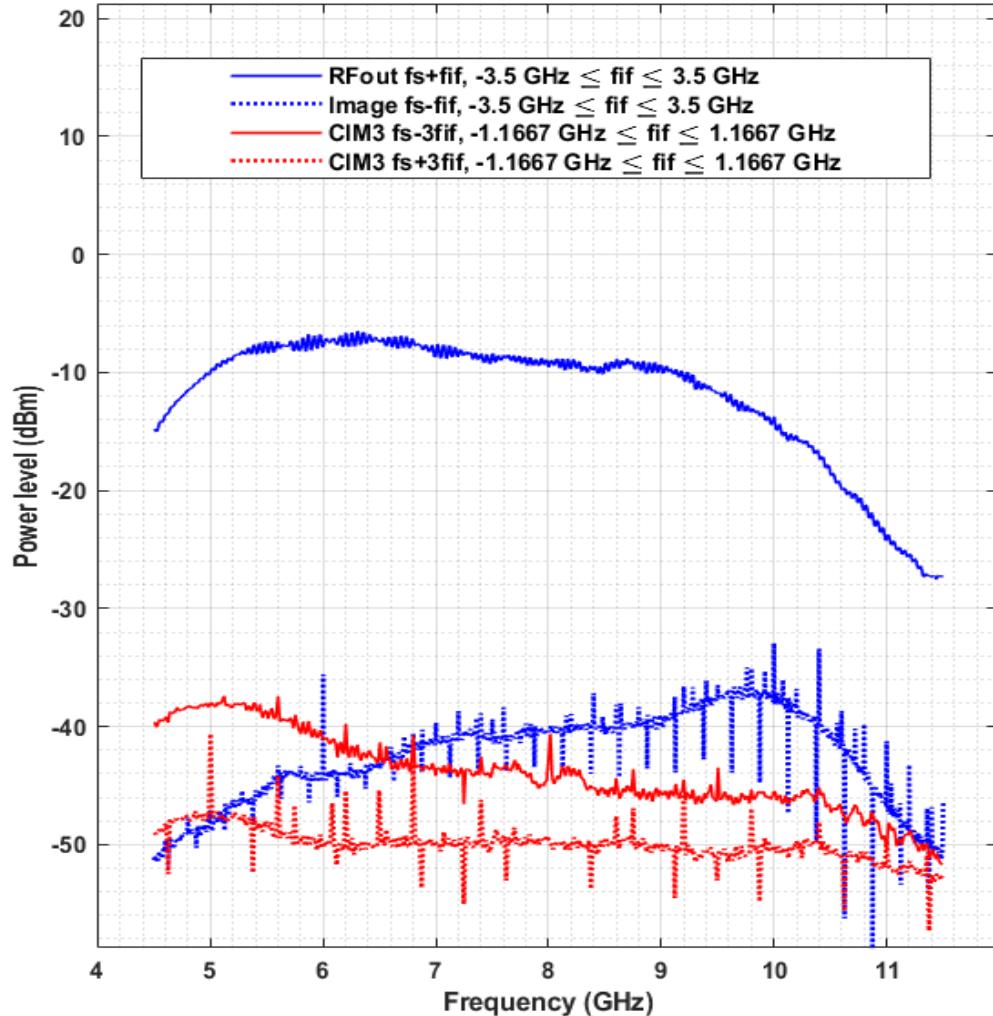


Block	f_{op} (GHz)	Power Consumption (mW)
RFDAC	8GHz	19
Buffer Amplifier	8GHz	6
LO Generation	16GHz	99
DFE	8GHz, 2GHz	135

Power consumption of DFE includes ramper, NCO, MSI, experimental and debugging blocks

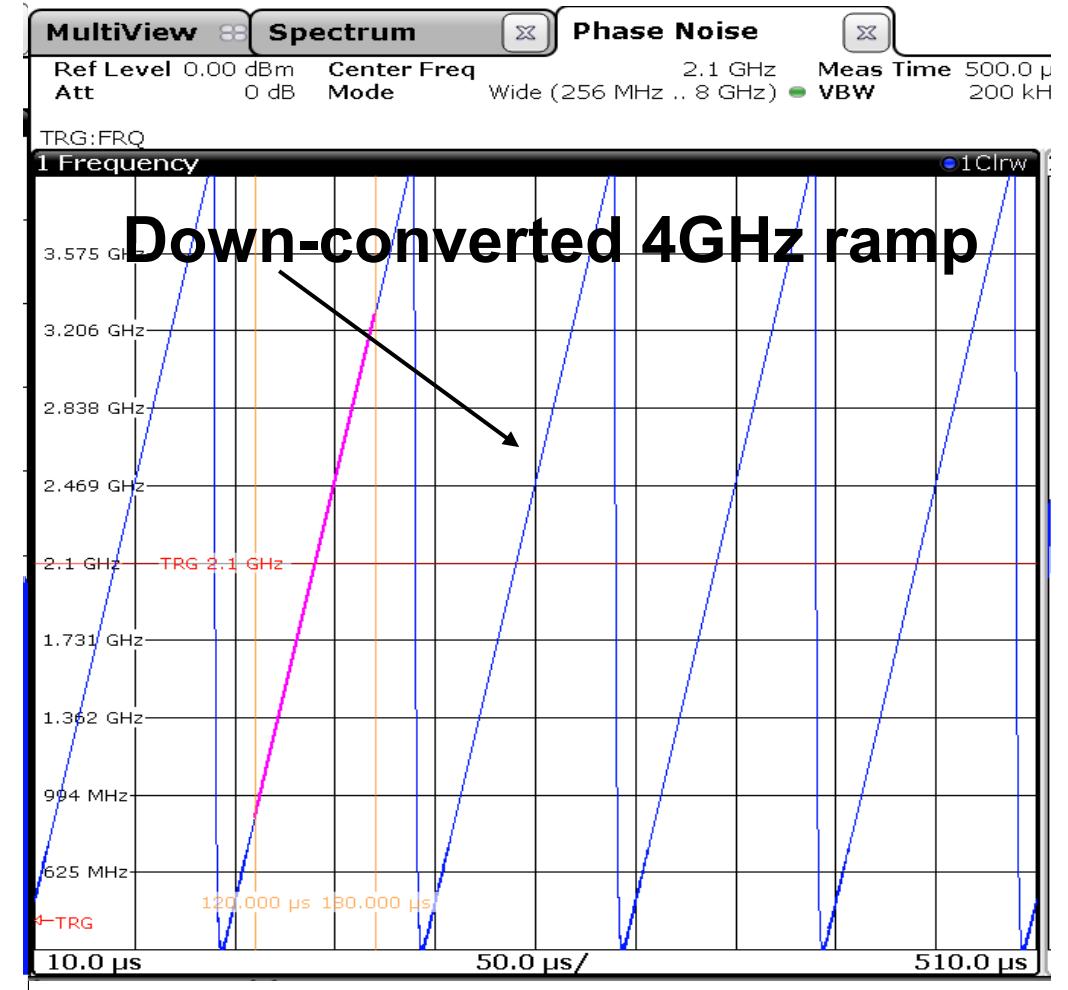
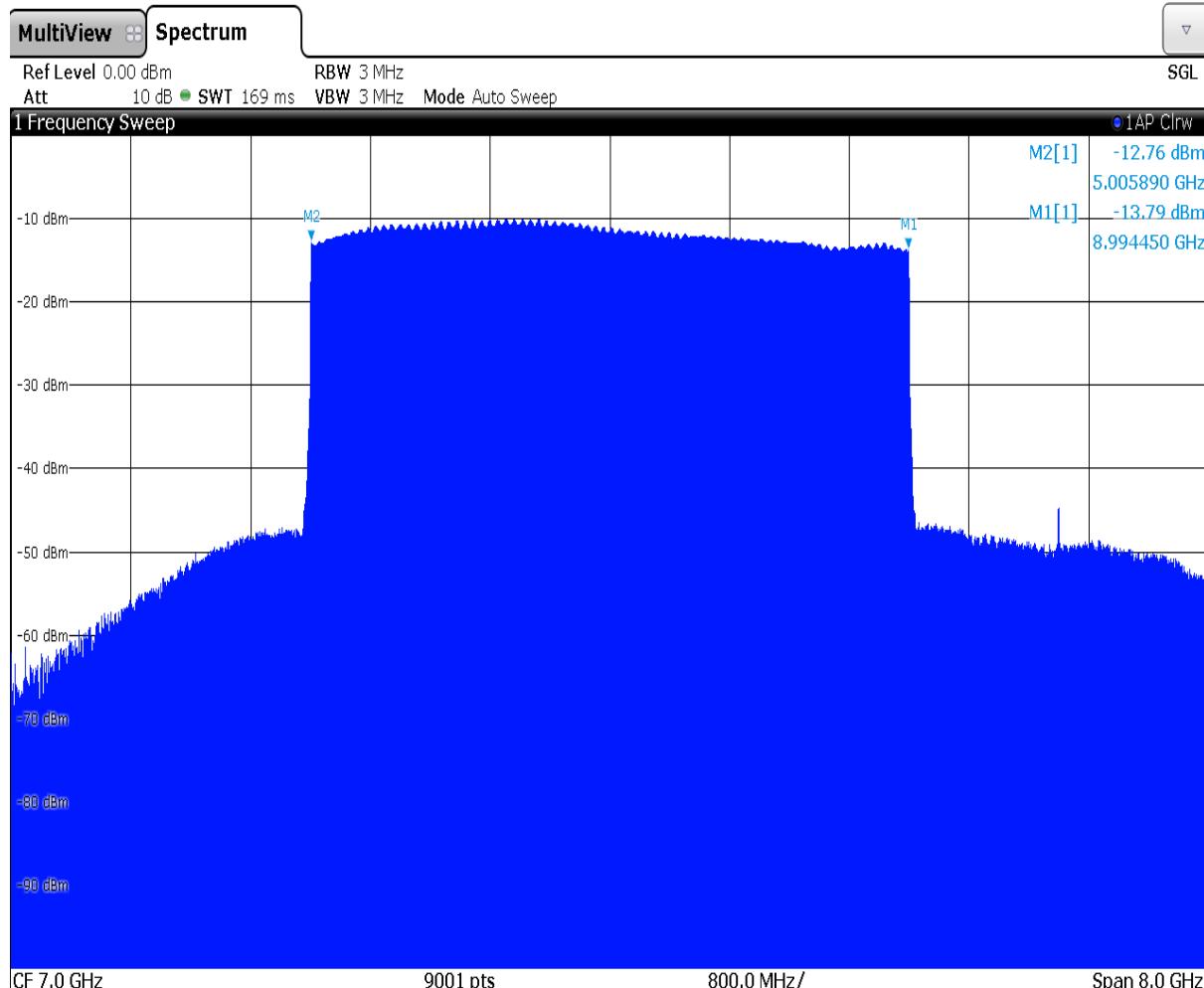
25.4: A 4b RFDAC at 8GS/s for FMCW Chirps with 4GHz Bandwidth in 10μs

Measurement Results - Spectral Characterization



- RF output power of -7dBm
- The average CIM3 level is at 32dBc
- The average image rejection 34dBc

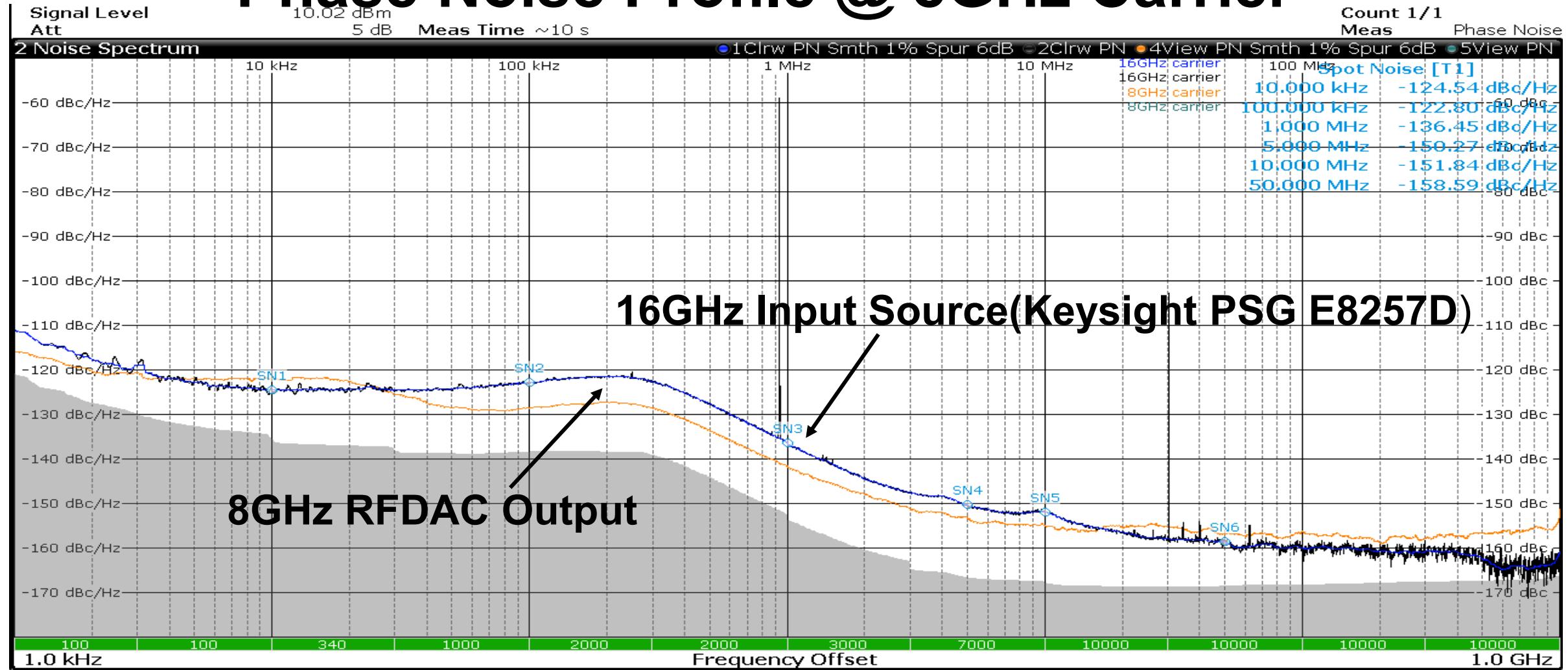
Spectral and Transient Characteristics



- Power variation within 3dB across the 4GHz bandwidth

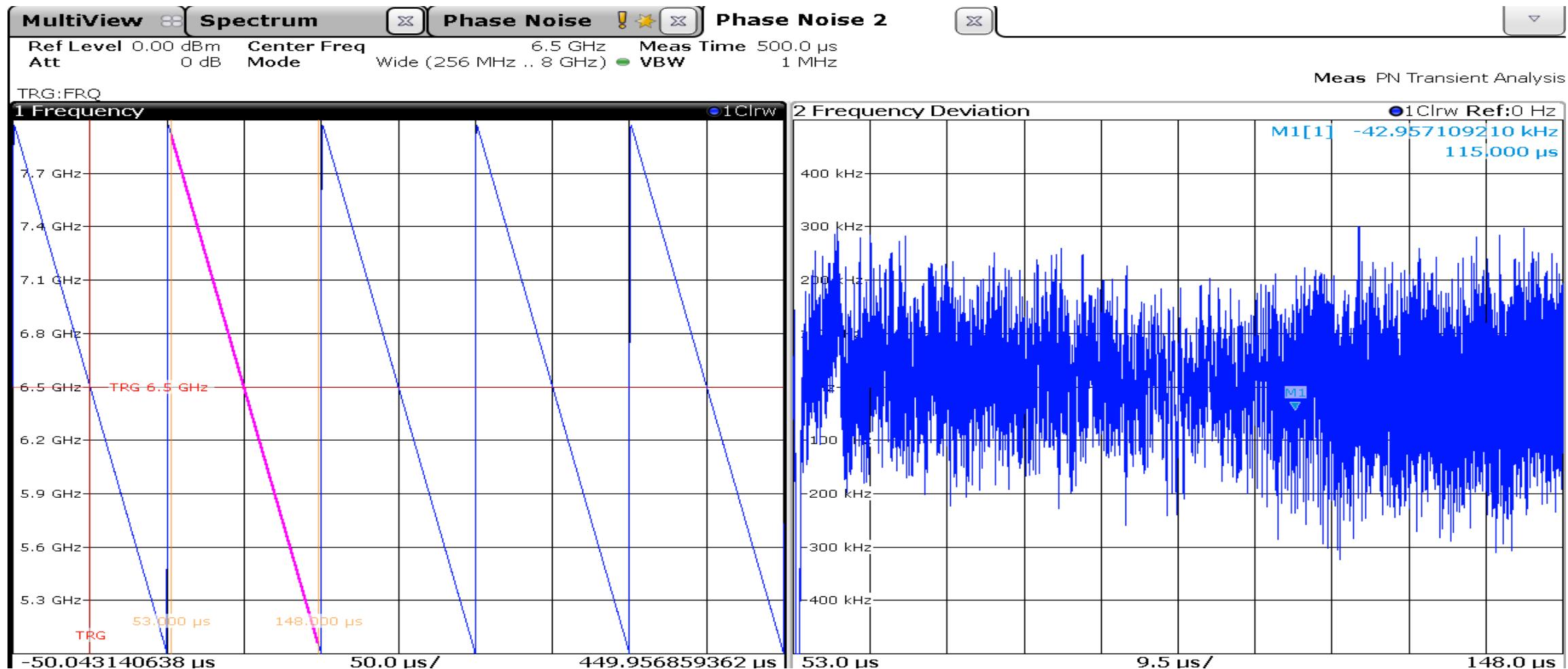
- Settling time is negligible

Phase Noise Profile @ 8GHz Carrier



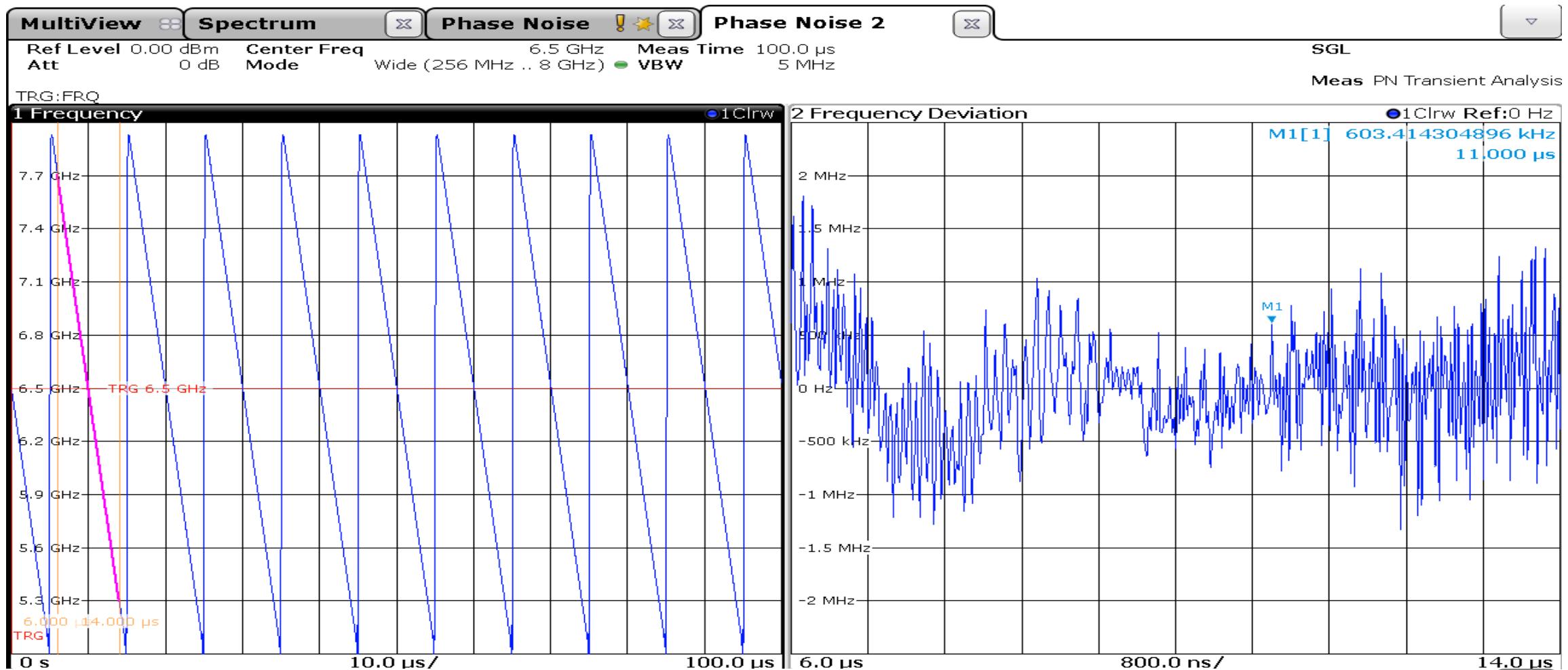
- 140dBc/Hz at 1MHz offset from the 8GHz carrier
 - 120dBc/Hz at 1MHz carrier from 79GHz carrier

Measurement Results – Transient Behavior



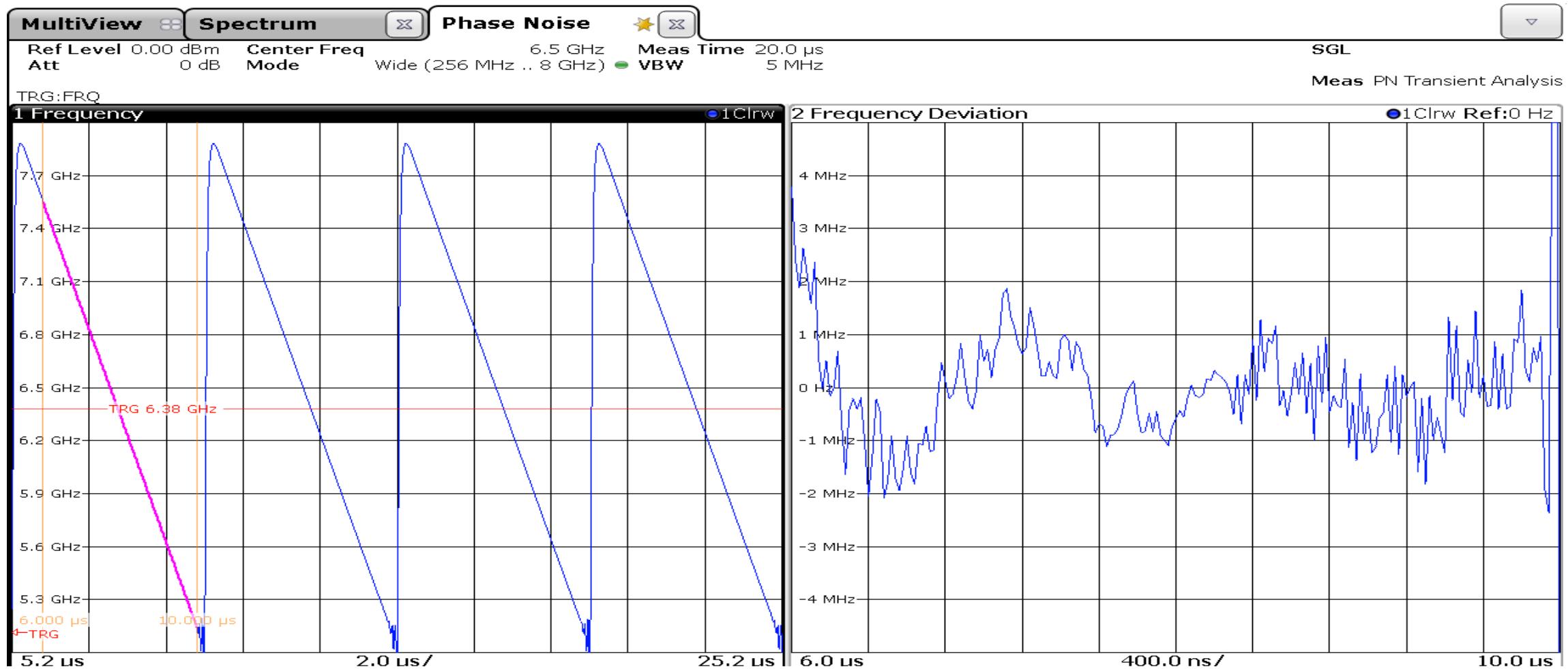
- 5 to 8GHz ramp in 100 μ s
- Rms frequency error for 30MHz/ μ s is 76kHz

Measurement Results – Transient Behavior



- 5 to 8GHz ramp in 10μs
- Rms frequency error for 300MHz/μs is 251kHz

Measurement Results – Transient Behavior



- 5 to 8GHz ramp in 5 μ s

Comparison Table

RFDAC's

Frequency Modulators

	Yiyu Shen, JSSC 2022	Mehrpoor, JSSC 2018	This work
Architecture	DDRM IQ	IQ interleaved RFDAC	DDFS + RFDAC
Matching Network	Off-Chip	Off-Chip	On-Chip
Amplitude Resolution Bits	12	9	4 + 1 sign
Peak Pout (dBm)	18.2	9.2	-8 to -20
Bandwidth (MHz)	320	57	4000
IQ Image (dBc)	-54@2GHz	-49	-39@5GHz, -30@9GHz
CIMD (dBc)	-57.5 ¹ @2GHz	-44	-36@9GHz
Frequency LO (GHz)	2.4	3	16 External LO)
Frequency Out (GHz)	0.5 to 3	0.9 to 3.1	5 to 9
Modulation Scheme	256 QAM	64 QAM	FMCW
DC Power (mW)	540	146 ²	Digital⁴ - 135
Technology	40nm	40nm	28 nm
Supply Voltage (V)	1.1 ¹ /1.7 ¹	1;1	0.9
Area (mm²)	1.1	0.21	RFDAC - 0.033⁵, DFE - 0.145⁵

	This work	Wei Deng, JSSC 2022	P.T.Renukaswamy[5], ISSCC 2020	Z.shen[1], ISSCC 2021	H. Shanan[2], ISSCC 2022	C.Dmytro[4], ISSCC 2018
Frequency Out (GHz)	5 to 9	11.1 to 14.2	8.3 to 11.7	21.8 to 25.4	8.8 to 12	20.4 to 24.6
Chirp BW (GHz)	4	2.27	1.21	3.2	0.65	0.208
RMS FM Error (kHz)	251(300MHz/us), 76(30MHz/us)	224(33.6MHz/μs)	168(94.5MHz/μs)	7.35 - 309	37(23MHz/20μs)	112(208MHz/1.2μs)
Idle time (μs)	0.01	-	5	-	12.5	0.2
Max Chirp Slope (MHz/us)	800	131	94.5	320	65	173.3
PN at 1MHz offset (dBc/Hz)³	-120.02	-95.7	-90.7	-82.9	-102	-90
DC Power (mW)	Analog⁴ - 125 Digital⁴ - 135	23	11.7	28	187	19.7
Technology	28nm	28nm	28nm	40nm	28nm	65nm
Supply Voltage (V)	0.9	1	0.9	1.1	-	-
Area (mm²)	RFDAC - 0.033⁵, DFE - 0.145⁵	0.31	0.99	0.26	2	0.48

1 - Inferred from figure, 2 - Without LO generation, 3 - Normalized to 79GHz, 4 - Including LO generation and distribution, 5 - Core area

Conclusion

- DDFS + RFDAC based frequency modulator for Automotive radar
- 4 bit RFDAC at 8GS/s in 28nm CMOS technology
- Phase noise of -140dBc/Hz at 1MHz offset from the 8GHz carrier
- Negligible settling time <10ns
- Frequency modulated ramps with 4GHz bandwidth
- Eliminates the trade-off between the modulation bandwidth and loop bandwidth needed for optimum phase noise
- Digital approach is well suited for CMOS integration

Radar measurements with range Doppler maps of a golf ball is ongoing !

A 1-5GHz All-Passive Frequency-Translational 4th Order N-path Filter with Low-Power Clock Boosting for High Linearity and Relaxed P_{dc}- Frequency Trade-Off

Aravind Nagulu¹, Mingyu Yuan¹, Yi Zhuang¹, Sasank Garikapati², Harish Krishnaswamy²

¹*Washington University in St. Louis, St. Louis, MO*

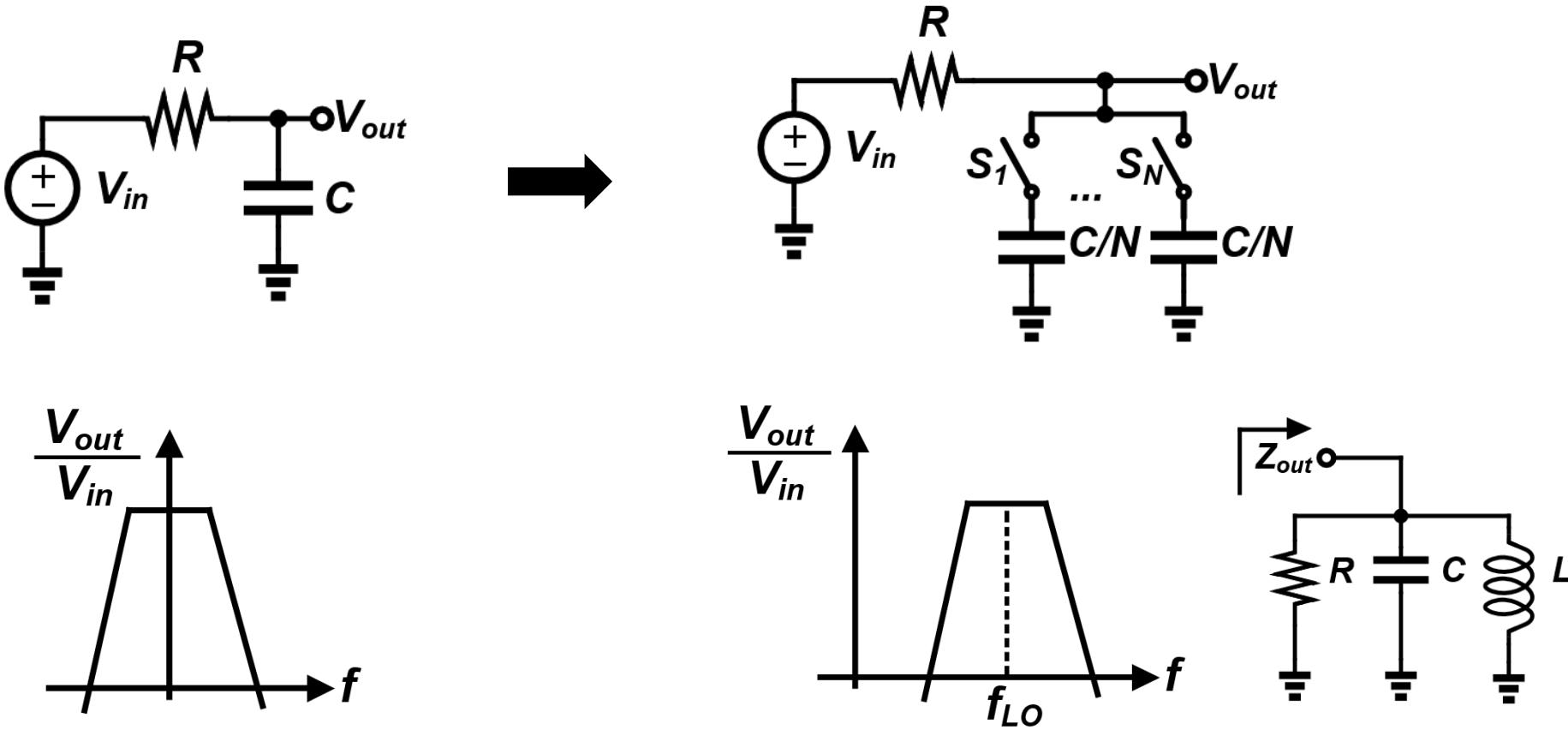
²*Columbia University, New York, NY*



Outline

- **Introduction**
- **A 1-5GHz All-Passive Higher-Order N-Path Filter in 65nm CMOS**
- **Measurement Results**
- **Conclusion**

N-Path Filters in RF Systems



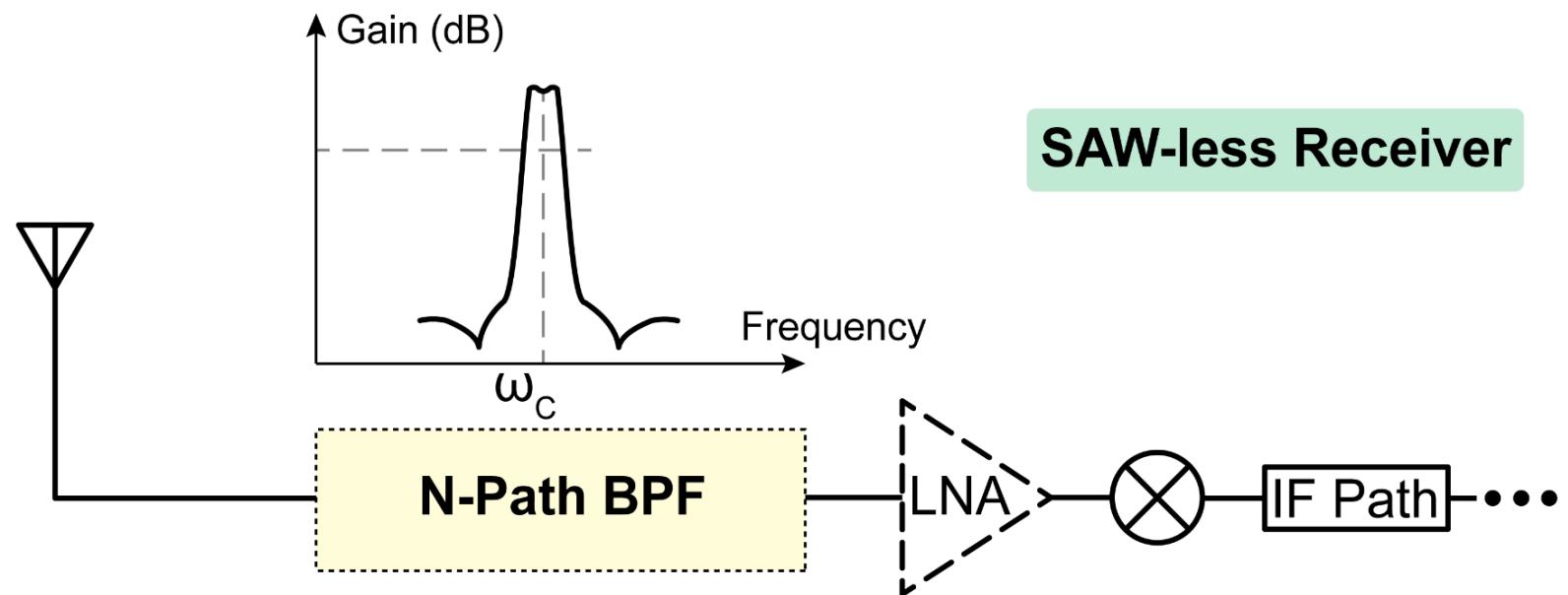
[Franks, Bell System Tech. Journal '60], [Ghaffari, JSSC '11]

N-path filters can enable compact, tunable, high-Q, and high-linearity filters on chip.

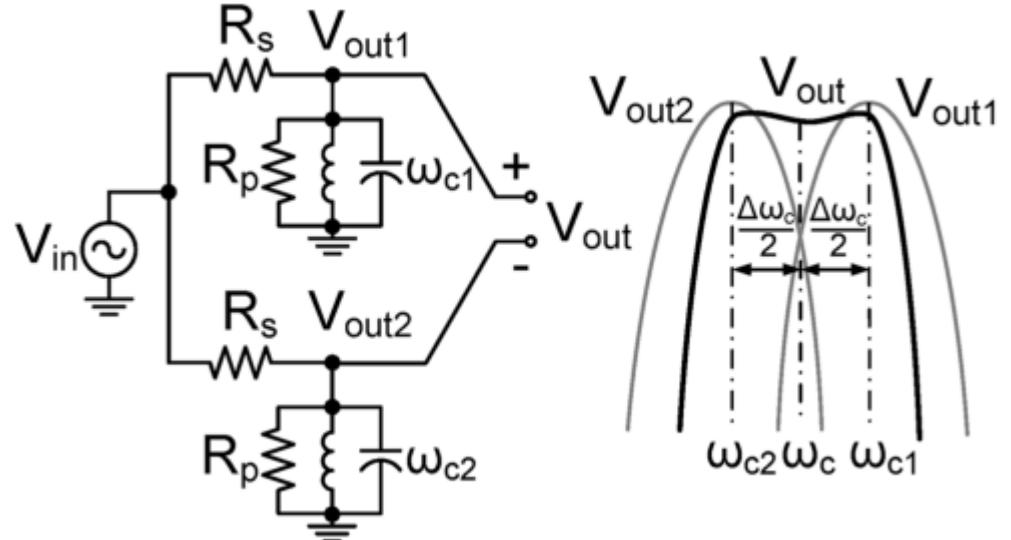
Applications of Higher Order N-Path Filters

Higher-Order N-path Filters:

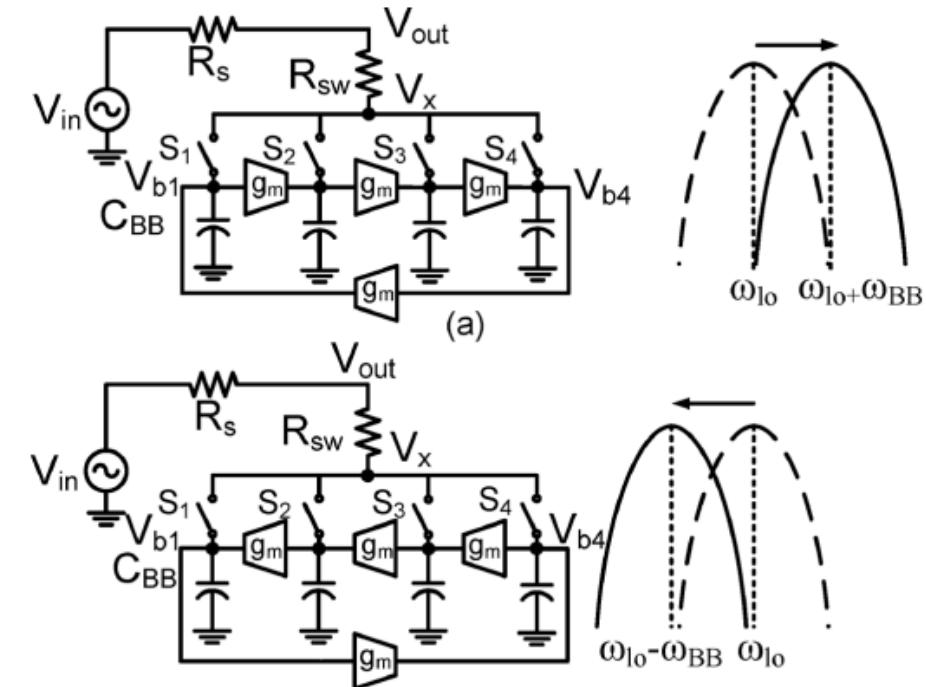
- ✓ High Selectivity
- ✓ High OOB Rejection
- ✓ Widely Tunable
- ✓ Good Linearity
- ✓ Small Area



Higher Order BPF: Subtraction of Low-Order BPFs

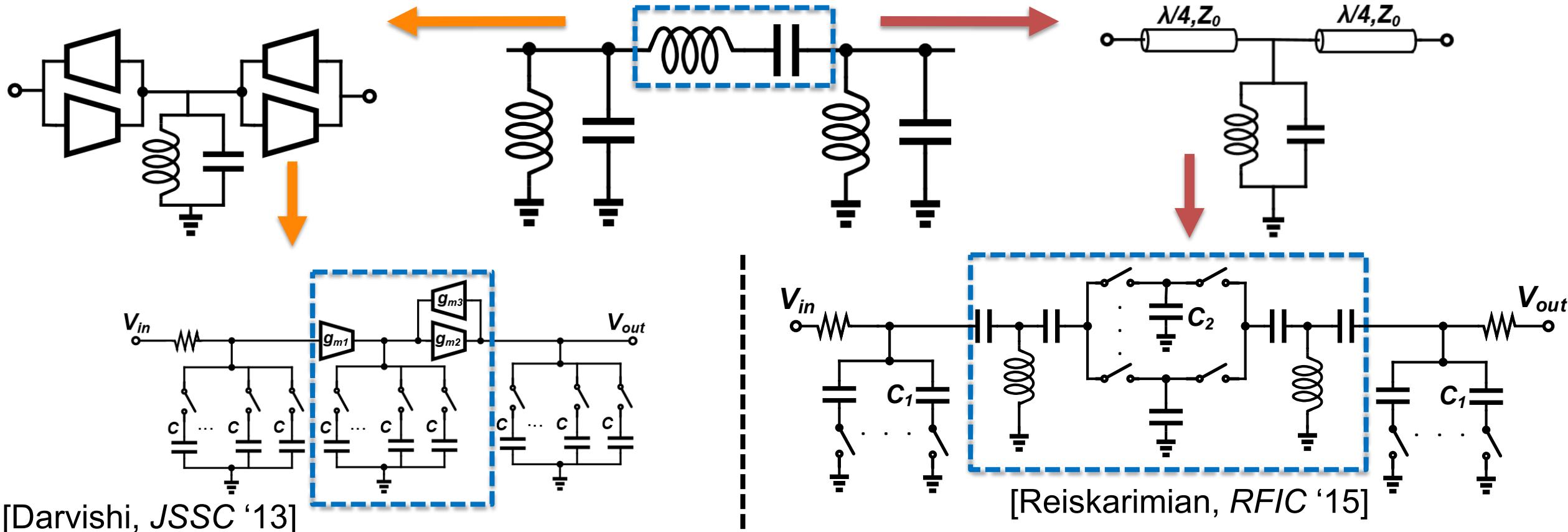


[Darvishi, JSSC 2012]



- Subtraction of 2 frequency shifted N-path filters also results in higher order filtering.
- Frequency shifting:
 - Active circuits – Adds noise, non-linearity and PDC.
 - Separate clock synthesizers – Complexity and spurious spurs.

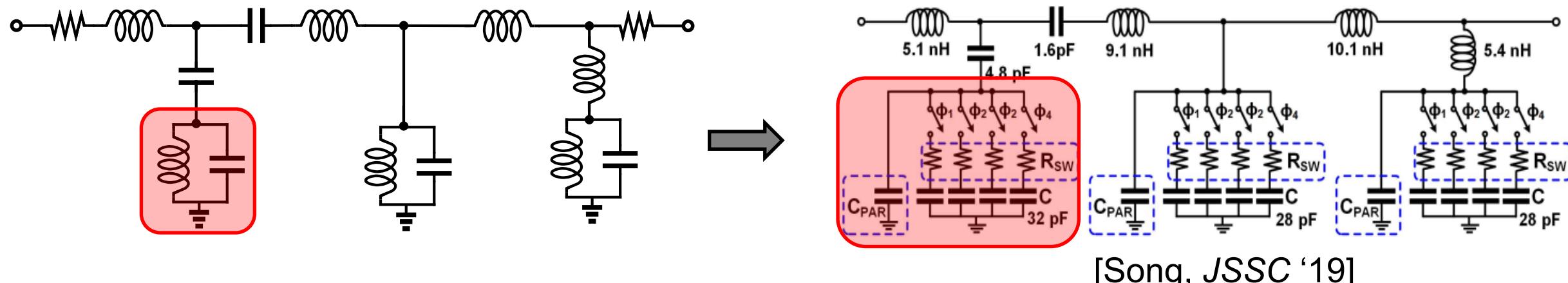
Higher Order BPF: Coupled N-Path Filters



Using active devices for impedance inversion leads to a power-hungry design.

Quarter Wavelength impedance inverters leads to large area and small tuning range

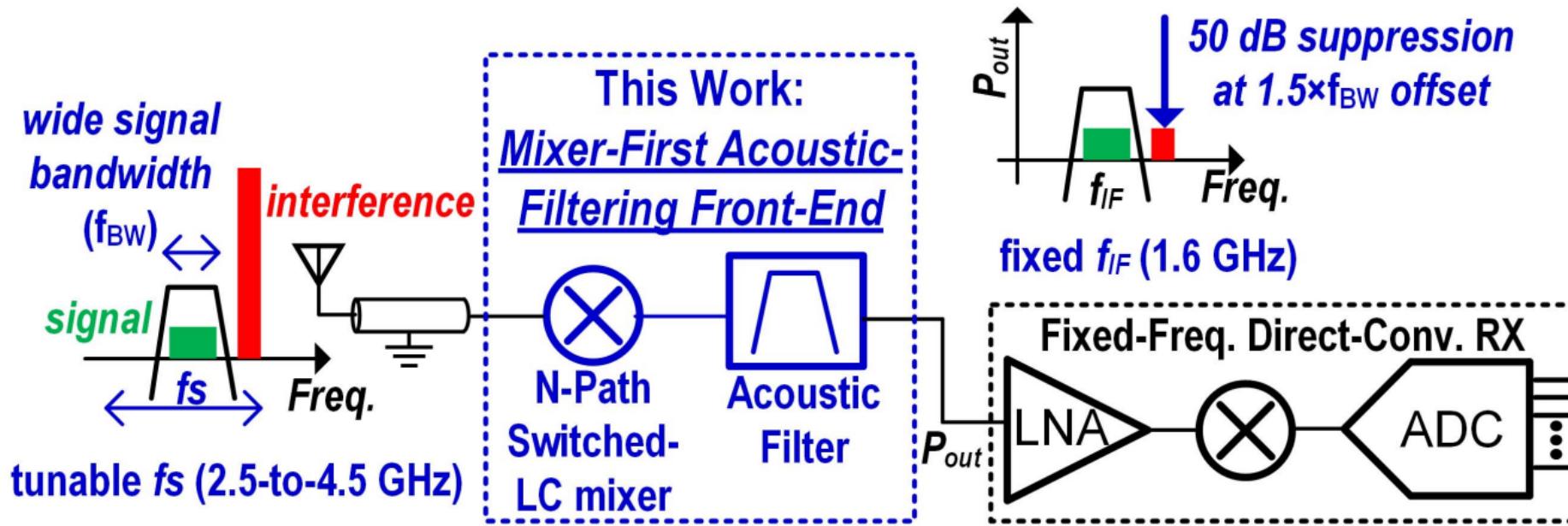
Higher Order BPF: Coupled N-Path Filters



[Song, JSSC '19]

- N-path resonators are coupled using passive components
- Using inductance for isolating N-path resonators leads to a bulky and lossy design.

Heterodyne RX with Fixed-Acoustic Filtering



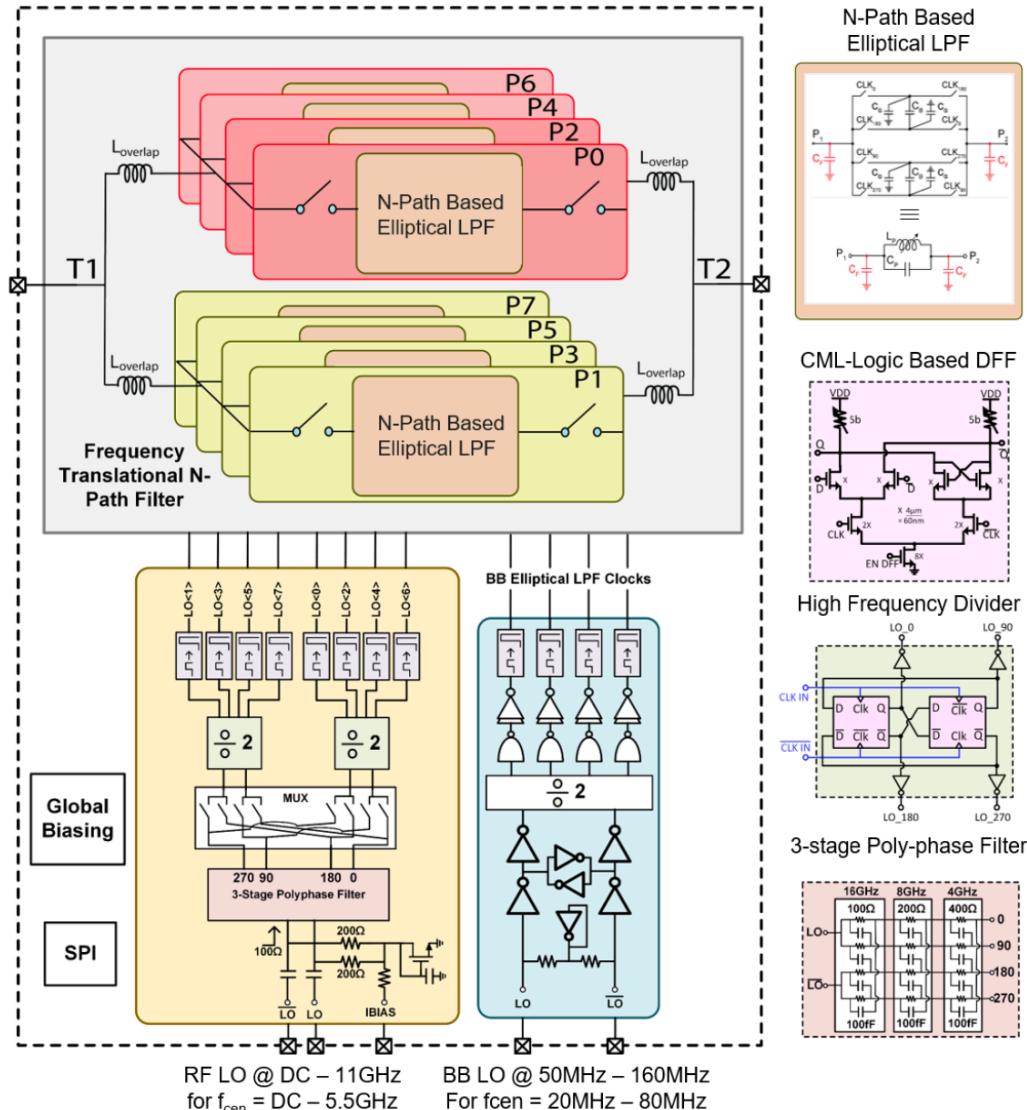
[Seo, JSSC 2021]

- A single fixed-frequency high-order acoustic filter is used after an N-path switched-LC mixer
- Requires off-chip acoustic filter, on-chip LC filters as acoustic filter shapers leading to high isolation.

Outline

- Introduction
- A 1-5GHz All-Passive Higher-Order N-Path Filter in 65nm CMOS
- Measurement Results
- Conclusion

Higher Order BPF With Elliptical LPFs



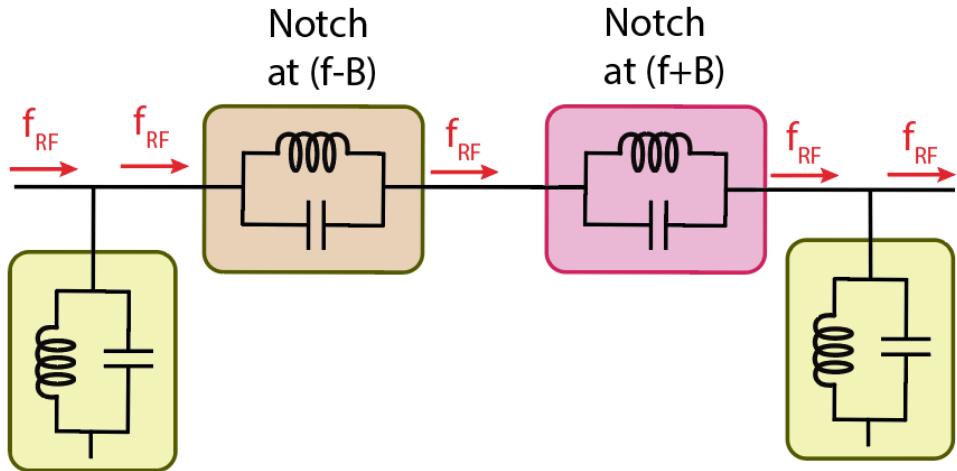
- **Higher-Order Filtering in N-Path Filters based on N-path elliptical LPFs** to enable high selectivity and OOB rejection.
- **N-Path filters with overlapping LOs** enables high frequency operation.
- **Switched-Capacitor Clock Boosting in N-path Filters** for high power handling

Outline

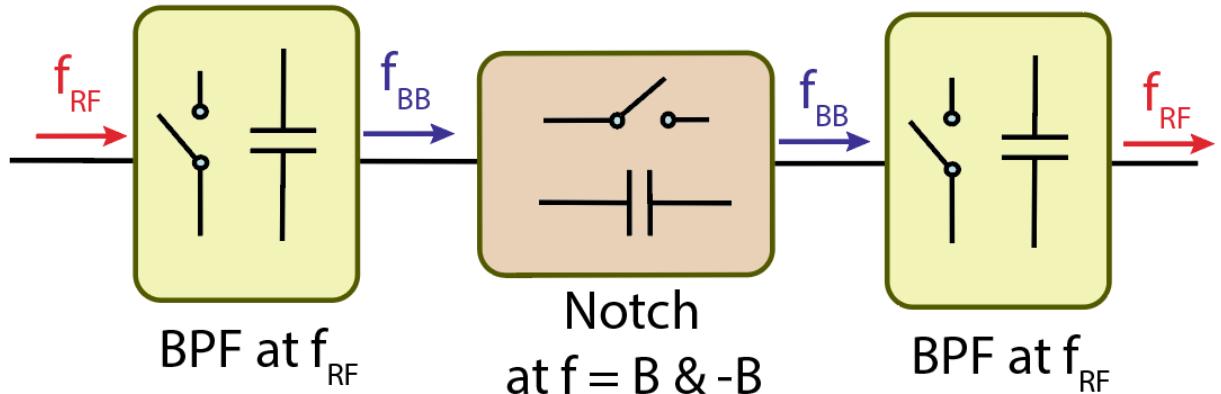
- Introduction
- A 1-5GHz All-Passive Higher-Order N-Path Filter in 65nm CMOS
 - Frequency-Translational N-path Filters
 - High Frequency N-Path Filters with Overlapping Clocks
 - Switch-Capacitor Clock Boosting in N-Path Filters
- Measurement Results
- Conclusion

Frequency-Translational N-Path Filters

Conventional Filter with OOB Notches



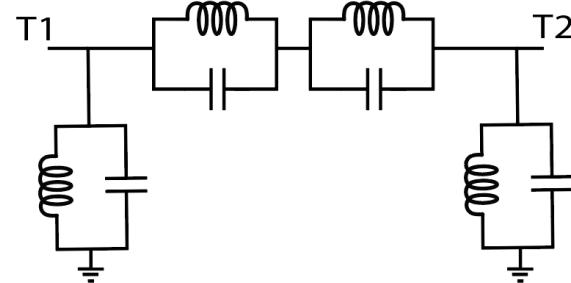
Frequency-Translational N-Path Filter with OOB Notches



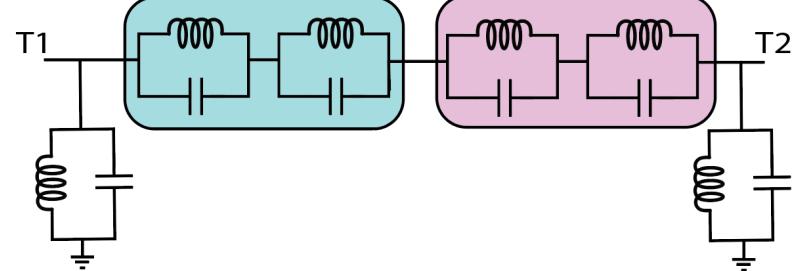
- Frequency translational N-path filter architectures enable intermediary filter nodes/resonators at lower frequencies, thus *breaking the trade-off between operating frequency and loss/power consumption*.
- Translation to baseband also reduces number of resonators by half due to symmetric filter profile around DC.

Higher Order N-Path Elliptical BPF

Conventional LC BPF
3rd Order

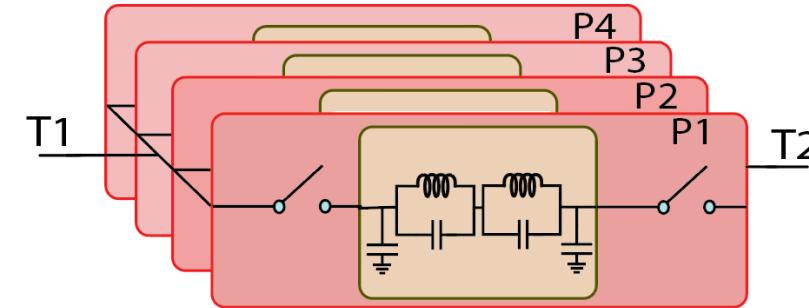
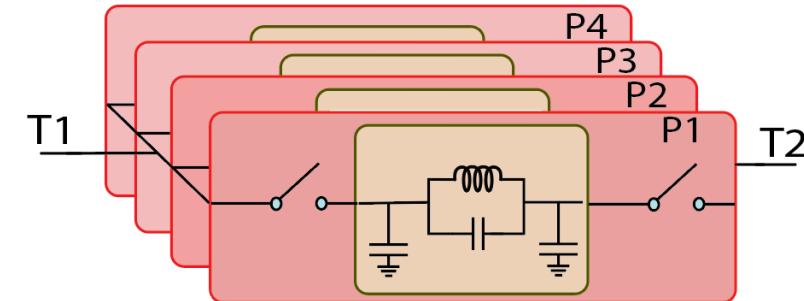


5th Order



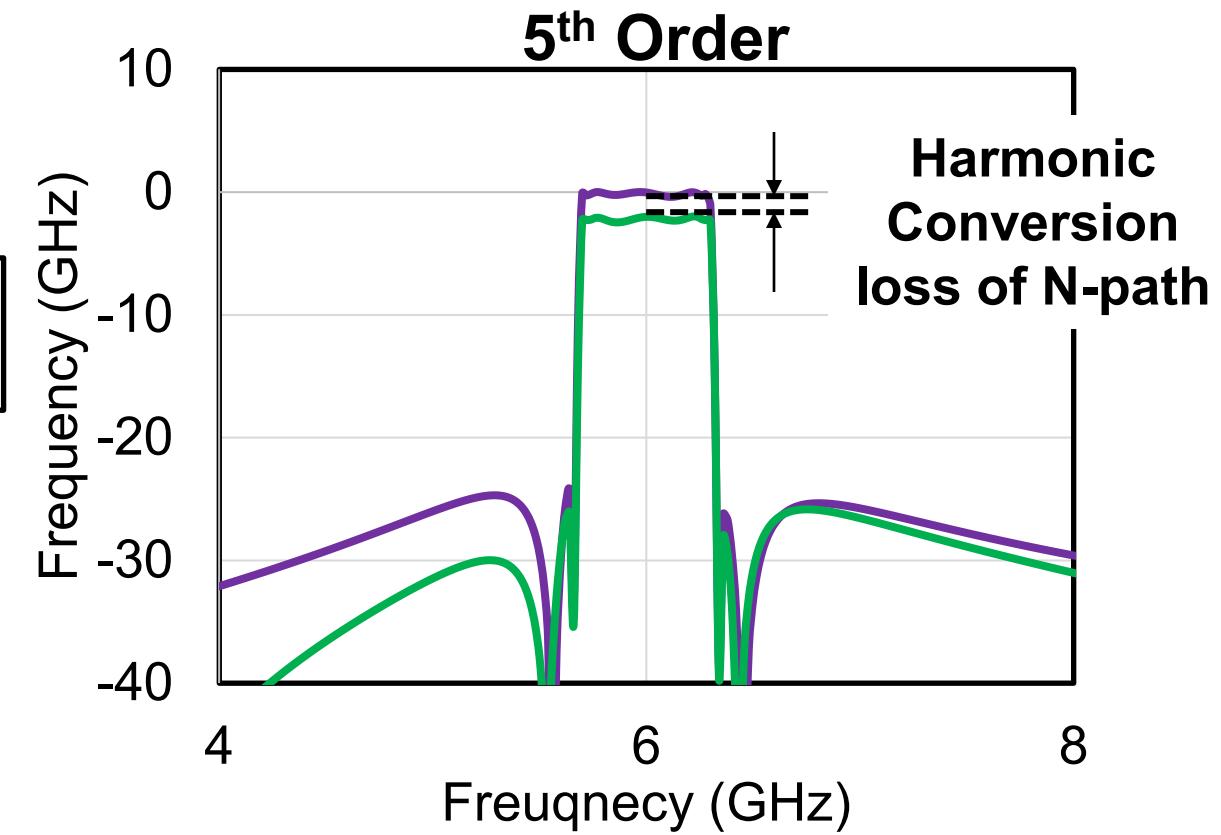
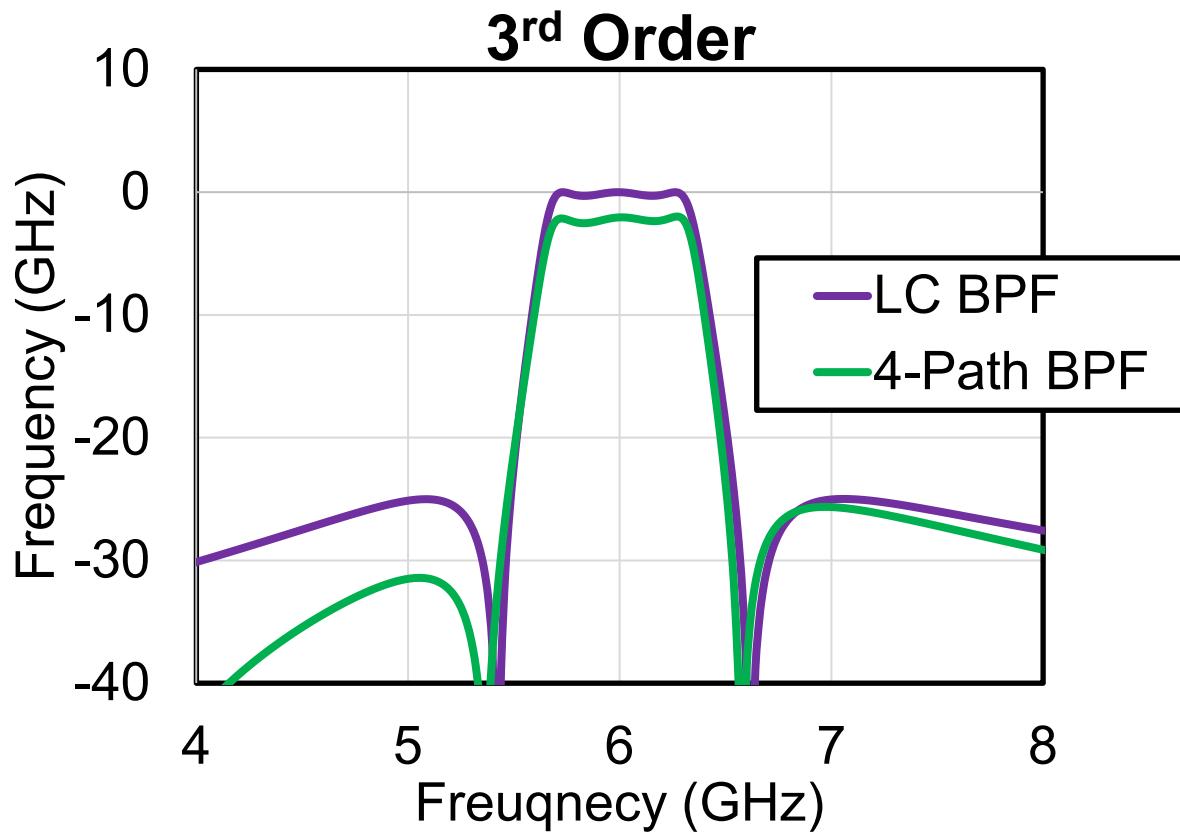
- ✗ Center Frequency cannot be tuned
- ✗ 3dB insertion loss requires an inductor Q of 100-120

N-Path Based BPF



- Center Frequency can be tuned easily
- 3dB insertion loss requires an inductor Q of 10-20

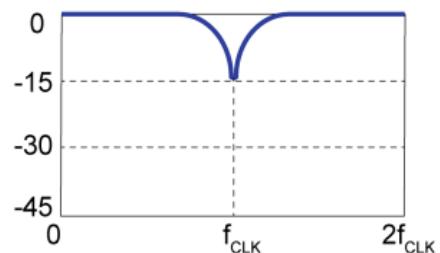
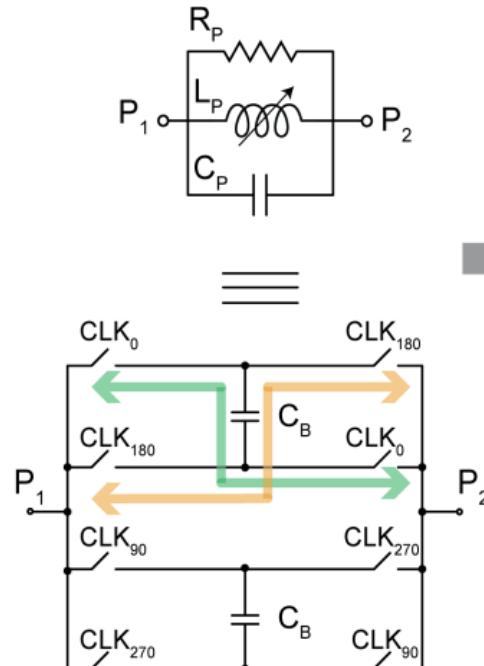
Higher Order N-Path Elliptical BPF



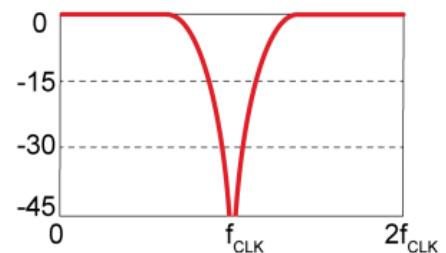
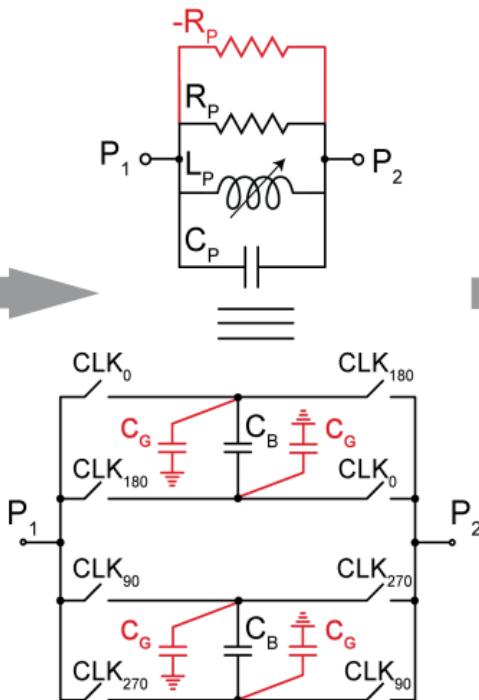
- Higher order BPFs can be realized by switching higher order LPFs
- Inductances required to create a higher order LPF are very large for on-chip integration

Inductorless N-Path Based Elliptical LPF

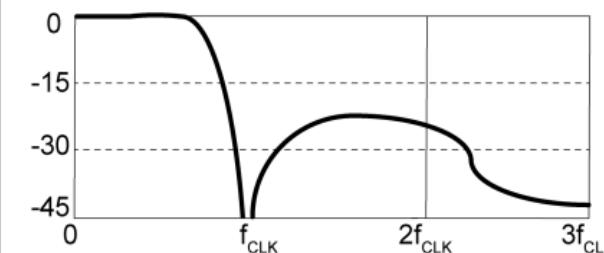
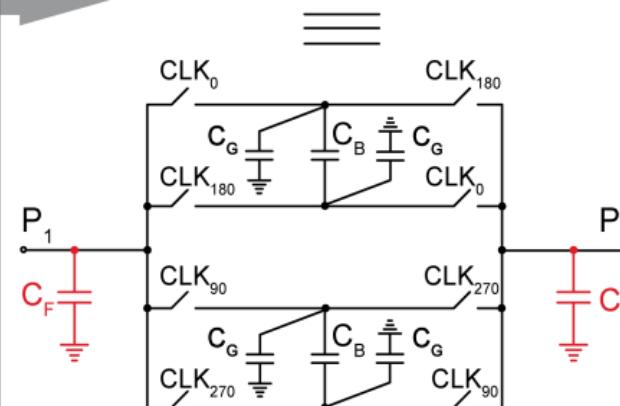
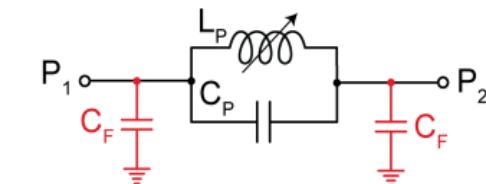
Notch Filter



Notch Filter w/ Deep Notch

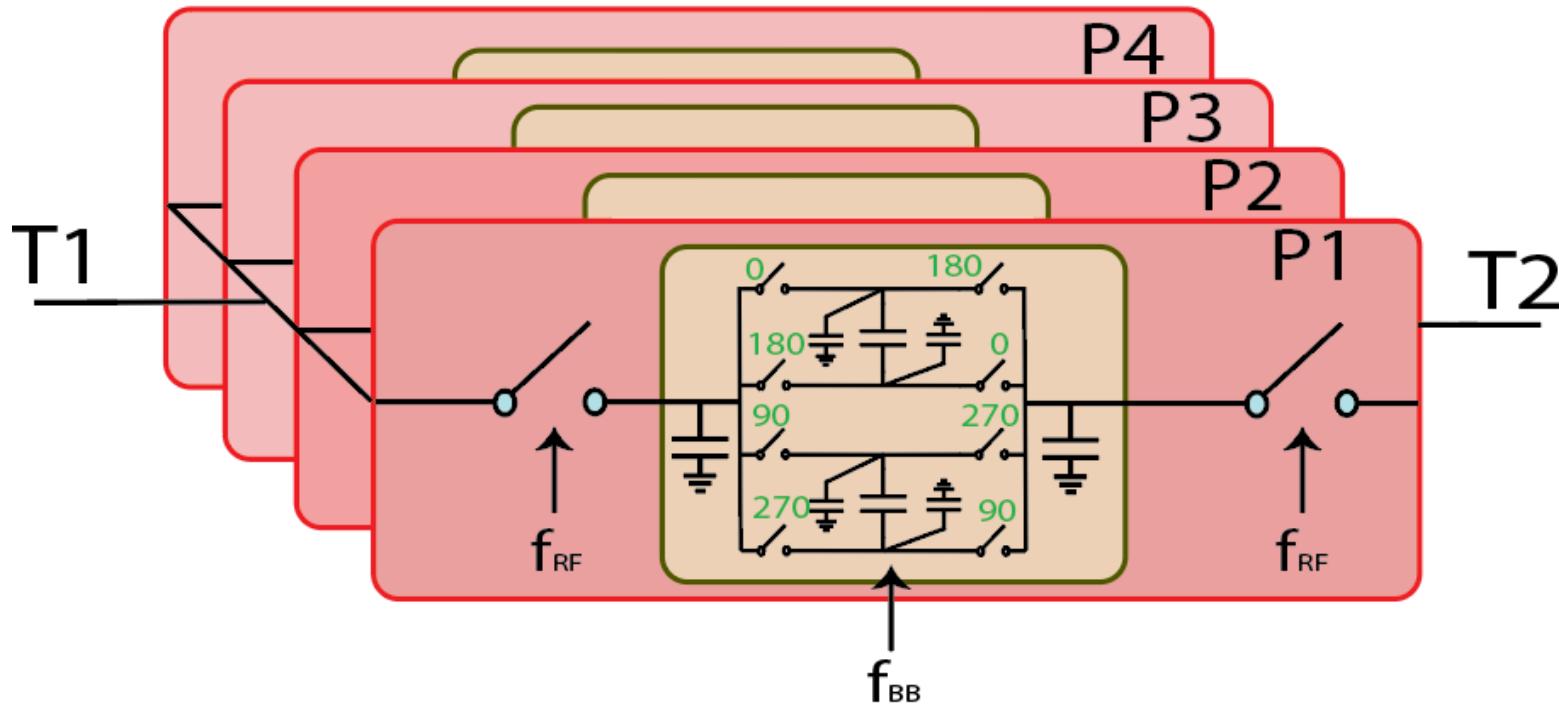


3rd Order Elliptical LPF



[Korshidian,
IMS 2020]

Inductorless Passive Higher Order N-Path

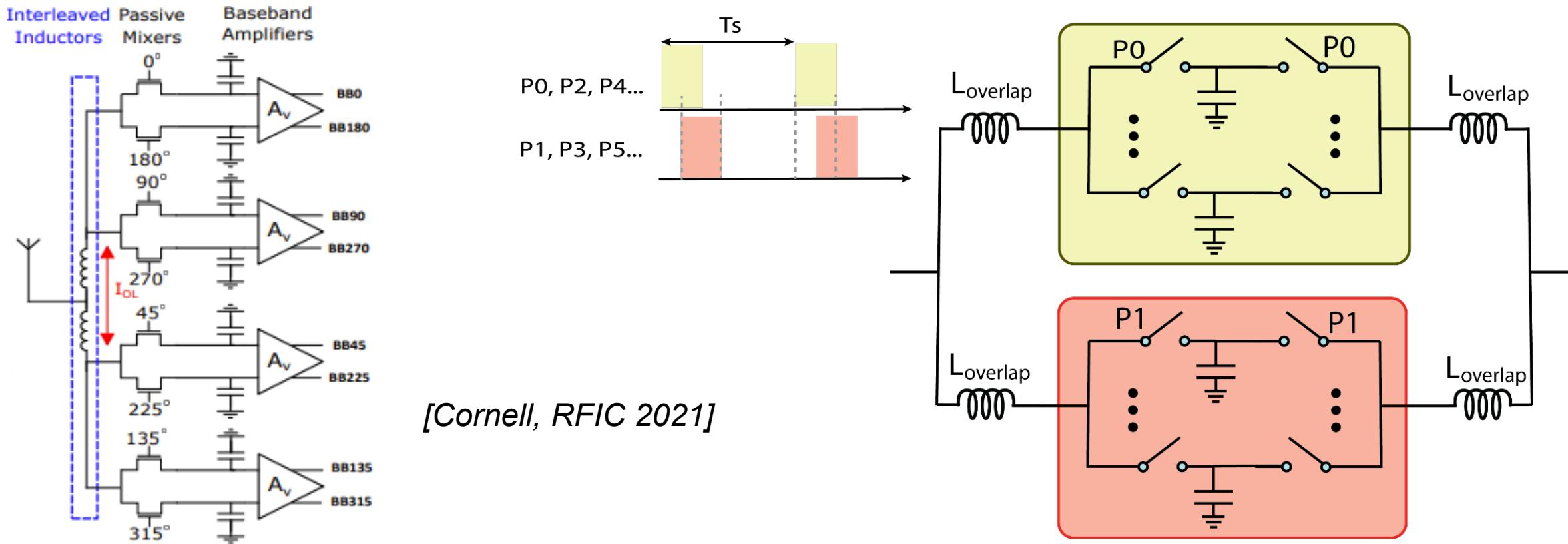


- A 3rd order elliptical BPF can be realized by clocking an N-path based elliptical LPF
- Center frequency of the BPF can be controlled by f_{RF}
- Bandwidth of the BPF can be controlled by f_{BB} and capacitors in the LPF

Outline

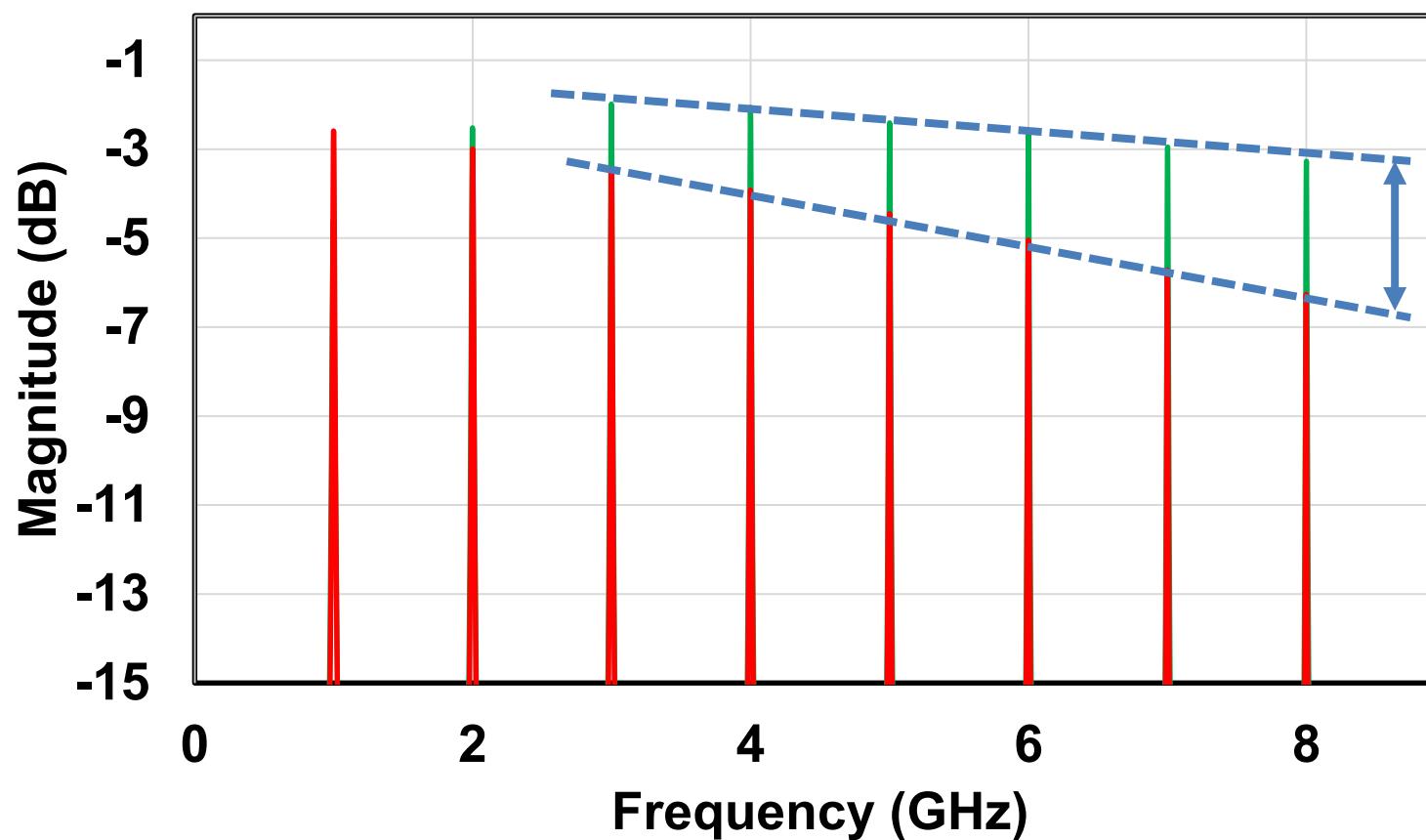
- Introduction
- A 1-5GHz All-Passive Higher-Order N-Path Filter in 65nm CMOS
 - Frequency-Translational N-path Filters
 - High Frequency N-Path Filters with Overlapping Clocks
 - Switch-Capacitor Clock Boosting in N-Path Filters
- Measurement Results
- Conclusion

N-Path Filters with Overlapping LOs



- At high frequencies, clock rise/fall time occupy significant portion of pulse width and increases the insertion loss of the N-path filters.
- **N-Path filters with overlapping LOs support higher pulse widths which enable lower loss at high frequencies.**

Loss vs. Frequency Using Realistic Clocks



Regular N-Path Filter
N-path w/ Overlapping LOs

High frequency Loss
improves by ~2-3 dB

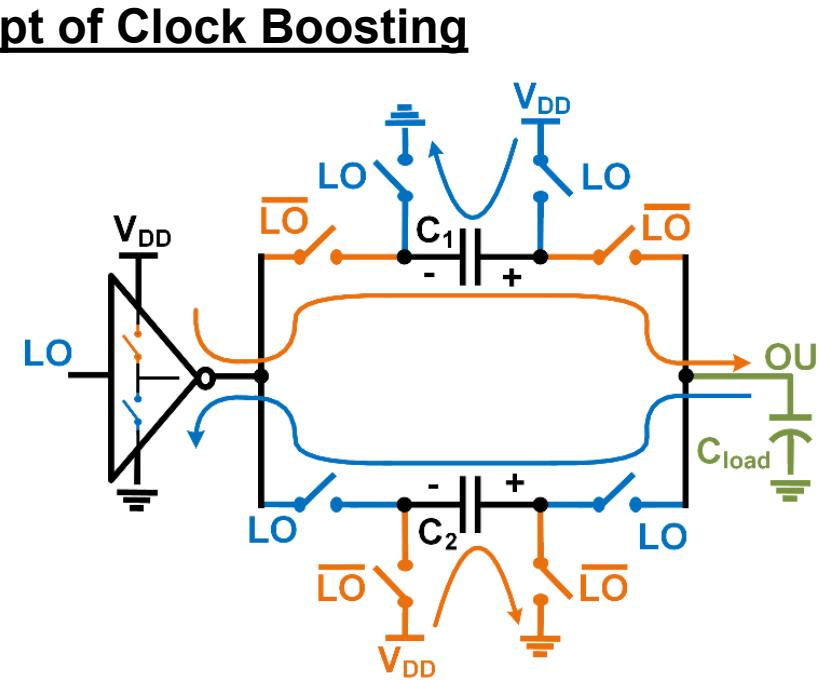
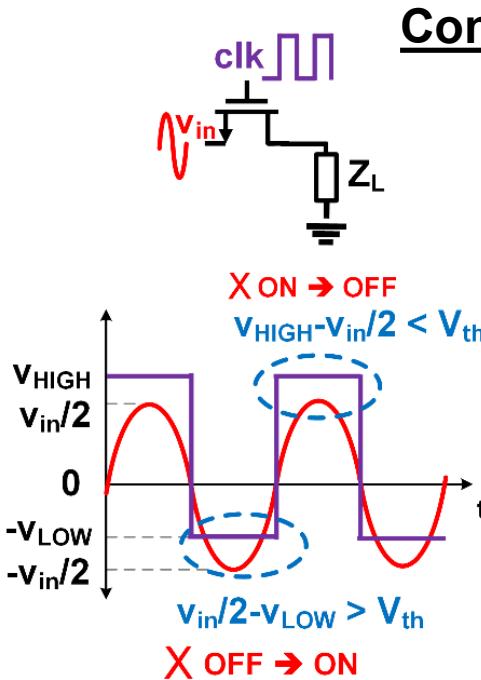
- Using 65nm transistors.
- 8-path N-path filters
- Clock rise/fall time=10ps

High frequency insertion loss of N-path w/ overlapping LOs is ~2-3dB lower when compared to regular 2-port N-path filter.

Outline

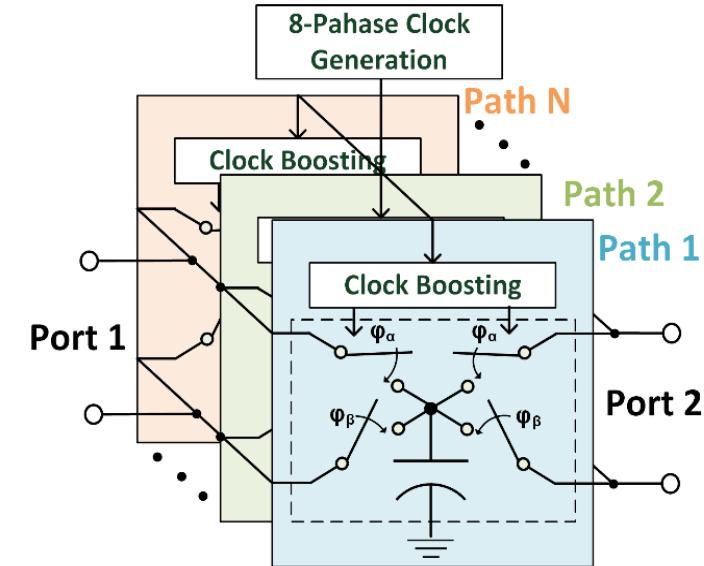
- Introduction
- A 1-5GHz All-Passive Higher-Order N-Path Filter in 65nm CMOS
 - Frequency-Translational N-path Filters
 - High Frequency N-Path Filters with Overlapping Clocks
 - Switch-Capacitor Clock Boosting in N-Path Filters
- Measurement Results
- Conclusion

Switched-Capacitor Clock Boosting in N-path Filters



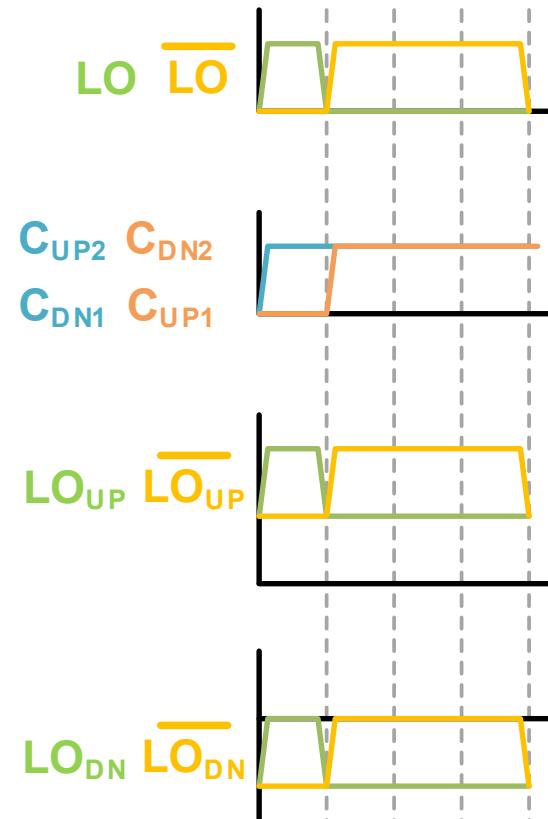
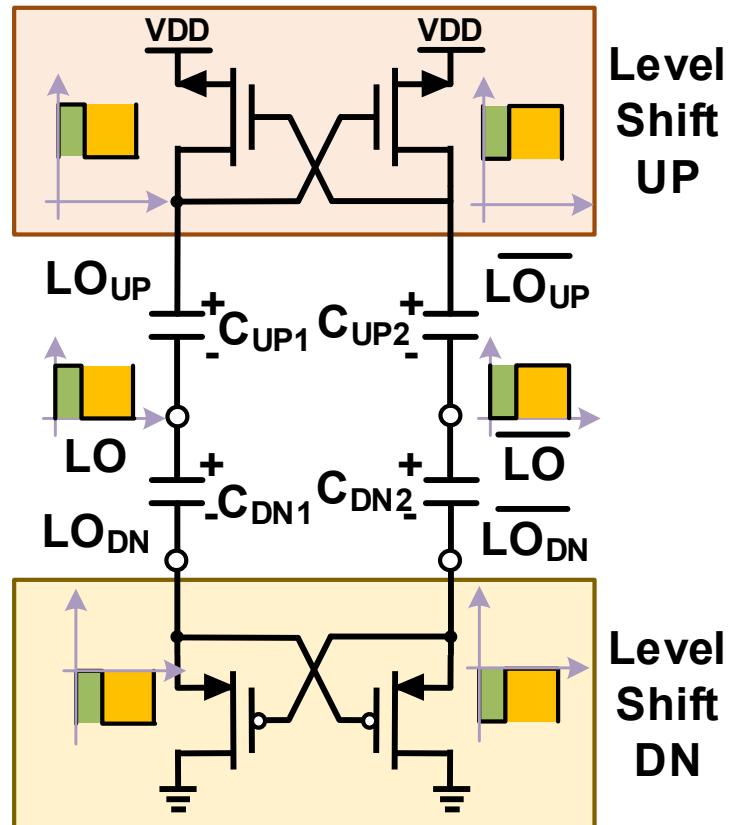
[Nagulu, ISSCC 2020]

N-path with Clock Boosting



- Clocking boosting provides 3x higher clock swing without compromising the device breakdown.
- Clock Boosting improves power handling by +6dBm (CMOS) - +12dBm (SOI).

Nakagome Charge-Pump Based Clock Boosting



A Nakagome Charge-Pump is used to shift the clock voltages up/ down by VDD

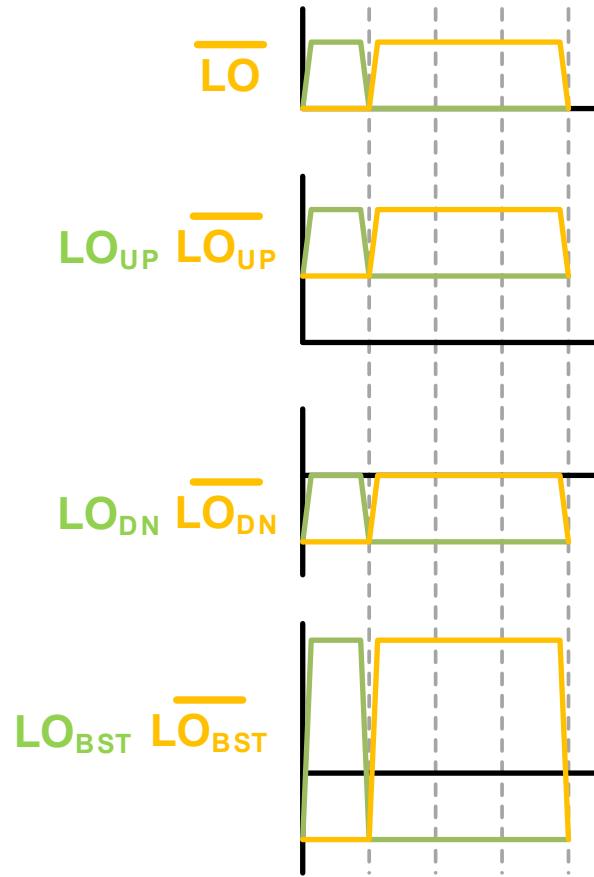
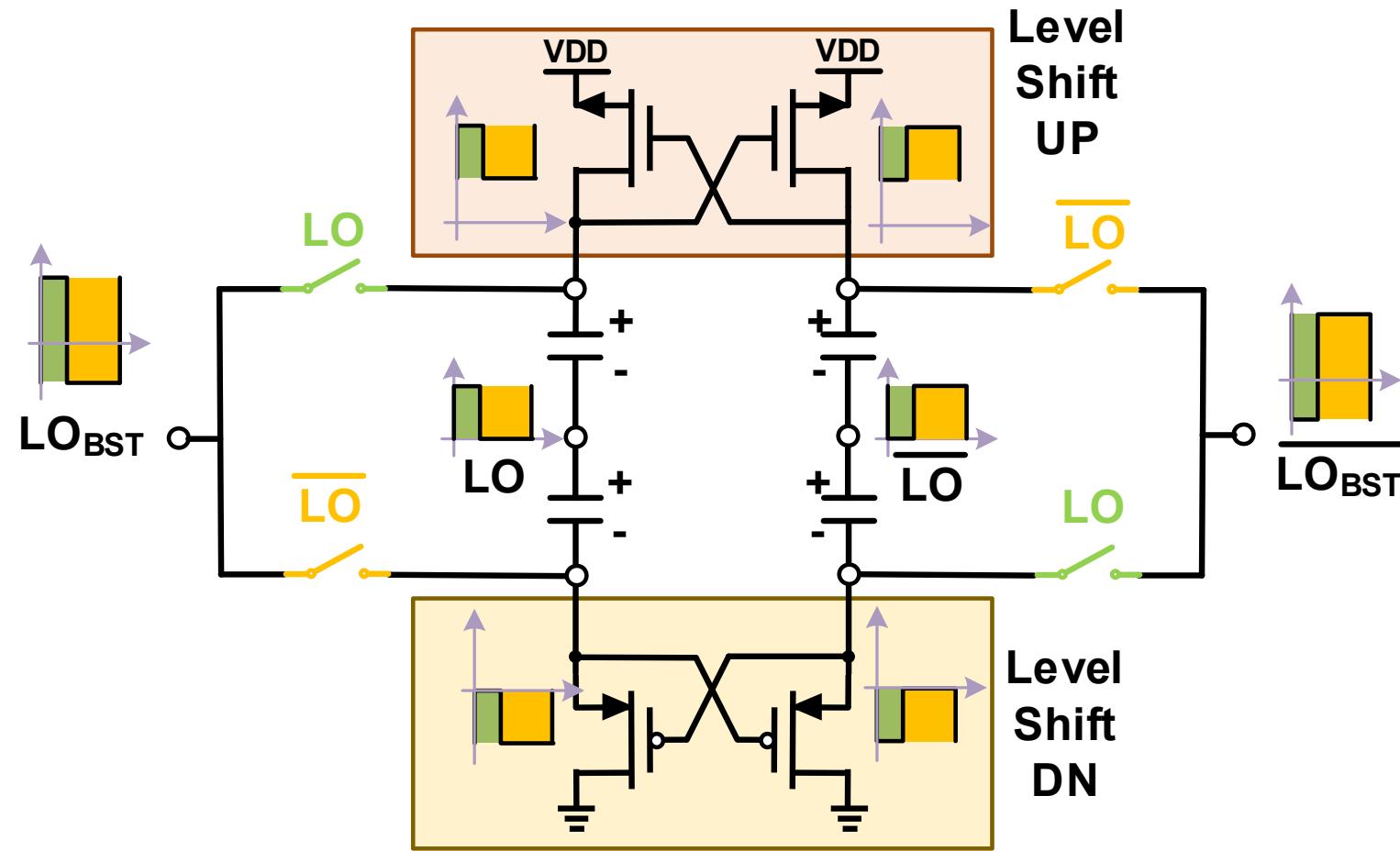
$$V_{LO_UP} = V_{LO} + VDD$$

$$V_{\overline{LO_UP}} = V_{\overline{LO}} + VDD$$

$$V_{LO_DN} = V_{LO} - VDD$$

$$V_{\overline{LO_DN}} = V_{\overline{LO}} - VDD$$

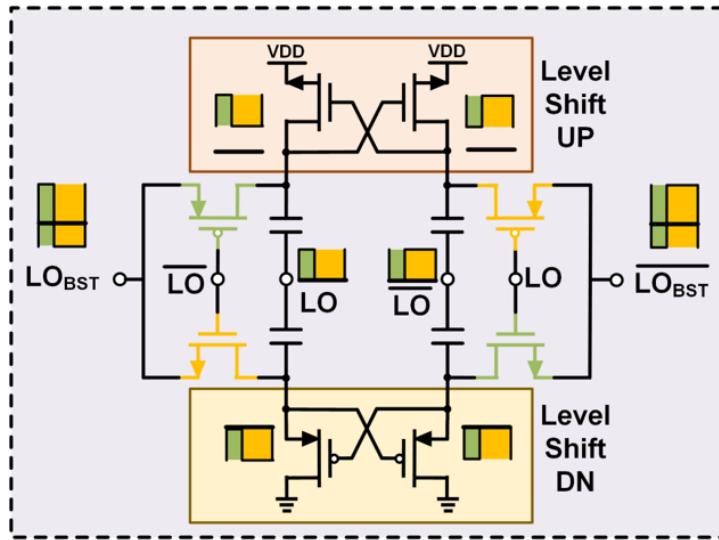
Nakagome Charge-Pump Based Clock Boosting



Switched-capacitor clock boosting technique generated a clock swing of $3 \times VDD$ from a driver supply voltage of VDD .

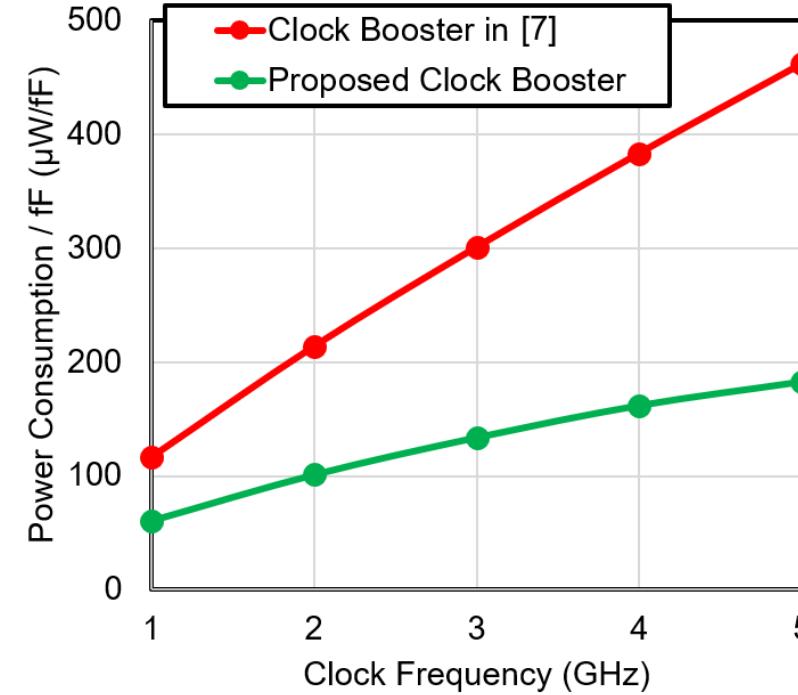
Power-Efficient Clock Boosting Circuit

Proposed Complementary Nakagome Charge-Pump Based Clock Booster



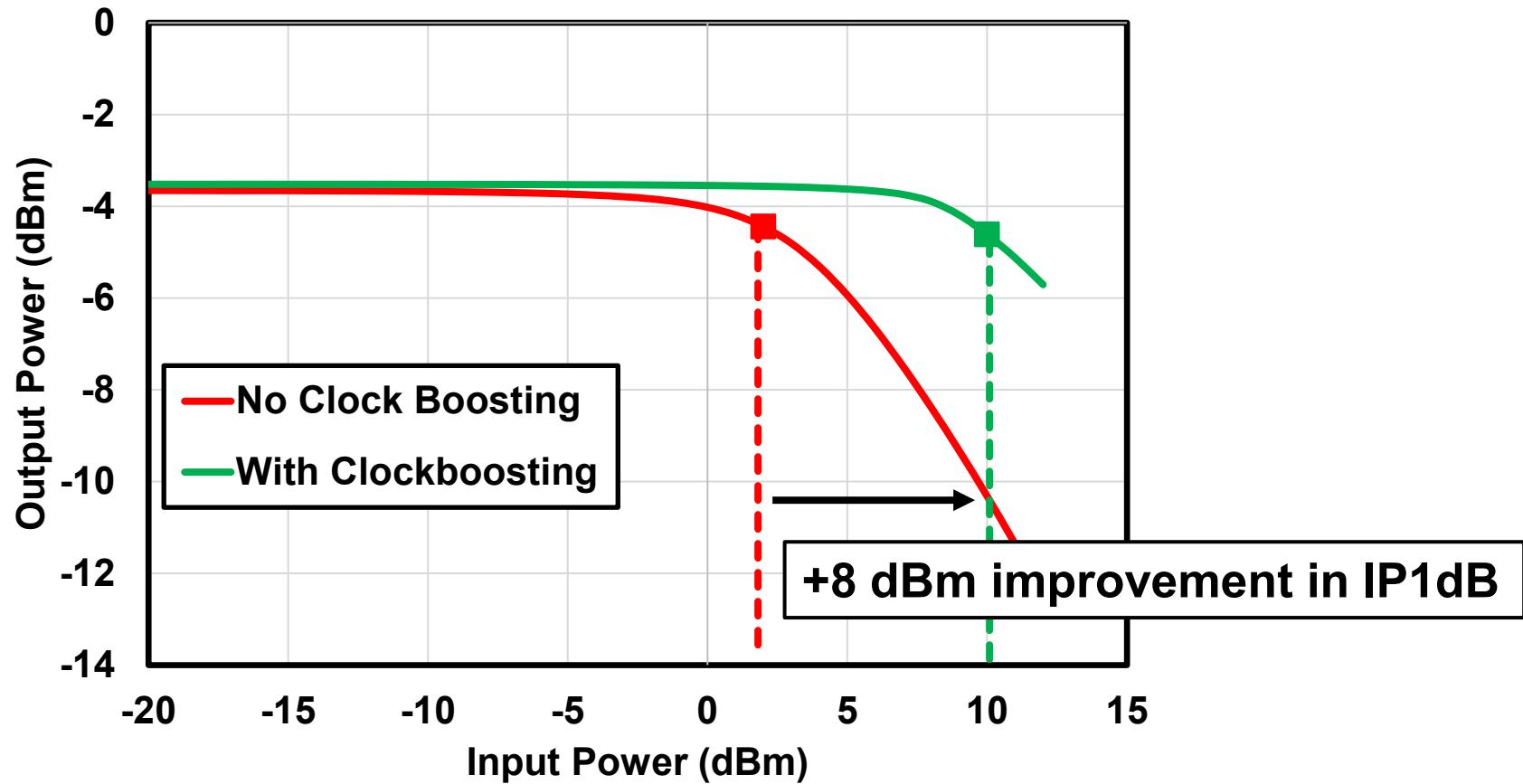
- ✓ High Voltage Swing → High Power handling
- ✓ Low rise time → Low Loss
- ✓ Low power consumption

Comparison of the proposed clock booster vs. clock booster in [7]



Modified schematic of the clock boosting circuit provides 3x voltage swing while resulting in 2x lower DC power than the original circuit proposed in ISSCC 2020

Large Signal Compression of N-path Filters

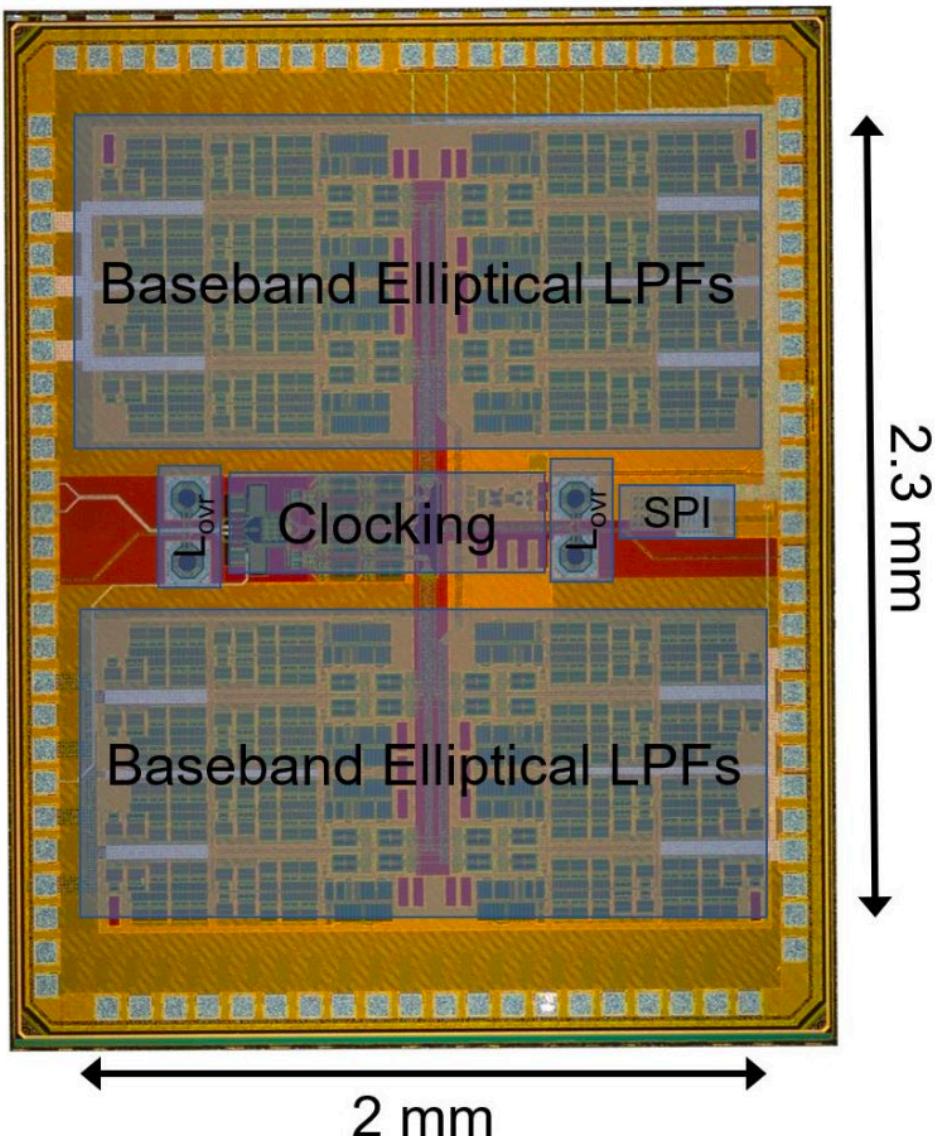


3x clock boosting circuit has increased the power handling of the N-path filter by +8dBm when operating at 6GHz

Outline

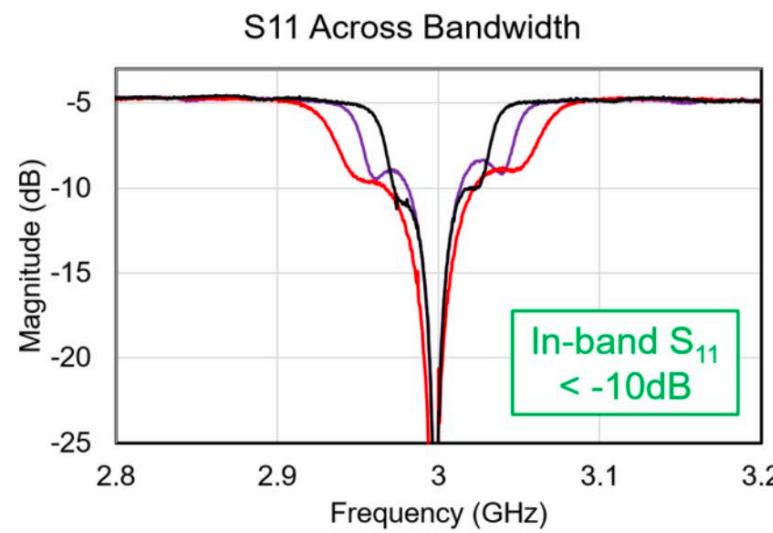
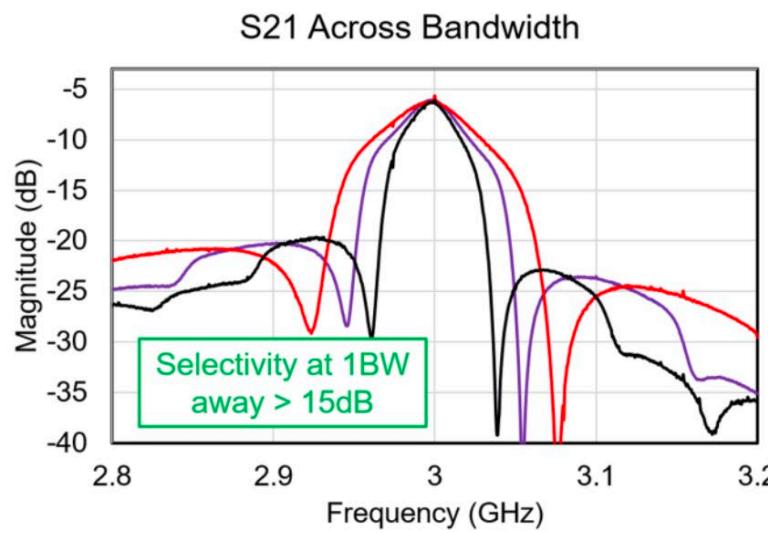
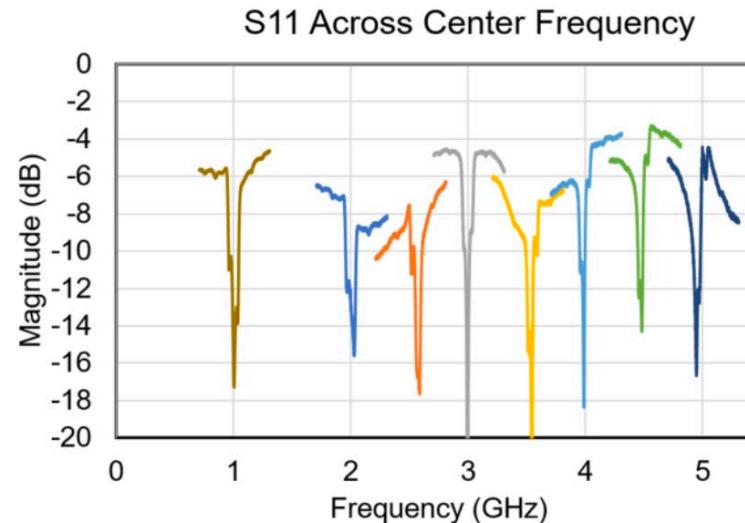
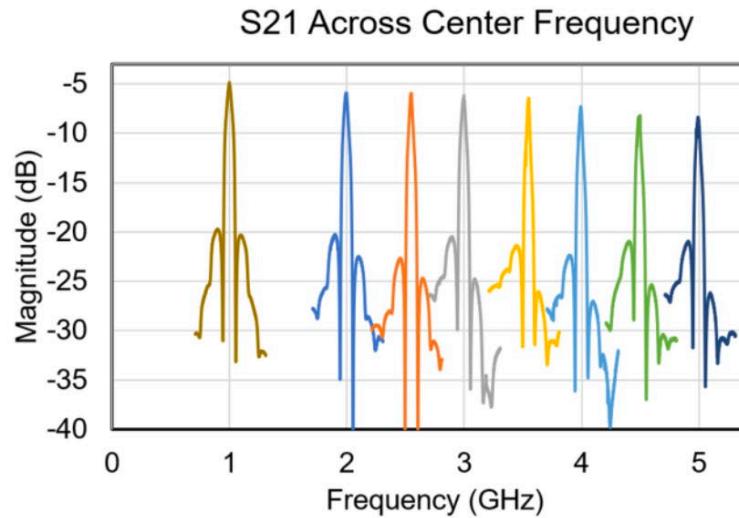
- Introduction
- A 1-5GHz All-Passive Higher-Order N-Path Filter in 65nm CMOS
- Measurement Results
- Conclusion

Chip Micrograph



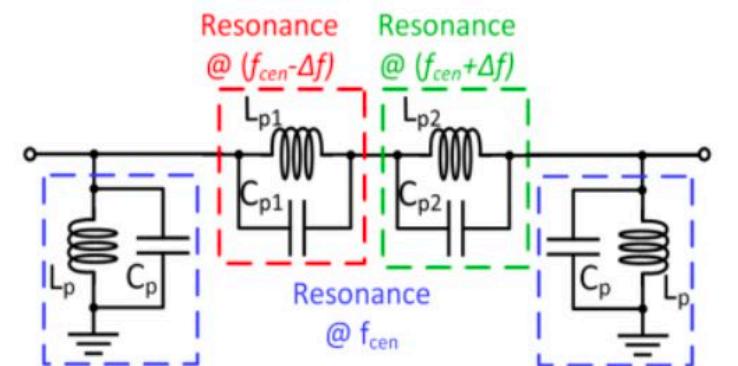
- IC implemented in a 65nm CMOS process and occupying $2\text{mm} \times 2.3\text{mm}$
- Capacitors dictate chip area and support bandwidth range of 5-80MHz

Small Signal Performance



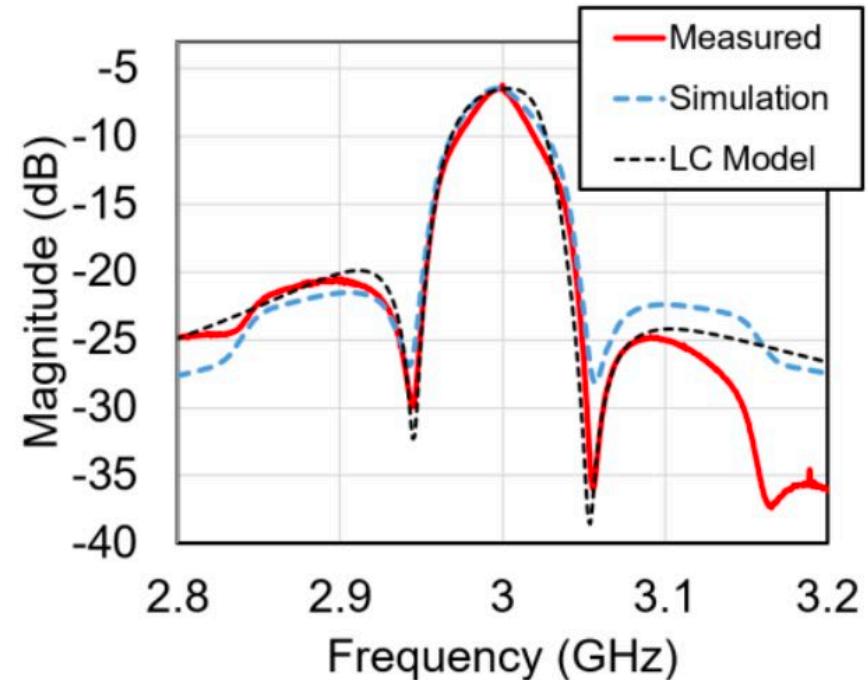
- 5 ~ 8.5 dB insertion loss over 1GHz ~ 5GHz.
- < -10 dB in-band matching.
- Tunable -3 dB bandwidth over entire frequency.

LC-Resonator-Based Filter Comparison



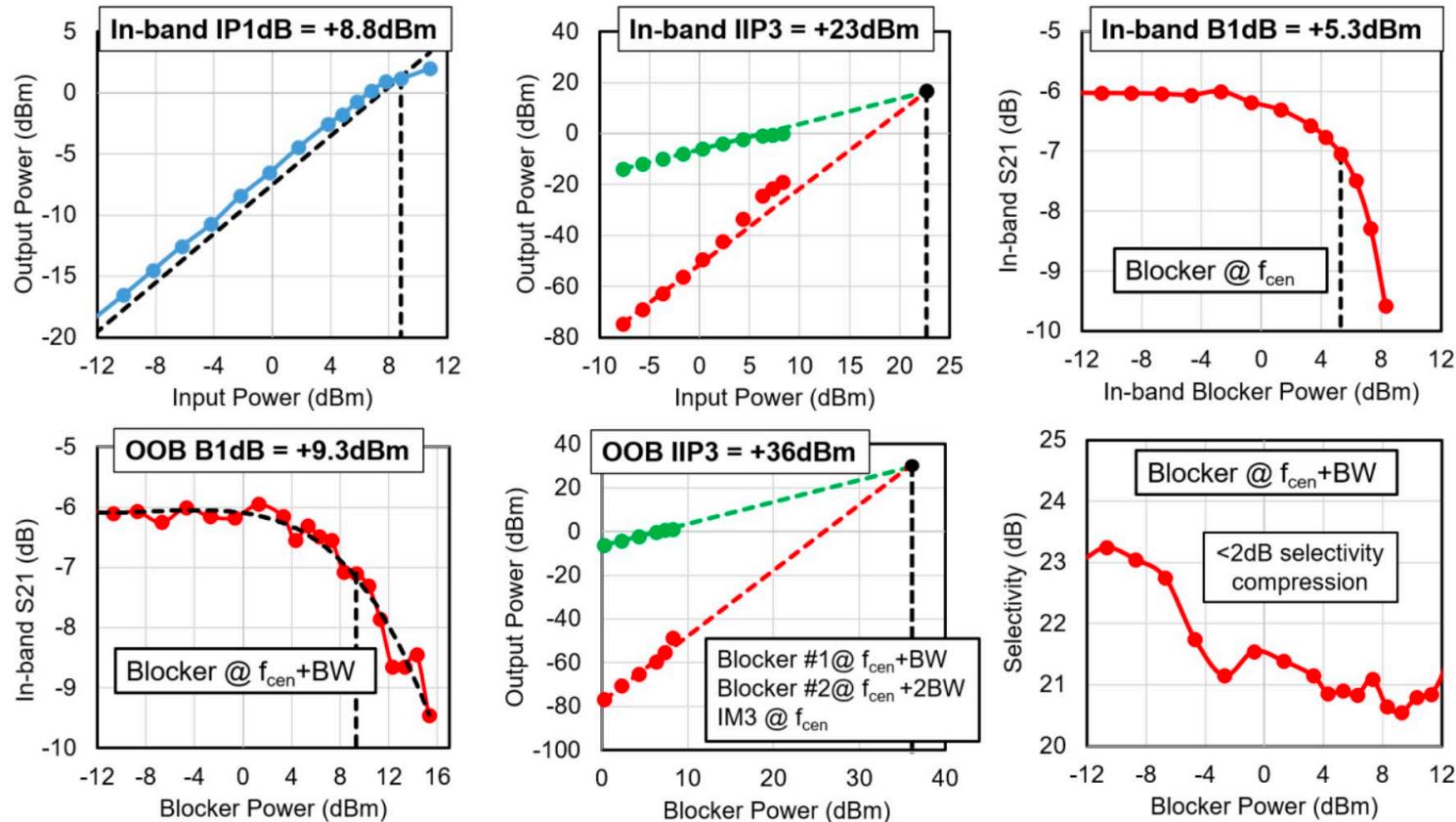
Measured loss is equivalent to an inductor Q of 100-600!

L_p Q@3G	L_{p1} Q@3G	L_{p2} Q@ 3G	C_p	C_{p1}	C_{p2}
60pH Q = 100	160pH Q = 600	80pH Q=600	47pF	18pF	34pF



The N-path based BPF approximates a fourth-order elliptical filter with an inductor quality factor of 100-600 at the center frequency.

Large Signal Performance



- In-band P1dB = +8.8 dBm
- In-band IIP3 = +23 dBm
- In-band B1dB = +5.3 dBm
- OOB Blocker P1dB = +9.3 dBm
- Out-of-band IIP3 = +36dBm
- < 2dB selectivity compression

Performance Comparison With Prior Work

	This Work	RFIC 2015	ISSCC 2018	IMS 2022	ISSCC 2012	ISSCC 2013
Architecture	Frequency-Translational N-Path Filter	Coupled N-path	Coupled N-Path	Rotary Clocking Based Subtraction	Switched gm-C Bandpass Filter	Active N-path BPF
Active/Passive	Passive	Passive	Passive	Passive	Active	Active
Frequency Tuning Range	1GHz – 5GHz	0.6 to 0.85GHz	0.8 to 1.1GHz	0.2 to 0.8GHz	0.4 to 1.2GHz	0.1 to 1.2GHz
BW (@ f_c)	5MHz – 80MHz (@ full RF range)	12MHz\$ (@ 0.75GHz)	40MHz (@875MHz)	40MHz (@ 500MHz)	21MHz (@1GHz)	8MHz (@1GHz)
Gain	-5dB to -8.4dB	-6.4 to -4.7 dB	-4.6 to -3.8dB	+10.2 dB	+3.5dB	+25dB Voltage gain
Selectivity (rejection @ BW away from fc)	>+15dB	+9.6dB\$	+18.2dB\$	+16.3dB	+10.1dB\$	+17dB\$
OOB Rejection	> +24dB	30-50dB	17dB	30-50dB	55dB	59dB
NF	5dB to 8.5dB	8.6dB	5-8.6dB	3.7 to 6.4dB	10dB£	2.6-3.1dB£
IB IP1dB	+8.8 dBm	+5 dBm	+7dBm	-8.2dBm	-4.4dBm	-23dBm
OOB B1dB	+9.3 dBm ($\Delta f/BW = 1$)	N/R	+9dBm ($\Delta f/BW = 1$)	-1dBm ($\Delta f/BW = 2.5$)	N/R	+7dBm ($\Delta f/BW = 6.25$)
IB IIP3	+23dBm	+7dBm	+24dBm	+4.2dBm	+9dBm	-12dBm
OOB IIP3	+36dBm ($\Delta f/BW = 1$)	+17.5dBm ($\Delta f/BW = N/R$)	+24dBm ($\Delta f/BW = 1$)	+12.9dBm ($\Delta f/BW = 2.5$)	+29dBm ($\Delta f/BW = 6.25$)	+26dBm ($\Delta f/BW = 6.25$)
Technology	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS
Power Consumption	40mW – 167mW (1GHz – 5GHz)	75mW	80-97mW	5.5 to 38mW 19mW (@ 0.5GHz)	21.4mW	21-69mW
P_{DC}/f_c @ High Freq	33.5 mW/GHz	88 mW/GHz	88 mW/GHz	38mW/GHz	21.4mW/GHz	57 mW/GHz
Active Area	4.6 mm ²	1.21mm ²	1.9mm ²	0.56mm ²	0.127mm ²	0.27mm ²

 Comparable to prior work
 Better than prior work

- >4x higher frequency of operation
- Superior linearity
- Lower power consumption normalized to frequency of operation
- Similar loss, noise and filtering as prior works.

Outline

- **Introduction**
- **A 1-5GHz All-Passive Higher-Order N-Path Filter in 65nm CMOS**
- **Measurement Results**
- **Conclusion**

Conclusion

- Fabricated and measured an all-passive, higher-order N-path IC in a 65nm CMOS process
 - Achieved $>4\times$ higher frequency of operation, 10-100 \times superior linearity, and lower power consumption normalized to frequency of operation, while exhibiting similar loss, noise and filtering as prior works.
- Evaluated the concept of the baseband elliptical LPF loads in N-path filters to achieve programmability of bandwidth, higher selectivity and OOB rejection.
- Proposed a power-efficient and frequency-scalable clock boosting architecture to generate voltage swing of 2.2~2.8x VDD over DC to 5GHz with small rise time.

Acknowledgements

- This work was supported by DARPA COFFEE and DARPA WARP programs
- Our special thanks to
 - Dr. Benjamin Griffin of DARPA for feedback and comments
 - Keysight Technologies for equipment support
 - Members of the Nagulu's lab and CoSMIC lab for discussion

Thank you for your attention