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Ex1, Ex2: check asq1.c, asq2.s on out

## Exercise 3:

(6):

ALUCAR MemWr MemzoReg ExtOp ALUSTE nPC-sel RegUst RegWr (a) Slt O × → Instruction<31:0> Memory Exercise 4: (m) nPC\_sel Equal <u>MemWr</u>  $\begin{array}{c|cccc}
\underline{\text{RegWr}} & & \text{Rs Rt} \\
\hline
& 5 & 5 & 5 \\
\hline
\end{array}$ Rw Ra Rb busA RegFile imm16\_\_\_\_ imm<sub>16</sub> ExtOp ALUSro

- 1. Before ALU, a MUX is added to determine whether the instruction is "700" or not
- 2. It it is "foo", then update the value on Reg[fre]
- 3. Update the value in memory address Registrd I.
- 4. Increment PC value for next instruction.
- LC) ALVER MemWr MemzoReg ExcOp ALUSre nPC-sel RegDer RegWr 700