L1 is not considered
Locality: temporal vs. spatial
Cache example;
Calculating hits and miss & miss type
AMAT calculation
CND & DNF
MUX & DEMUX
Draw half adder, full adder, and mux
In exam there may be 6 or 8 way mux or adder
Flip-flops
Registers patterns
MIPS Assembly: RTL, datapath, and instructions
Registers in simplified datapath: highlight or modify the datapath; one colored pencil needed
Like highlight (L10; examples;)
You should remember the exact meaning of MIPS instructions and types, and sign.unsign, i and u in addi, addu
FSM one MCQ
Tracing control signals, ie.e, tracing lw in L11
Draw pipelining Stage table
Calculate the performance of single cycle datapath and multi-cycle datapath(pipeline) - it may not be 5 stages only, it could be 4 or 7.
Pipeline hazards, forwarding, causes: what kind of data hazard there is? (check examples in L 13) and how to fix it? (forwarding, stall, or re-arrange codes) ALU-ALU forwarding, MEM-ALU forwarding, know whether it is valid or not.
Loop unrolling (1 question): how to unroll the loop
Superscalar
Renaming 1 example - how to rename registers
Pipelineing vs superscalar vs VLIU
L15 - 1 question about definition comparison, you should give one example to tell difference between multithreading and something (maybe multicore?)

35 total
8 mcq
6-7 written questions