# CS3350B Computer Organization Chapter 1: CPU and Memory Cache Miss Types Explained

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#### Three Types of Cache Misses

#### Cold Miss

□ Caused by the **first** time you try to access a particular memory address (and it is not contained in some other previously accessed cache block).

#### Capacity Miss

- → Occurs when you are working with too much memory at one time.
- → This is caused by *poor temporal locality*.

#### Conflict Miss

- Occurs when two different memory addresses being accessed map to the same set in a cache.
- One expects a cache hit based on the cache's capacity and good temporal locality, but it ends up being a miss.
- → "Conflict misses are misses that would not occur if the cache
  was fully-associative and had LRU replacement." (Jouppi, 1990)
- Just because two addresses map to the same block does not mean it is a conflict miss.

### Differentiating By Example: Cold Miss

Say we have a direct-mapped cache with two one-word lines:

0	
1	

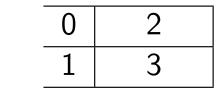
and the sequence of memory accesses:

- These will all be cold misses.
- No capacity misses. These imply poor temporal locality and working with too much data at one time.
- Since no address is accessed twice, it all cold misses.

0	0	0
	1	

1	0	0
_	1	1

0	2
1	1



4	0	4
	1	3

5	0	4
•	1	5

3

#### Differentiating By Example: Cold Miss

Same cache as before. Two lines:

0	
1	

New sequence of memory accesses:

- First few are cold misses, then we get capacity misses.
- We use too much data before accessing 0, 1, 2 again.
- (For this limited cache size) poor temporal locality in 0, 1, 2.

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1, cold

0	0
1	

0	0
1	1

0	2
1	1

0	2
1	3

0	0
1	3

0	2
1	0

### Differentiating By Example: Conflict Miss 1

0, cold

0 0

Same cache as before. Two lines:

0	
1	

16, cold

- 0 16 1
- 0, conflict
- 0 0

New sequence of memory accesses:

16, conflict

0	16	
1		

- Temporal locality is good, and everything fits into the cache's size, but we get many misses.
- 0, conflict

0	0	
1		

Characteristic thrashing.

16, conflict

0	16	
1		

0, conflict

0	0
1	

### Differentiating By Example: Conflict Miss 2

0, cold

Now a direct-mapped cache with two two-word lines:

16, cold

17, hit

New sequence of memory accesses:

1, conflict

0, 16, 17, 1, 18, 2, 18, ...

18, cold

 0
 0
 1

 1
 18
 19

Would increasing associativity fix the miss?

2, cold

 0
 0
 1

 1
 2
 3

18, conflict

0	0	1
1	18	19

## Differentiating By Example: Conflict Miss 3

0, cold

0 0 1

Now a cache with two two-word lines but 2-way associativity:

16, cold

17, hit

1, hit

0, 16, 17, 1, 18, 2, 18, ...

18, cold

Increasing associativity made previous conflict misses hits!

Same sequence of memory accesses:

0

2, cold

0 2 3 19

18, hit

Λ	2	3
U	18	19

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