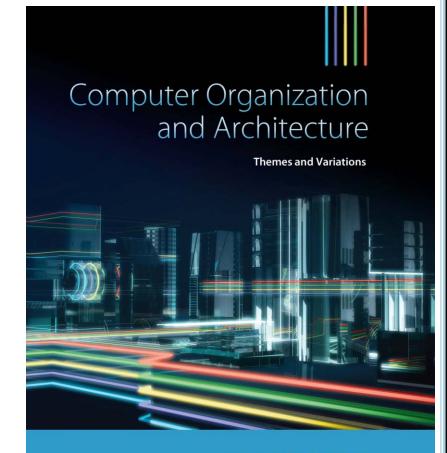
# Part 0xC

# CHAPTER 3

Architecture and Organization



Alan Clements

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☐ The following conventional ARM code demonstrates how to load four registers from *consecutive* memory-locations. ADR **r0**, DataToGo ; load r0 with the address of the data area 3rd LDR **r1**,[r0] ;load r1 with the word pointed at by r0 ADD **r0**, #4 ;update the pointer LDR **r2**,[r0] ;load r2 with the word pointed at by r0 ADD **r0**, #4 ; update the pointer 7th LDR **r3**,[r0] ; load r3 with the word pointed at by r0 ADD **r0**, #4 ; update the pointer 9th LDR **r5**,[r0] ; load r5 with the word pointed at by r0 ADD **r0**, #4 ; update the pointer Memory Memory After 3rd After 7th After 1st After 5th After 9th instruction instruction instruction instruction instruction addressesDataToGo + 4 rO DataToGo + 12 DataToGo DataToGo + 8 rO DataToGo + 16 DataToGo 0xAAAAAAAA 0xAAAAAAAA 0x00000000 **OXAAAAAAA** 0xAAAAAAAA r1 0xAAAAAAAA DataToGo + 4 0xBBBBBBBB DataToGo + 8 0xCCCCCCC 0x00000000 0x00000000 0xBBBBBBBB 0xBBBBBBBB r2 0xBBBBBBBB DataToGo + 12 0xDDDDDDDD **r**3 **r**3 0x00000000 0x00000000 r3 0x00000000 0xCCCCCCCC r3 oxccccccc DataToGo + 16 168 r4 r4 0x00000000 r4 0x00000000 0x0000000 r4 r4 0x00000000 0x00000000 r5 r5 0x00000000 0x00000000 0x0000000 r5 <sub>0xDDDDDDDD</sub> 0x0000000

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□ *A more efficient way* to load four registers from <u>consecutive</u> memory-locations.

```
ADR r0,DataToGo ;load r0 with the address of the data area

LDR r1,[r0],#4 ;load r1 with the word pointed at by r0

;and post-update the pointer

;load r2 with the word pointed at by r0

;and post-update the pointer

;load r3 with the word pointed at by r0

;and post-update the pointer

LDR r5,[r0],#4 ;load r5 with the word pointed at by r0

;and post-update the pointer

;and post-update the pointer
```

- ☐ ARM has
  - o a block move from memory to registers instruction, LDM, and
  - o a block move from registers to memory instruction, STM

that can copy *group of registers* from and to memory.

This is even more efficient than the above solution.

□ Both block move instructions take a **suffix** to describe *how* the data is accessed.

- ☐ Think of block move instructions as if they are stack operations
  - o STM: to push a group of registers' content to memory
  - o **LDM:** to **pop** values from memory and load them to a group of registers
- □ Let's start by copying the contents of registers r1, r2, r3, and r5, into *sequential* memory-locations with

ADR **r0**, DataToGo • •

This is a different example. It is an **STM** and the example in the previous two slides was **LDM**.

STMIA **r0!**, {r1-r3,r5}

inote the syntax of this instruction

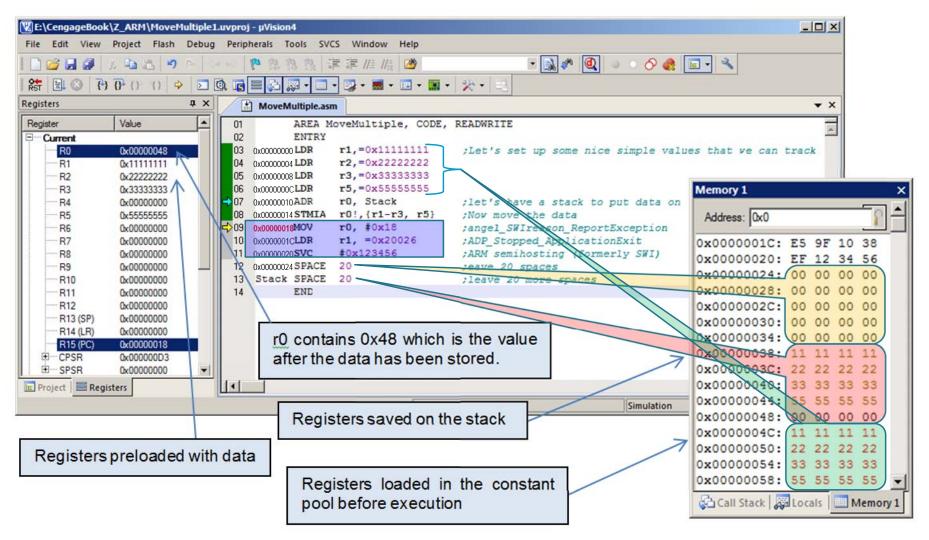
;the register list is put between

curly braces and it can have a range

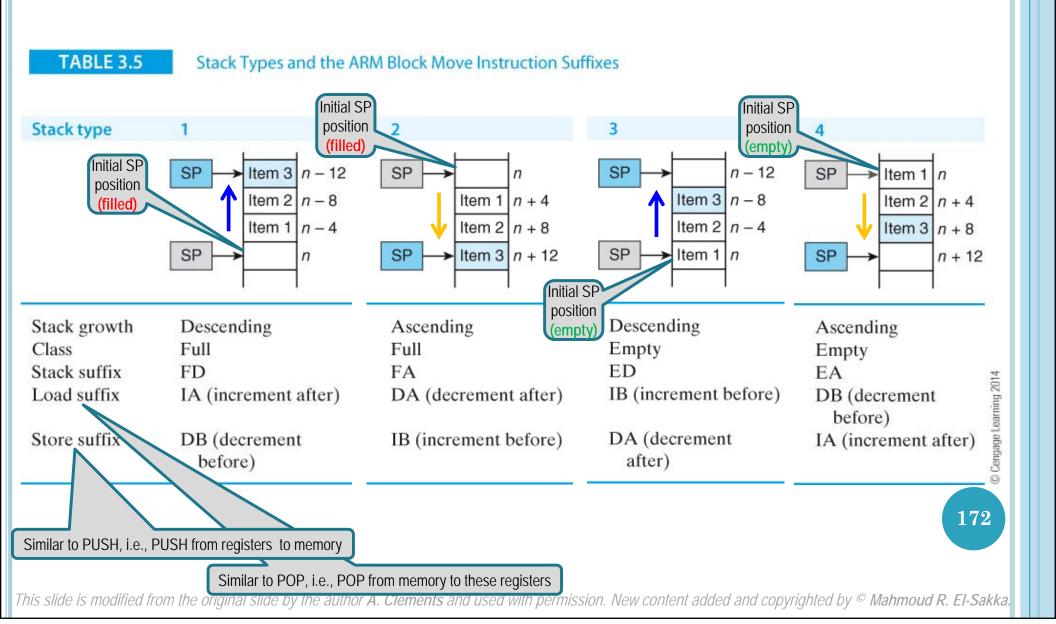
- ☐ This instruction copies registers r1 to r3, and r5, into sequential memory-locations, using r0 as a pointer with *auto-indexing* (indicated by the ! suffix).
- ☐ The suffix IA indicates that index register r0 is *incremented after* the transfer, with data transfer in the order of increasing addresses.
- Although ARM's block move instructions have several variations, *ARM always stores the lowest numbered register first at the lowest memory address*, followed by the next lowest numbered register, and so on, regardless of the order in the instruction.

  For example, "STMIA **r0!**, {r5, r1-r3}" and "STMIA **r0!**, {r2, r3, r5, r1}"

have the same effect as "STMIA ro!, {r1-r3,r5}"

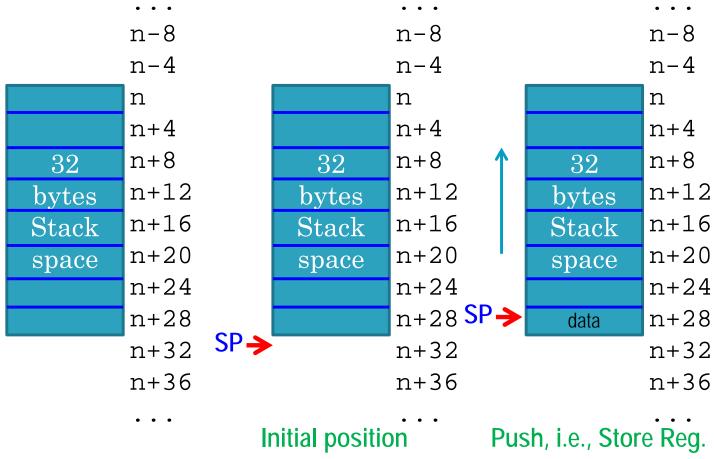


- ☐ In LDM/STM, the access happens in the order of increasing register numbers,
  - ☐ the lowest numbered register occupies the lowest memory address and
  - □ the highest numbered register occupies the highest memory address



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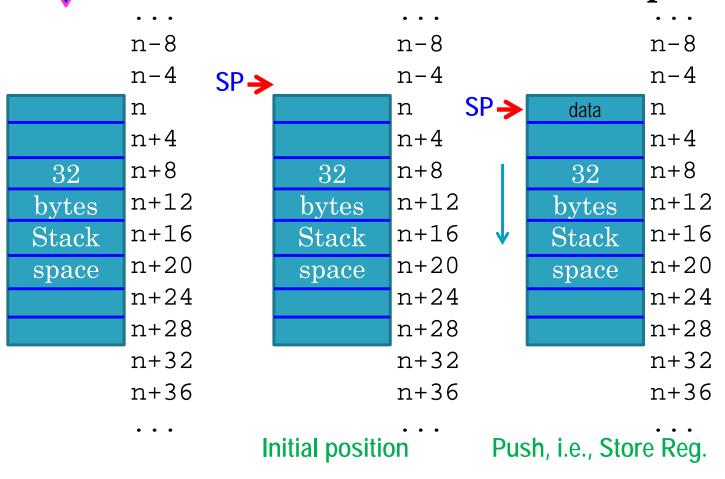
# **Block Moves and Stack Operations**



Occupied \

memory

- □ Stack type: FD (i.e., Class=Full and Stack growth=Descending)
  (STMFD and LDMFD)
  - o Empty stack → SP points to just after the stack space
  - o Pushing on the stack → SP to be Decremented Before (STMDB)
  - o Popping off the stack → SP to be Incremented After (LDMIA)



Grows down Organ

memory

- ☐ Stack type: FA (i.e., Class=Full and Stack growth=Ascending)
  (STMFA and LDMFA)
  - o Empty stack → SP points to just before the stack space
  - o Pushing on the stack → SP to be Incremented Before (STMIB)
  - o Popping off the stack → SP to be Decremented After (LDMDA)

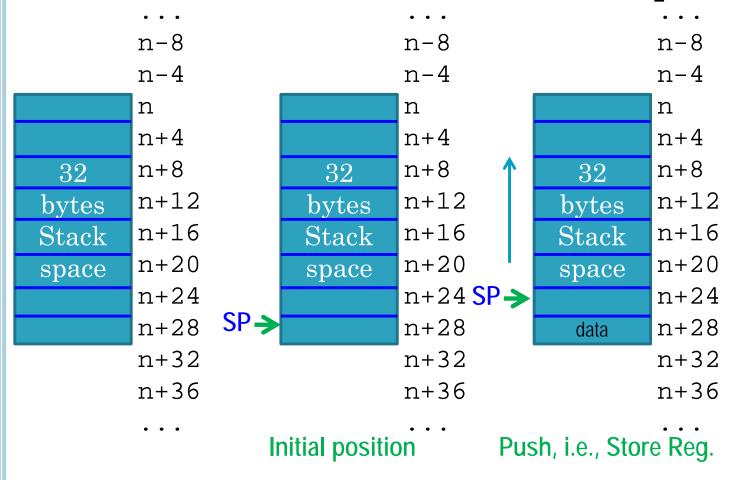
Grows up

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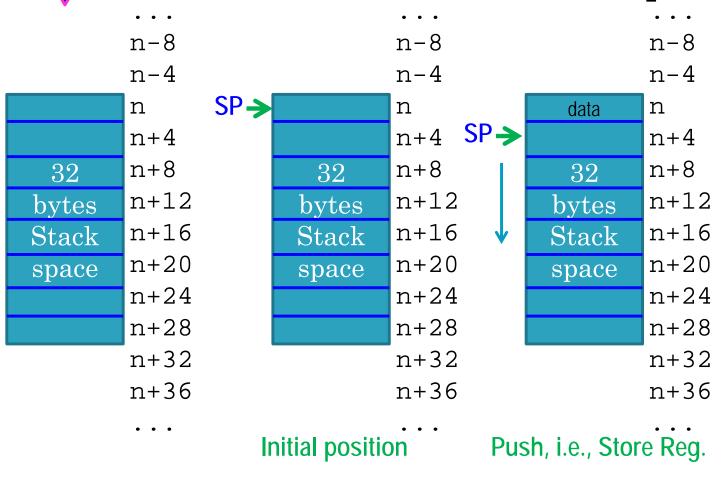
**Empty** 

memory

#### **Block Moves and Stack Operations**



- ☐ Stack type: ED (i.e., Class=Empty and Stack growth=Descending)
  (STMED and LDMED)
  - o Empty stack → SP points to the last memory word in the stack
  - o Pushing on the stack → SP to be Decremented After (STMDA)
  - o Popping off the stack → SP to be Incremented Before (LDMIB)



Grows down Organ

**Empty** 

memory

- ☐ Stack type: EA (i.e., Class=Empty and Stack growth=Ascending)
  (STMEA and LDMEA)
  - o Empty stack → SP points to the first memory word in the stack
  - o Pushing on the stack → SP to be Incremented After (STMIA)
  - o Popping off the stack → SP to be Decremented Before (LDMDB)

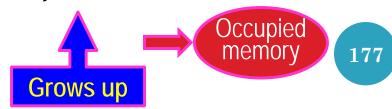
- ☐ A stack operation can be described either by
  - what it does
    - o FD Full Descending
    - o FA Full Ascending
    - o ED Empty Descending
    - o EA Empty Ascending
  - **how** it does
    - o **DB** Decremented Before
    - o **DA D**ecremented **A**fter
    - o IB Incremented Before
    - o IA Incremented After

**FD, FA, ED,** and **EA** are *pseudo* notation.

Thea assembler will translate these *pseudo* notation to the IA, DB, DA, and IB notation.

For example,

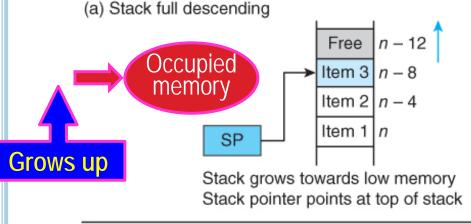
- □ We can write STMFD sp!, {r0,r1} when pushing r0 and r1 onto the stack,
  - Also can be written as STMDB sp!, {r0,r1}
- $\square$  We can write LDMFD sp!,  $\{r0,r1\}$  when popping r0 and r1 off the stack.
  - Also can be written as LDMIA sp!, {r0,r1}

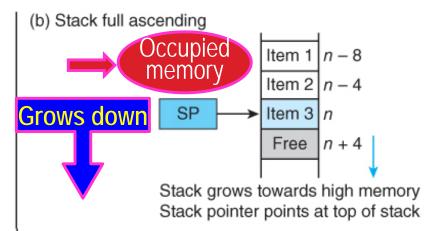


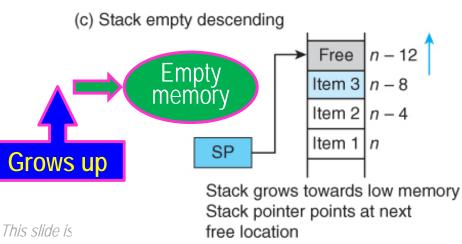
- ☐ The ARM's literature uses four terms to describe stacks:
  - a) FD full descending Figure 3.52a
  - b) FA full ascending Figure 3.52b
  - c) ED empty descending Figure 3.52c
  - d) EA empty ascending Figure 3.52d

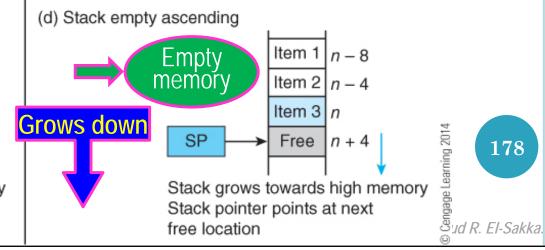
**FIGURE 3.59** 

ARM's four stack modes

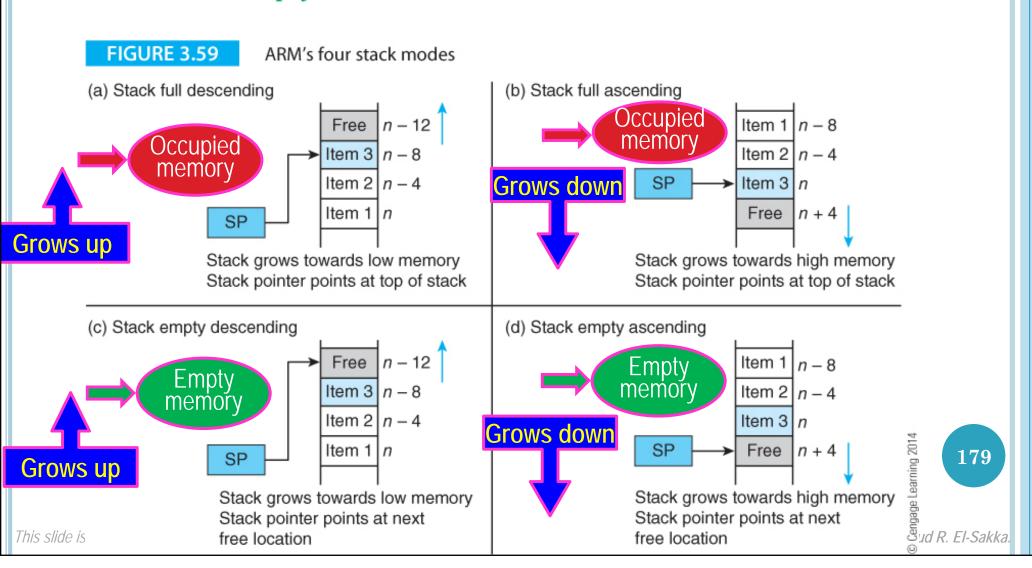








- ☐ A stack is described as *full* if the stack pointer *points to the top element* of the stack.
- ☐ If the stack pointer *points to the next free* element in the stack, then the stack is called *empty*.



Bit#23 (Up/down)

# **Block Moves and Stack Operations**

- □ ARM's block move instruction is useful because it supports *four* possible
  - stack types.
- ☐ The differences among these four types are
  - o the *direction* in which the stack grows
    - up (i.e., descending toward lower addresses), or
    - down (i.e., ascending toward higher addresses)

ARM uses the terms *ascending* and *descending* to describe the growth of the stack toward *higher* or *lower* addresses, respectively.

- o whether the stack pointer points at
  - the item currently at the top of the stack or
  - the *next free item* on the stack.

Bit#24 (Pre-post)

# **Block Move Example**

- ☐ The block move provides a convenient means of copying data between memory regions. *This is NOT a stack application*.
- $\square$  In the next example we copy 256 words (1024 bytes) from Table 1 to Table 2.

```
ADR
            r0,Table1
                          ;r0 points to source
                           ; (note pseudo-op ADR)
            r1,Table2
                           ;rl points to the destination
    ADR
    VOM
         r2, #32
                           ;32 \text{ blocks of } 8 = 256 \text{ words to move}
Loop LDMFD r0!, {r3-r10} ; REPEAT Load 8 registers (r3 to r10)
    STMFD r1!, {r3-r10} ; store the registers at
                           ;their destination
     SUBS
            r2, r2, #1
                           ;decrement loop counter
                           ;UNTIL all 32 blocks of
    BNE
            Loop
                           ;8 registers moved
       Is it right to
   use LDMFD and STMFD?
```

☐ The two block move instructions above allow us to move eight registers (i.e., 32 bytes) at once.

# **Block Move Example**

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                         ;their destination
    SUBS
            r2, r2, #1
                         ;decrement loop counter
                          ;UNTIL all 32 blocks of
    BNE
            Loop
                         ;8 registers moved
    not LDRFD and STRFD
```

☐ The two block move instructions above allow us to move eight registers (i.e., 32 bytes) at once.

Not correct in the book page 220