Tutorial 09: ARM Pseudo Instructions

Computer Science Department
CS2208: Introduction to Computer Organization and Architecture
Fall 2022-2023
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ARM pseudo-instructions

- The ARM assembler supports several *pseudo instructions* that are translated into the appropriate combination of ARM words at assembly time.
- Consider the following assembly program:

```
      AREA prog1, code, READONLY
      ENTRY
      LDR r0,[r1]        copy 4 bytes in address pointed by r1
      LDR r0, =0xFF     ; pseudo-instruction
      LDR r0, =0xFFF    ; pseudo-instruction => literal pool
      LDR r0, X         ; pseudo-instruction } Add/Sub
      LDR r0, =X        ; pseudo-instruction } literal pool.
      ADR r0, X         ; pseudo-instruction
loop  B loop
X     DCD 0xAAAAAAAA
      END
```

ARM pseudo-instructions

C:\Users\elsakka2\Desktop\ARM\ex1.uvproj - µVision4

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Target 1

Project

Target 1

Project | Books | Funct... | Temp...

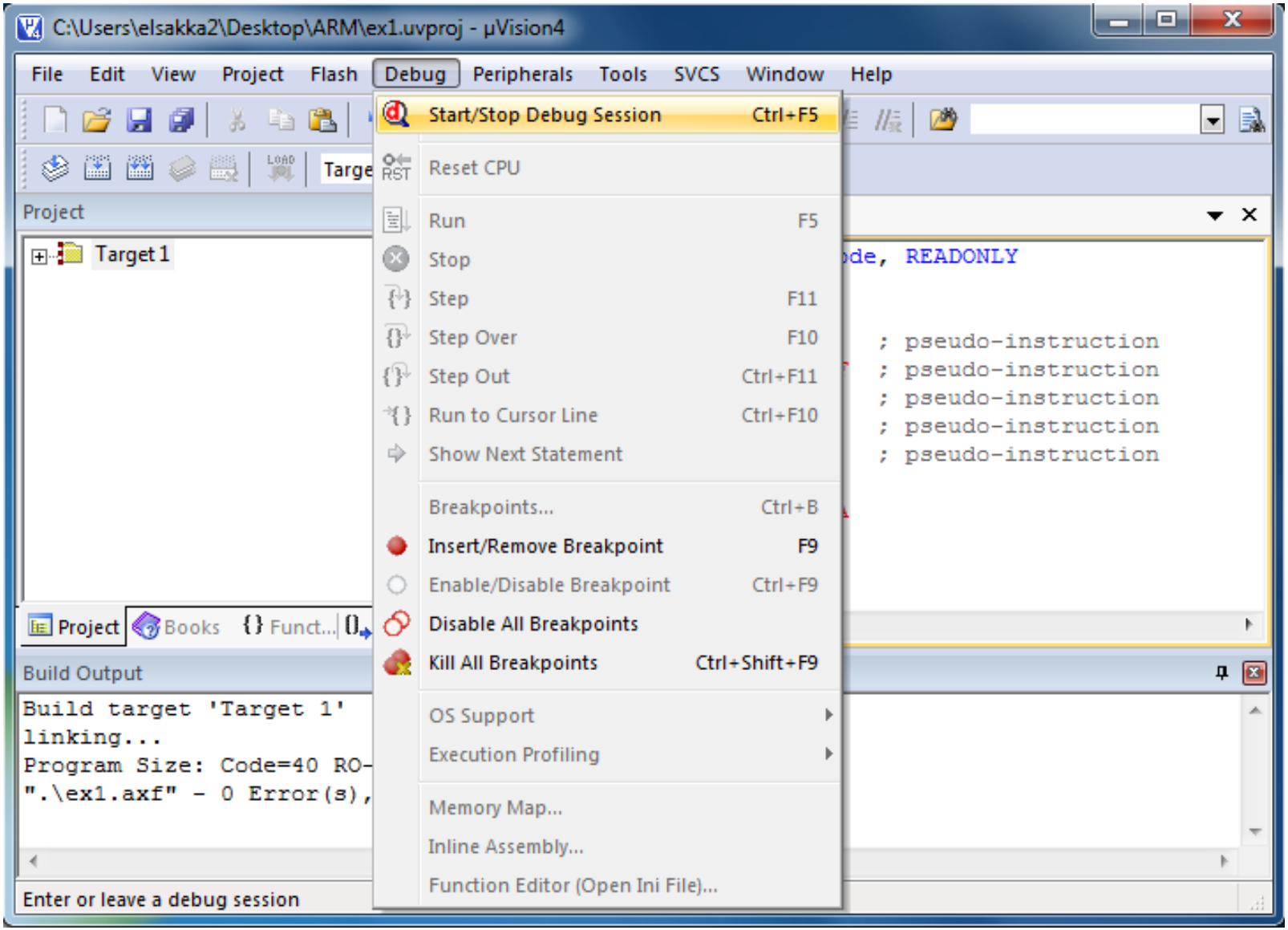
ex1.asm

```
      AREA prog1, code, READONLY
      ENTRY
      LDR r0,[r1]
      LDR r0, =0xFF    ; pseudo-instruction
      LDR r0, =0xFFF   ; pseudo-instruction
      LDR r0, X        ; pseudo-instruction
      LDR r0, =X       ; pseudo-instruction
      ADR r0, X        ; pseudo-instruction
loop  B loop
X     DCD 0xAAAAAAAA
      END
```

Build Output

```
Build target 'Target 1'
linking...
Program Size: Code=40 RO-data=0 RW-data=0 ZI-data=0
".\ex1.axf" - 0 Error(s), 0 Warning(s).
```

ARM pseudo-instructions



ARM pseudo-instructions

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Target 1

Project

Target 1

ex1.asm

```
1      AREA prog1, code, READONLY
2      ENTRY
3      LDR r0, [r1]
4      LDR r2, [r3]
5      LDR r4, [r5]
6      LDR r6, [r7]
7      LDR r8, [r9]
```

µVision

EVALUATION MODE
Running with Code Size Limit: 32K

OK

Project Books {} Funct... {} Temp...

Build Output

```
Build target 'Target 1'
linking...
Program Size: Code=40 RO-data=0 RW-data=0 ZI-data=0
".\ex1.axf" - 0 Error(s), 0 Warning(s).
```

ARM pseudo-instructions

C:\Users\elsakka2\Desktop\ARM\ex1.uvproj - µVision4

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Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000000
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC $	0x00000000
Mode	Supervisor
States	0
Sec	0.00000000

Project | Registers

Disassembly

```
     3:        LDR r0,[r1]
0x00000000  E5910000  LDR       R0,[R1]
     4:        LDR r0, =0xFF    ; pseudo-instruction
0x00000004  E3A000FF  MOV       R0,#0x000000FF
     5:        LDR r0, =0xFFF   ; pseudo-instruction
0x00000008  E59F0010  LDR       R0,[PC,#0x0010]
     6:        LDR r0, X        ; pseudo-instruction
0x0000000C  E59F0008  LDR       R0,[PC,#0x0008]
     7:        LDR r0, =X       ; pseudo-instruction
0x00000010  E59F000C  LDR       R0,[PC,#0x000C]
     8:        ADR r0, X        ; pseudo-instruction
0x00000014  E28F0000  ADD       R0,PC,#0x00000000
     9: loop B loop
0x00000018  EAFFFFFE  B         0x00000018
0x0000001C  AAAAAAAA  BGE       0xFEAAAACC
0x00000020  00000FFF  ???EQ
0x00000024  0000001C  ANDEQ     R0,R0,R12,LSL R0
0x00000028  00000000  ANDEQ     R0,R0,R0
```

ex1.asm

```
1        AREA prog1, code, READONLY
2        ENTRY
3        LDR r0,[r1]
4        LDR r0, =0xFF    ; pseudo-instruction
5        LDR r0, =0xFFF   ; pseudo-instruction
6        LDR r0, X        ; pseudo-instruction
7        LDR r0, =X       ; pseudo-instruction
8        ADR r0, X        ; pseudo-instruction
9 loop   B loop
10 X     DCD 0xAAAAAAAA
11       END
12
```

Press Step, or F11

ARM pseudo-instructions

C:\Users\elsakka2\Desktop\ARM\ex1.uvproj - µVision4

File Edit View Project Flash Debug Peripherals Tools SVCS Window Help

Registers

Register	Value
Current	
R0	0xE5910000
R1	0x00000000
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000004
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC $	0x00000004
Mode	Supervisor
States	3
Sec	0.00000000

Project | Registers

Disassembly

```
     3:        LDR r0,[r1]
0x00000000  E5910000  LDR       R0,[R1]
     4:        LDR r0, =0xFF    ; pseudo-instruction
0x00000004  E3A000FF  MOV       R0,#0x000000FF
     5:        LDR r0, =0xFFF   ; pseudo-instruction
0x00000008  E59F0010  LDR       R0,[PC,#0x0010]
     6:        LDR r0, X        ; pseudo-instruction
0x0000000C  E59F0008  LDR       R0,[PC,#0x0008]
     7:        LDR r0, =X       ; pseudo-instruction
0x00000010  E59F000C  LDR       R0,[PC,#0x000C]
     8:        ADR r0, X        ; pseudo-instruction
0x00000014  E28F0000  ADD       R0,PC,#0x00000000
     9: loop B loop
0x00000018  EAFFFFFE  B         0x00000018
0x0000001C  AAAAAAAA  BGE       0xFEAAAACC
0x00000020  00000FFF  ???EQ
0x00000024  0000001C  ANDEQ     R0,R0,R12,LSL R0
0x00000028  00000000  ANDEQ     R0,R0,R0
```

ex1.asm

```
1        AREA prog1, code, READONLY
2        ENTRY
3        LDR r0,[r1]
4        LDR r0, =0xFF    ; pseudo-instruction
5        LDR r0, =0xFFF   ; pseudo-instruction
6        LDR r0, X        ; pseudo-instruction
7        LDR r0, =X       ; pseudo-instruction
8        ADR r0, X        ; pseudo-instruction
9 loop   B loop
10 X     DCD 0xAAAAAAAA
11       END
12
```

Press Step, or F11

ARM pseudo-instructions

When executing the instruction at location 0x00000008, the PC value will be 0x00000010

How is this offset calculated?

Press Step, or F11

C:\Users\elsakka2\Desktop\ARM\ex1.uvproj - µVision4

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Registers

Register	Value
Current	
R0	0x000000FF
R1	0x00000000
R2	0x00000000
	0x00000000
R4	0x00000000
R5	
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000008
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC $	0x00000008
Mode	Supervisor
States	4
Sec	0.00000000

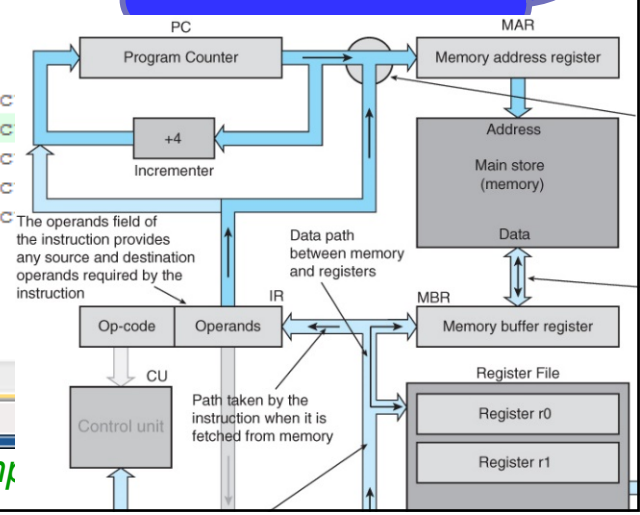
Project | Registers

Disassembly

```
     3:        LDR r0,[r1]
0x00000000  E5910000  LDR       R0,[R1]
     4:        LDR r0, =0xFF    ; pseudo-instruction
0x00000004  E3A000FF  MOV       R0,#0x000000FF
     5:        LDR r0, =0xFFF   ; pseudo-instruction
0x00000008  E59F0010  LDR       R0,[PC,#0x0010]
     6:        LDR r0, X        ; pseudo-instruction
0x0000000C  E59F0008  LDR       R0,[PC,#0x0008]
     7:        LDR r0, =X       ; pseudo-instruction
0x00000010  E59F000C  LDR       R0,[PC,#0x000C]
     8:        ADR r0, X        ; pseudo-instruction
0x00000014  E28F0000  ADD       R0,PC,#0x00000000
     9: loop B loop
0x00000018  EAFFFFFE  B         0x00000018
0x0000001C  AAAAAAAA  BGE       0xFEAAAACC
0x00000020  00000FFF  ???EQ
0x00000024  0000001C  ANDEQ     R0,R0,R12,LSL R0
0x00000028  00000000  ANDEQ     R0,R0,R0
```

ex1.asm

```
1        AREA prog1, code, READONLY
2        ENTRY
3        LDR r0,[r1]
4        LDR r0, =0xFF    ; pseudo-instruc
5        LDR r0, =0xFFF   ; pseudo-instruc
6        LDR r0, X        ; pseudo-instruc
7        LDR r0, =X       ; pseudo-instruc
8        ADR r0, X        ; pseudo-instruc
9 loop   B loop
10 X     DCD 0xAAAAAAAA
11       END
12
```



ARM pseudo-instructions

When executing the instruction at location 0x0000000C, the PC value will be 0x00000014

How is this offset calculated?

IL-C-8

Press Step, or F11

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Registers

Register	Value
Current	
R0	0x00000FFF
R1	0x00000000
R2	0x00000000
R3	0x00000000
R4	0x00000000
	0x00000000
R6	0x00000000
R7	
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x0000000C
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC $	0x0000000C
Mode	Supervisor
States	7
Sec	0.00000000

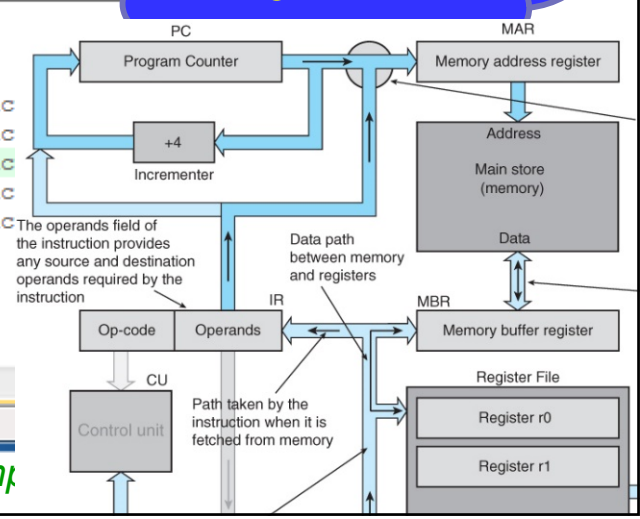
Project | Registers

Disassembly

```
     3:        LDR r0,[r1]
0x00000000  E5910000  LDR       R0,[R1]
     4:        LDR r0, =0xFF    ; pseudo-instruction
0x00000004  E3A000FF  MOV       R0,#0x000000FF
     5:        LDR r0, =0xFFF   ; pseudo-instruction
0x00000008  E59F0010  LDR       R0,[PC,#0x0010]
     6:        LDR r0, X        ; pseudo-instruction
0x0000000C  E59F0008  LDR       R0,[PC,#0x0008]
     7:        LDR r0, =X       ; pseudo-instruction
0x00000010  E59F000C  LDR       R0,[PC,#0x000C]
     8:        ADR r0, X        ; pseudo-instruction
0x00000014  E28F0000  ADD       R0,PC,#0x00000000
     9: loop B loop
0x00000018  EAFFFFFE  B         0x00000018
0x0000001C  AAAAAAAA  BGE       0xFEAAAACC
0x00000020  00000FFF  ???EQ
0x00000024  0000001C  ANDEQ     R0,R0,R12,LSL R0
0x00000028  00000000  ANDEQ     R0,R0,R0
```

ex1.asm

```
1        AREA prog1, code, READONLY
2        ENTRY
3        LDR r0,[r1]
4        LDR r0, =0xFF    ; pseudo-instruc
5        LDR r0, =0xFFF   ; pseudo-instruc
6        LDR r0, X        ; pseudo-instruc
7        LDR r0, =X       ; pseudo-instruc
8        ADR r0, X        ; pseudo-instruc
9 loop   B loop
10 X     DCD 0xAAAAAAAA
11       END
12
```



ARM pseudo-instructions

When executing the instruction at location 0x00000010, the PC value will be 0x00000018

How is this offset calculated?

Press Step, or F11

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Disassembly

```
     3:        LDR r0,[r1]
0x00000000  E5910000  LDR       R0,[R1]
     4:        LDR r0, =0xFF    ; pseudo-instruction
0x00000004  E3A000FF  MOV       R0,#0x000000FF
     5:        LDR r0, =0xFFF   ; pseudo-instruction
0x00000008  E59F0010  LDR       R0,[PC,#0x0010]
     6:        LDR r0, X        ; pseudo-instruction
0x0000000C  E59F0008  LDR       R0,[PC,#0x0008]
     7:        LDR r0, =X       ; pseudo-instruction
0x00000010  E59F000C  LDR       R0,[PC,#0x000C]
     8:        ADR r0, X        ; pseudo-instruction
0x00000014  E28F0000  ADD       R0,PC,#0x00000000
     9: loop B loop
0x00000018  EAFFFFFE  B         0x00000018
0x0000001C  AAAAAAAA  BGE       0xFEAAAACC
0x00000020  00000FFF  ???EQ
0x00000024  0000001C  ANDEQ     R0,R0,R12,LSL R0
0x00000028  00000000  ANDEQ     R0,R0,R0
```

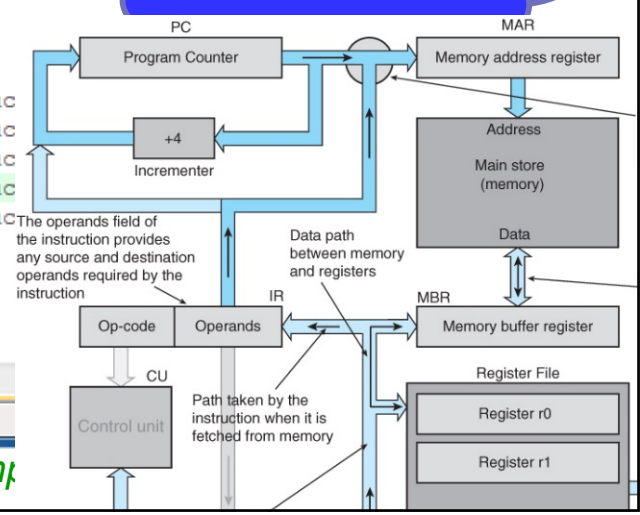
Registers

Register	Value
Current	
R0	0xAAAAAAAA
R1	0x00000000
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000010
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC $	0x00000010
Mode	Supervisor
States	10
Sec	0.00000000

Project | Registers

ex1.asm

```
1        AREA prog1, code, READONLY
2        ENTRY
3        LDR r0,[r1]
4        LDR r0, =0xFF    ; pseudo-instruc
5        LDR r0, =0xFFF   ; pseudo-instruc
6        LDR r0, X        ; pseudo-instruc
7        LDR r0, =X       ; pseudo-instruc
8        ADR r0, X        ; pseudo-instruc
9 loop   B loop
10 X     DCD 0xAAAAAAAA
11       END
12
```



ARM pseudo-instructions

Compare the translations of
`LDR r0, =X`
and
`ADR r0, X`

When executing the instruction at location 0x00000014, the PC value will be 0x0000001C

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Registers

Register	Value
Current	
R0	0x0000001C
R1	0x00000000
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
	0x00000000
R9	0x00000000
R10	
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000014
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC $	0x00000014
Mode	Supervisor
States	13
Sec	0.00000000

Project | Registers

Disassembly

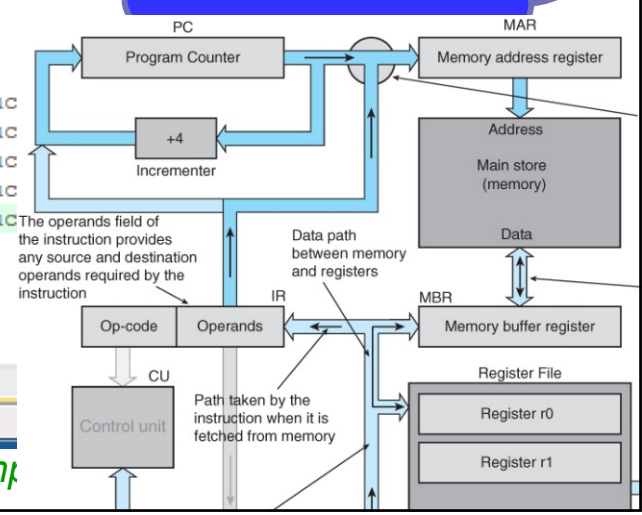
```
     3:        LDR r0,[r1]
0x00000000  E5910000  LDR       R0,[R1]
     4:        LDR r0, =0xFF    ; pseudo-instruction
0x00000004  E3A000FF  MOV       R0,#0x000000FF
     5:        LDR r0, =0xFFF   ; pseudo-instruction
0x00000008  E59F0010  LDR       R0,[PC,#0x0010]
     6:        LDR r0, X        ; pseudo-instruction
0x0000000C  E59F0008  LDR       R0,[PC,#0x0008]
     7:        LDR r0, =X       ; pseudo-instruction
0x00000010  E59F000C  LDR       R0,[PC,#0x000C]
     8:        ADR r0, X        ; pseudo-instruction
0x00000014  E28F0000  ADD       R0,PC,#0x00000000
     9: loop B loop
0x00000018  EAFFFFFE  B         0x00000018
0x0000001C  AAAAAAAA  BGE       0xFEAAAACC
0x00000020  00000FFF  ???EQ
0x00000024  0000001C  ANDEQ     R0,R0,R12,LSL R0
0x00000028  00000000  ANDEQ     R0,R0,R0
```

ex1.asm

```
1        AREA prog1, code, READONLY
2        ENTRY
3        LDR r0,[r1]
4        LDR r0, =0xFF    ; pseudo-instruc
5        LDR r0, =0xFFF   ; pseudo-instruc
6        LDR r0, X        ; pseudo-instruc
7        LDR r0, =X       ; pseudo-instruc
8        ADR r0, X        ; pseudo-instruc
9 loop   B loop
10 X     DCD 0xAAAAAAAA
11       END
12
```

How is this offset calculated?

Press Step, or F11



ARM pseudo-instructions

Same address (no change)

C:\Users\elsakka2\Desktop\ARM\ex1.uvproj - µVision4

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Registers

Register	Value
Current	
R0	0x0000001C
R1	0x00000000
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000018
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC $	0x00000018
Mode	Supervisor
States	14
Sec	0.00000000

Project | Registers

Disassembly

```
     3:        LDR r0,[r1]
0x00000000  E5910000  LDR       R0,[R1]
     4:        LDR r0, =0xFF    ; pseudo-instruction
0x00000004  E3A000FF  MOV       R0,#0x000000FF
     5:        LDR r0, =0xFFF   ; pseudo-instruction
0x00000008  E59F0010  LDR       R0,[PC,#0x0010]
     6:        LDR r0, X        ; pseudo-instruction
0x0000000C  E59F0008  LDR       R0,[PC,#0x0008]
     7:        LDR r0, =X       ; pseudo-instruction
0x00000010  E59F000C  LDR       R0,[PC,#0x000C]
     8:        ADR r0, X        ; pseudo-instruction
0x00000014  E28F0000  ADD       R0,PC,#0x00000000
     9: loop B loop
0x00000018  EAFFFFFE  B         0x00000018
0x0000001C  AAAAAAAA  BGE       0xFEAAAACC
0x00000020  00000FFF  ???EQ
0x00000024  0000001C  ANDEQ     R0,R0,R12,LSL R0
0x00000028  00000000  ANDEQ     R0,R0,R0
```

ex1.asm

```
1        AREA prog1, code, READONLY
2        ENTRY
3        LDR r0,[r1]
4        LDR r0, =0xFF    ; pseudo-instruction
5        LDR r0, =0xFFF   ; pseudo-instruction
6        LDR r0, X        ; pseudo-instruction
7        LDR r0, =X       ; pseudo-instruction
8        ADR r0, X        ; pseudo-instruction
9 loop B loop
10 X     DCD 0xAAAAAAAA
11       END
12
```

ARM pseudo-instructions

- Consider we changed the previous program as follow:

```
AREA prog1, code, READONLY
     ENTRY
     LDR r0,[r1]
     LDR r0, =0xFF    ; pseudo-instruction
     LDR r0, =0xFFF   ; pseudo-instruction
     LDR r0, X        ; pseudo-instruction
     LDR r0, =X       ; pseudo-instruction
     ADR r0, X        ; pseudo-instruction
loop B loop
X    DCD 0xAAAAAAAA
     END
```

```
     AREA prog1, code, READONLY
     ENTRY
     LDR r0,[r1]
     LDR r0, =0xFF    ; pseudo-instruction
     LDR r0, =0xFFF   ; pseudo-instruction
     LDR r0, X        ; pseudo-instruction
     LDR r0, =X       ; pseudo-instruction
     ADR r0, X        ; pseudo-instruction
loop B loop

     AREA prog1, data, READONLY
X    DCD 0xAAAAAAAA
     END
```

- What is the effect of this change on the generated code?

ARM pseudo-instructions

C:\Users\elsakka2\Desktop\ARM\ex1.uvproj - µVision4

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Registers

Register	Value
Current	
R0	0x0000001C
R1	0x00000000
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000018
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC $	0x00000018
Mode	Supervisor
States	14
Sec	0.00000000

Disassembly

```
     3:      LDR r0,[r1]
0x00000000  E5910000  LDR       R0,[R1]
     4:      LDR r0, =0xFF    ; pseudo-instruction
0x00000004  E3A000FF  MOV       R0,#0x000000FF
     5:      LDR r0, =0xFFF   ; pseudo-instruction
0x00000008  E59F0010  LDR       R0,[PC,#0x0010]
     6:      LDR r0, X        ; pseudo-instruction
0x0000000C  E59F0008  LDR       R0,[PC,#0x0008]
     7:      LDR r0, =X       ; pseudo-instruction
0x00000010  E59F000C  LDR       R0,[PC,#0x000C]
     8:      ADR r0, X        ; pseudo-instruction
0x00000014  E28F0000  ADD       R0,PC,#0x00000000
     9: loop B loop
0x00000018  EAFFFFFE  B         0x00000018
0x0000001C  AAAAAAAA  BGE       0xFEAAAACC
0x00000020  00000FFF  ???EQ
0x00000024  0000001C  ANDEQ     R0,R0,R12,LSL R0
0x00000028  00000000  ANDEQ     R0,R0,R0
```

ex1.asm

```
1       AREA prog1, code, READONLY
2       ENTRY
3       LDR r0,[r1]
4       LDR r0, =0xFF    ; pseudo-instruction
5       LDR r0, =0xFFF   ; pseudo-instruction
6       LDR r0, X        ; pseudo-instruction
7       LDR r0, =X       ; pseudo-instruction
8       ADR r0, X        ; pseudo-instruction
9 loop  B loop
10 X    DCD 0xAAAAAAAA
11      END
12
```

Project Registers

C:\Users\elsakka2\Desktop\ARM\ex1.uvproj - µVision4

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Registers

Register	Value
Current	
R0	0x00000024
R1	0x00000000
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000018
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC $	0x00000018
Mode	Supervisor
States	14
Sec	0.00000000

Disassembly

```
     3:      LDR r0,[r1]
0x00000000  E5910000  LDR       R0,[R1]
     4:      LDR r0, =0xFF    ; pseudo-instruction
0x00000004  E3A000FF  MOV       R0,#0x000000FF
     5:      LDR r0, =0xFFF   ; pseudo-instruction
0x00000008  E59F000C  LDR       R0,[PC,#0x000C]
     6:      LDR r0, X        ; pseudo-instruction
0x0000000C  E59F0010  LDR       R0,[PC,#0x0010]
     7:      LDR r0, =X       ; pseudo-instruction
0x00000010  E59F0008  LDR       R0,[PC,#0x0008]
     8:      ADR r0, X        ; pseudo-instruction
0x00000014  E28F0008  ADD       R0,PC,#0x00000008
     9: loop B loop
0x00000018  EAFFFFFE  B         0x00000018
0x0000001C  00000FFF  ???EQ
0x00000020  00000024  ANDEQ     R0,R0,R4,LSR #32
0x00000024  AAAAAAAA  BGE       0xFEAAAAD4
0x00000028  00000000  ANDEQ     R0,R0,R0
```

ex1.asm

```
3       LDR r0,[r1]
4       LDR r0, =0xFF    ; pseudo-instruction
5       LDR r0, =0xFFF   ; pseudo-instruction
6       LDR r0, X        ; pseudo-instruction
7       LDR r0, =X       ; pseudo-instruction
8       ADR r0, X        ; pseudo-instruction
9 loop  B loop
11      AREA prog1, data, READONLY
12 X    DCD 0xAAAAAAAA
13      END
14
```

Project Registers