Remind:

RIS: SP RI4:LR RIS:PC

STR Rt, Dan, Hoffset] inomediate-indexed:不影響 Prissio.

STR Rt, LRn, Hoffset]! pre-indexed: 先用再更新

STR Rt, IRn7, # offset post-indexed

Occupied memory

Pre-update, grows up writeback.

STR RO. [sp, 4-4]!

LDR RO. ISP]. A4.

Emply memory

Post-update, grows up

STR RO, ISP1, A-4

LDR RO. [Sp. 747!

Occupied

Pre-update- grows down

STR Ro, [sp, #4]!

LDR RO, [sp], #-4.

Emply memory

Post-update, grows down

STR Ro. isp1, #4

LDR RO ESP, #-47!

Occupied memory -> pre-index -> top item

Empty memory -> postindex > First Free empty space.

CISC processor automatically maintain the stack, while RISC have to be mintained by the programmar.

Block More Instruction

ADR: