# Computer Organization COMPSCI 3350B

## Quiz #1

## Total Marks 7.5

**General Quiz Information**

- This quiz is to be performed and submitted using OWL(In Dropbox).
- This quiz is to be completed as an individual, not as a team.
- Make sure to write your full name and enrolment number on the top of the Page.

**Select the best possible answer.**

**Question 1:** Which of the following is a type of architecture used in computers nowadays? (1)
a) Microarchitecture
b) Harvard Architecture
c) Von-Neumann Architecture
d) System Design

**Question 2:** Given the following instructions, their relative frequencies in a program, and the number of clock cycles of each instruction on some processor, calculate the effective CPI (cycles per instruction) of that program.

| Operation | Frequency | $CPI_i$ |
|---|---|---|
| ALU | 25% | 1 |
| Load | 30% | 6 |
| Store | 25% | 4 |
| Branch | 20% | 2 |

a) 3.95
b) 3.46
c) 3.45
d) 2.23

**Question 3:** A new processor results in twice the load speed as that of the processor used in part (a) and also increases a branch instruction to take 3 cycles. Calculate the new effective CPI of the program from part (a) when run on this new processor. (1)

a) 2.67
b) 3.39
c) 2.75
d) 3.00

**Question 4:** Assume a memory access to main memory on a cache "miss" takes 30 ns and a memory access to the cache on a cache "hit" takes 3 ns. If 80% of the processor's memory requests result in a cache "hit", what is the average memory access time? (1)

a) 8.4 nS

b) 33 nS

c) 24.6 nS

d) 27.0 nS

**Question 5:** Which one of the statements is true regarding spatial and temporal locality in the following code? (1.5)

```
Char var[N], res;
For (j=0; j<M; j++){
   For(i=0; i<T; i++){
          Res+= var[i];
}
}
```

a) We have spatial locality when N> 1.
b) We have temporal locality if N=1, M=1 and T=2
c) We have temporal locality when N>1
d) Regardless of M, N and T Values we have temporal locality for res.

**Question 6:** A computer has a single cache (off-chip) with a 2 ns hit time and a 98% hit rate. Main memory has 40 ns access time. What is the computer's effective access time? If we add an on-chip cache with a .5 ns hit time and a 94% hit rate, what is the computer's effective access time? How much speedup does the on-chip cache give the computer? (1)

a) 3.5 ns
b) 2.8 ns
c) 4.1 ns
d) 2.7 ns

**Question 7:** The register that includes the address of the memory unit is termed as the ----------(1)

a) MAR
b) PC
c) IR
d) None