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Ex1, Ex2: check a3q1.c, a3q2.s on owl.

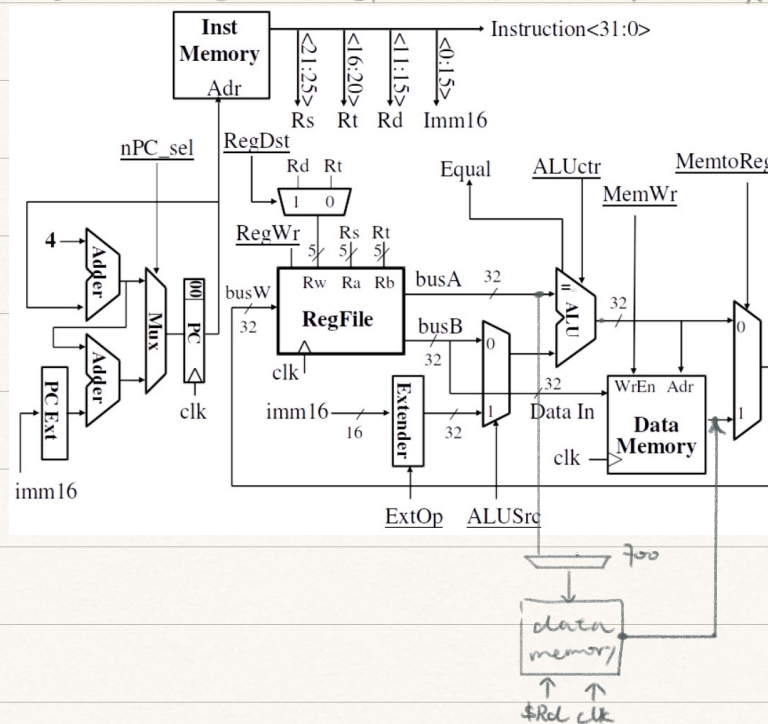
Exercise 3:

ALUctr MemWr MemtoReg ExtOp ALUSrc nPC_sel RegDst RegWr

(a) slt 0 0 x 0 0 1 1
 (b) bne 0 0 t1 0 1 x 0

Exercise 4:

(a) -



(b) :

1. Before ALU, a MUX is added to determine whether the instruction is "foo" or not

2. If it is "foo", then update the value in Reg[rt]

3. Update the value in memory address Reg[rd].

4. Increment PC value for next instruction.

(c) ALUctr MemWr MemtoReg ExtOp ALUSrc nPC_sel RegDst RegWr foo

foo 0 1 x 0 0 0 1 1