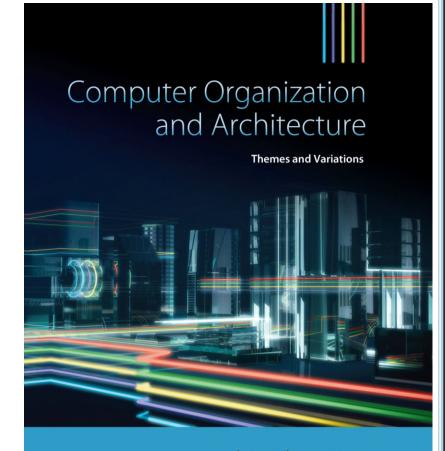
Part 4

CHAPTER 2

Computer
Arithmetic and
Digital Logic



Alan Clements

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Computer Logic

- □ Computers are constructed from two basic circuit elements *gates* and *flip-flops*, known as *combinational* and *sequential* logic elements.
 - = both take input to give output
- A combinational logic element is a circuit whose output depends only on its current inputs, no history: we memory.

whereas

A sequential logic element is a circuit whose output depends on its <u>past history</u> as well as its <u>current inputs</u>.

-> has memory.

- □ A sequential element can remember its previous value (memory element).
- □ Sequential elements themselves can be made from simple combinational logic elements.
 - o Hence, we can simply say that *computers can be constructed using just gates*

fupflops can be built using gases.

Logic Values

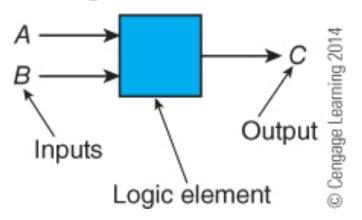
- ☐ A *logic value* can be either
 - o the *logical 1* (also called the *true* or *high* state)
 - o the *logical 0* (also called the *false* or *low* state)
- □ Each logic state has an *inverse* or a *complement* that is the opposite of its current state.
 - \circ The complement of a *true* or 1 state is a *false* or 0 state
 - The complement of a *false* or *0* state is a *true* or *1* state

Gates

- ☐ Figure 2.14 shows a black box of a gate with two *input* terminals, *A* and *B*, and a single *output* terminal *C*.
 - This gate takes the two logic
 values at its input terminals and
 - o produces *a logic output value* that *depends only on*
 - the *states of the inputs* and
 - the nature of the logic element.

FIGURE 2.13

The logic element



- ☐ Examples of gates include
 - o AND, OR, NOT, NAND, NOR, Exclusive OR gates.

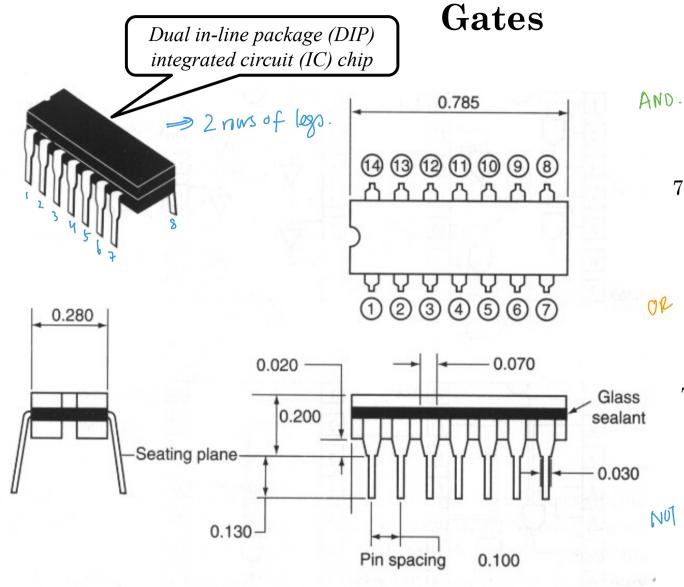
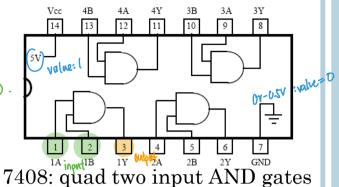
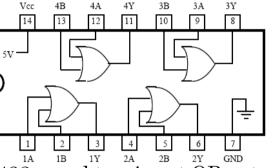


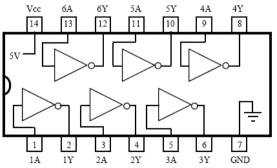
FIGURE 3.17

14-pin ceramic package (all linear dimensions are in inches).





7432: quad two input OR gates



7404: hex inverter gates

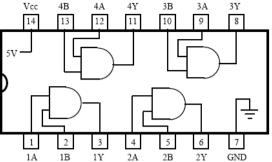
4 produce compliment

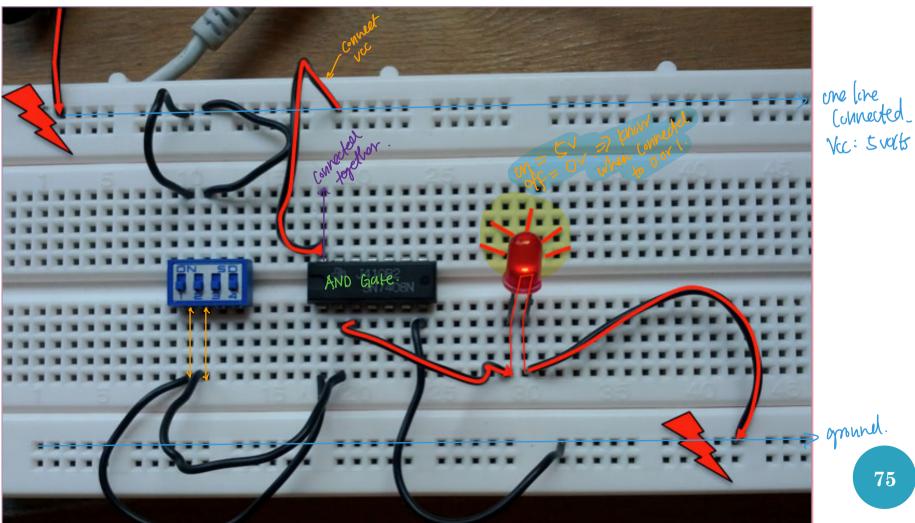
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Computer Organization and Architecture: Themes and Variations, 1st Edition

Clements

Gates





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Computer Organization and Architecture: Themes and Variations, 1st Edition Clements output = | When all input = [.

The AND Gate

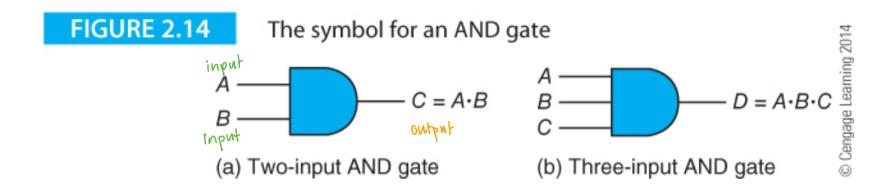
- ☐ The behavior of a gate is described by its *truth table* that *defines its* output for each of the possible inputs.
- \square Table 2.8a provides the truth table for the *two-input* **AND** gate.
 - o If the two input are *A* and *B*, then the output *C* will be true (i.e., 1) if and only if both inputs *A* and *B* are true (i.e., 1) simultaneously.
- ☐ Table 2.8b gives the truth table for the *three input* AND gate.
 - o If A, B, and C are the inputs, then the output D will be true (i.e., 1) if and only if all inputs are true (i.e., 1) simultaneously.
- ☐ The AND is represented by a "."
 - o the operation A AND B can be written as A. B

| T. | ABLE 2 | .8 Trut | Table for the AN | D Gate | truth table: | all possible |
|-------|---------|-----------------|------------------|--------|--------------|-------------------------|
| В | Α | $C = A \cdot B$ | C | В | Α | $D = A \cdot B \cdot C$ |
| 0 | 0 | 0 | 0 | O | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| a) Tw | o-input | AND gate | 1 | 0 | 0 | 0 |
| | | 3 | 1 | 0 | 1 | 0 |
| | | | 1 | 1 | 0 | 0 0 0 1 |
| | | | 1 | 1 | 1 | 1 |

(b) Three-input AND gate

The AND Gate

☐ Figure 2.14 gives the symbols for 2-input and 3-input AND gates



The OR Gate produce 0 if all input >0.

- \square The output of an **OR** gate is 1 if at least one of its inputs is 1.
- ☐ The only way to make the output of an OR gate go to a logical 0 is to set all its inputs to 0.
- ☐ The OR is represented by a "+"
 - o the operation A OR B can be written as A + B

| TABLE 2.9 | ruth Table for the OR Gate |
|-----------|----------------------------|
|-----------|----------------------------|

| В | Α | C = A + B | |
|---|---|-----------|--|
| 0 | 0 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 1 | |
| 1 | 1 | 1 | |

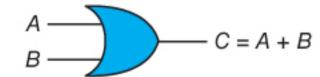
(a) Two-input OR gate

| C | В | A | D = A + B + C |
|---|---|---|---------------|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

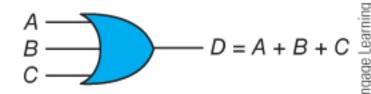
(b) Three-input OR gate

FIGURE 2.15

The symbol for an OR gate



(a) Two-input OR gate



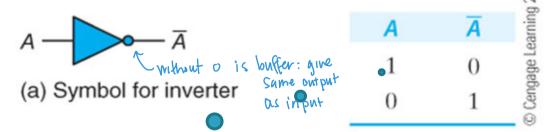
(b) Three-input OR gate

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The NOT gate or inverter

- ☐ The **NOT** is represented by
 - o an "overbar", e.g., the operation NOT A is written as A
 - o a superscript c, e.g., the operation **NOT** A is written as A^c or
 - o a tilde mark ~, e.g., the operation **NOT** A is written as ~ A or
 - o a negation mark ¬, e.g., the operation **NOT** A is written as ¬ A or
 - o an exclamation mark!, e.g., the operation NOT A is written as !A
- \square Note that, $\overline{\overline{A}} = A$

FIGURE 2.16 The symbol and truth table for an inverter



This bit is 1 not 0.
The book wrote it incorrectly as 0.

(b) Truth table of inverter

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