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Ex. 1:

$$\overline{A}BC + \overline{A}B\overline{C} + \overline{A}B\overline{C} + A\overline{B}C + A\overline{B}\overline{C}$$

$$\equiv \overline{A}B(\overline{C}+C) + \overline{A}B\overline{C} + A\overline{B}C(\overline{C}+C)$$

$$\equiv \overline{A}B(1) + \overline{A}B\overline{C} + A\overline{B}C(1)$$

$$\equiv \overline{A}B + \overline{A}B\overline{C} + A\overline{B}$$

$$\equiv \overline{B}(\overline{A}+A) + \overline{A}B\overline{C}$$

$$\equiv \overline{B}(1) + \overline{A}B\overline{C}$$

$$\equiv \overline{B} + \overline{A}B\overline{C}$$

factor $\overline{A}B$, $A\overline{B}$.

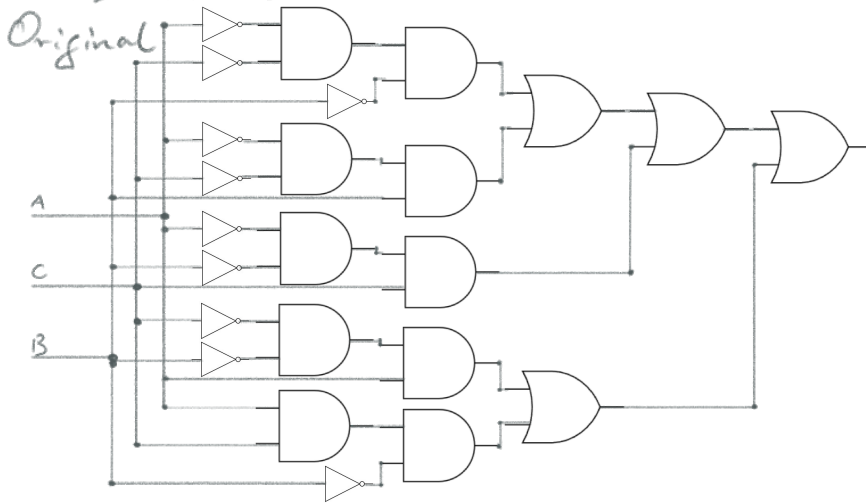
complement of C

identity with $\overline{A}B$ and $A\overline{B}$.

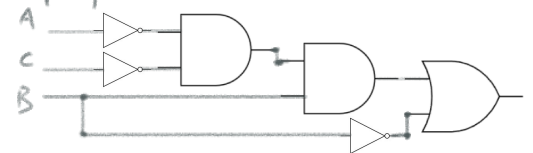
factor \overline{B} .

complement of A

identity with \overline{B} .



Simplified:

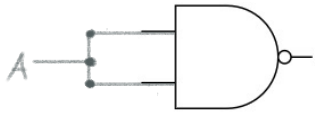


Ex. 2:

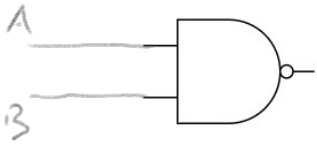
NAND and NOR are called functionally complete gates since every operation or function could be described as an algebra using only one of these two gates.

using NAND gates only:

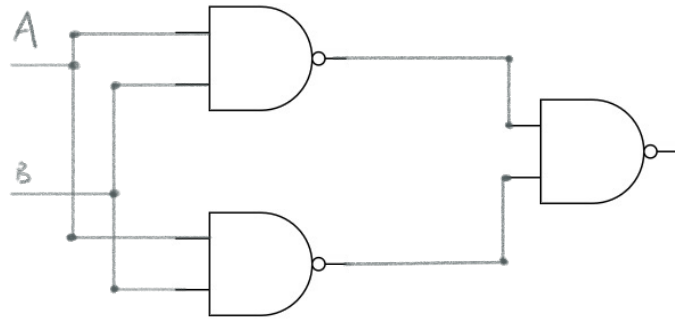
$$\text{NOT } A = A \text{ NAND } A$$



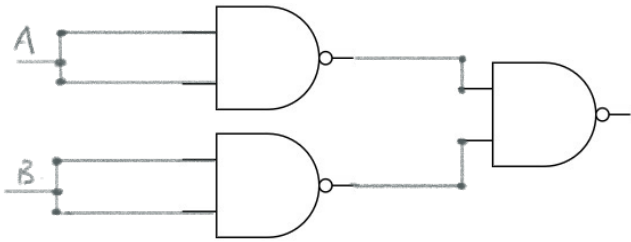
$$A \text{ NAND } B = A \text{ NAND } B$$



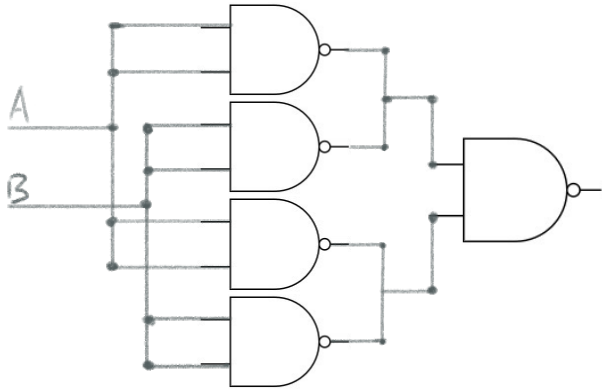
$$A \text{ AND } B = (A \text{ NAND } B) \text{ NAND } (B \text{ NAND } A)$$



$$A \text{ OR } B = (A \text{ NAND } A) \text{ NAND } (B \text{ NAND } B)$$

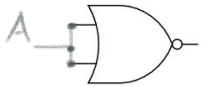


$$A \text{ NOR } B = [(A \text{ NAND } A) \text{ NAND } (B \text{ NAND } B)] \text{ NAND } [(A \text{ NAND } A) \text{ NAND } (B \text{ NAND } B)]$$



using NOR Gates only:

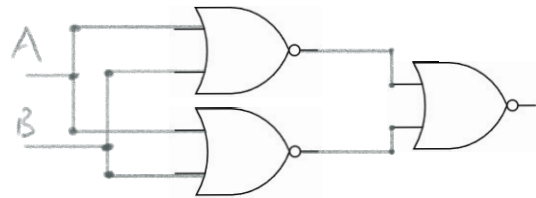
$$\text{NOT } A = A \text{ NOR } A$$



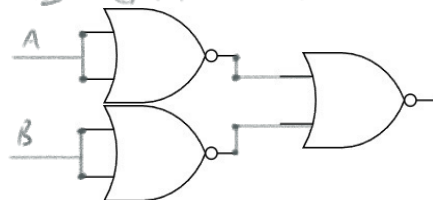
$$A \text{ NOR } B = A \text{ NOR } B$$



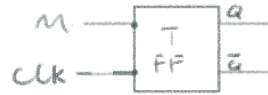
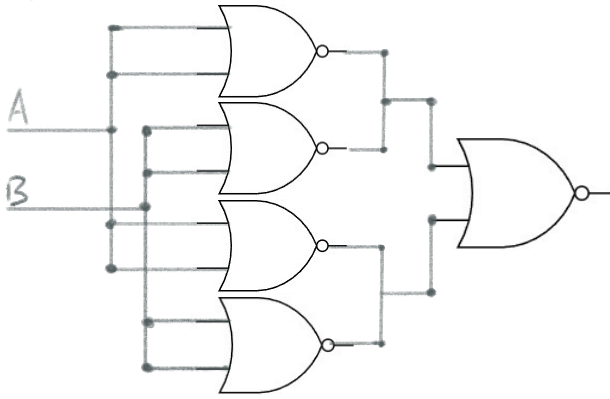
$$A \text{ OR } B = (A \text{ NOR } B) \text{ NOR } (B \text{ NOR } A)$$



$$A \text{ AND } B = (A \text{ NOR } A) \text{ NOR } (B \text{ NOR } B)$$



$$A \text{ NAND } B = [(A \text{ NOR } A) \text{ NOR } (B \text{ NOR } B)] \text{ NOR } [(A \text{ NOR } A) \text{ NOR } (B \text{ NOR } B)]$$



Ex. 3:

$$S \equiv S_0 S_1$$

$$Q_{n+1} \equiv \text{MUX}(a, b, c, d, S)$$

$$Q_{n+1} \equiv \overline{S_0 S_1} a + \overline{S_0} S_1 b + \overline{S_1} S_0 c + S_0 S_1 d$$

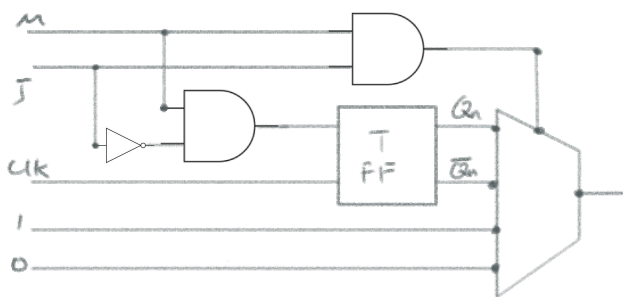
Assuming that $a=1$, $b=0$, $c=\overline{Q_n}$, $d=Q_n$, we could get:

$$Q_{n+1} \equiv \overline{S_0 S_1} \cdot 1 + \overline{S_0} S_1 \cdot 0 + \overline{S_1} S_0 \cdot \overline{Q_n} + S_0 S_1 \cdot Q_n$$

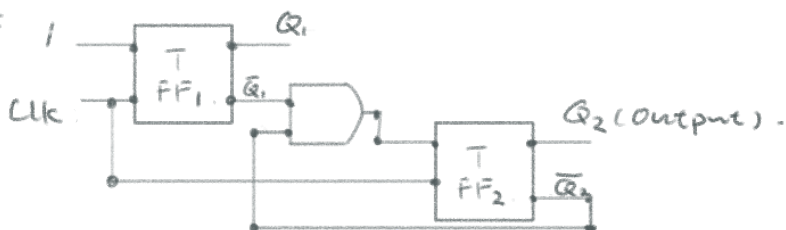
$$\equiv \overline{S_0 S_1} + \overline{S_1} S_0 \overline{Q_n} + S_0 S_1 Q_n$$

Given that MJ Flipflop is controlled by M and J, we could get

$$Q_{n+1} \equiv \overline{M} J + \overline{M} J \overline{Q_n} + M J Q_n$$

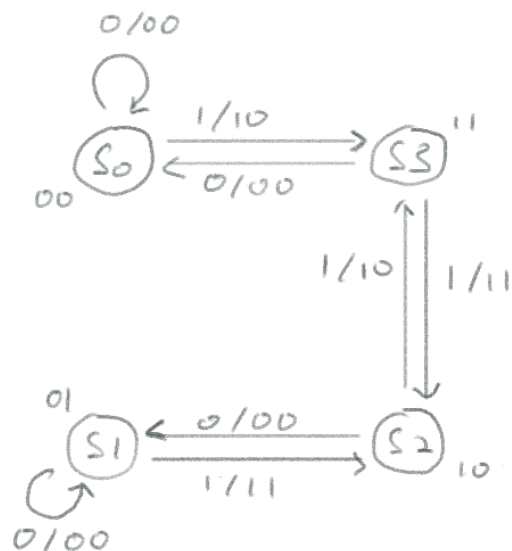


Ex. 4



Ex. 5.

(a)



(b)

PS	In	NS	G	F	* Out is broken
00	0	00	0	0	into G and F
00	1	11	1	0	
01	0	01	0	0	
01	1	10	1	1	
10	0	01	0	0	
10	1	11	1	0	
11	0	00	0	0	
11	1	10	1	1	

(c).

DNF for G:

$$G \equiv \overline{PS0} \cdot \overline{PS1} \cdot In + \overline{PS0} \cdot PS1 \cdot In + \overline{PS1} \cdot PS0 \cdot In + PS0 \cdot PS1 \cdot In$$

$$\equiv In \cdot (\overline{PS0} \cdot \overline{PS1} + \overline{PS0} \cdot PS1 + \overline{PS1} \cdot PS0 + PS1 \cdot PS0)$$

$$\equiv I$$

DNF for F :

$$F \equiv \overline{PS0} \cdot \overline{PS1} \cdot In + PS1 \cdot \overline{PS0} \cdot In$$

$$\equiv \overline{PS0} \cdot In \cdot (\overline{PS1} + PS1)$$

$$\equiv \overline{PS0} \cdot In$$

DNF for $NS0$:

$$NS0 \equiv \overline{PS0} \cdot \overline{PS1} \cdot \overline{In} + \overline{PS0} \cdot \overline{PS1} \cdot In + PS1 \cdot \overline{PS0} \cdot \overline{In} + PS1 \cdot \overline{PS0} \cdot In$$

$$\equiv \overline{PS0} \cdot \overline{PS1} \cdot In + \overline{PS0} \cdot \overline{PS1} \cdot \overline{In} + PS1 \cdot \overline{PS0}$$

DNF for $NS1$:

$$NS1 \equiv \overline{PS0} \cdot \overline{PS1} \cdot In + \overline{PS0} \cdot \overline{PS1} \cdot \overline{In} + \overline{PS0} \cdot PS1 \cdot In + \overline{PS0} \cdot PS1 \cdot \overline{In}$$

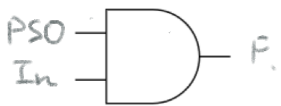
$$\equiv \overline{PS0}$$

cd)

G :

In G

F :



$NS0$:

$NS1$:

In $NS1$.