Study Questions (Chapter 03 – Part A)

1. Write an ARM LDR/STR address register indirect instruction(See slide 129). LDR r0, [r1]
   a) Encode this instruction to machine language.
   b) Use the ARM simulator to verify that your answer is correct.
   c) Decode the generated machine language instruction to generate the original assembly instruction.

2. Write an ARM LDR/STR program counter relative instruction(See slide 129) . LDR r0, [PC, #imm]
   a) Encode this instruction to machine language.
   b) Use the ARM simulator to verify that your answer is correct.
   c) Decode the generated machine language instruction to generate the original assembly instruction.

3. Write an ARM LDR/STR address register indirect with offset instructoin(See slide 129) . LDR r0, [r1, #4].
   a) Encode this instruction to machine language.
   b) Use the ARM simulator to verify that your answer is correct.
   c) Decode the generated machine language instruction to generate the original assembly instruction.

4. Write an ARM LDR/STR address register indirect with index instructoin(See slide 129). LDR r2 [r0, r1].
   a) Encode this instruction to machine language.
   b) Use the ARM simulator to verify that your answer is correct.
   c) Decode the generated machine language instruction to generate the original assembly instruction.

5. Write an ARM LDR/STR address register indirect with offset and pre-update instructoin(See slide 129) .
   a) Encode this instruction to machine language. LDR r0, [r1, #8]!
   b) Use the ARM simulator to verify that your answer is correct.
   c) Decode the generated machine language instruction to generate the original assembly instruction.

6. Write an ARM LDR/STR address register indirect with index and pre-update instructoin(See slide 129).
   a) Encode this instruction to machine language. LDR r0, [r0, r1]!
   b) Use the ARM simulator to verify that your answer is correct.
   c) Decode the generated machine language instruction to generate the original assembly instruction.

7. Write an ARM LDR/STR address register indirect with offset and post-update instructoin(See slide 129) .
   a) Encode this instruction to machine language.
   b) Use the ARM simulator to verify that your answer is correct.
   c) Decode the generated machine language instruction to generate the original assembly instruction.

8. Write an ARM LDR/STR address register indirect with index and post-update instructoin(See slide 129).
   a) Encode this instruction to machine language.
   b) Use the ARM simulator to verify that your answer is correct.
   c) Decode the generated machine language instruction to generate the original assembly instruction.