Project 6: Layout & Verification

Zachary Kearney NetID: zck190000

Yu Feng NetID: yxf160330

Chang Tu NetID: cxt190006

EE 6325

Introduction

The Arithmetic Logic Unit (ALU) is the foundational digital circuit within a computer. The ALU is where all mathematical and logical operations occur such as addition, multiplication, and bitwise and occur in the ALU. Specifically, a 32bit ALU with functions:

- Addition
- Subtraction
- Multiplication
- Pass Input A
- Pass Input B
- Bitwise AND
- Bitwise OR
- Bitwise XOR
- Bitwise Not Input A
- Bitwise Not Input B
- No Operation (NOP)

The ALU has four different input signals:

1. Operand A (op_A) is a 32 bit number that is the first operand in one of the above functions.
2. Operand B (op_B) is a 32 bit number that is the second operand in one of the above functions.
3. Control (ctrl) is a 4 bit input that selects which of the above function is executed.
4. Clock Signal (clk) is the clock that drives the flip flops.

The ALU has one output signal:

1. Result (result) is a 32 bit number that is the result of one of the above functions.

The ALU was implemented using 65nm technology and designed utilizing Cadence tools.

Procedure

Behavioral Verilog

First, behavioral Verilog was written to describe the functionality of the ALU. Verilog includes constructs that can and cannot be synthesized. Great care was taken to ensure that constructs used to implement the ALU were synthesizable. Additionally, the standard cell library being used only included a D Flip-Flop. Specific Verilog constructs infer latches when the code is synthesized. Therefore, it was necessary to write the behavior so that flip-flops would be generated. Once the design was complete, the waveforms were simulated to ensure functionality. The results of the simulation can be viewed in Figure 1.

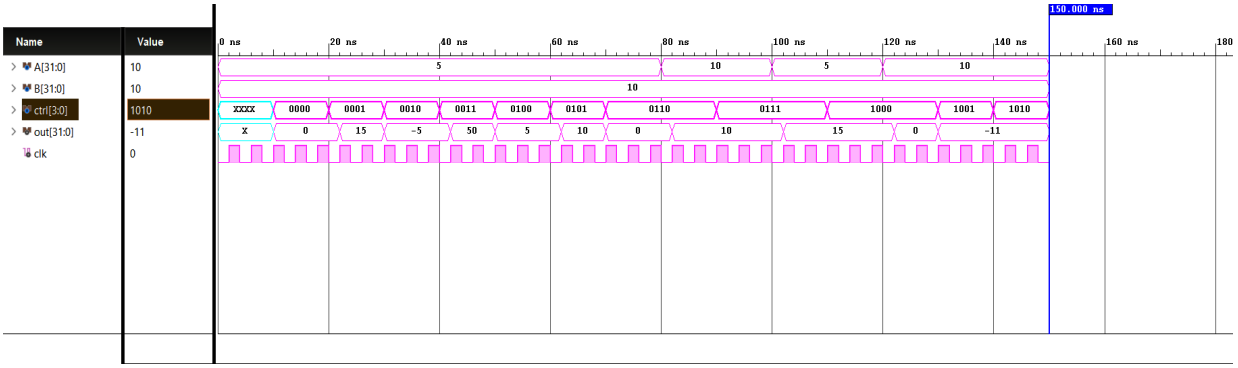

Figure 1. Verilog Behavioral Simulation

Synthesized Verilog

Once the behavioral Verilog was written, Synopsys Design Vision was used to generate mapped Verilog. A functional cell library and corresponding Verilog header was provided for the purposes of testing the design. The mapped Verilog was simulated to ensure the functionality matched the behavioral Verilog. The results of the simulation can be viewed in Figure 2.

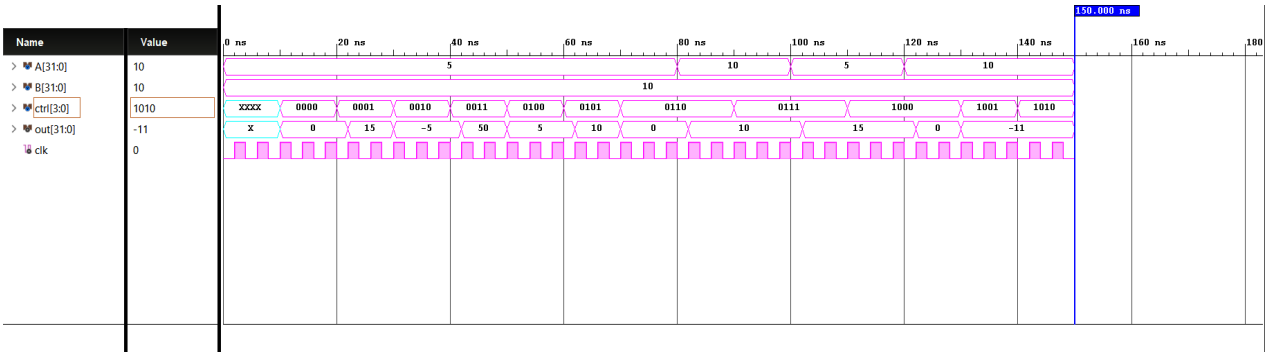

Figure 2. Mapped Verilog Simulation

The simulations matched, indicating the mapped Verilog functioned correctly.

Standard Cell Library

With the functionality of the design verified, the implementation of the design began with creation of the standard cell library. Cadence Virtuoso was used to create the cells. The standard cell library consisted of nine standard cells.

- INV
- NAND2
- NOR2
- XOR2
- AOI22
- AOI211
- OAI21
- D Flip-Flop

- MUX2:1

After creating the layouts for each of the standard cells, the cells needed to be checked for technology compliance. Software called Calibre was used to run a check called Design Rule Checker (DRC). DRC verifies that the layout can be fabricated using the gf65 technology. For each cell a schematic was created for the logical circuit the layout was implementing. Calibre was used to run another check called Layout vs Schematic (LVS). LVS ensures that the layout and schematic have the same ports, nets, and other parameters. Once LVS has been cleared, Parasitic Extraction (PEX) can be run using Calibre. PEX generates spice netlists for the layout that include parasitic components.

Cell Simulations

The software HSPICE was used to simulate each cell in the cell library. A spice setup file was created to test all input combinations. The slew rate for inputs was defined as 40ps from 0.2*VDD to 0.8*VDD and a 90fF. The spice setup file imported the netlist generated by PEX. After, completing the setup file, the HSPICE simulation was run and the results were viewed using a separate software called WaveView. In WaveView the waveforms were analyzed to ensure the cells functioned properly. The D flip-flop required some additional measurements to be taken such as setup time and clk to q time.

SiliconSmart

The next step was to use the netlists generated by PEX to create a library of the standard cells. The software SiliconSmart generated delay tables for each cell. Once all cells were characterized, a single library file was compiled and converted to a db library file for later use with PrimeTime.

Generate Synthesized Verilog using Cell Library

Next, Design Vision was used again to create a mapped netlist. This time the library file generated using SiliconSmart was used instead of the provided library file.

Create Abstract and LEF

Cadence Virtuoso was used to generate abstract views of all the cells in the cell library. These abstract views would be used for placement and routing. A filler cell was created that only comprised of VDD and GND nets. The filler cell will fill in any gaps between cells once the design is placed. A lef file was generated that contained the abstract view of all cells and the filler cell.

Placing and Routing with Innovus

With the generated lef file and mapped Verilog from Design Vision placement and routing could begin. Cadence Innovus was used to import the lef and mapped Verilog. A floorplan was created and Innovus was used to place all the cells. Filler cells were added in the locations where cells were not placed. Next, Innovus used NanoRoute to route all connections necessary for the design to function properly.

After Innovus completed routing, the placed and routed design was exported as a Verilog file and def file.

Full Layout

Next, Cadence Virtuoso was used to create a new library, and used to import the def file and Verilog file generated by Innovus. The lef generated by Virtuoso was imported and the standard cell library was linked to the new library. These three files along with the standard cell library create a layout and schematic of the full design. The full layout can be seen in Figure 3. DRC was run for a final time to ensure that the final layout met the gf65 design rules. Figure 4 verifies that the full layout passed DRC. LVS was run for a final time to ensure that the full layout matched the schematic generated by Innovus. Figure 5 shows that LVS succeeded for the full layout.

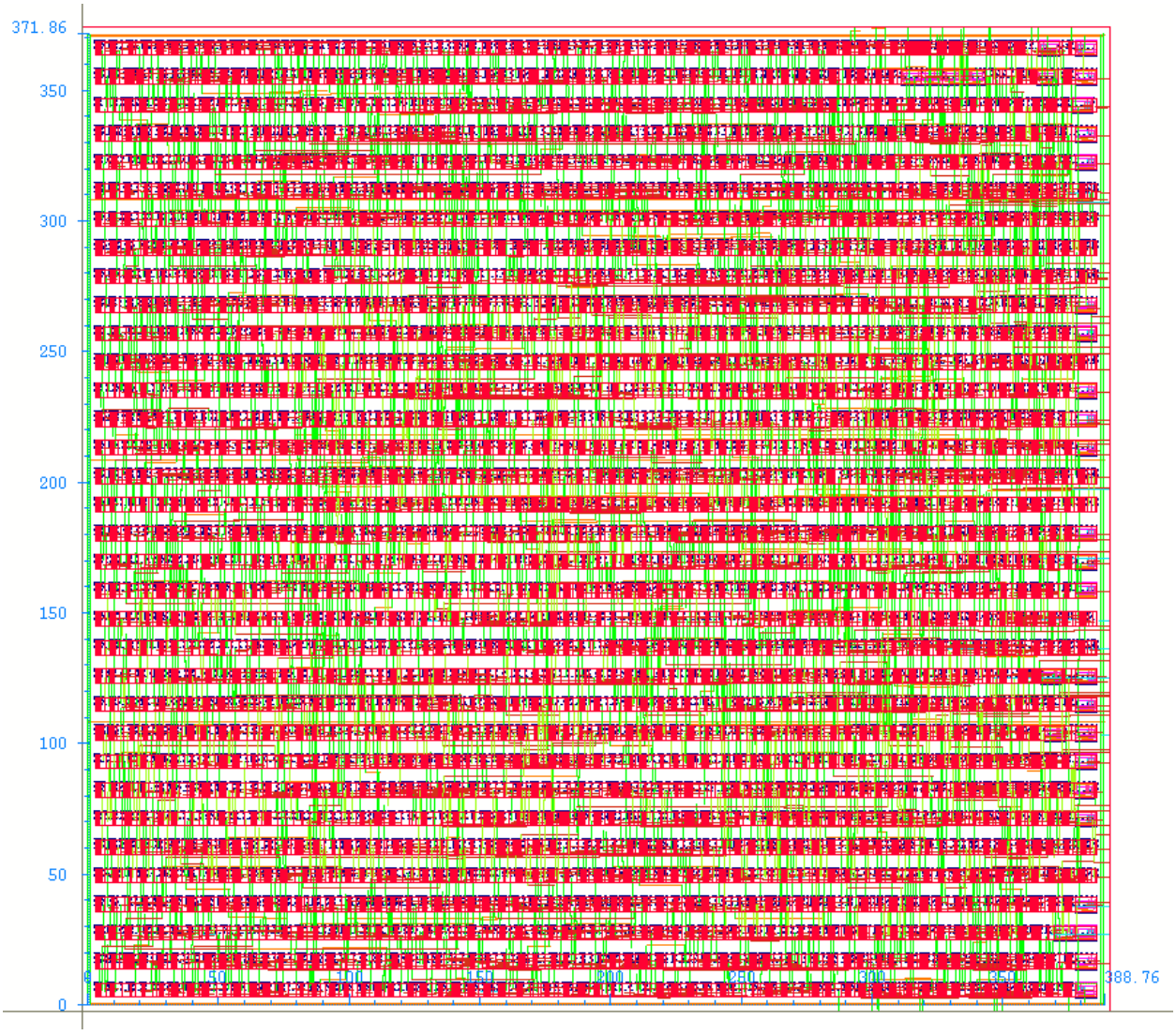

Figure 3. ALU Full Layout with Rulers

Figure 4. Full Layout DRC

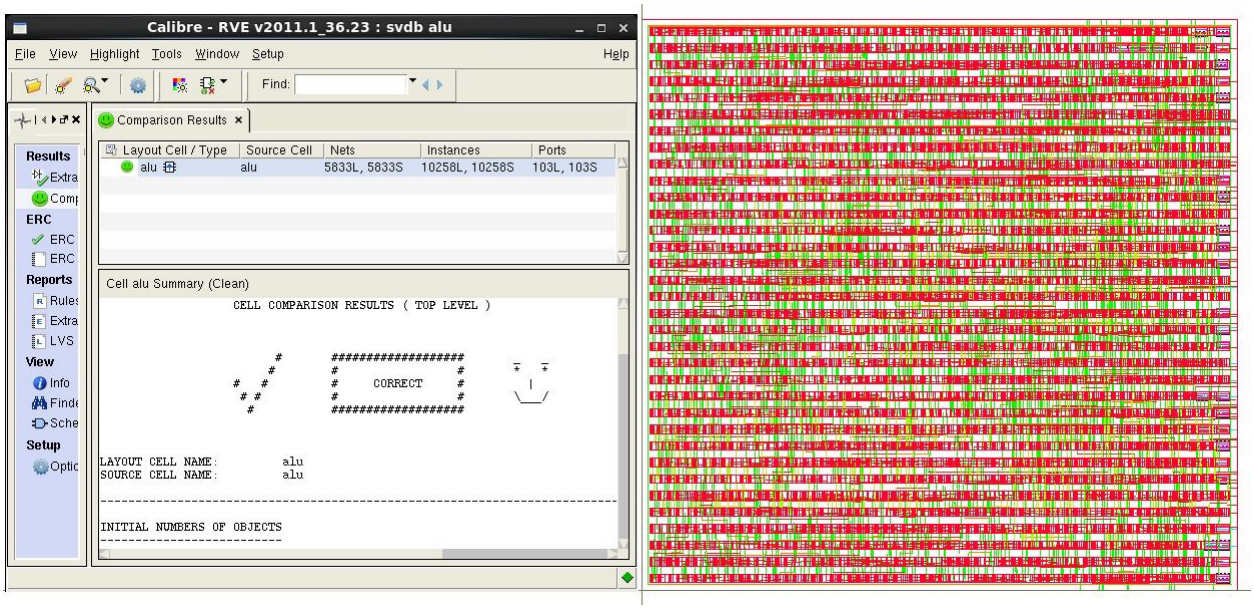

Figure 5. Full Layout LVS

PrimeTime

To measure the min delay, max delay, and power consumption, Synopsys PrimeTime was run using the flattened Verilog file and library file generated by Design Vision. The min delay was measured to be 3.55ns and the max delay was measured to be 13.45ns. The min delay can be seen in Figure 6 and the

max delay can be seen in Figure 7. Based on the PrimeTime the best clock period is 20ns. The power consumption was measured as 5.430e-4 W.

```
Startpoint: result_reg[0]
            (falling edge-triggered flip-flop clocked by clk')
Endpoint: result_reg[0]
            (falling edge-triggered flip-flop clocked by clk')
Path Group: clk
Path Type: min

Point                                   Cap      Trans       Incr       Path
-----------------------------------------------------------------------------
clock clk' (fall edge)                            0.00       0.00       0.00
clock network delay (ideal)                                  0.00       0.00
result_reg[0]/CLK (dffP6)                         0.00       0.00       0.00 f
result_reg[0]/Q (dffP6)                 2.00      6.85       4.78       4.78 r
U355/C (AOI22P6)                                  6.85       0.00       4.78 r
U355/OUT (AOI22P6)                      0.00      0.03       0.01       4.79 f
U346/A (nand2P6)                                  0.03       0.00       4.79 f
U346/OUT (nand2P6)                      0.00      0.02       0.02       4.81 r
result_reg[0]/D (dffP6)                           0.02       0.00       4.81 r
data arrival time                                                       4.81

clock clk' (fall edge)                           20.00       0.00       0.00
clock network delay (ideal)                                  0.00       0.00
clock reconvergence pessimism                                0.00       0.00
result_reg[0]/CLK (dffP6)                                                0.00 f
library hold time                                            1.26       1.26
data required time                                                      1.26
-----------------------------------------------------------------------------
data required time                                                      1.26
data arrival time                                                      -4.81
-----------------------------------------------------------------------------
slack (MET)                                                             3.55
```

Figure 6. Min Delay PrimeTime Results

```
Startpoint: result_reg[0]
              (falling edge-triggered flip-flop clocked by clk')
Endpoint: result_reg[0]
              (falling edge-triggered flip-flop clocked by clk')
Path Group: clk
Path Type: max

Point                                   Cap      Trans       Incr       Path
-----------------------------------------------------------------------------
clock clk' (fall edge)                           20.00       0.00       0.00
clock network delay (ideal)                                  0.00       0.00
result_reg[0]/CLK (dffP6)                        20.00       0.00       0.00 f
result_reg[0]/Q (dffP6)                 2.00      5.42       6.30       6.30 r
U355/C (AOI22P6)                                  5.42       0.00       6.30 r
U355/OUT (AOI22P6)                      0.00      0.75       0.05       6.35 f
U346/A (nand2P6)                                  0.75       0.00       6.35 f
U346/OUT (nand2P6)                      0.00      0.15       0.14       6.49 r
result_reg[0]/D (dffP6)                           0.15       0.00       6.49 r
data arrival time                                                       6.49

clock clk' (fall edge)                            0.00      20.00      20.00
clock network delay (ideal)                                  0.00      20.00
clock reconvergence pessimism                                0.00      20.00
result_reg[0]/CLK (dffP6)                                                20.00 f
library setup time                                                      -0.07      19.93
data required time                                                                 19.93
-----------------------------------------------------------------------------
data required time                                                                 19.93
data arrival time                                                                  -6.49
-----------------------------------------------------------------------------
slack (MET)                                                                        13.45
```

Figure 7. Max Delay PrimeTime Results

```
  Attributes
  ----------
     i  -  Including register clock pin internal power
     u  -  User defined power group

                                 Internal  Switching  Leakage    Total
Power Group                      Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------------
clock_network                    3.323e-07 4.979e-06 4.871e-11 5.311e-06 ( 0.98%)  i
register                         8.079e-06 1.553e-04 1.143e-07 1.635e-04 (30.10%)
combinational                    1.930e-04 1.809e-04 2.976e-07 3.743e-04 (68.92%)
sequential                          0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                              0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                              0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                           0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 3.412e-04   (62.83%)
  Cell Internal Power  = 2.015e-04   (37.10%)
  Cell Leakage Power   = 4.119e-07   ( 0.08%)
                         ---------
Total Power            = 5.430e-04  (100.00%)
```

Figure 8. Power Usage PrimeTime Results

Simulation

The Verilog file generated by Innovus was simulated to confirm that the layout's behavior matched the behavior of the original design. The results of the simulation can be seen in Figure 9.

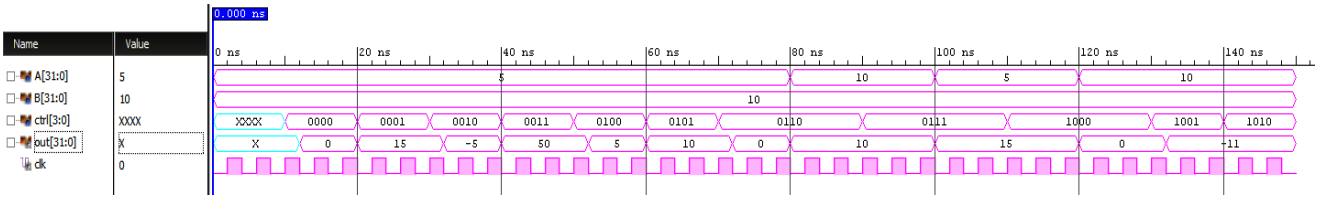

Figure 9. Full Layout Verilog Simulation

Conclusions

The design originated with behavioral Verilog and was converted into synthesized Verilog using a created standard cell library. The standard cell library and synthesized Verilog were used to place and route the cells together to implement a full layout. The full layout implements a 32-bit ALU with various functions.

Tradeoffs

The largest trade off was during the design of the D Flip-Flop. The three parameters that could be adjusted were diffusion breaks, cell height, and M2 usage. With two diffusion breaks the cell height would need to be large or metal two would be required. With 3 diffusion breaks the cell height could be small and no metal two would be needed. It was assessed that reducing the number of diffusion breaks which reduces the number of effective transistors was the most important of the three parameters. Therefore, the D Flip-Flop was implemented with two diffusion breaks, a larger cell height, and no metal two usage.

Design Parameters

Major Design Parameters are outlined in Table 1.

Table 1. Design Parameters

Category	Parameter	Value
Sizing	Full Layout Height	372 µm
	Full Layout Width	389 µm
	Full Layout Area	144708 µm^2
	Individual Cell Height	5.46 µm
Timing	Min Delay	3.55 ns
	Max Delay	13.45 ns
	Clock Period	20 ns
Power	Net Switching Power	3.412e-4 W
	Cell Internal Power	2.015e-4 W
	Cell Leakage Power	4.119e-7 W
	Total Power	5.430e-4 W
I/O	Input Pins	69
	Output Pins	32