

EEDG/CE 6303: Testing and Testable Design (Fall'2021)

Department of Electrical & Computer Engineering

The University of Texas at Dallas

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Cover Page for All Submissions

(Assignment, Project, Codes/Simulations/CAD, Examinations, etc.)

Last Name (as shown in the official UT Dallas Student ID Card): Feng

First Name: Yu

Submission Materials for (e.g. Homework #, Project #): HW 5

Statement of Academic Honesty

I certify that:

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- ii. I have acknowledged all material and sources used in its preparation, whether they be books, articles, reports, lecture notes, and any other kind of document, electronic or personal communication,
- iii. this report has not previously been submitted for assessment in EEDG/CE 6303 or any other course at UT Dallas or elsewhere,
- iv. I have not copied in part or whole or otherwise plagiarized the work of other students and/or persons, and
- v. I have read and understood the Department and University policies on scholastic dishonesty as outlined in: <http://www.utdallas.edu/deanofstudents/dishonesty/>.

Name: Yu Feng

Date: 12/1/2021

Signature: 

The University of Texas at Dallas
Dept. of Electrical and Computer Engineering

EEDG/CE 6303: Testing and Testable Design

HW # 6: Due on Sunday, Dec. 5, 2021 - 11:59 pm (US CST)

When you submit your homework, to help us grade and identify your work, you need to comply with the following guidelines carefully:

- **Have a cover page** for each document (e.g. homework, project, report, etc.) that you submit. A sample of cover page is provided in the course webpage. This page must include: (1) your name as it appears in your **student ID card**, (2) course name/number, (3) homework/project number, and (4) the **Statement of Academic Honesty** that you sign.

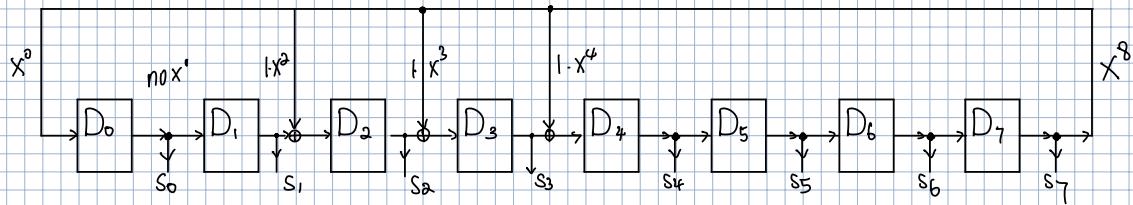
1. Chapter 12: 1, 8, 13, 22, 24, 25.
2. Show the circuits of the following six 8-bit designs using the primitive polynomial $x^8 + x^4 + x^3 + x^2 + 1$: [1] Internal-XOR LFSR, [2] External-XOR LFSR, [3] complete LFSR (that produces also zero-state), [4] weighted LFSR (that produces weights of 0.875, 0.75, 0.625, 0.5, 0.375, 0.25, 0.125), [5] MISR and [6] BILBO. In a table summarize their characteristics in terms of estimate of cost, delay, etc.
3. Simulate circuit [2] above and show the first 16 pseudo-random patterns generated assuming the initial value of LFSR is all-1. You can use Synopsys or matrix/vector MOD 2 calculations (hand-driven or a short script/program). Explain your approach and include the details.
4. Consider the circuit under test (CUT) is a 4-bit unsigned multiplier unit that receives $X = x_3x_2x_1x_0$ and $Y = y_3y_2y_1y_0$ as inputs and produces $Z = z_7z_6z_5z_4z_3z_2z_1z_0$ as outputs such that $Z = X * Y$. For uniformity, assume that $x_3x_2x_1x_0$ and $y_3y_2y_1y_0$ are connected in order to $e_7e_6e_5e_4e_3e_2e_1e_0$ the outputs of 8-bit LFSR, respectively. Similarly, assume that eight outputs $z_7z_6z_5z_4z_3z_2z_1z_0$ are connected in order to $d_7d_6d_5d_4d_3d_2d_1d_0$ of the 8-bit MISR (circuit [5] above), respectively.

Suppose the first 16 pseudo-random patterns that you found in previous part are used to test the CUT. Find the fault-free 8-bit signature assuming the initial value of MISR is all-0.

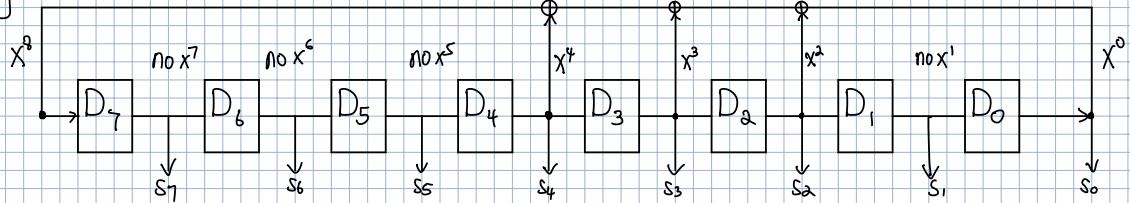
Note: You need to first apply 16 8-bit patterns to the CUT and find 16 8-bit outputs. Then, find the result of compacting the outputs using the MISR. The final signature will be 8-bit content of MISR at the end. You can find this using either an implementation in Synopsys or matrix/vector MOD 2 calculations (hand-driven or a short script/program). Explain your approach and include the details.

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 [1] Internal-XOR LFSR, [2] External-XOR LFSR, [3] complete LFSR (that produces also zero-state), [4] weighted LFSR (that produces weights of 0.875, 0.75, 0.625, 0.5, 0.375, 0.25, 0.125), [5] MISR and [6] BILBO. In a table summarize their characteristics in terms of estimate of cost, delay, etc.

[1]



[2]

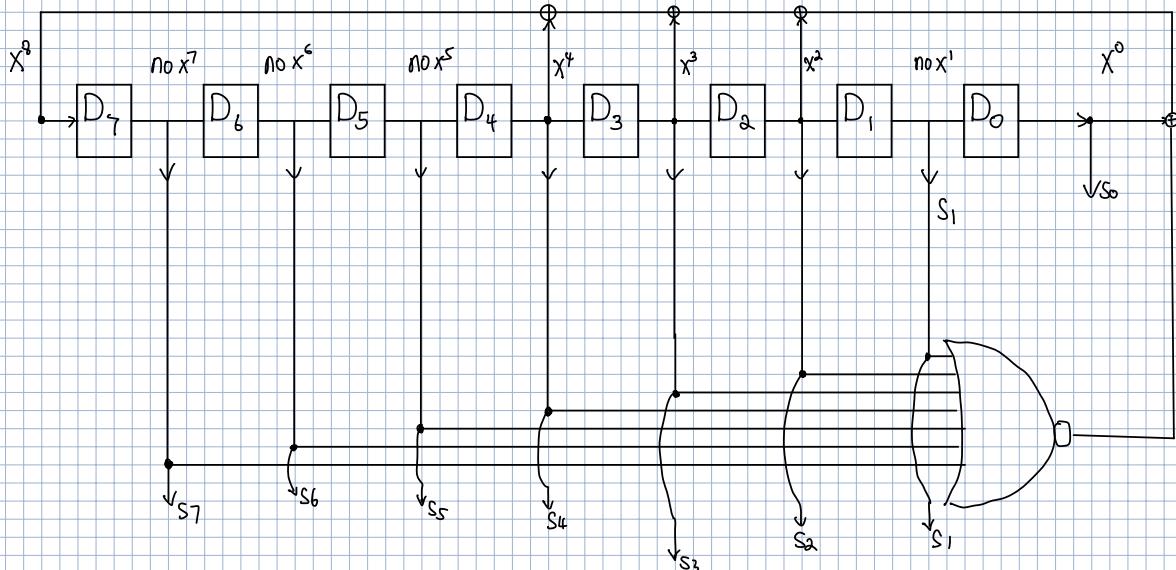


Trans Matrix:

$$\begin{bmatrix} 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \end{bmatrix}$$

$\Psi_0 \Psi_1 \Psi_2 \Psi_3 \Psi_4 \Psi_5 \Psi_6 \Psi_7$

[3] assuming Standard CFSR

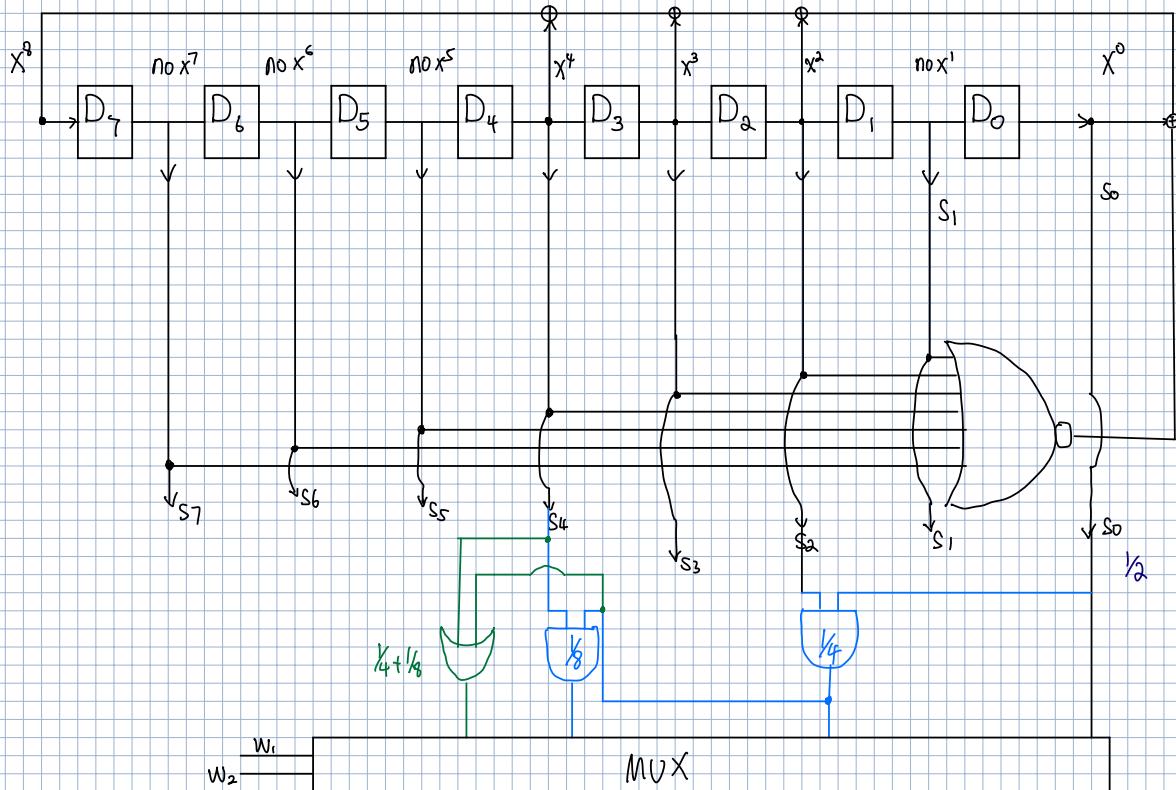


[4]

$$0.875, 0.75, 0.625, 0.5, 0.375, 0.25, 0.125,$$

$$\frac{1}{8}, \frac{3}{8}, \frac{5}{8}, \frac{1}{2}, \frac{3}{4}, \frac{1}{4}, \frac{1}{8}$$

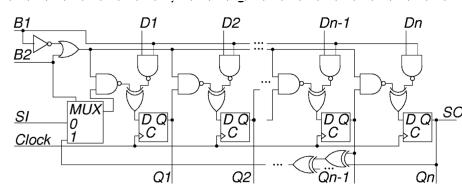
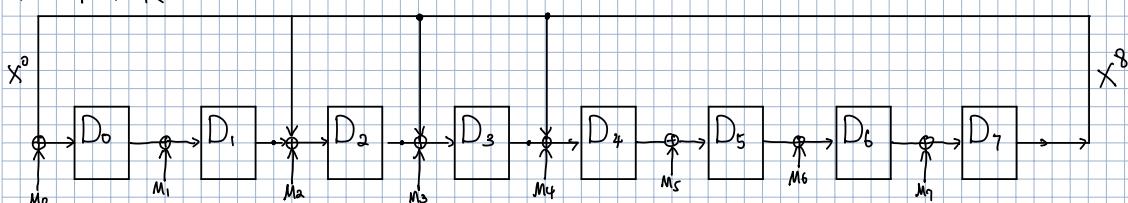
$$\frac{1}{8} + \frac{1}{4}$$

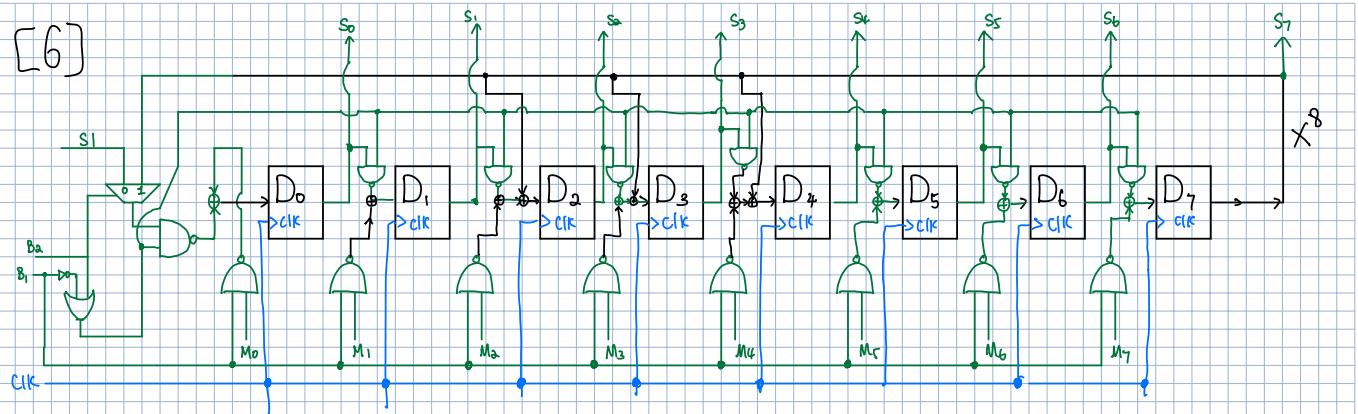


\$W_1\$	\$W_2\$	INV	\$P(\text{out})\$
0	0	0	\$\frac{1}{2} (0.5)\$
0	0	1	\$\frac{1}{2} (0.5)\$
0	1	0	\$\frac{1}{4} (0.25)\$
0	1	1	\$\frac{3}{4} (0.75)\$
1	0	0	\$\frac{1}{8} (0.125)\$
1	0	1	\$\frac{7}{8} (0.875)\$
1	1	0	\$\frac{1}{8} + \frac{1}{4} = \frac{3}{8} (0.375)\$
1	1	1	\$\frac{5}{8} (0.625)\$



[5] MISR





TYPE	function	COST	delay
Internal XOR LFSR	pattern generation	Reduce testing & maintenance cost.	Small performance delay due to overhead
External XOR LFSR	pattern generation	Generate repeatable test if same seed is used. No repeat patterns consecutively	
Complete LFSR	pattern generation	adds NOR gates to cost to accommodate all '0' pattern	Additional gates lengthen the delay of pattern generation
Weighted LFSR	pattern generation	Controls the amount of 1 adds MUX, AND, and XOR gates to cost	Based on the complete LFSR, extra delay to control amount of 0/1 in test pattern
MISR	Compaction	Use to Reduce the amount of response generated by patterns so it's handleable on chip bring down chip cost	Reduce time to test all response of generated patterns at a cost of a small missing rate
BILBO	Register, Scan In, pattern generation Compaction	Reuse preexisting hardware for LFSR/ Compaction to Reduce Redundancy of hardware onchip, adds cost on some MUX and AND gates	Brought in Modes to use the repeated component in the hardware.

3. C code submitted

Approach:

1. Define the transition matrix as a 2d array and input the matrix in the code
2. Define iterations of patterns
3. Input initial value (seed)
4. Have result matrix and previous value matrix to hold concurrent result and previous result, respectively .
5. The program will Convert patterns of 1 and 0 into decimal and multiply them when the value is reconstructed.

4. Consider the circuit under test (CUT) as a 4-bit unsigned multiplier unit that receives $X = x_3x_2x_1x_0$ and $Y = y_3y_2y_1y_0$ as inputs and produces $Z = z_7z_6z_5z_4z_3z_2z_1z_0$ as outputs such that $Z = X \cdot Y$. For uniformity, assume that $x_3x_2x_1x_0$ and $y_3y_2y_1y_0$ are connected in order to $e_7e_6e_5e_4e_3e_2e_1e_0$ the outputs of 8-bit LFSR, respectively. Similarly, assume that eight outputs $z_7z_6z_5z_4z_3z_2z_1z_0$ are connected in order to $d_7d_6d_5d_4d_3d_2d_1d_0$ of the 8-bit MISR (circuit [5] above), respectively.

Suppose the first 16 pseudo-random patterns that you found in previous part are used to test the CUT. Find the fault-free 8-bit signature assuming the initial value of MISR is all-0.

Note: You need to first apply 16 8-bit patterns to the CUT and find 16 8-bit outputs. Then, find the result of compacting the outputs using the MISR. The final signature will be 8-bit content of MISR at the end. You can find this using either an implementation in Synopsys or matrix/vector MOD 2 calculations (hand-driven or a short script/program). Explain your approach and include the details.

X	Y	Z	76343210 01101001	Signature 0110001
7	15	105	0010 1101	0010 1101
3	15	45	0000 1111	0000 1111
1	15	15	0000 0000	0000 0000
0	15	0	0000 0000	0000 0000
0	7	0	0000 0000	0000 0000
0	3	0	0000 0000	0000 0000
8	1	8	0000 1000	0000 1000
12	0	0	0000 0000	0000 0000
6	0	0	0000 0000	0000 0000
3	0	0	0000 0000	0000 0000
9	8	72	0100 1010	0100 1000
4	12	48	0011 0000	0011 0000
2	6	12	0000 1100	0000 1100
9	3	27	0001 1011	0001 1011
4	9	36	0010 0100	0010 0100
2	4	8	0000 1000	0000 1000

$$\begin{array}{r}
 \overbrace{\quad\quad\quad}^0 \\
 x^8 + x^4 + x^2 + x^2 + 1) \overbrace{x^6 + x^5 + x^3 + 1}^0 \\
 \hline
 \overbrace{\quad\quad\quad}^0 \\
 x^6 + x^5 + x^3 + 1 \\
 \hline
 \overbrace{\quad\quad\quad}^0 \\
 x^8 + x^4 + x^2 + x^2 + 1) \overbrace{x^5 + x^3 + x^2 + 1}^0 \\
 \hline
 \overbrace{\quad\quad\quad}^0 \\
 x^5 - x^3 + x^2 + 1
 \end{array}$$

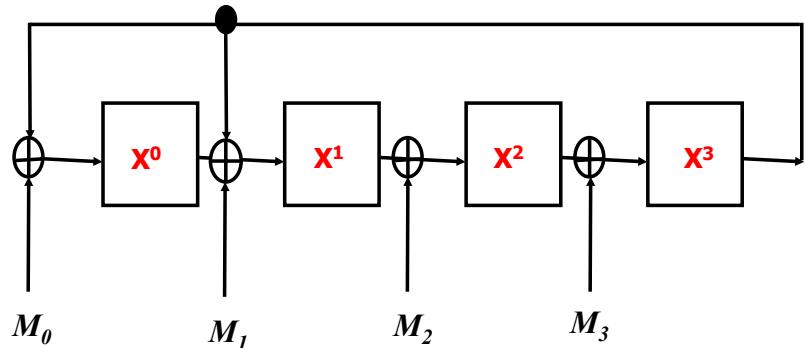
\therefore The result has 8 bits, highest possible order in polynomial is X^7 .

\therefore Quotient = 0

\therefore Remainder = result

$\therefore \text{Signature} = \text{result}$.

MISR Division Example



$$\begin{array}{r} x^3 + x^2 \\ \hline x^4 + x + 1 \quad \left[\begin{array}{ccc} x^7 + x^6 & + x^4 + x^3 & + x^0 \\ x^7 & + x^4 + x^3 \\ \hline \end{array} \right] \\ \hline x^6 & & + x^0 \\ x^6 & + x^3 + x^2 \\ \hline x^3 + x^2 & + x^0 \end{array}$$

Remainder = Signature = $x^0 \ x^1 \ x^2 \ x^3 = 1 \ 0 \ 1 \ 1$

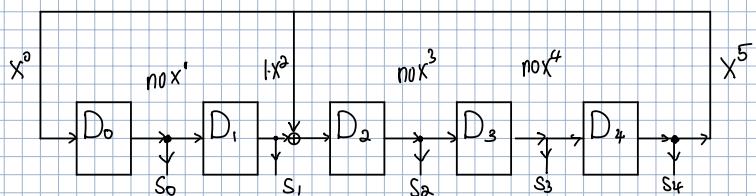
12.1 Draw an internal-XOR LFSR with feedback polynomial $\phi(x) = x^5 + x^2 + 1$.

Simulate the LFSR and obtain the sequence generated at the output of the last

stage of the LFSR, s_4 . Use the generating function of the LFSR (Equation (12.4))

to also derive the sequence generated at s_4 . Are the two sequences identical?

$$\text{Matrix Relation: } \begin{bmatrix} S_0(t+1) \\ S_1(t+1) \\ S_2(t+1) \\ S_3(t+1) \\ S_4(t+1) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} S_0(t) \\ S_1(t) \\ S_2(t) \\ S_3(t) \\ S_4(t) \end{bmatrix}$$



Sequence:

S_0	0	1	0	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	0	0	0	
S_1	0	0	1	0	0	1	0	1	0	0	1	1	0	6	0	1	1	1	0	1	0	0
S_2	0	1	0	1	1	0	0	1	1	1	1	0	0	0	1	0	1	0	1	0	0	0
S_3	0	0	1	0	1	1	0	0	1	1	1	1	0	0	0	1	0	1	1	0	1	0
S_4	1	0	0	1	0	1	1	0	0	1	1	1	1	0	0	0	1	0	1	0	1	0

$$G_4(x) = \frac{1}{x^5(x^4+x^2+1)}$$

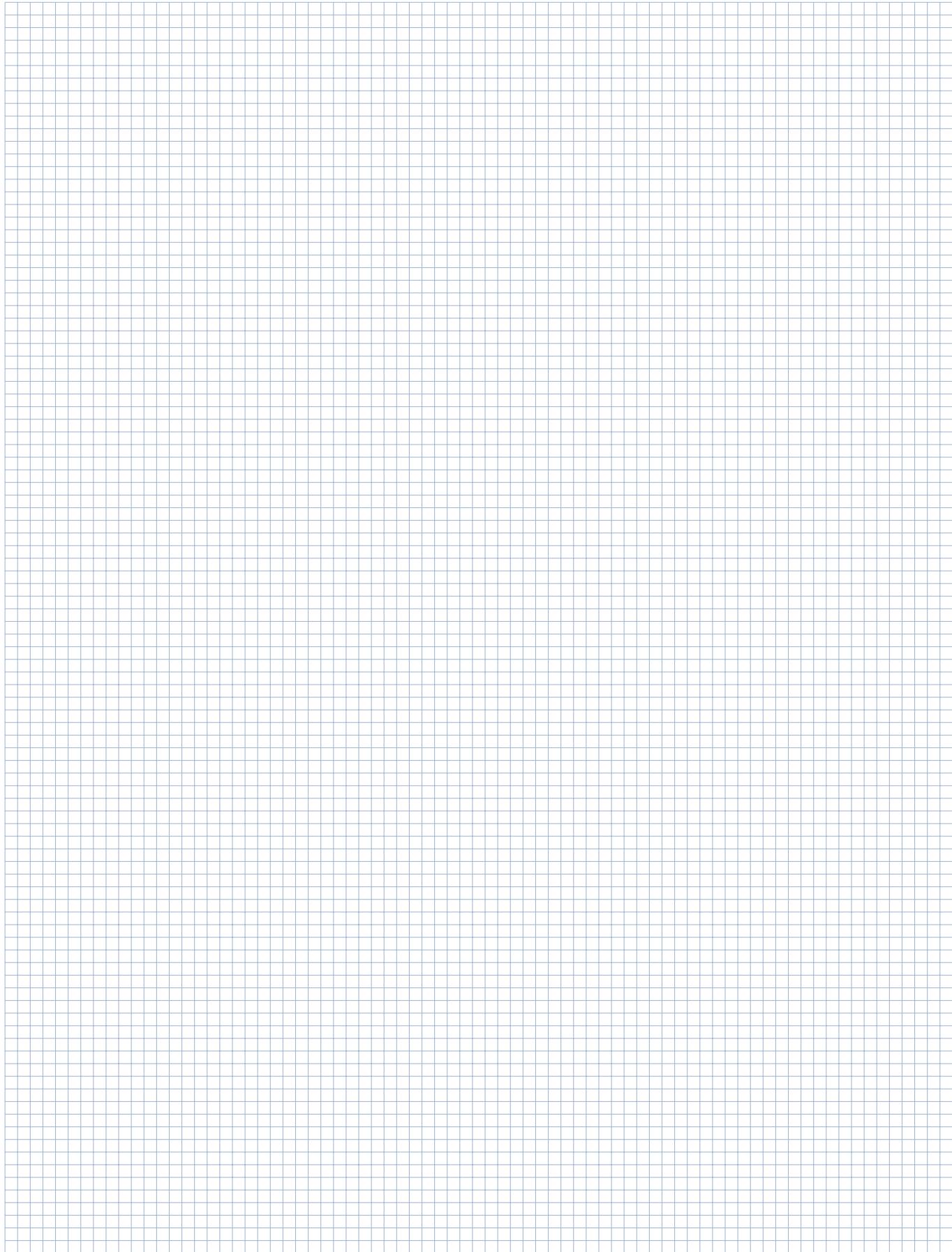
$$= \frac{1}{x^9+x^7+x^4}$$

begin:

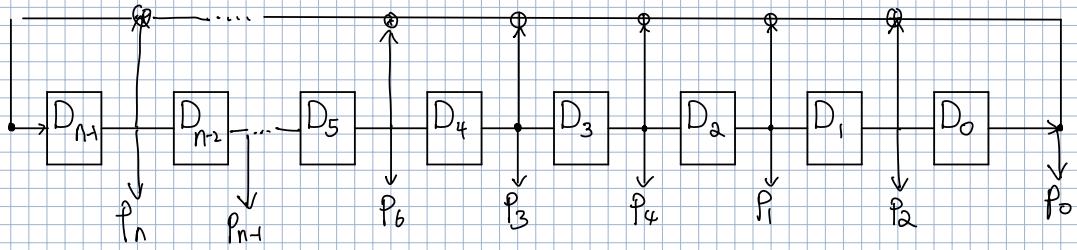
$$\begin{array}{r} x^5 + x^3 + 1 \\ x^4) x^9 + x^7 + x^4 \\ \underline{x^9} \\ x^7 + x^4 \\ \underline{x^7} \\ x^4 \\ \underline{x^4} \\ 0 \end{array}$$

$$G_3(x) = \frac{1}{x^4(x^4+x^2+1)}$$

$$= \frac{1}{x^8+x^6+x^3}$$



- parameter, and (b) serial.
- 12.8 Modify the design of an n -stage external-XOR ML-LFSR to enable it to generate a complete set of n -bit PTVs.



12.13 Estimate probabilistic controllabilities and observability for each line in the circuit shown in Figure 4.24(a) using the circuit traversal approach. Use the above values to obtain an estimate of the detectability profile for this circuit.

$$CC_p^o(c_3) = 0.25 \checkmark$$

$$CC_p^o(c_5) = 0.75$$

$$CC_p^o(c_4) = 0.75$$

$$CC_p^o(c_6) = 0.25$$

$$CC_p^o(c_7) = 0.375$$

$$CC_p^o(c_8) = 0.625$$

$$CC_p^o(c_9) = 0.625 \checkmark$$

$$CC_p^o(c_{10}) = 0.375$$

$$CC_p^o(c_1) = \max(0.5 \times 0.375, 0.5 \times 0.625) = 0.3125$$

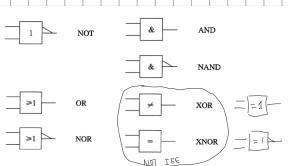
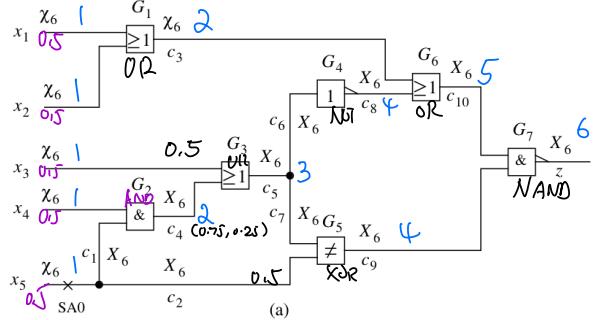
$$CC_p^o(c_2) = 0.3125$$

$$CC_p^o(c_3) = 0.10625$$

$$CC_p^o(c_4) = 0.94375$$

$$CC_p^o(z) = 0.263671875$$

$$CC_p^o(c_5) = 0.736328125$$



$$O_p(z) = 1.0$$

$$O_p(c_{10}) = 1.0 \times 0.94375 = 0.94375$$

$$O_p(c_9) = 1.0 \times 0.3125 = 0.3125$$

$$O_p(c_8) = 0.375$$

12.22 Modify the compressor design shown in Figure 12.22 to enable the counting of only the $0 \rightarrow 1$ transitions in the response sequence.

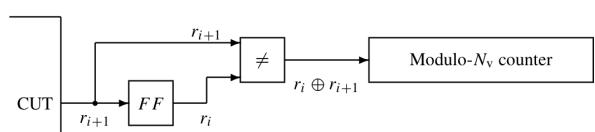
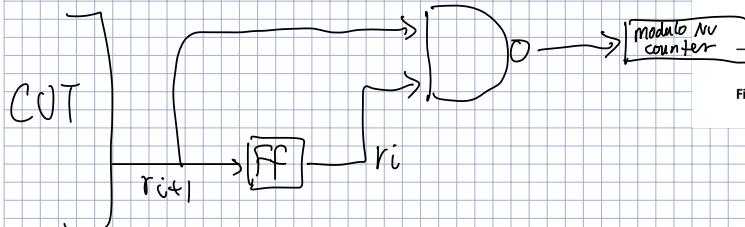


Figure 12.22 A transition count compressor

a transition count compressor?

- 12.24 An LFSR compressor with feedback polynomial $\phi(x) = x^4 + x^3 + 1$ is used to compress the CUT response $Res = r_7, r_6, r_5, r_4, r_3, r_2, r_1 = \{1, 1, 1, 0, 1, 0, 0\}$, i.e., $Res(x) = x^6 + x^4 + x^2 + x + 1$. Use polynomial division to compute the value of the signature obtained by using the above compression. Verify by simulating the LFSR compression.

$$\begin{array}{r} x^2 + x \\ \overline{x^4 + x^3 + 1)} \quad \overline{x^6 + x^4 + x^2 + x + 1} \\ x^6 + x^5 + x^2 \\ \hline -x^5 + x^4 + x + 1 \\ x^5 + x^4 + x \\ \hline \end{array}$$

|

$\therefore \quad r_1 = 000001 \neq 11010$

\therefore The response was faulty.

- 12.25 An m -output circuit is tested using a sequence of N_v vectors and its response compressed using an m -stage MISR compressor. Compute the number of possible error sequences that map to the all-zero equivalent LFSR error sequence.

$$m\text{-output circuit} : L = m \times N_v$$

$$\text{possible error sequence} = 2^{(mN_v - m)} - 1$$