For circuit 3.23, The schematic of which the VHDL represents can be seen in Figure 1. The VHDL code can be found in the 323 folder.

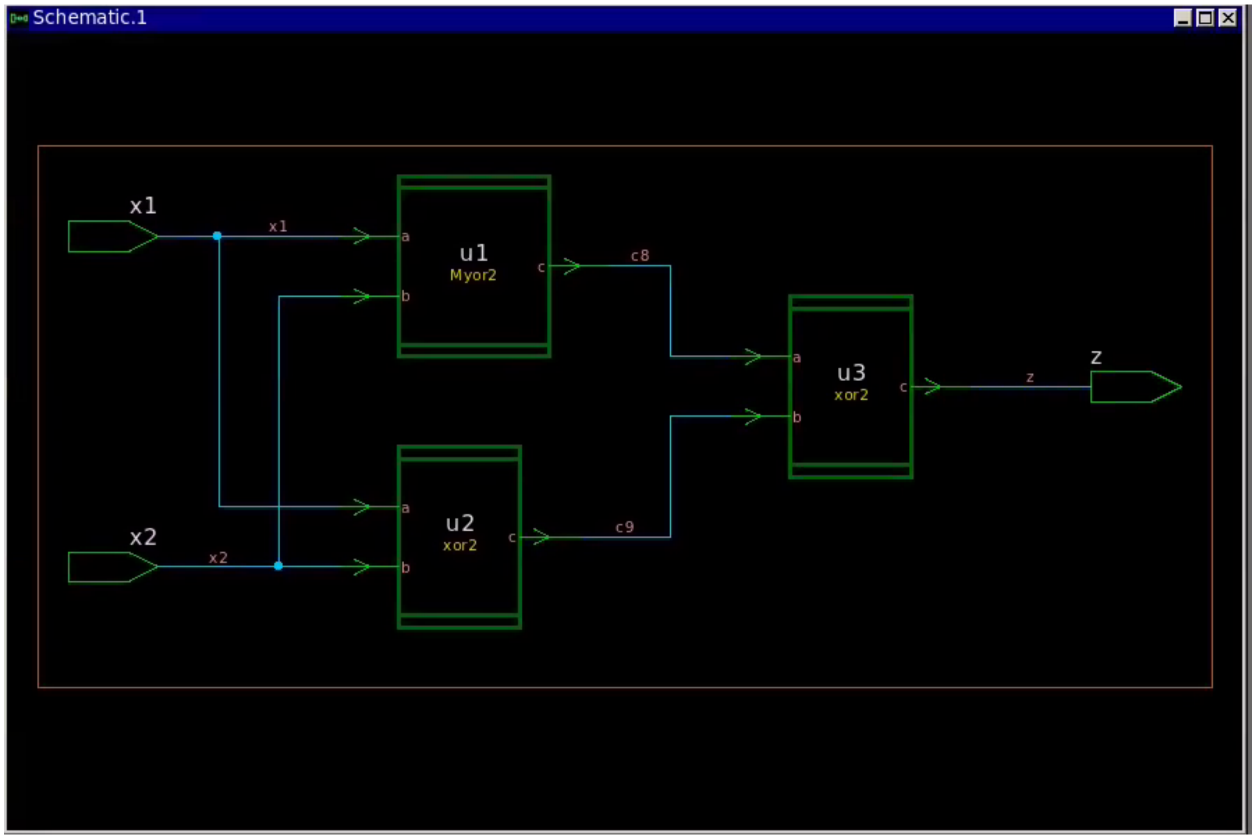


Figure 1 Schematic of circuit 3.23

Simulation waveform presented in Figure 2 shows that it functions the same as circuit 3.23.

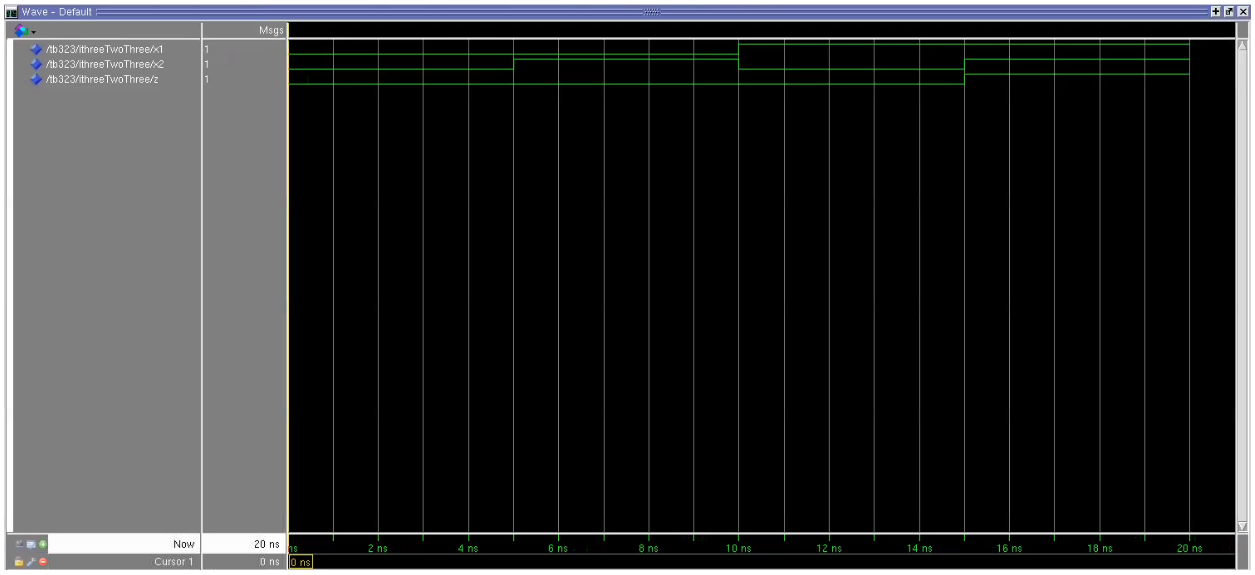


Figure 2 Waveform of VHDL Simulation

The synthesis result, which reports the timing and area, can be found in the threeTwoThree.report in 323 folder. The post-synthesis VHDL code can be found in the folder as well.

After importing the VHDL into TetraMax, shown in Figure 3, and build the ATPG model followed by the design rule check using the tool, one can see the schematic shown in TetraMax remains the same as Figure 1.

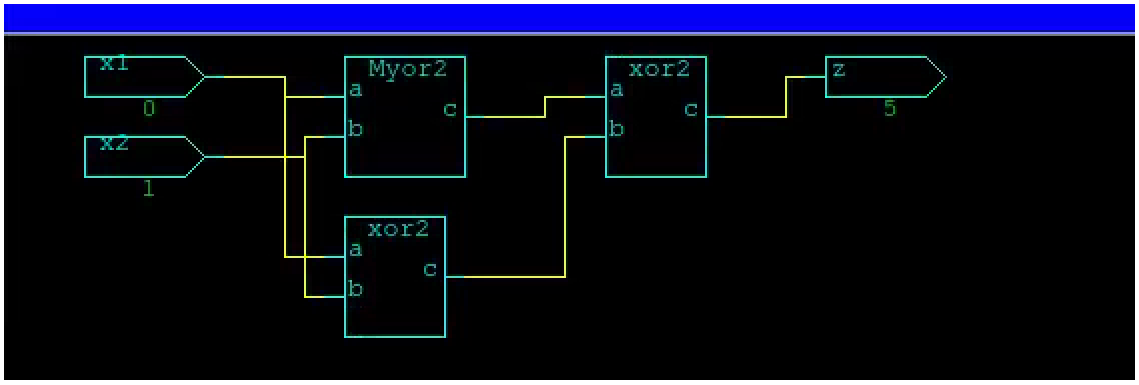
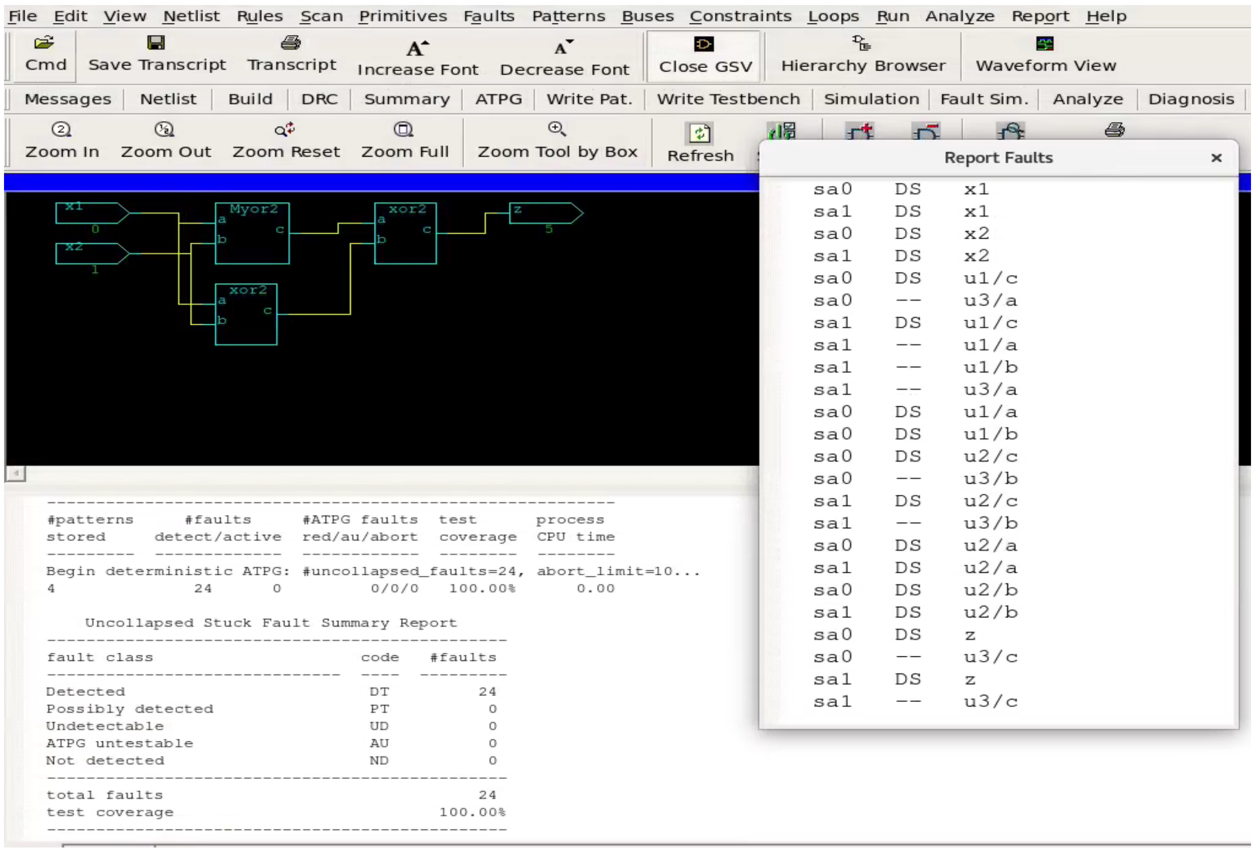


Figure 3 Schematic of 3.23 in TetraMax

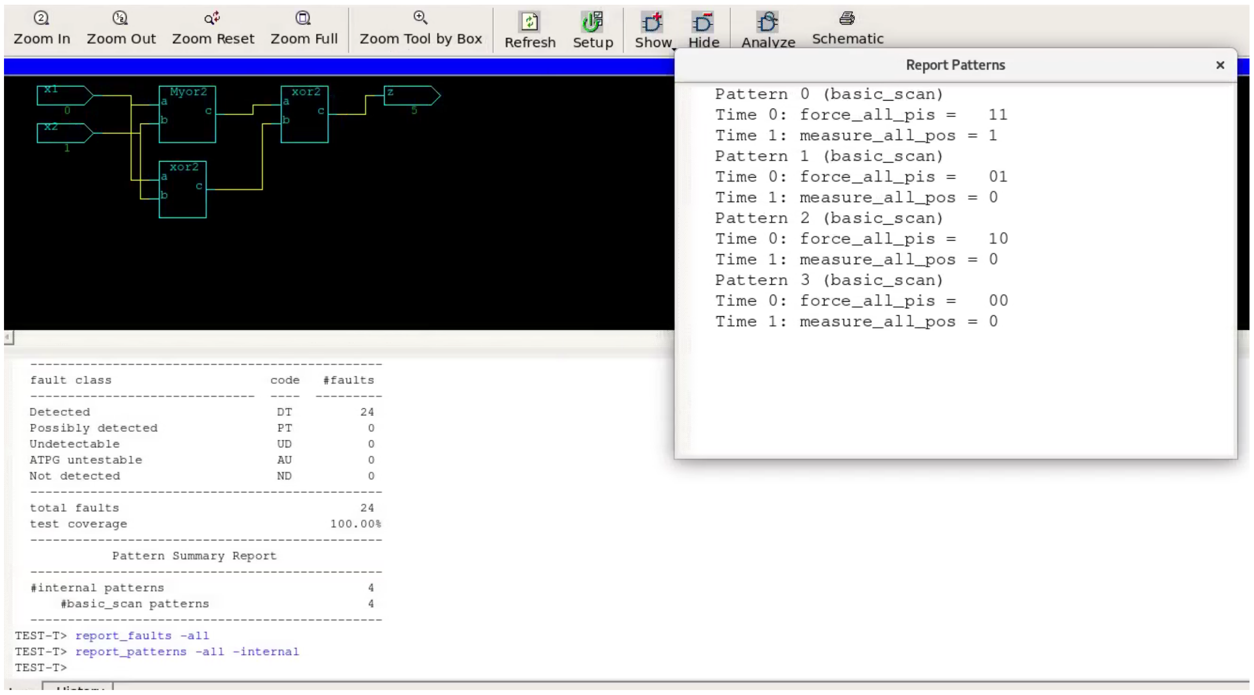
All faults were able to be detected using ATPG. Since TetraMax sees faults on the same wire as different ones, 24 faults were detected before collapsing. Figure 4 shows the faults found, and Figure 5 shows the patterns used.



```
-------------------------------------------------------
#patterns     #faults     #ATPG faults  test      process
stored      detect/active  red/au/abort  coverage  CPU time
---------   -------------  ------------  --------  --------
Begin deterministic ATPG: #uncollapsed_faults=24, abort_limit=10...
4               24      0       0/0/0     100.00%      0.00

    Uncollapsed Stuck Fault Summary Report
-----------------------------------------------
fault class                    code    #faults
------------------------------ ----  ---------
Detected                        DT         24
Possibly detected               PT          0
Undetectable                    UD          0
ATPG untestable                 AU          0
Not detected                    ND          0
-----------------------------------------------
total faults                               24
test coverage                         100.00%
-----------------------------------------------
```

```
sa0   DS   x1
sa1   DS   x1
sa0   DS   x2
sa1   DS   x2
sa0   DS   u1/c
sa0   --   u3/a
sa1   DS   u1/c
sa1   --   u1/a
sa1   --   u1/b
sa1   --   u3/a
sa0   DS   u1/a
sa0   DS   u1/b
sa0   DS   u2/c
sa0   --   u3/b
sa1   DS   u2/c
sa1   --   u3/b
sa0   DS   u2/a
sa1   DS   u2/a
sa0   DS   u2/b
sa1   DS   u2/b
sa0   DS   z
sa0   --   u3/c
sa1   DS   z
sa1   --   u3/c
```

Figure 4 Faults in circuit 3.23



```
Pattern 0 (basic_scan)
Time 0: force_all_pis =   11
Time 1: measure_all_pos = 1
Pattern 1 (basic_scan)
Time 0: force_all_pis =   01
Time 1: measure_all_pos = 0
Pattern 2 (basic_scan)
Time 0: force_all_pis =   10
Time 1: measure_all_pos = 0
Pattern 3 (basic_scan)
Time 0: force_all_pis =   00
Time 1: measure_all_pos = 0
```

```
 -----------------------------------------------
 fault class                     code   #faults
 ------------------------------  ----  ---------
 Detected                         DT         24
 Possibly detected                PT          0
 Undetectable                     UD          0
 ATPG untestable                  AU          0
 Not detected                     ND          0
 -----------------------------------------------
 total faults                                24
 test coverage                          100.00%
 -----------------------------------------------
            Pattern Summary Report
 -----------------------------------------------
 #internal patterns                           4
     #basic_scan patterns                     4
 -----------------------------------------------
TEST-T> report_faults -all
TEST-T> report_patterns -all -internal
TEST-T>
```

Figure 5 Patterns used in finding faults

As can be seen, the patterns used to test faults are the same as the hand-work analysis. The reason of discrepancy in fault count is fault collapsing using fault equivalence and fault dominance theory reduces the need to repeatedly examine faults that do not provide new knowledge.

For circuit 3.28, The schematic of which the VHDL represents can be seen in Figure 7. The VHDL code can be found in the folder named 328. Figure 6 shows the simulation waveform, proving its correct functionality.

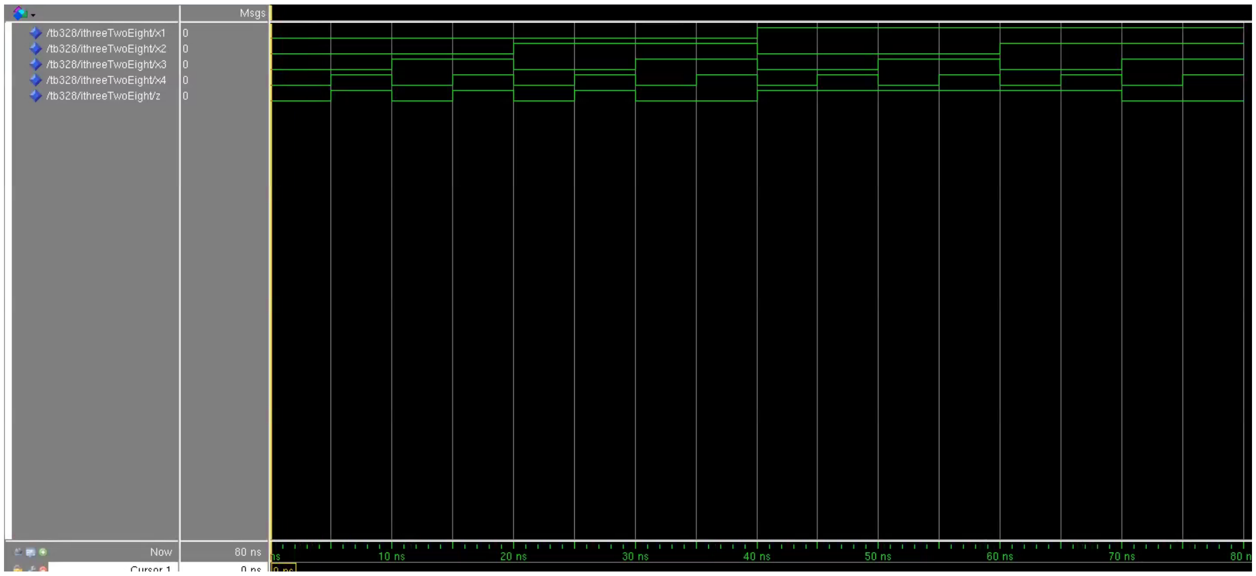
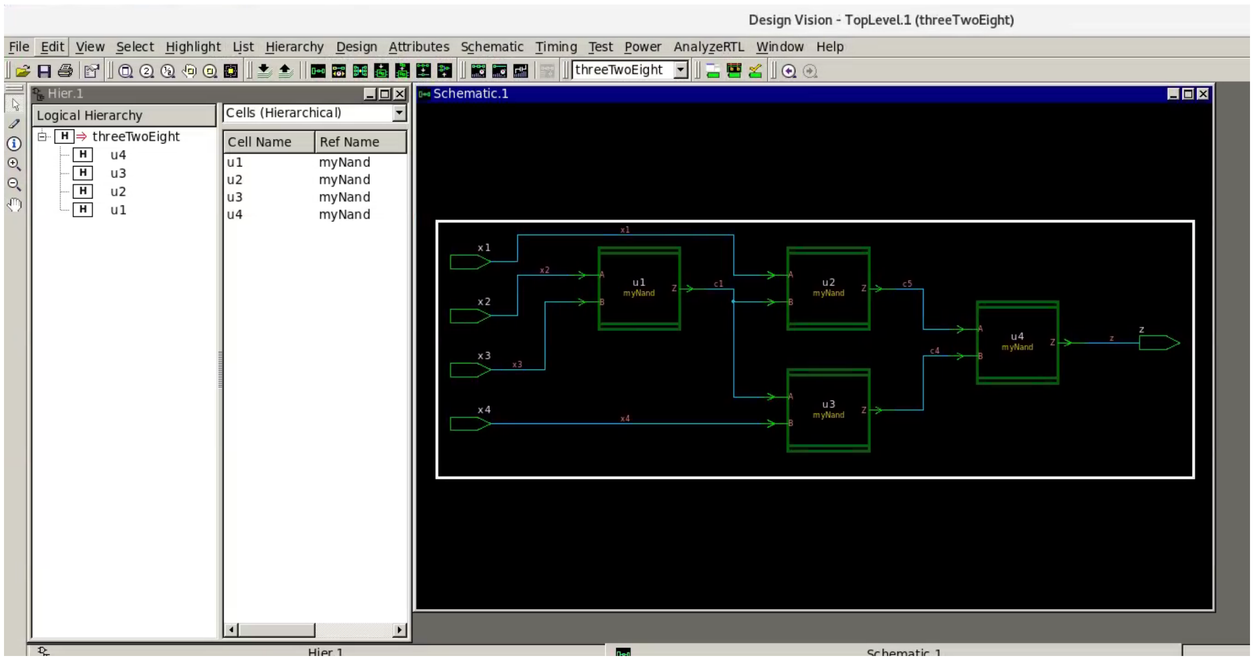


Figure 6 Waveform of Circuit 3.28

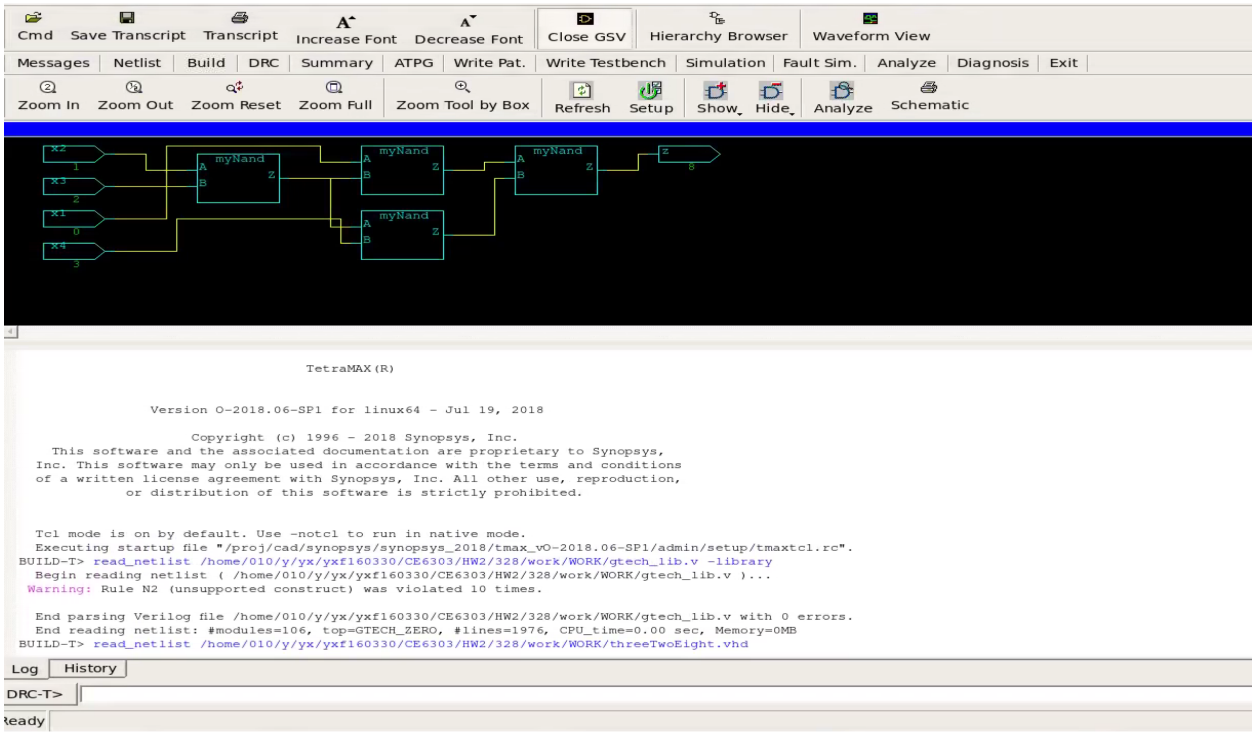

Design Vision - TopLevel.1 (threeTwoEight)
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window Help
threeTwoEight
Hier.1
Logical Hierarchy
threeTwoEight
u4
u3
u2
u1
Cells (Hierarchical)
Schematic.1
x1
x2
x3
x4
u1 myNand
u2 myNand
u3 myNand
u4 myNand
c1
c5
c4
z
Hier.1
Schematic.1

Cell Name	Ref Name
u1	myNand
u2	myNand
u3	myNand
u4	myNand

Figure 7 Schematic view of Circuit 3.28

The synthesis result, which reports the timing and area, can be found in the threeTwoEight.report in 328 folder. The post-synthesis VHDL code can be found in the folder as well.

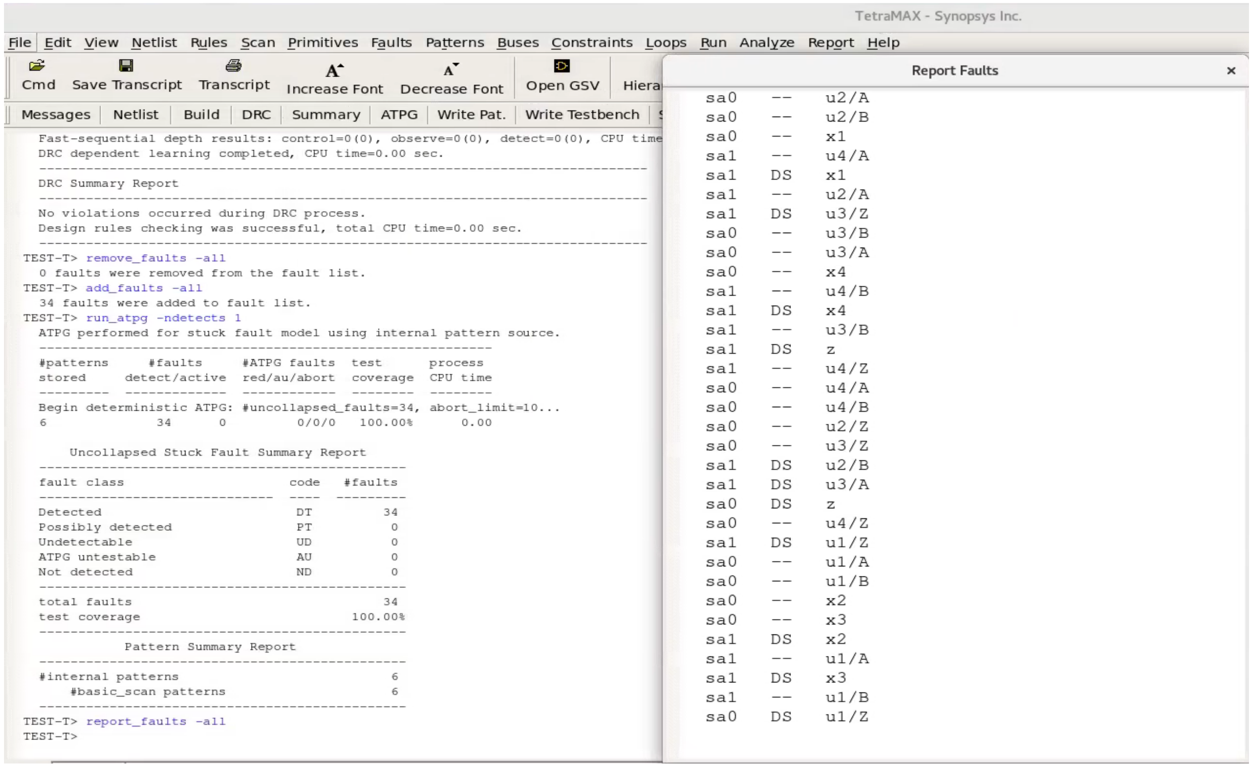
After importing into TetraMax, and have ATPG model built followed by design rule checked, the same the schematic in Figure 8, presented by TetraMax, matches that of Figure 7.



```
                         TetraMAX(R)


            Version O-2018.06-SP1 for linux64 - Jul 19, 2018

                 Copyright (c) 1996 - 2018 Synopsys, Inc.
   This software and the associated documentation are proprietary to Synopsys,
  Inc. This software may only be used in accordance with the terms and conditions
  of a written license agreement with Synopsys, Inc. All other use, reproduction,
             or distribution of this software is strictly prohibited.


  Tcl mode is on by default. Use -notcl to run in native mode.
  Executing startup file "/proj/cad/synopsys/synopsys_2018/tmax_vO-2018.06-SP1/admin/setup/tmaxtcl.rc".
BUILD-T> read_netlist /home/010/y/yx/yxf160330/CE6303/HW2/328/work/WORK/gtech_lib.v -library
  Begin reading netlist ( /home/010/y/yx/yxf160330/CE6303/HW2/328/work/WORK/gtech_lib.v )...
 Warning: Rule N2 (unsupported construct) was violated 10 times.

  End parsing Verilog file /home/010/y/yx/yxf160330/CE6303/HW2/328/work/WORK/gtech_lib.v with 0 errors.
  End reading netlist: #modules=106, top=GTECH_ZERO, #lines=1976, CPU_time=0.00 sec, Memory=0MB
BUILD-T> read_netlist /home/010/y/yx/yxf160330/CE6303/HW2/328/work/WORK/threeTwoEight.vhd
```

Figure 8 Schematic presented in TetraMax for Circuit 3.28

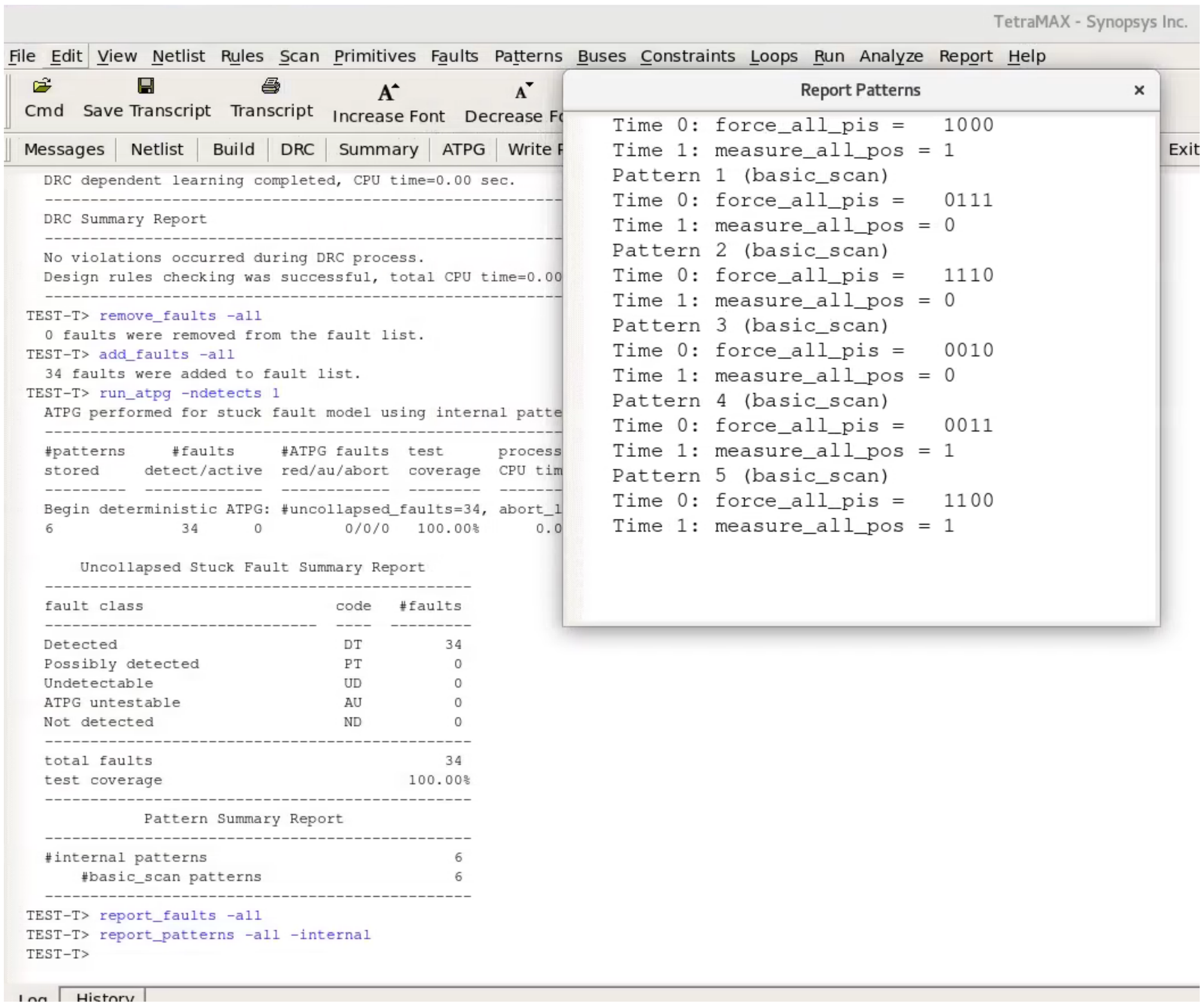
Thus, after running ATPG, faults can be reported as seen in Figure 9 and patterns used are reported in Figure 10.



```
  Fast-sequential depth results: control=0(0), observe=0(0), detect=0(0), CPU time
  DRC dependent learning completed, CPU time=0.00 sec.
  -----------------------------------------------------------------------------
  DRC Summary Report
  -----------------------------------------------------------------------------
  No violations occurred during DRC process.
  Design rules checking was successful, total CPU time=0.00 sec.
  -----------------------------------------------------------------------------
TEST-T> remove_faults -all
  0 faults were removed from the fault list.
TEST-T> add_faults -all
  34 faults were added to fault list.
TEST-T> run_atpg -ndetects 1
  ATPG performed for stuck fault model using internal pattern source.
  ----------------------------------------------------------
  #patterns     #faults     #ATPG faults  test      process
  stored     detect/active  red/au/abort  coverage  CPU time
  ---------  ------------- ------------  --------  --------
  Begin deterministic ATPG: #uncollapsed_faults=34, abort_limit=10...
  6              34      0        0/0/0   100.00%      0.00

      Uncollapsed Stuck Fault Summary Report
  -----------------------------------------------
  fault class                     code   #faults
  ------------------------------  ----  ---------
  Detected                         DT         34
  Possibly detected                PT          0
  Undetectable                     UD          0
  ATPG untestable                  AU          0
  Not detected                     ND          0
  -----------------------------------------------
  total faults                                34
  test coverage                          100.00%
  -----------------------------------------------
             Pattern Summary Report
  -----------------------------------------------
  #internal patterns                           6
      #basic_scan patterns                     6
  -----------------------------------------------
TEST-T> report_faults -all
TEST-T>
```

```
sa0   --   u2/A
sa0   --   u2/B
sa0   --   x1
sa1   --   u4/A
sa1   DS   x1
sa1   --   u2/A
sa1   DS   u3/Z
sa0   --   u3/B
sa0   --   u3/A
sa0   --   x4
sa1   --   u4/B
sa1   DS   x4
sa1   --   u3/B
sa1   DS   z
sa1   --   u4/Z
sa0   --   u4/A
sa0   --   u4/B
sa0   --   u2/Z
sa0   --   u3/Z
sa1   DS   u2/B
sa1   DS   u3/A
sa0   DS   z
sa0   --   u4/Z
sa1   DS   u1/Z
sa0   --   u1/A
sa0   --   u1/B
sa0   --   x2
sa0   --   x3
sa1   DS   x2
sa1   --   u1/A
sa1   DS   x3
sa1   --   u1/B
sa0   DS   u1/Z
```

Figure 9 Faults Report for 3.28


TetraMAX - Synopsys Inc.
File Edit View Netlist Rules Scan Primitives Faults Patterns Buses Constraints Loops Run Analyze Report Help
Cmd Save Transcript Transcript Increase Font Decrease Fo
Messages Netlist Build DRC Summary ATPG Write F Exit
Report Patterns
Log History

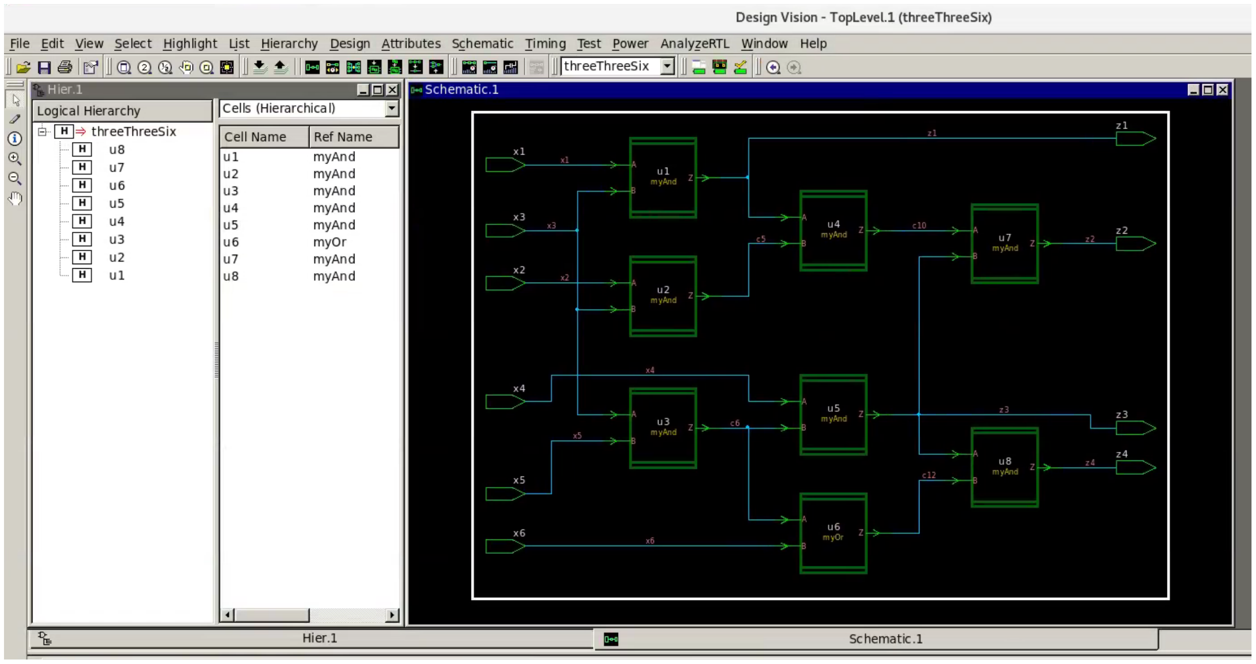
```
  DRC dependent learning completed, CPU time=0.00 sec.
  -------------------------------------------------------
  DRC Summary Report
  -------------------------------------------------------
  No violations occurred during DRC process.
  Design rules checking was successful, total CPU time=0.00
  -------------------------------------------------------
TEST-T> remove_faults -all
  0 faults were removed from the fault list.
TEST-T> add_faults -all
  34 faults were added to fault list.
TEST-T> run_atpg -ndetects 1
  ATPG performed for stuck fault model using internal patte
  -------------------------------------------------------
  #patterns     #faults      #ATPG faults  test      process
  stored     detect/active  red/au/abort  coverage  CPU tim
  ---------  -------------  ------------  --------  -------
  Begin deterministic ATPG: #uncollapsed_faults=34, abort_l
  6              34      0         0/0/0   100.00%      0.0

      Uncollapsed Stuck Fault Summary Report
  -----------------------------------------------
  fault class                     code   #faults
  ------------------------------  ----  ---------
  Detected                         DT         34
  Possibly detected                PT          0
  Undetectable                     UD          0
  ATPG untestable                  AU          0
  Not detected                     ND          0
  -----------------------------------------------
  total faults                                34
  test coverage                          100.00%
  -----------------------------------------------
             Pattern Summary Report
  -----------------------------------------------
  #internal patterns                           6
      #basic_scan patterns                     6
  -----------------------------------------------
TEST-T> report_faults -all
TEST-T> report_patterns -all -internal
TEST-T>
```

```
Time 0: force_all_pis =   1000
Time 1: measure_all_pos = 1
Pattern 1 (basic_scan)
Time 0: force_all_pis =   0111
Time 1: measure_all_pos = 0
Pattern 2 (basic_scan)
Time 0: force_all_pis =   1110
Time 1: measure_all_pos = 0
Pattern 3 (basic_scan)
Time 0: force_all_pis =   0010
Time 1: measure_all_pos = 0
Pattern 4 (basic_scan)
Time 0: force_all_pis =   0011
Time 1: measure_all_pos = 1
Pattern 5 (basic_scan)
Time 0: force_all_pis =   1100
Time 1: measure_all_pos = 1
```

Figure 10 Pattern Report for 3.28

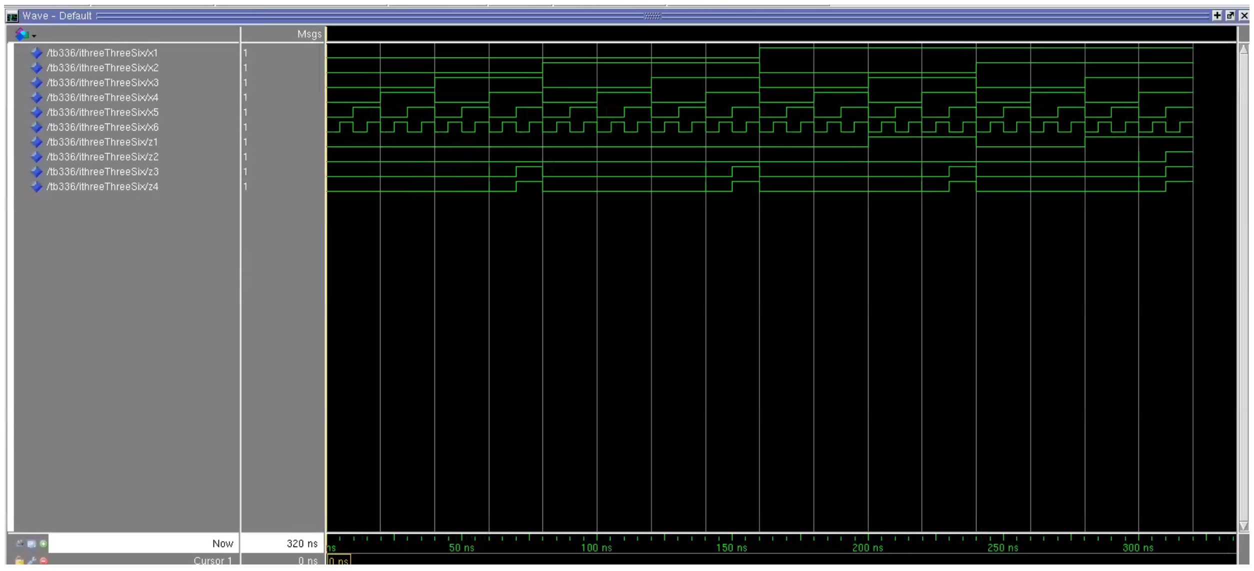
Due to the usage of fault collapsing and critical path tracing, hand-work uses less pattern to detect all faults than TetraMax, and less faults need to be analysed.

For circuit 3.36, The schematic of which the VHDL represents can be seen in Figure 11. The VHDL code can be found in the folder named 336. Figure 12 shows the simulation waveform, proving its correct functionality.



Cell Name	Ref Name
u1	myAnd
u2	myAnd
u3	myAnd
u4	myAnd
u5	myAnd
u6	myOr
u7	myAnd
u8	myAnd

Figure 11 Schematic of 3.36

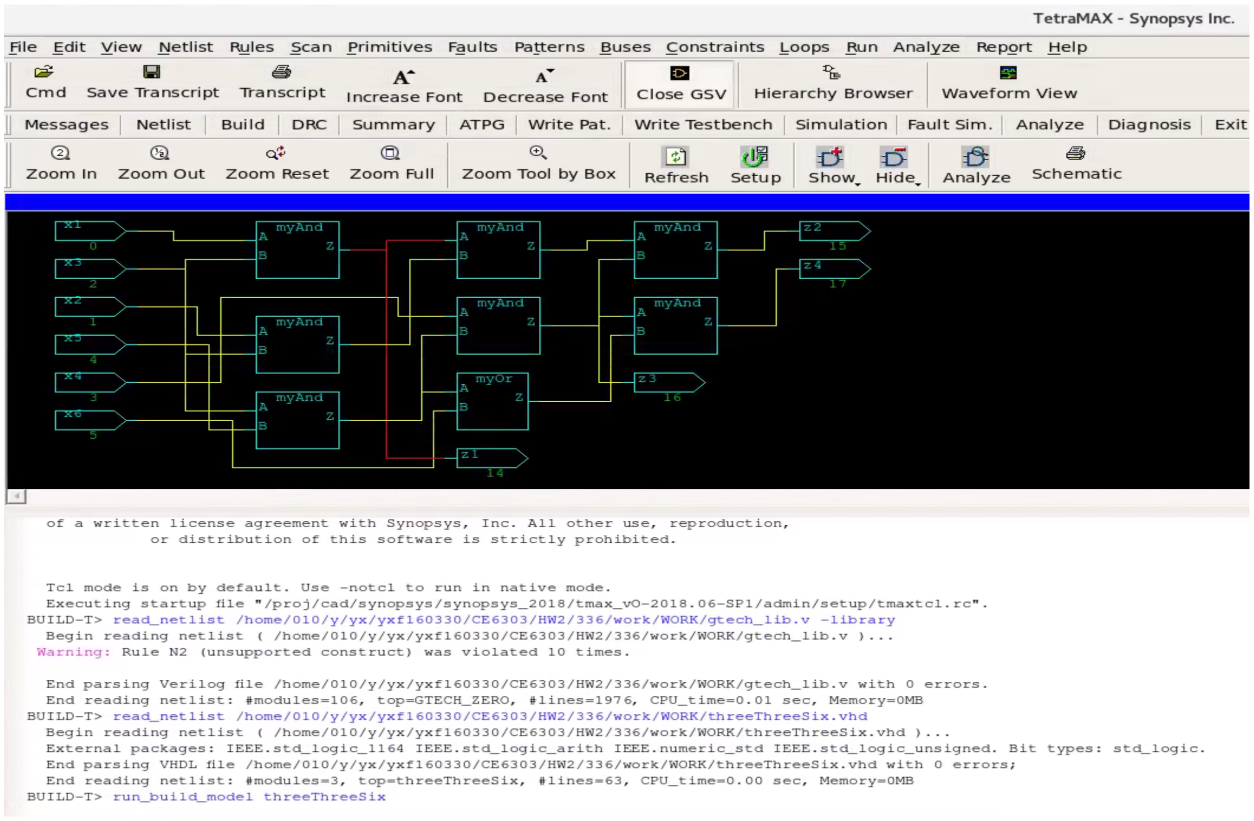


```
/tb336/ithreeThreeSix/x1  1
/tb336/ithreeThreeSix/x2  1
/tb336/ithreeThreeSix/x3  1
/tb336/ithreeThreeSix/x4  1
/tb336/ithreeThreeSix/x5  1
/tb336/ithreeThreeSix/x6  1
/tb336/ithreeThreeSix/z1  1
/tb336/ithreeThreeSix/z2  1
/tb336/ithreeThreeSix/z3  1
/tb336/ithreeThreeSix/z4  1
```

Figure 12 Simulation Waveform of 3.36

The synthesis result, which reports the timing and area, can be found in the threeThreeSix.report in 336 folder. The post-synthesis VHDL code can be found in the folder as well.

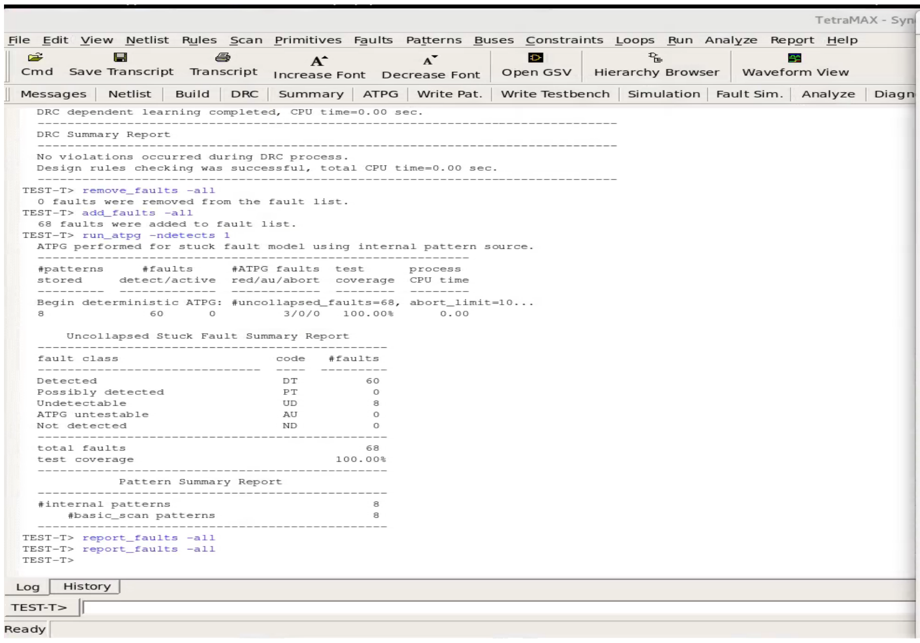
After importing into TetraMax, and have ATPG model built followed by design rule checked, the same the schematic in Figure 13, presented by TetraMax, matches that of Figure 12.


TetraMAX - Synopsys Inc.
File Edit View Netlist Rules Scan Primitives Faults Patterns Buses Constraints Loops Run Analyze Report Help
Cmd Save Transcript Transcript Increase Font Decrease Font Close GSV Hierarchy Browser Waveform View
Messages Netlist Build DRC Summary ATPG Write Pat. Write Testbench Simulation Fault Sim. Analyze Diagnosis Exit
Zoom In Zoom Out Zoom Reset Zoom Full Zoom Tool by Box Refresh Setup Show Hide Analyze Schematic
x1 0
x3 2
x2 1
x5 4
x4 3
x6 5
myAnd
myOr
A
B
Z
z2 15
z4 17
z3 16
z1 14

```
  of a written license agreement with Synopsys, Inc. All other use, reproduction,
              or distribution of this software is strictly prohibited.


  Tcl mode is on by default. Use -notcl to run in native mode.
  Executing startup file "/proj/cad/synopsys/synopsys_2018/tmax_vO-2018.06-SP1/admin/setup/tmaxtcl.rc".
BUILD-T> read_netlist /home/010/y/yx/yxf160330/CE6303/HW2/336/work/WORK/gtech_lib.v -library
  Begin reading netlist ( /home/010/y/yx/yxf160330/CE6303/HW2/336/work/WORK/gtech_lib.v )...
 Warning: Rule N2 (unsupported construct) was violated 10 times.

  End parsing Verilog file /home/010/y/yx/yxf160330/CE6303/HW2/336/work/WORK/gtech_lib.v with 0 errors.
  End reading netlist: #modules=106, top=GTECH_ZERO, #lines=1976, CPU_time=0.01 sec, Memory=0MB
BUILD-T> read_netlist /home/010/y/yx/yxf160330/CE6303/HW2/336/work/WORK/threeThreeSix.vhd
  Begin reading netlist ( /home/010/y/yx/yxf160330/CE6303/HW2/336/work/WORK/threeThreeSix.vhd )...
  External packages: IEEE.std_logic_1164 IEEE.std_logic_arith IEEE.numeric_std IEEE.std_logic_unsigned. Bit types: std_logic.
  End parsing VHDL file /home/010/y/yx/yxf160330/CE6303/HW2/336/work/WORK/threeThreeSix.vhd with 0 errors;
  End reading netlist: #modules=3, top=threeThreeSix, #lines=63, CPU_time=0.00 sec, Memory=0MB
BUILD-T> run_build_model threeThreeSix
```

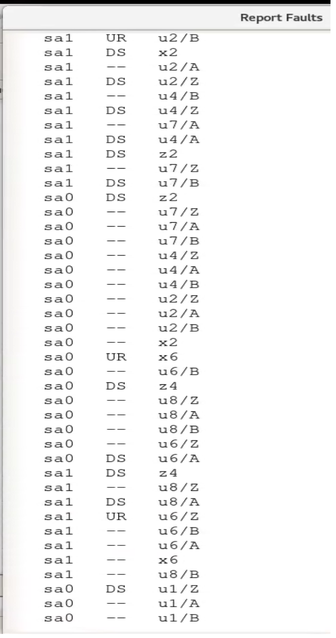
Figure 13 Schematic produced in TetraMax for 3.36

Thus, after running ATPG, faults can be reported as seen in Figure 14 a and b; and patterns used are reported in Figure 15.

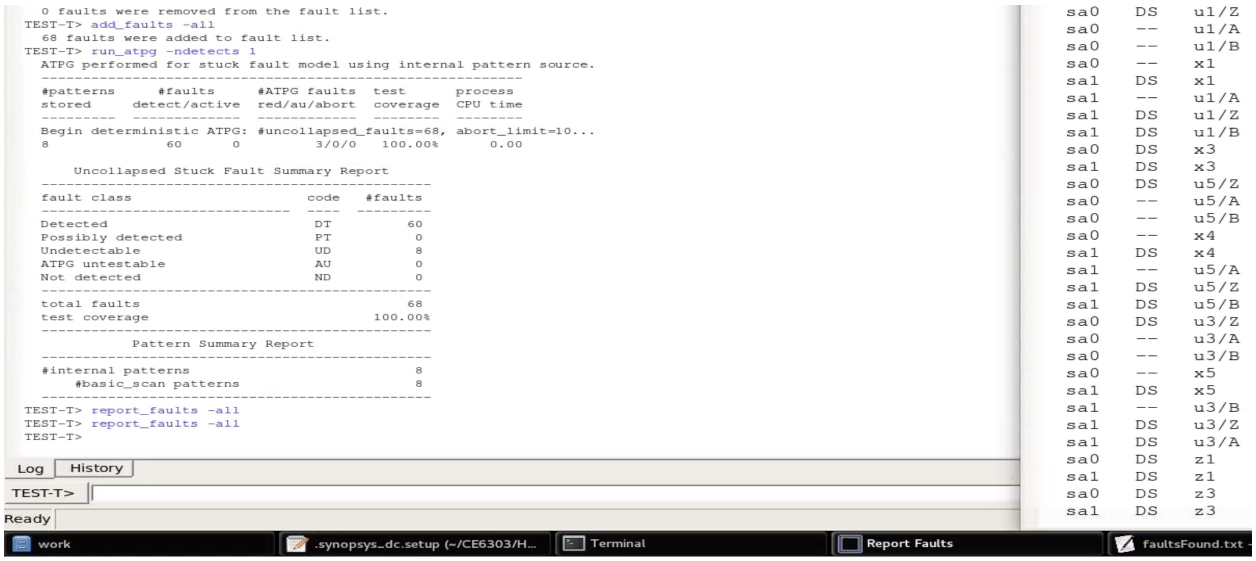

TetraMAX - Syn
File Edit View Netlist Rules Scan Primitives Faults Patterns Buses Constraints Loops Run Analyze Report Help
Cmd Save Transcript Transcript Increase Font Decrease Font Open GSV Hierarchy Browser Waveform View
Messages Netlist Build DRC Summary ATPG Write Pat. Write Testbench Simulation Fault Sim. Analyze Diagn
Log History
Ready

```
  DRC dependent learning completed, CPU time=0.00 sec.
  ------------------------------------------------------------------------------
  DRC Summary Report
  ------------------------------------------------------------------------------
  No violations occurred during DRC process.
  Design rules checking was successful, total CPU time=0.00 sec.
  ------------------------------------------------------------------------------
TEST-T> remove_faults -all
  0 faults were removed from the fault list.
TEST-T> add_faults -all
  68 faults were added to fault list.
TEST-T> run_atpg -ndetects 1
  ATPG performed for stuck fault model using internal pattern source.
  ----------------------------------------------------------
  #patterns     #faults      #ATPG faults  test      process
  stored      detect/active  red/au/abort  coverage  CPU time
  ---------   ------------   ------------  --------  --------
  Begin deterministic ATPG: #uncollapsed_faults=68, abort_limit=10...
  8              60       0         3/0/0   100.00%      0.00

      Uncollapsed Stuck Fault Summary Report
  -----------------------------------------------
  fault class                       code   #faults
  ------------------------------    ----   ---------
  Detected                           DT         60
  Possibly detected                  PT          0
  Undetectable                       UD          8
  ATPG untestable                    AU          0
  Not detected                       ND          0
  -----------------------------------------------
  total faults                                  68
  test coverage                            100.00%
  -----------------------------------------------
              Pattern Summary Report
  -----------------------------------------------
  #internal patterns                             8
      #basic_scan patterns                       8
  -----------------------------------------------
TEST-T> report_faults -all
TEST-T> report_faults -all
TEST-T>
```

`TEST-T>`



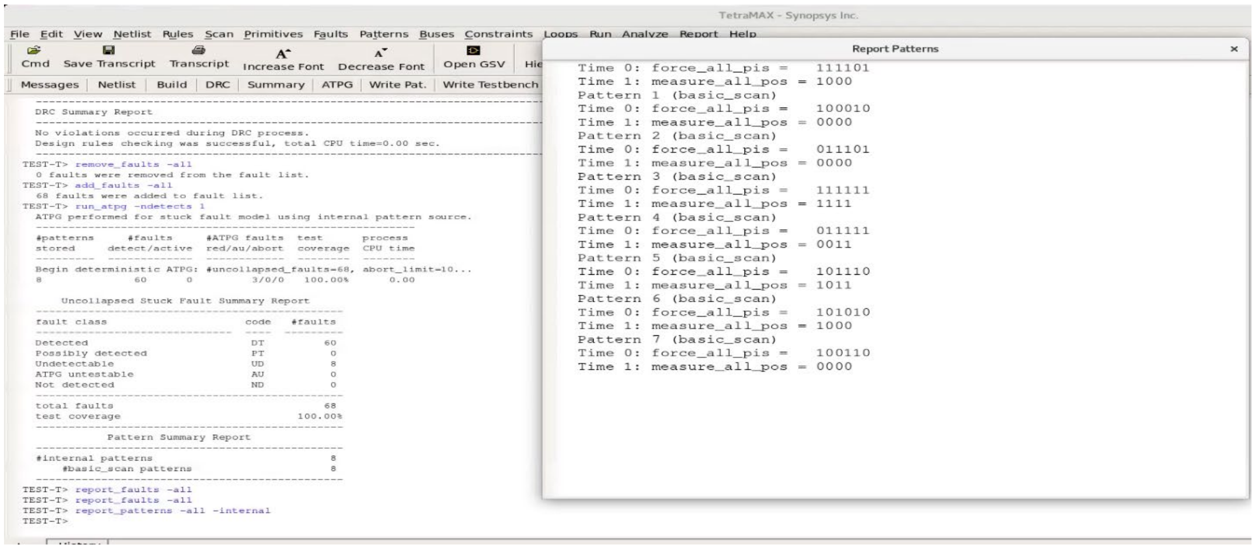
```
sa1   UR   u2/B
sa1   DS   x2
sa1   --   u2/A
sa1   DS   u2/Z
sa1   --   u4/B
sa1   DS   u4/Z
sa1   --   u7/A
sa1   DS   u4/A
sa1   DS   z2
sa1   --   u7/Z
sa1   DS   u7/B
sa0   DS   z2
sa0   --   u7/Z
sa0   --   u7/A
sa0   --   u7/B
sa0   --   u4/Z
sa0   --   u4/A
sa0   --   u4/B
sa0   --   u2/Z
sa0   --   u2/A
sa0   --   u2/B
sa0   --   x2
sa0   UR   x6
sa0   --   u6/B
sa0   DS   z4
sa0   --   u8/Z
sa0   --   u8/A
sa0   --   u8/B
sa0   --   u6/Z
sa0   DS   u6/A
sa1   DS   z4
sa1   --   u8/Z
sa1   DS   u8/A
sa1   UR   u6/Z
sa1   --   u6/B
sa1   --   u6/A
sa1   --   x6
sa1   --   u8/B
sa0   DS   u1/Z
sa0   --   u1/A
sa0   --   u1/B
```



```
  0 faults were removed from the fault list.
TEST-T> add_faults -all
  68 faults were added to fault list.
TEST-T> run_atpg -ndetects 1
  ATPG performed for stuck fault model using internal pattern source.
  ----------------------------------------------------------
  #patterns     #faults      #ATPG faults  test      process
  stored     detect/active   red/au/abort  coverage  CPU time
  ---------  -------------   ------------  --------  --------
  Begin deterministic ATPG: #uncollapsed_faults=68, abort_limit=10...
  8               60       0          3/0/0   100.00%       0.00

      Uncollapsed Stuck Fault Summary Report
  -----------------------------------------------
  fault class                       code   #faults
  ------------------------------    ----  ---------
  Detected                           DT         60
  Possibly detected                  PT          0
  Undetectable                       UD          8
  ATPG untestable                    AU          0
  Not detected                       ND          0
  -----------------------------------------------
  total faults                                  68
  test coverage                            100.00%
  -----------------------------------------------
             Pattern Summary Report
  -----------------------------------------------
  #internal patterns                             8
      #basic_scan patterns                       8
  -----------------------------------------------
TEST-T> report_faults -all
TEST-T> report_faults -all
TEST-T>
```

```
sa0   DS   u1/Z
sa0   --   u1/A
sa0   --   u1/B
sa0   --   x1
sa1   DS   x1
sa1   --   u1/A
sa1   DS   u1/Z
sa1   DS   u1/B
sa0   DS   x3
sa1   DS   x3
sa0   DS   u5/Z
sa0   --   u5/A
sa0   --   u5/B
sa0   --   x4
sa1   DS   x4
sa1   --   u5/A
sa1   DS   u5/Z
sa1   DS   u5/B
sa0   DS   u3/Z
sa0   --   u3/A
sa0   --   u3/B
sa0   --   x5
sa1   DS   x5
sa1   --   u3/B
sa1   DS   u3/Z
sa1   DS   u3/A
sa0   DS   z1
sa1   DS   z1
sa0   DS   z3
sa1   DS   z3
```

Figure 14 a&b Faults found in 3.36



```
  DRC Summary Report
  -----------------------------------------------------------------
  No violations occurred during DRC process.
  Design rules checking was successful, total CPU time=0.00 sec.
  -----------------------------------------------------------------
TEST-T> remove_faults -all
  0 faults were removed from the fault list.
TEST-T> add_faults -all
  68 faults were added to fault list.
TEST-T> run_atpg -ndetects 1
  ATPG performed for stuck fault model using internal pattern source.
  ----------------------------------------------------------
  #patterns     #faults      #ATPG faults  test      process
  stored     detect/active   red/au/abort  coverage  CPU time
  ---------  -------------   ------------  --------  --------
  Begin deterministic ATPG: #uncollapsed_faults=68, abort_limit=10...
  8               60       0          3/0/0   100.00%       0.00

      Uncollapsed Stuck Fault Summary Report
  -----------------------------------------------
  fault class                       code   #faults
  ------------------------------    ----  ---------
  Detected                           DT         60
  Possibly detected                  PT          0
  Undetectable                       UD          8
  ATPG untestable                    AU          0
  Not detected                       ND          0
  -----------------------------------------------
  total faults                                  68
  test coverage                            100.00%
  -----------------------------------------------
             Pattern Summary Report
  -----------------------------------------------
  #internal patterns                             8
      #basic_scan patterns                       8
  -----------------------------------------------
TEST-T> report_faults -all
TEST-T> report_faults -all
TEST-T> report_patterns -all -internal
TEST-T>
```

Report Patterns

```
 Time 0: force_all_pis =    111101
 Time 1: measure_all_pos = 1000
 Pattern 1 (basic_scan)
 Time 0: force_all_pis =    100010
 Time 1: measure_all_pos = 0000
 Pattern 2 (basic_scan)
 Time 0: force_all_pis =    011101
 Time 1: measure_all_pos = 0000
 Pattern 3 (basic_scan)
 Time 0: force_all_pis =    111111
 Time 1: measure_all_pos = 1111
 Pattern 4 (basic_scan)
 Time 0: force_all_pis =    011111
 Time 1: measure_all_pos = 0011
 Pattern 5 (basic_scan)
 Time 0: force_all_pis =    101110
 Time 1: measure_all_pos = 1011
 Pattern 6 (basic_scan)
 Time 0: force_all_pis =    101010
 Time 1: measure_all_pos = 1000
 Pattern 7 (basic_scan)
 Time 0: force_all_pis =    100110
 Time 1: measure_all_pos = 0000
```

Figure 15 Patterns used in fault testing for 3.36

As can be seen, not all faults can be detected and tested due to the fact that the circuit has multiple fanouts. In the hand-work, the circuit needs to be divided into 4 Fan-out-free Regions to perform fault analysis and critical path tracing. As a result, the analysed pattern and fault counts has discrepancies between each other.