

**EEDG/CE 6303: Testing and Testable Design (Fall'2021)**

**Department of Electrical & Computer Engineering**

**The University of Texas at Dallas**

**Instructor: Mehrdad Nourani (nourani@utdallas.edu)**

**Cover Page for All Submissions**

**(Assignment, Project, Codes/Simulations/CAD, Examinations, etc.)**

Last Name (as shown in the official UT Dallas Student ID Card): Feng

First Name: Yu

Submission Materials for (e.g. Homework #, Project #): HW 3

**Statement of Academic Honesty**

I certify that:

- i. the attached report (for assignment, project, codes/simulations/CAD, examinations, etc.) is my own work, based on my personal study and/or research,
- ii. I have acknowledged all material and sources used in its preparation, whether they be books, articles, reports, lecture notes, and any other kind of document, electronic or personal communication,
- iii. this report has not previously been submitted for assessment in EEDG/CE 6303 or any other course at UT Dallas or elsewhere,
- iv. I have not copied in part or whole or otherwise plagiarized the work of other students and/or persons, and
- v. I have read and understood the Department and University policies on scholastic dishonesty as outlined in: <http://www.utdallas.edu/deanofstudents/dishonesty/>.

Name: Yu Feng

Date: 10/10/2021

Signature: 

**The University of Texas at Dallas**  
**Dept. of Electrical and Computer Engineering**

**EEDG/CE 6303: Testing and Testable Design**

**HW # 3: Due on Monday, Oct. 11, 2021 - 12:00 pm NOON (US CST)**

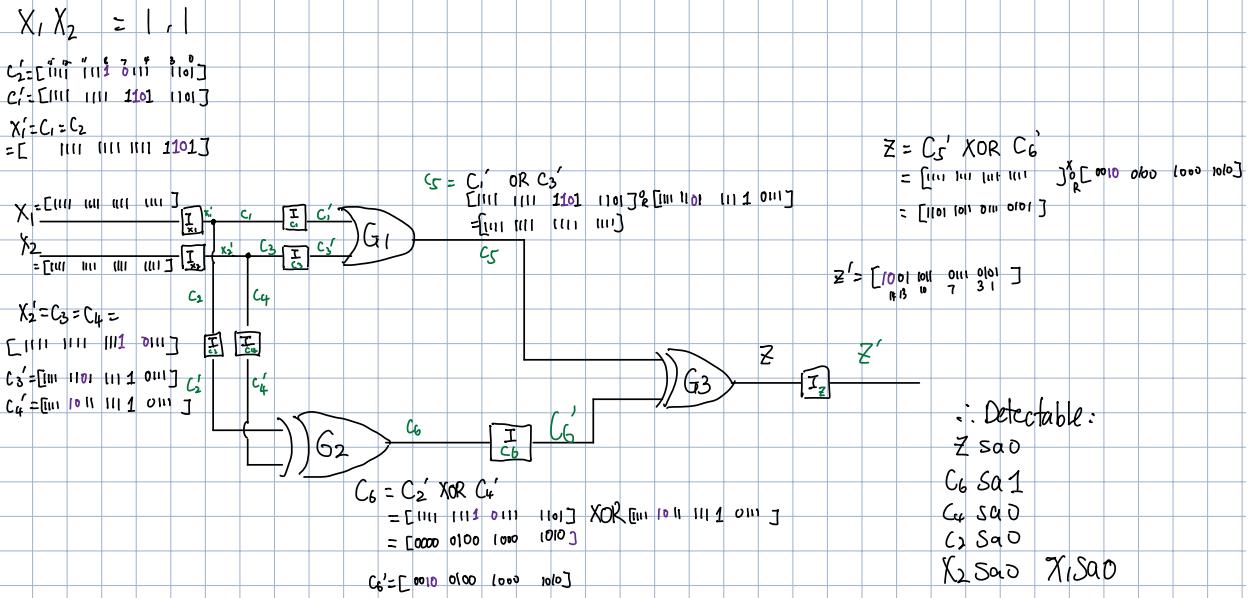
*When you submit your homeworks, to help us grade and identify your work, you need to comply with the following guidelines carefully:*

- **Have a cover page** for each document (e.g. homework, project, report, etc.) that you submit. A sample of cover page is provided in the course webpage. This page must include: (1) your name as it appears in your **student ID card**, (2) course name/number, (3) homework/project number, and (4) the **Statement of Academic Honesty** that you sign.

1. For two circuits shown in Figures 3.23 and 3.34 of your text book (exactly as they are with no change to an equivalent topology) and for patterns  $x_1x_2 = 00$  and  $x_1x_2 = 11$  (for Figure 3.23) and patterns  $x_1x_2x_3 = 001$  and  $x_1x_2x_3 = 110$  (for Figure 3.34):
  - (a) Demonstrate **parallel** fault simulation.
  - (b) Demonstrate **deductive** fault simulation.
  - (c) Demonstrate **concurrent** fault simulation.
  - (d) Demonstrate **critical path tracing** fault simulation
2. For the two circuits shown in Figures 3.23 and 3.34 of your text book (exactly as shown),
  - (a) Calculate all SCOP measures.
  - (b) Calculate the testability index for the circuit and comment on it.
3. Consider Figure 5.5 in your book. Assume FF is a D flip-flop without any set/reset line. Analyze this sequential circuit for 4 stuck-at faults: (i)  $x_1$  s-a-0, (ii)  $x_1$  s-a-1, (iii)  $x_2$  s-a-0, (iv)  $x_2$  s-a-1.
4. Consider Figure 5.27 in your book. Assume FF is a D flip-flop without any set/reset line. Analyze this sequential circuit for 4 stuck-at faults: (i)  $x_1$  s-a-0, (ii)  $x_1$  s-a-1, (iii)  $x_2$  s-a-0, (iv)  $x_2$  s-a-1.
5. Consider Figure 5.5 in your book. Use Synopsys toolset to implement two versions of it: (i) with D-FF without any set/reset, and (ii) with D-FF with set/reset. Run ATPG for sequential circuits in Tetramax on both versions and report and discuss the results.

**Note:** Your report should include HDL (VHDL or Verilog) description, schematic of the circuit, some simulations to show the correct behavior, test analysis by Tetramax (e.g. faults, test patterns) and any other interesting observations.

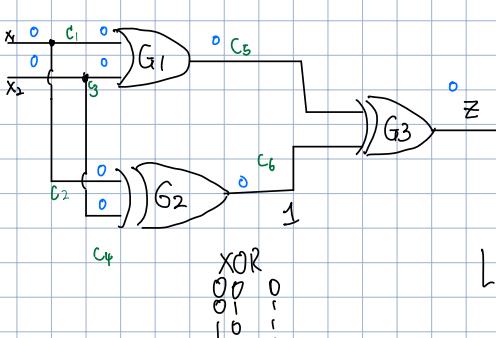




b) deductive

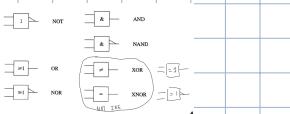
$$X_1 X_2 = 00$$

$$F = \left( \begin{array}{l} X_1 \text{ Sa0} \\ X_1 \text{ Sa1} \\ X_2 \text{ Sa0} \\ X_2 \text{ Sa1} \\ C_1 \text{ Sa0} \\ C_1 \text{ Sa1} \\ C_2 \text{ Sa0} \\ C_2 \text{ Sa1} \\ C_3 \text{ Sa0} \\ C_3 \text{ Sa1} \\ C_4 \text{ Sa0} \\ C_4 \text{ Sa1} \\ C_5 \text{ Sa0} \\ C_5 \text{ Sa1} \\ C_6 \text{ Sa0} \\ C_6 \text{ Sa1} \\ Z \text{ Sa0} \\ Z \text{ Sa1} \end{array} \right)$$

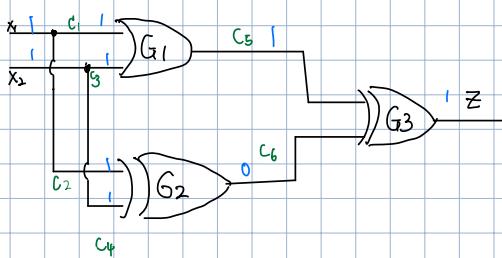


$$\begin{aligned}
 L_{X_1} &= \{X_1 \text{ Sa1}\} \quad L_{X_2} = \{X_2 \text{ Sa1}\} \\
 L_C = L_{X_1} \cup \{C_1 \text{ Sa1}\} &\quad L_{C_2} = L_{X_2} \cup \{C_2 \text{ Sa1}\} \\
 &= \{X_1 \text{ Sa1}, C_1 \text{ Sa1}\} \quad = \{X_2 \text{ Sa1}, C_2 \text{ Sa1}\} \\
 L_{C_3} &= L_{X_2} \cup \{C_3 \text{ Sa1}\} \quad L_{C_4} = L_{X_2} \cup \{C_4 \text{ Sa1}\} \\
 &= \{X_2 \text{ Sa1}\} \quad = \{X_2 \text{ Sa1}, C_4 \text{ Sa1}\} \\
 L_{C_5} &= L_{C_1} \cup L_{C_3} \cup \{C_5 \text{ Sa1}\} \\
 &= \{X_1 \text{ Sa1}, C_1 \text{ Sa1}, X_2 \text{ Sa1}\} \\
 L_{C_6} &= L_{C_2} \cup L_{C_4} \cup \{C_6 \text{ Sa1}\} \\
 &= \{X_1 \text{ Sa1}, C_2 \text{ Sa1}, X_2 \text{ Sa1}, C_4 \text{ Sa1}, C_6 \text{ Sa1}\} \\
 L_Z &= L_{C_5} \cup L_{C_6} \cup \{Z \text{ Sa1}\} \\
 &= \{X_1 \text{ Sa1}, C_1 \text{ Sa1}, X_2 \text{ Sa1}, C_2 \text{ Sa1}, C_4 \text{ Sa1}, C_6 \text{ Sa1}, Z \text{ Sa1}\}
 \end{aligned}$$

$\therefore \text{detectable faults from analysis}$   
 $\{X_1 \text{ Sa1}, C_1 \text{ Sa1}, X_2 \text{ Sa1}, C_2 \text{ Sa1}, C_4 \text{ Sa1}, C_6 \text{ Sa1}, Z \text{ Sa1}\}$   
 but  $X_1 \text{ Sa1}$  and  $X_2 \text{ Sa1}$  may not be detected  
 They propagate due to XOR gate's control value is undefined.



$$X_1 X_2 = 11$$



$$L_{x_1} \{ X_1 S_{A0} \} \quad L_{x_2} \{ X_2 S_{A0} \}$$

$$\begin{aligned} L_{c_1} &= L_{x_1} \cup \{ C_1 S_{A0} \} & L_{c_3} &= L_{x_2} \cup \{ C_3 S_{A0} \} \\ &= \{ X_1 S_{A0}, C_1 S_{A0} \} & &= \{ X_2 S_{A0}, C_3 S_{A0} \} \end{aligned}$$

$$\begin{aligned} L_{c_2} &= L_{x_1} \cup \{ C_2 S_{A0} \} & L_{c_4} &= L_{x_2} \cup \{ C_4 S_{A0} \} \\ &= \{ X_1 S_{A0}, C_2 S_{A0} \} & &= \{ X_2 S_{A0}, C_4 S_{A0} \} \end{aligned}$$

$$\begin{aligned} L_{c_5} &= L_{c_1} \cap L_{c_3} \cup \{ C_5 S_{A0} \} \\ &= \emptyset \cup \{ C_5 S_{A0} \} \\ &= \{ C_5 S_{A0} \} \end{aligned}$$

$$\begin{aligned} L_{c_6} &= L_{c_2} \cup L_{c_4} \cup \{ C_6 S_{A1} \} \\ &= \{ X_1 S_{A0}, C_2 S_{A0}, X_2 S_{A0}, C_4 S_{A0}, C_6 S_{A1} \} \end{aligned}$$

$$\begin{aligned} L_z &= L_{c_5} \cup L_{c_6} \cup \{ Z S_{A0} \} \\ &= \{ X_1 S_{A0}, C_2 S_{A0}, X_2 S_{A0}, \\ &\quad C_4 S_{A0}, C_6 S_{A1}, Z S_{A0} \} \end{aligned}$$

$\therefore$  Detectable:

$$Z S_{A0}$$

$$C_6 S_{A1}$$

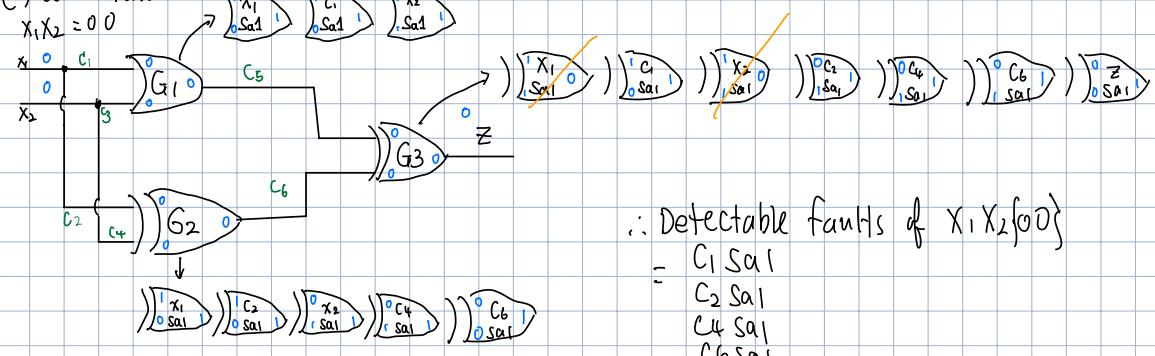
$$C_4 S_{A0}$$

$$C_2 S_{A0}$$

$$X_2 S_{A0} \quad X_1 S_{A0}$$

C) concurrent

$$X_1 X_2 = 00$$



$\therefore$  Detectable faults of  $X_1 X_2 \{ 00 \}$

$$= C_1 S_{A1}$$

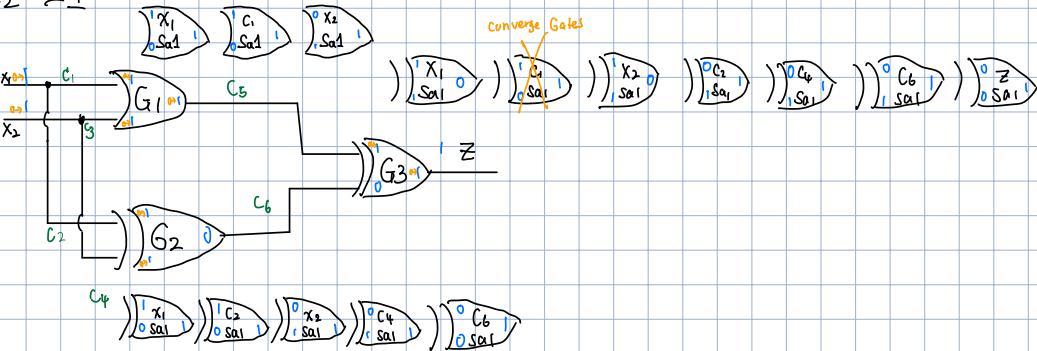
$$C_2 S_{A1}$$

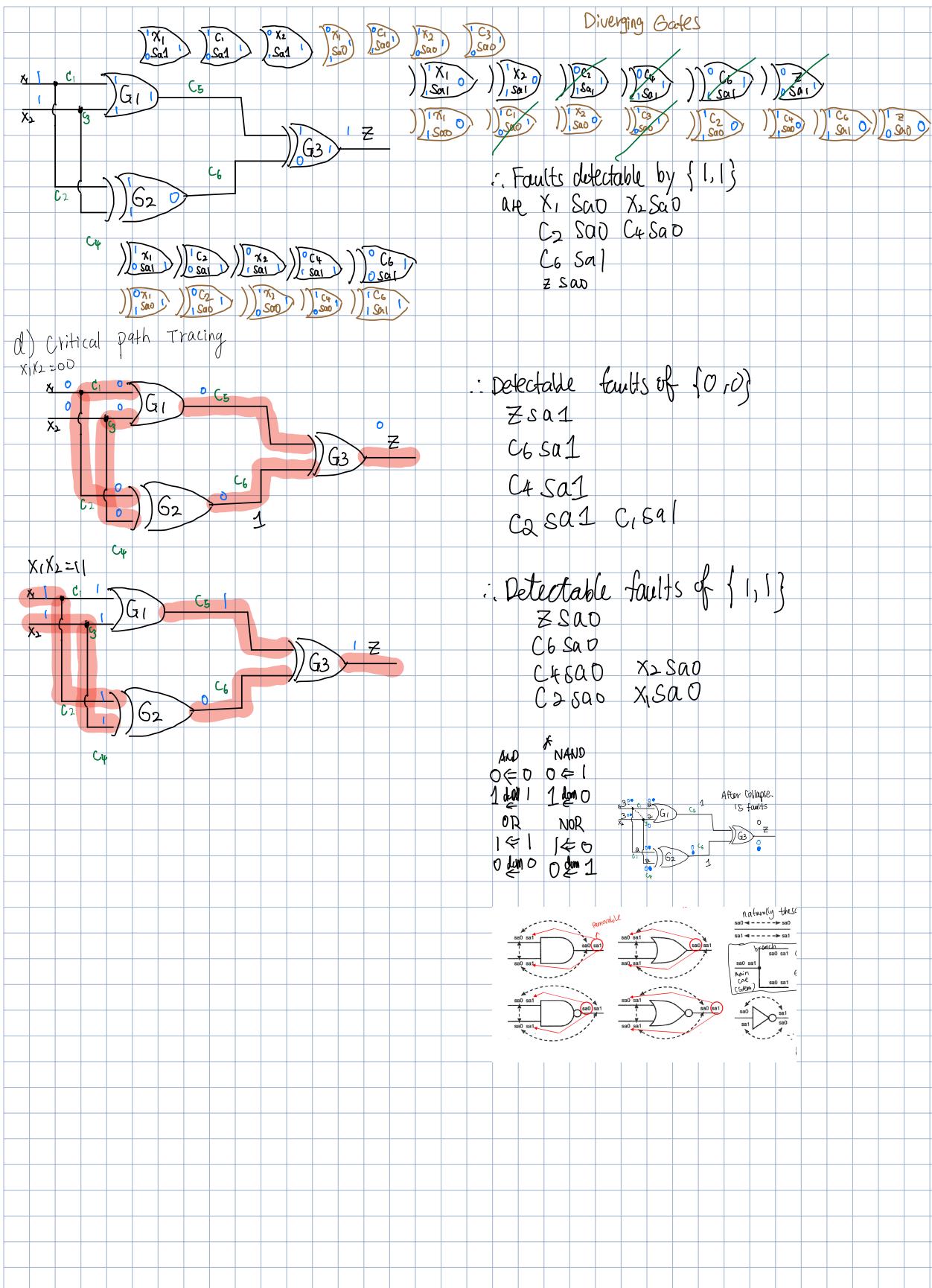
$$C_4 S_{A1}$$

$$C_6 S_{A1}$$

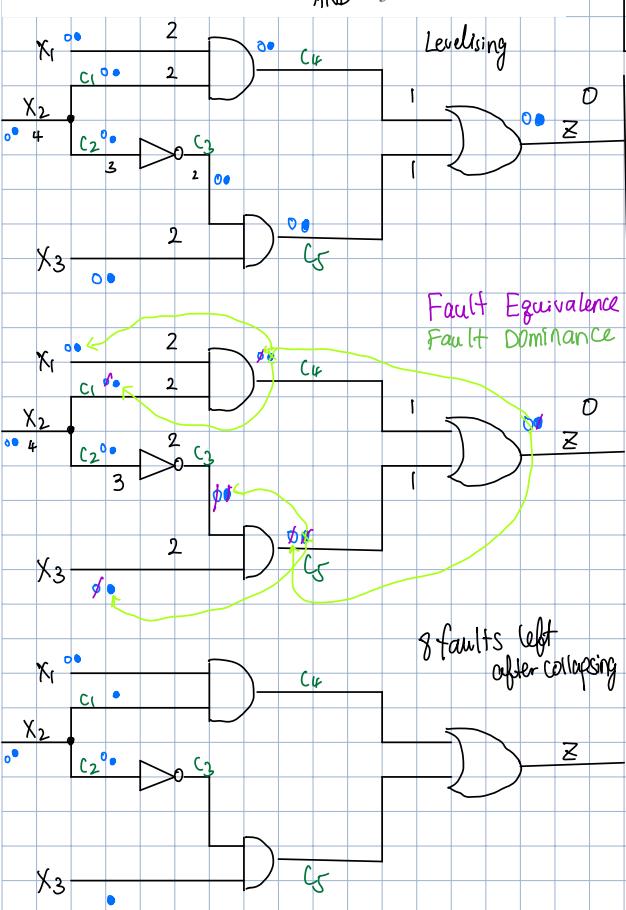
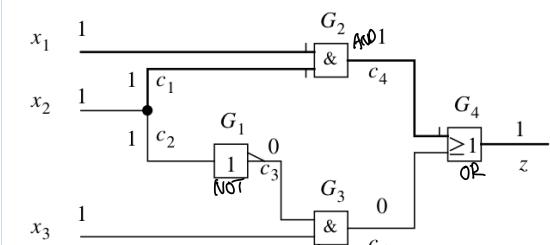
$$Z S_{A1}$$

$$X_1 X_2 = 11$$

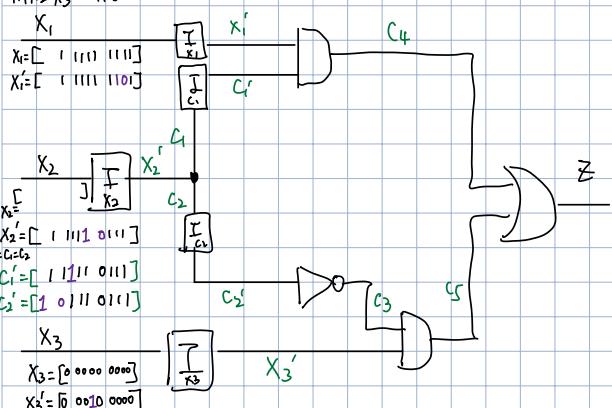




2.34



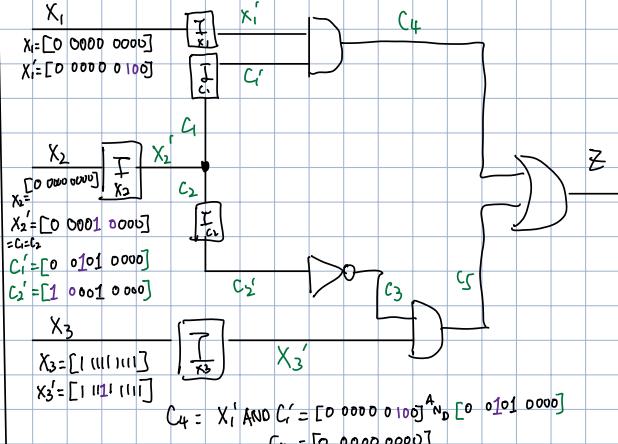
$$X_1 X_2 X_3 = 001$$



a) parallel

Faults	pos	I	S
Fault-free	0	[ 0 0000 0000 ]	[ 0 0000 0000 ] (0m <sup>4</sup> )
X <sub>1</sub> Sa0	1	[ 0 0000 0100 ]	[ 0 0000 0100 ]
X <sub>1</sub> Sa1	2	[ 0 0001 0000 ]	[ 0 0001 0000 ]
X <sub>2</sub> Sa0	3	[ 0 0001 1000 ]	[ 0 0001 1000 ]
X <sub>2</sub> Sa1	4	[ 0 0010 0000 ]	[ 0 0010 0000 ]
X <sub>3</sub> Sa1	5	[ 0 0010 0000 ]	[ 0 0010 0000 ]
C <sub>1</sub> Sa1	6	[ 0 0100 0000 ]	[ 0 0100 0000 ]
C <sub>2</sub> Sa0	7	[ 1 0000 0000 ]	[ 1 0000 0000 ]
C <sub>2</sub> Sa1	8	[ 1 0000 0000 ]	[ 1 0000 0000 ]

$$X_1 X_2 X_3 = 001$$



$$C_4: X'_1 \text{ AND } C'_1 = [ 0 0000 0100 ] \text{ AND } [ 0 0101 0000 ]$$

$$C_F = [ 0 0000 0000 ]$$

$$C_3 = \overline{C_2} = [ 1 0001 0000 ]$$

$$C_3 = [ 0 1110 1111 ]$$

$$C_5 = C_3 \text{ AND } X'_3 = [ 0 1101 1111 ] \text{ AND } [ 1 1111 1111 ]$$

$$C_5 = [ 0 1110 1111 ]$$

$$Z = C_4 \text{ OR } C_5$$

$$= [ 0 0000 0000 ] \text{ OR } [ 0 1110 1111 ]$$

$$= [ 0 1110 1111 ]$$

∴ faults detectable by  $X_1 X_2 X_3 = 001$

$C_2 \text{ Sa1}, X_2 \text{ Sa1}$

$$C_4: X'_1 \text{ AND } C'_1 = [ 1 1111 1101 ] \text{ AND } [ 1 1111 0111 ]$$

$$C_3 = \overline{C_2}$$

$$= [ 1 0111 0111 ]$$

$$= [ 0 1000 1000 ]$$

$$C_5: C_3 \text{ AND } X'_3 = [ 0 1000 0000 ] \text{ AND } [ 0 0000 0000 ]$$

$$= [ 0 0000 0000 ]$$

$$Z = C_4 \text{ OR } C_5$$

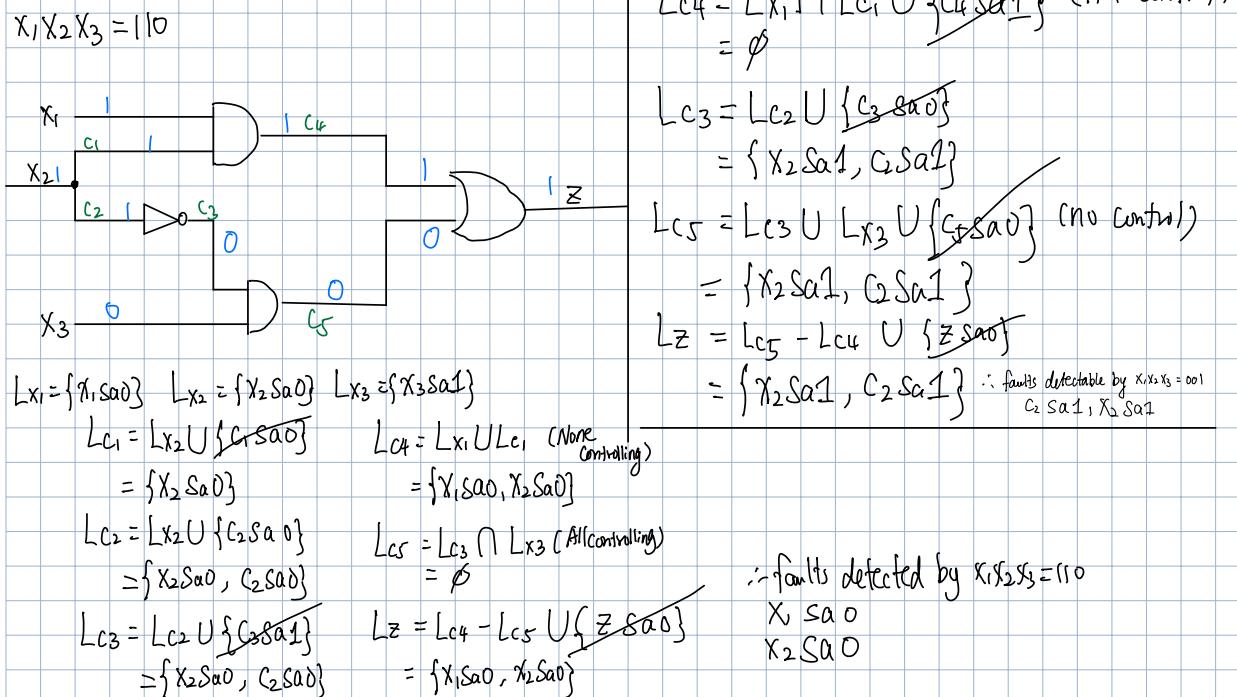
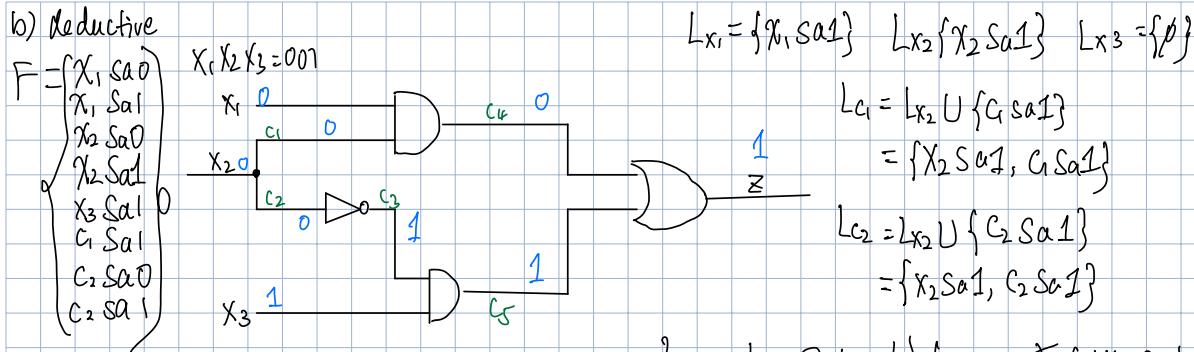
$$= [ 1 1111 0101 ] \text{ OR } [ 0 0000 0000 ]$$

$$= [ 1 1111 0101 ]$$

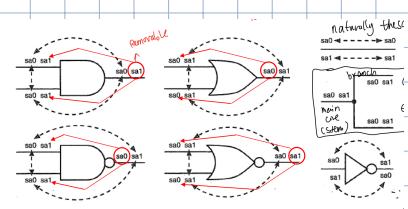
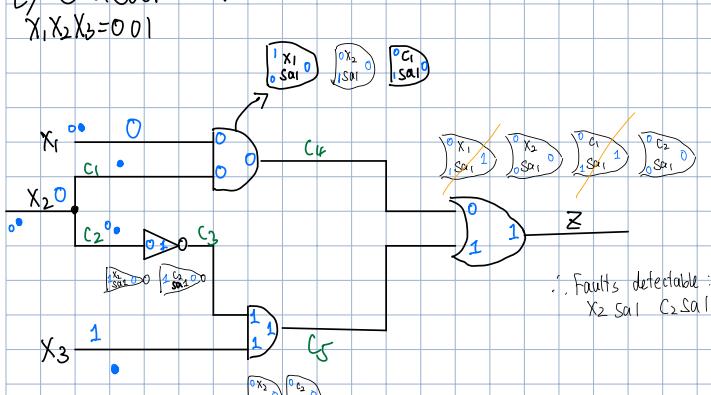
∴ faults detected:

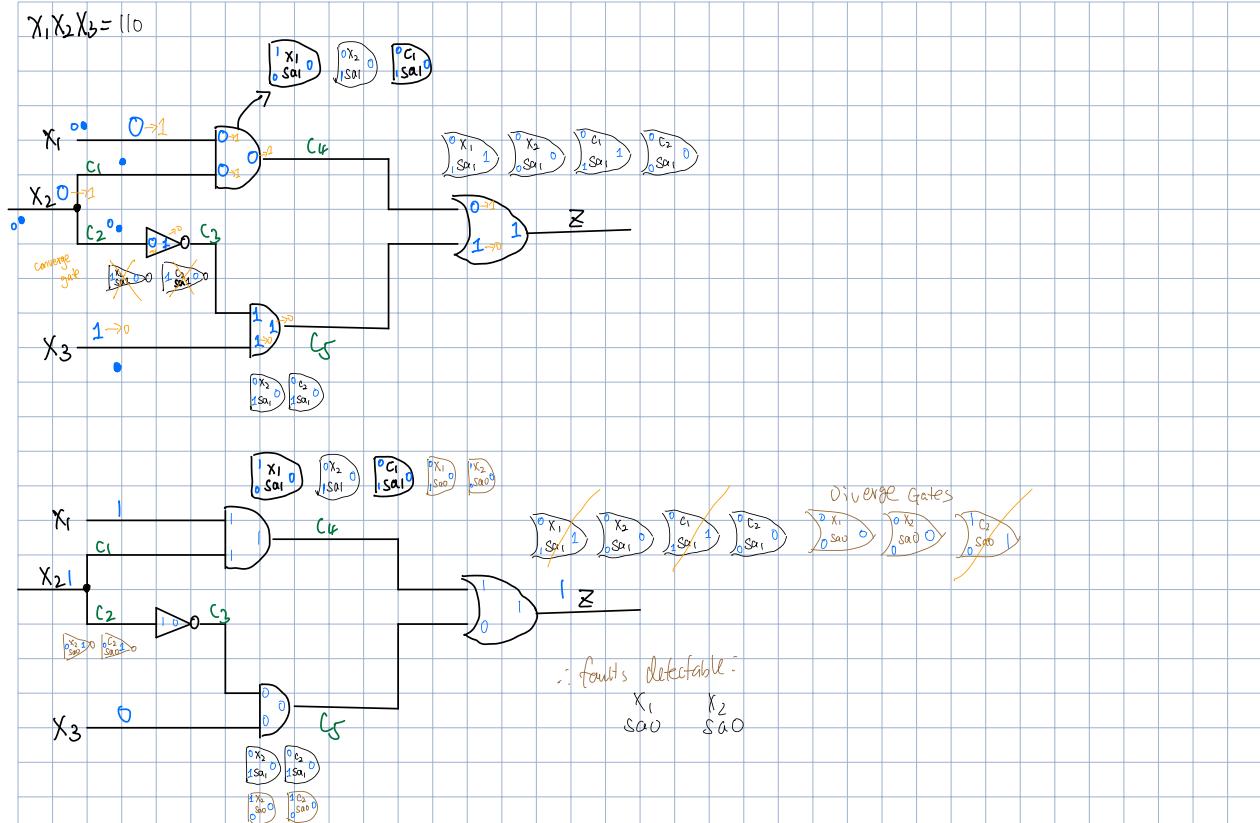
$X_1 \text{ Sa0}$

$X_2 \text{ Sa0}$



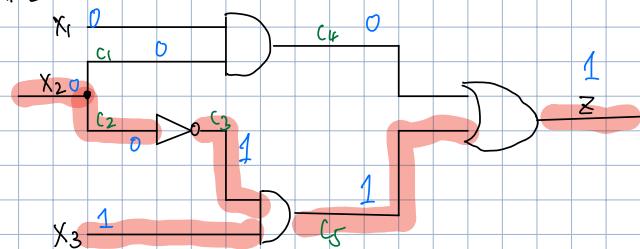
### c) Concurrent





#### d) Critical Path Tracing

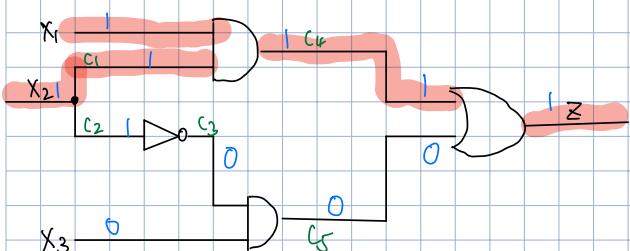
$$X_1 X_2 X_3 = 001$$



$\therefore$  faults detected by  $\{0, 0, 1\}$

$C_2 S_{A1} 1$   
 $X_2 S_{A1} 1$

$$X_1 X_2 X_3 = 110$$



$\therefore$  faults detected by  $\{1, 1, 0\}$

$X_1 S_{A1} 0$   
 $X_2 S_{A1} 0$

2. For the two circuits shown in Figures 3.23 and 3.34 of your text book (exactly as shown),

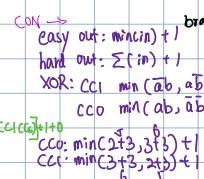
  - Calculate all SCOAP measures.
  - Calculate the testability index for the circuit and comment on it.

$$\begin{aligned}CC_4 &= CC(C_0) + CC(C_3) + 1 \\&= 4 + 1 + 1 \quad CC(C_3) = CC(C_0) + CC(C_1) + 1 \\&= 6 \quad \quad \quad = 4 + 1 + 1 \\&= 6\end{aligned}$$

For 3,2) (CC0, CC1) CO

Handwritten logic circuit diagram:

- Gates:**
  - G1:** AND gate with inputs  $x_1$  and  $x_2$ . Output is labeled  $a$ .
  - G2:** OR gate with inputs  $x_1$  and  $x_2$ . Output is labeled  $b$ .
  - G3:** AND gate with inputs  $a$  and  $b$ . Output is labeled  $z$ .
- Inputs:**  $x_1$  and  $x_2$  (labeled  $x_1$  and  $x_2$ ).
- Outputs:**  $a$ ,  $b$ , and  $z$ .
- Annotations:**
  - Inputs  $x_1$  and  $x_2$  are each labeled with their values:  $(1, 1)$ .
  - Output  $a$  is labeled with its value:  $(1, 1)$ .
  - Output  $b$  is labeled with its value:  $(1, 1)$ .
  - Output  $z$  is labeled with its value:  $(6, 6)$ .
  - Intermediate values  $c_1, c_2, c_3, c_4, c_5, c_6$  are labeled with their respective values:  $5, 5, 4, 5, 6, 1$ .
  - Equations for  $c_1$  through  $c_6$  are shown, along with their minimum values.
  - Equation for  $z$ :  $z = \min(c_1, c_2) + 1$



OR  
0 0 0 hard  
0 1 :  
1 0 : easy  
1 1 |

obs ←

**AND, NAND**:  $OUT = CO + CC1(CO) + 1$   
**OR, NOR**:  $OUT = CO + CC0(CO) + 1$   
**XOR, XNOR**:  $OUT = min(CO, CO + CC0(CO) + 1)$

**branch**: take min

branch: take min

- Compute *testabilities* for stuck-at faults

$$T(x \text{ sa } 0) = CC1(x) + CO(x)$$

$$T(x \text{ sa1}) = CO(x) + CO(x)$$

— Testability index =  $\log \sum T(f_i)$ , i.e. compu

Testability:

$F = \left\{ \begin{array}{l} X_1, Sa0 \\ X_1, Sa1 \\ X_2, Sa0 \\ X_2, Sa1 \\ C_1, Sa0 \\ C_1, Sa1 \\ C_2, Sa0 \\ C_2, Sa1 \\ C_3, Sa0 \\ C_4, Sa0 \\ C_4, Sa1 \\ C_6, Sa0 \\ C_6, Sa1 \\ Z, Sa0 \\ Z, Sa1 \end{array} \right\}$	$CC1(X_1) + CO(X_1) = 1+5=6$
	$CCO(X_1) + CO(X_1) = 1+5=6$
	$CC1(X_2) + CO(X_2) = 1+5=6$
	$CCO(X_2) + CO(X_2) = 1+5=6$
	$CC1(C_1) + CO(C_1) = 1+6=7$
	$CCO(C_1) + CO(C_1) = 1+6=7$
	$CC1(C_2) + CO(C_2) = 1+5=6$
	$CCO(C_2) + CO(C_2) = 1+5=6$
	$CC1(C_3) + CO(C_3) = 1+6=7$
	$CC1(C_4) + CO(C_4) = 1+5=6$
	$CCO(C_4) + CO(C_4) = 1+5=6$
	$CC1(C_6) + CO(C_6) = 3+3=6$
	$CCO(C_6) + CO(C_6) = 3+3=6$
	$CC1(Z) + CO(Z) = 6+0=6$
	$CCO(Z) + CO(Z) = 6+0=6$

$$\sum(f_i) = 93$$

$$\text{Index: } \log \sum (f_i) = 1.968483$$

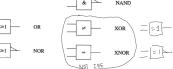
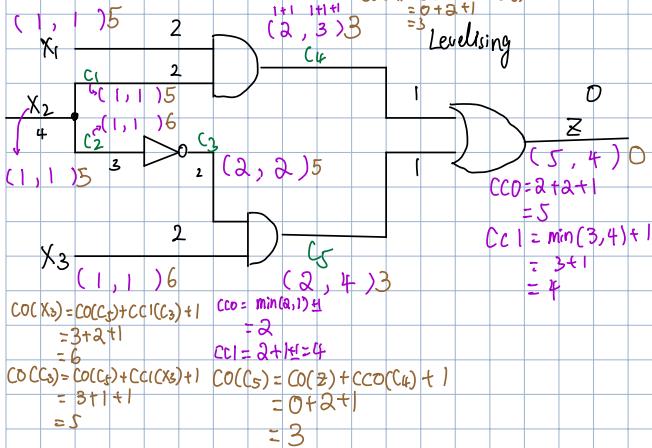
Since the testability Index = 1.96  
It is easy to test the entire circuit.

$$\text{CO}(x_1) = \text{CO}(c_4) + c_1 \\ = 3 + 1 + 1 \\ = 5$$

$$0+1 \quad C_0(c_1) = C_0(c_4) + CC1(x_1) + 1 \\ = 3+1+1 \\ = 5$$

AND	OR
0 0 0	0 0 0
0 1 0	0 1 1
1 0 0	1 0 1
1 1 0	1 1 1
hard	easy

For 3.34 (CCO, CCl) CO  
 $\text{CO}(\text{CH}_3) = (\text{CO}_2) + \text{CCO}(\text{C}_2) +$



Testability :

$$F = \left\{ \begin{array}{l} X_1, S_{A,0} \\ X_1, S_{A,1} \\ X_2, S_{A,0} \\ X_2, S_{A,1} \\ X_3, S_{A,1} \\ C_1, S_{A,1} \\ C_2, S_{A,0} \\ C_2, S_{A,1} \end{array} \right\} \quad \begin{array}{l} CC1(X_1) + CO(X_1) = 1+5=6 \\ CC0(X_1) + CO(X_1) = 1+5=6 \\ CC1(X_2) + CO(X_2) = 1+5=6 \\ CC0(X_2) + CO(X_2) = 1+5=6 \\ CC0(X_3) + CO(X_3) = 1+6=7 \\ CC0(C_1) + CO(C_1) = 1+5=6 \\ CC1(C_2) + CO(C_2) = 1+6=7 \\ CC0(C_2) + CO(C_2) = 1+6=7 \end{array}$$

$$\sum T(f_i) = 51$$

$$\text{Index} = \log \sum T(f_i) = 1.70757$$

This circuit is easy to test as its testability index is low.

It's even simpler to fast than previous.

3. Consider Figure 5.5 in your book. Assume FF is a D flip-flop without any set/reset line. Analyze this sequential circuit for 4 stuck-at faults: (i)  $x_1$  s-a-0, (ii)  $x_1$  s-a-1, (iii)  $x_2$  s-a-0, (iv)  $x_2$  s-a-1.

3.

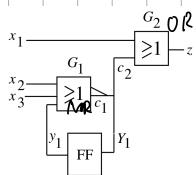
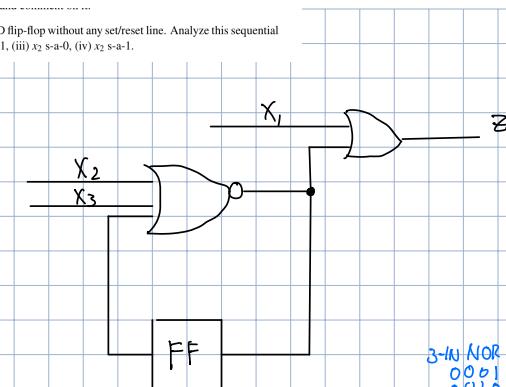
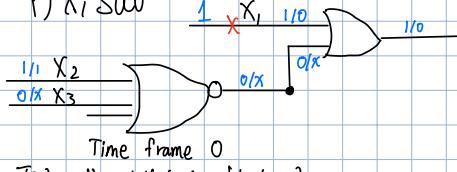


Figure 5.5 A circuit illustrating the self-hiding effect



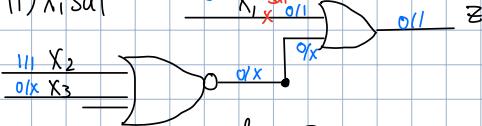
3-in NOR  
000  
001  
010  
011  
100  
101  
110  
111

i)  $x_1$  S-a-0



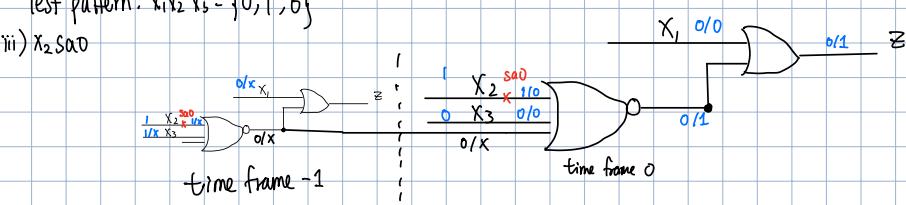
Time frame 0  
Test pattern:  $x_1 x_2 x_3 = \{1, 1, 0\}$

ii)  $x_1$  S-a-1



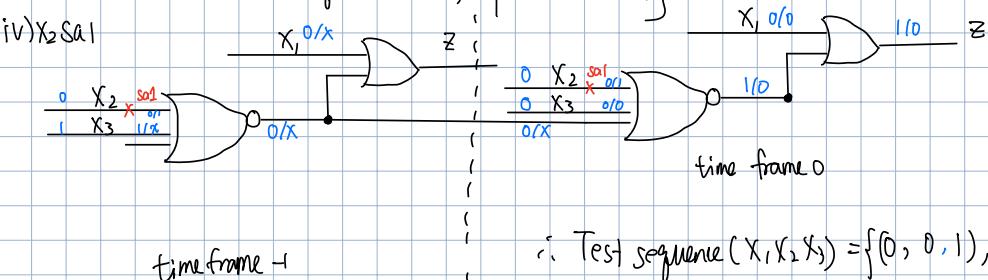
Time frame 0  
Test pattern:  $x_1 x_2 x_3 = \{0, 1, 0\}$

iii)  $x_2$  S-a-0

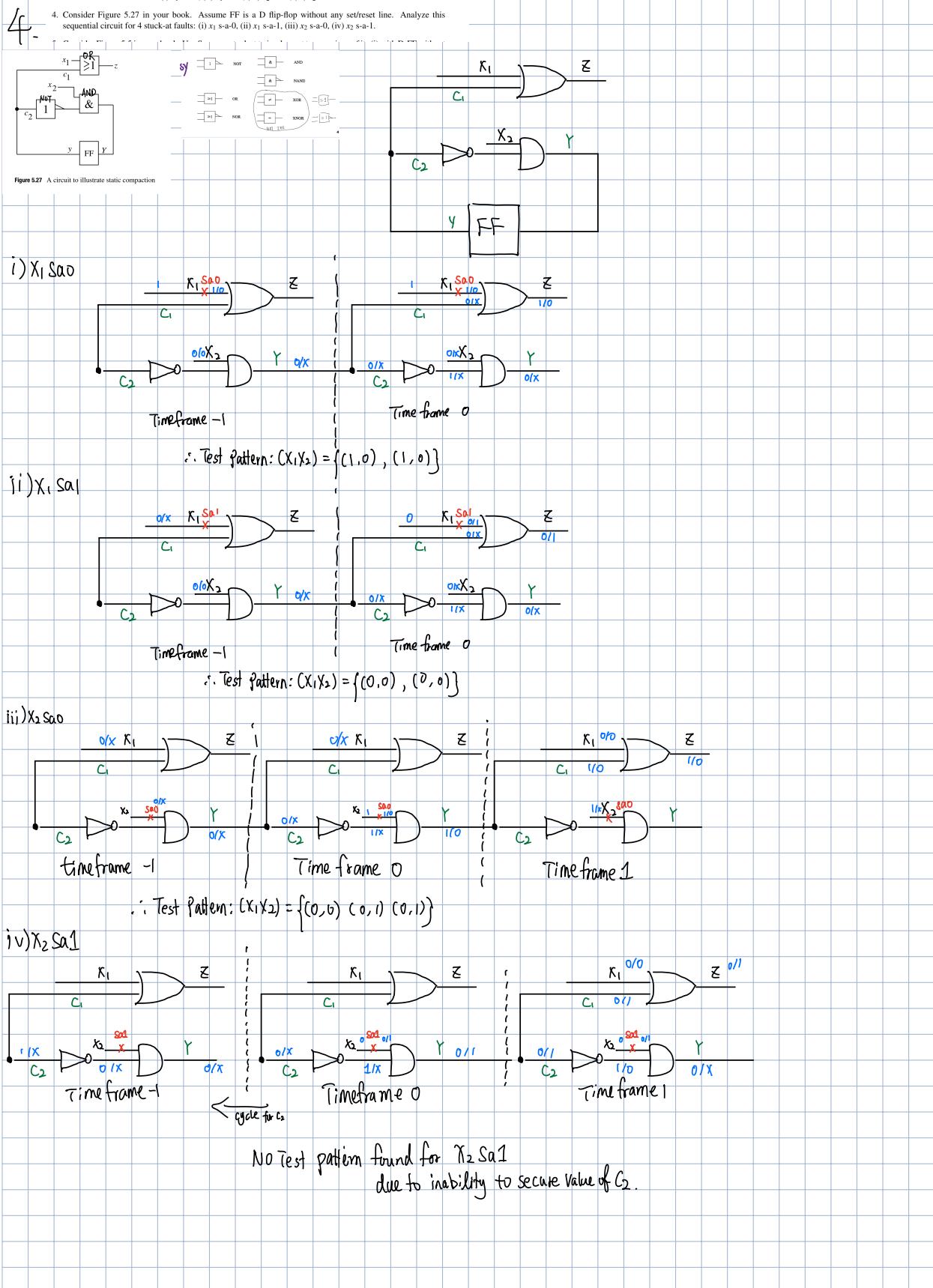


$\therefore$  Test sequence  $(x_1 x_2 x_3) = \{(0, 1, 1), (0, 1, 0)\}$

iv)  $x_2$  S-a-1



$\therefore$  Test sequence  $(x_1 x_2 x_3) = \{(0, 0, 1), (0, 0, 0)\}$



## 5-i DFF without set/reset

In Figure 1, the original VHDL was simulated using ModelSim to show its correct functionality. It is then elaborated in Design Vision with gtech profile. Since there is no NOR3 gate in gtech, an OA21 with inverted y1 line is used in its place, which may make the schematic differ as can be seen in Figure 2 and Figure 3. Comparing to previous analysis with combinational logic, the fault coverage is deteriorated to only ~20% instead of ~70%. The fault report and designed pattern used can be seen in Figure 4. Since a clock signal is needed to drive the DFF during testing, more primitive inputs can be seen in patterns provided by TetraMax.

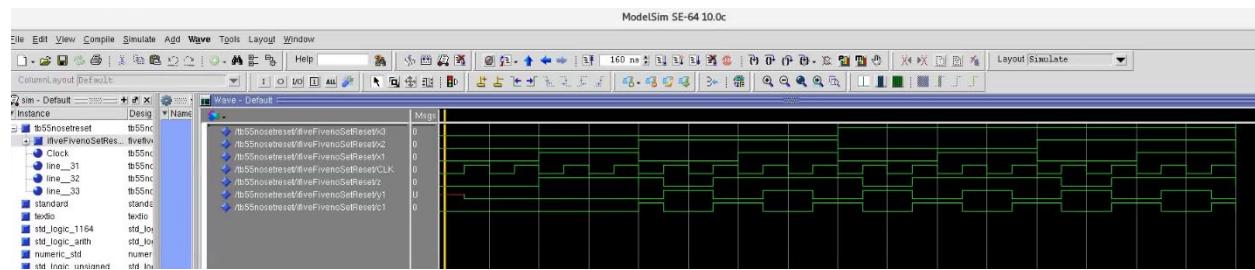


Figure 1 Waveform of 5.5(No Set/Reset) VHDL

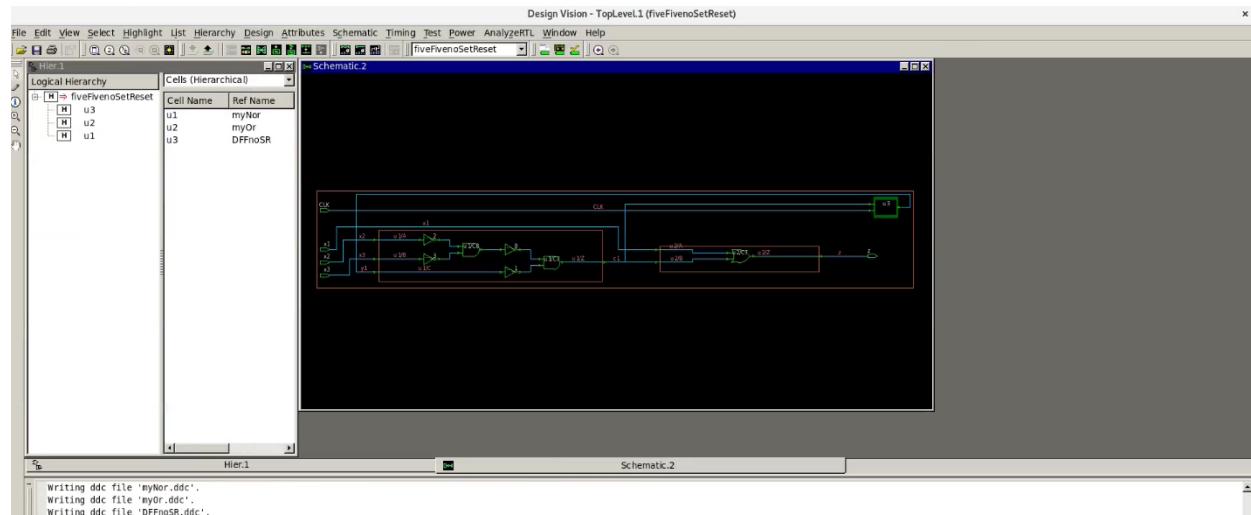


Figure 2 Schematic after Design Vision Elaboration

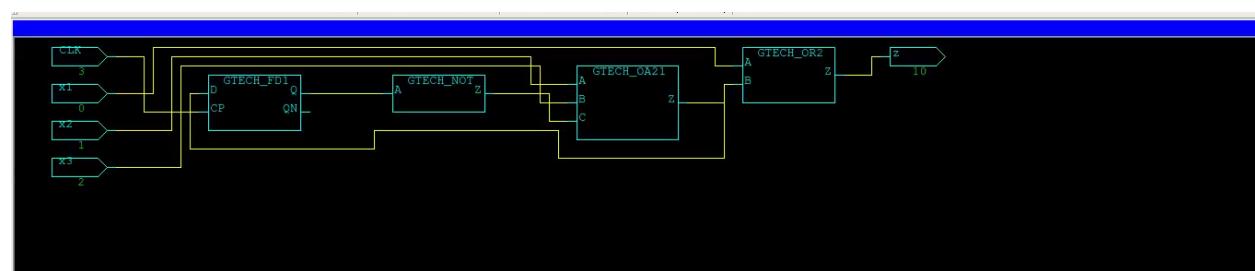


Figure 3 Schematic in TetraMax

TetraMAX - Synopsys Inc.

File Edit View Netlist Rules Scan Primitives Faults Patterns Buses Config

Cmd Save Transcript Transcript Increase Font Decrease Font Open G

Messages Netlist Build DRC Summary ATPG Write Pat. Write Test

-----

TEST-T> set\_faults -fault\_coverage  
Warning: Unused gate deletion affects fault coverage calculation. (M245)

TEST-T> remove\_faults -all  
Warning: Internal pattern set is now deleted. (M133)

34 faults were removed from the fault list.

TEST-T> add\_faults -all  
34 faults were added to fault list.

TEST-T> run\_atpg -ndetects 1  
ATPG performed for stuck fault model using internal pattern source.

#patterns #faults #ATPG faults test process  
stored detect/active red/au/abort coverage CPU time

-----  
Begin deterministic ATPG: #uncollapsed\_faults=10, abort\_limit=10...  
2 10 0 0/0/0 29.41% 0.00

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	10
Possibly detected	PT	0
Undetectable	UD	0
ATPG untestable	AU	24
Not detected	ND	0

total faults 34  
test coverage 29.41%  
fault coverage 29.41%

Pattern Summary Report

#internal patterns	2
#basic_scan patterns	2

-----

TEST-T> report\_faults -all  
TEST-T> report\_patterns -all -internal  
TEST-T>

Report Faults

sa0 -- u1/U1/A  
sa1 DS u1/U1/Z  
sa1 AN u1/U2/Z  
sa0 -- u1/U2/A  
sa0 -- u3/Q\_reg/Q  
sa1 -- u1/U1/C  
sa0 AN u1/U1/Z  
sa0 -- u1/U1/C  
sa0 -- u1/U2/Z  
sa1 -- u1/U2/A  
sa1 -- u3/Q\_reg/Q  
sa0 AN x3  
sa0 -- u1/U1/B  
sa1 AN u1/U1/A  
sa1 -- u1/U1/B  
sa1 -- x2  
sa1 -- x3  
sa0 AN u3/Q\_reg/CP  
sa0 -- CLK  
sa1 AN u3/Q\_reg/D  
sa0 AN u3/Q\_reg/D  
sa1 AN u3/Q\_reg/CP  
sa1 -- CLK  
sa0 AN u2/U1/B  
sa1 DS z  
sa1 -- u2/U1/Z  
sa1 -- u2/U1/A  
sa1 -- u2/U1/B  
sa1 -- x1  
sa0 DS z  
sa0 -- u2/U1/Z  
sa0 DS x1  
sa0 -- u2/U1/A

Report Patterns

Pattern 0 (basic\_scan)  
Time 0: force\_all\_pis = 1001  
Time 1: measure\_all\_pos = 1  
Pattern 1 (basic\_scan)  
Time 0: force\_all\_pis = 0001  
Time 1: measure\_all\_pos = 0

Figure 4 Fault Report and Test Patterns in TetraMax

## 5-ii DFF with set/reset

In Figure 5, the original VHDL with set and reset DFF was simulated using ModelSim to show its correct functionality. Its elaboration in Design Vision with gtech profile can be seen in Figure 6. Similarly, design vision replaced NOR3 with OA21 and inverted line y1. The fault report and designed pattern used can be seen in Figure 8. Since a clock signal is needed to drive the DFF during testing, and that set and reset deserve their own primitive input lines, more primitive inputs can be seen in patterns provided by TetraMax.

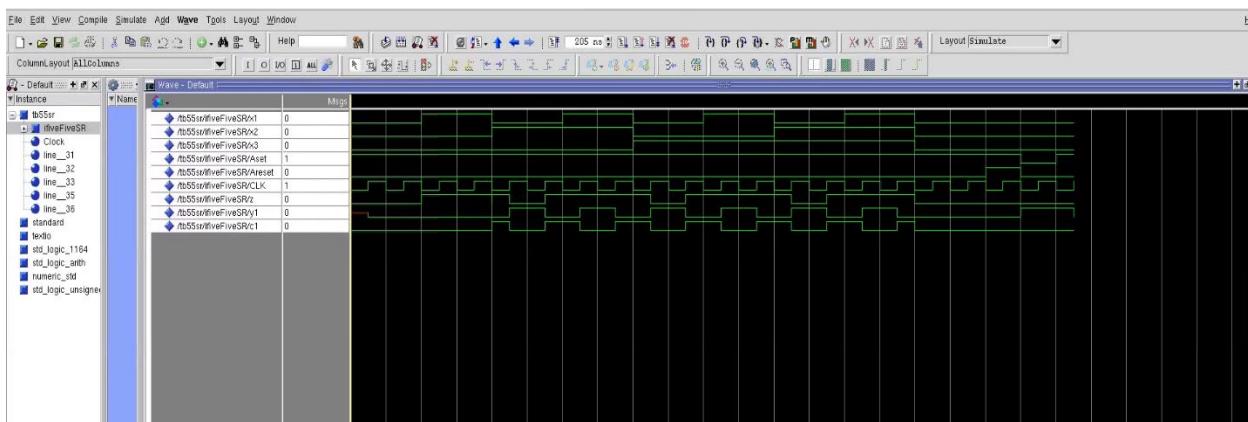


Figure 5 Waveform of 5.5(with Set/Reset) VHDL

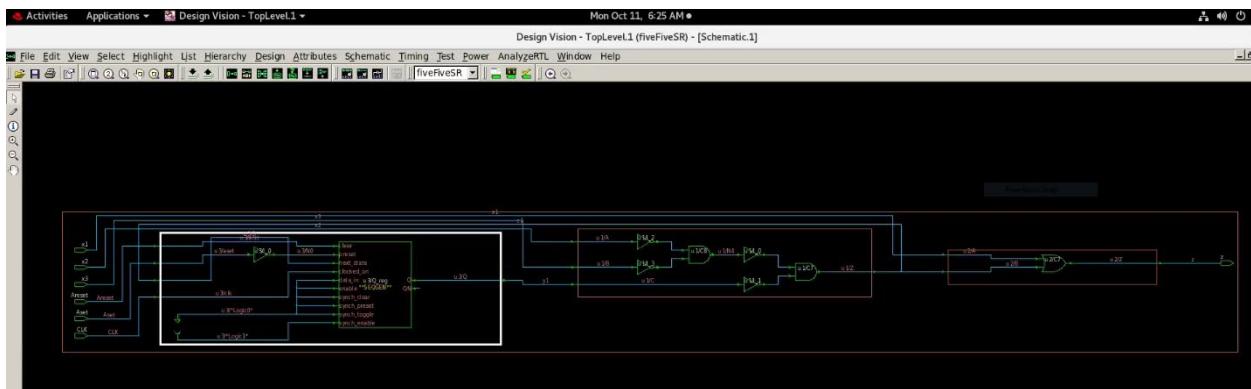


Figure 6 Schematic after Design Vision Elaboration

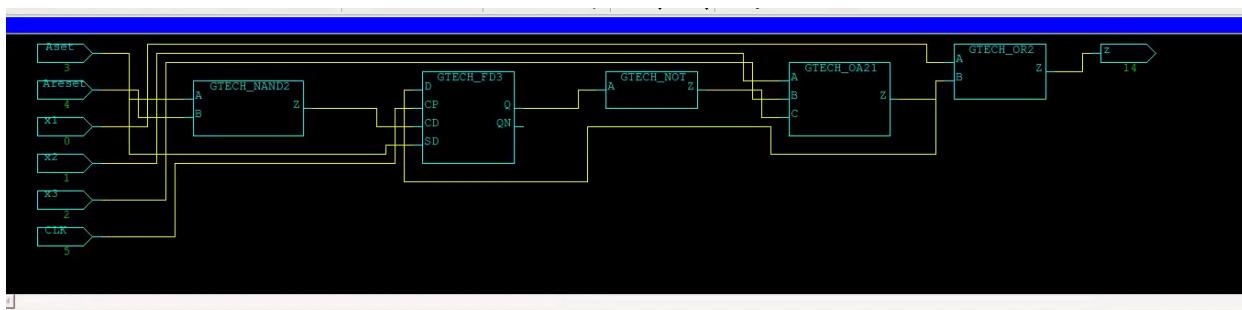


Figure 7 Schematic in TetraMax

```

Report Faults
sa0 AN x2
sa0 -- u1/U1/A
sa1 DS u1/U1/Z
sa1 AN u1/U2/Z
sa0 -- u1/U2/H
sa0 -- u3/Q_reg/Q
sa1 -- u1/U1/C
sa0 AN u1/U1/Z
sa0 -- u1/U1/C
sa0 -- u1/U2/Z
sa1 -- u1/U2/A
sa0 -- u3/Q_reg/Q
sa0 AN x3
sa0 -- u1/U1/B
sa1 AN u1/U1/A
sa1 -- u1/U1/B
sa1 -- x2
sa1 -- x3
sa0 AN Areset
sa1 AN Areset
sa1 AN u3/U3/Z
sa0 -- u3/U3/A
sa0 -- u3/U3/B
sa0 -- Areset
sa1 -- u3/Q_reg/CD
sa1 AN u3/Q_reg/D
sa1 AN u3/Q_reg/D
sa1 AN u3/U3/A
sa0 -- u3/Q_reg/CD
sa1 AN u3/Q_reg/SD
sa0 AN u3/Q_reg/SD
sa1 AN u3/Q_reg/CP
sa1 -- CLK
sa0 AN u3/Q_reg/CP
sa0 -- CLK
sa1 AN Areset
sa1 -- u3/U3/B
sa0 AN u2/U1/B
sa1 DS z
sa1 -- u2/U1/Z
sa1 -- u2/U1/A
sa1 -- u2/U1/B
sa1 -- x1
sa0 DS z
sa0 -- u2/U1/Z
sa0 DS x1
sa0 -- u2/U1/A

```

Figure 8 Fault Report and Test Pattern in TetraMax