## 5-i DFF without set/reset

In Figure 1, the original VHDL was simulated using ModelSim to show its correct functionality. It is then elaborated in Design Vision with gtech profile. Since there is no NOR3 gate in gtech, an OA21 with inverted y1 line is used in its place, which may make the schematic differ as can be seen in Figure 2 and Figure 3. Comparing to previous analysis with combinational logic, the fault coverage is deteriorated to only ~20% instead of ~70%. The fault report and designed pattern used can be seen in Figure 4. Since a clock signal is needed to drive the DFF during testing, more primitive inputs can be seen in patterns provided by TetraMax.

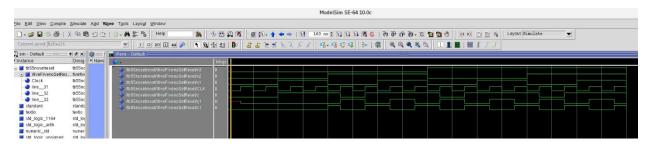


Figure 1 Waveform of 5.5(No Set/Reset) VHDL

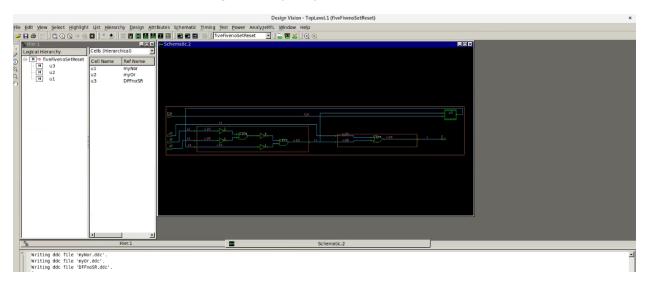


Figure 2 Schematic after Design Vision Elaboration

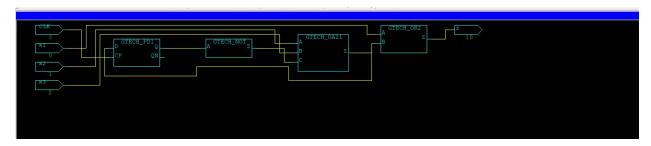


Figure 3 Schematic in TetraMax

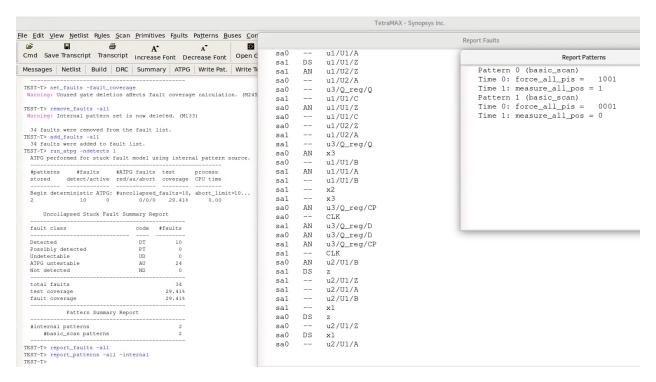


Figure 4 Fault Report and Test Patterns in TetraMax

## 5-ii DFF with set/reset

In Figure 5, the original VHDL with set and reset DFF was simulated using ModelSim to show its correct functionality. Its elaboration in Design Vision with gtech profile can be seen in Figure 6. Similarly, design vision replaced NOR3 with OA21 and inverted line y1The fault report and designed pattern used can be seen in Figure 8. Since a clock signal is needed to drive the DFF during testing, and that set and reset deserve their own primitive input lines, more primitive inputs can be seen in patterns provided by TetraMax.

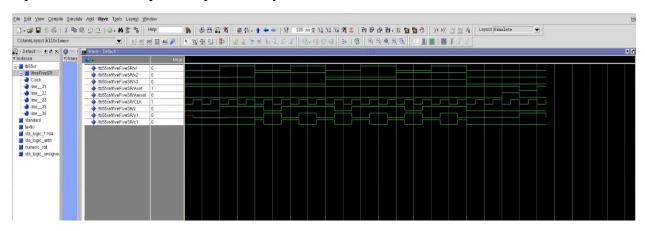


Figure 5 Waveform of 5.5(with Set/Reset) VHDL

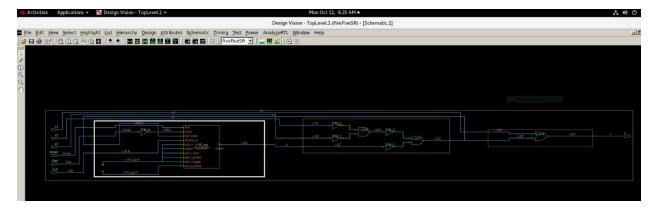


Figure 6 Schematic after Design Vision Elaboration

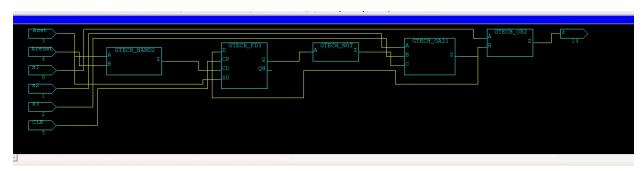


Figure 7 Schematic in TetraMax

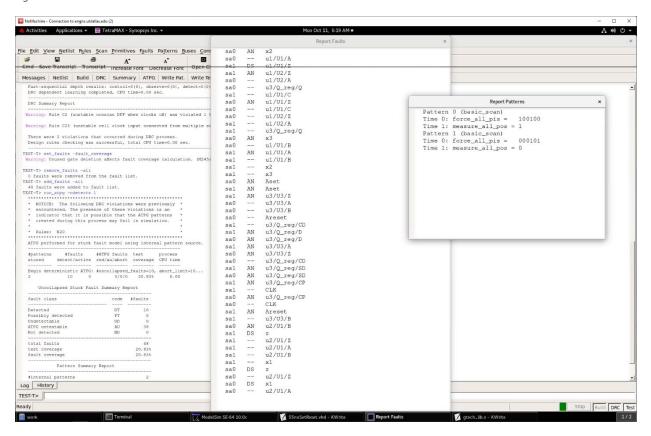


Figure 8 Fault Report and Test Pattern in TetraMax