

**EEDG/CE 6303: Testing and Testable Design (Fall'2021)**

**Department of Electrical & Computer Engineering**

**The University of Texas at Dallas**

**Instructor: Mehrdad Nourani (nourani@utdallas.edu)**

**Cover Page for All Submissions**

**(Assignment, Project, Codes/Simulations/CAD, Examinations, etc.)**

Last Name (as shown in the official UT Dallas Student ID Card): Feng

First Name: Yu

Submission Materials for (e.g. Homework #, Project #): HW 2

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- ii. I have acknowledged all material and sources used in its preparation, whether they be books, articles, reports, lecture notes, and any other kind of document, electronic or personal communication,
- iii. this report has not previously been submitted for assessment in EEDG/CE 6303 or any other course at UT Dallas or elsewhere,
- iv. I have not copied in part or whole or otherwise plagiarized the work of other students and/or persons, and
- v. I have read and understood the Department and University policies on scholastic dishonesty as outlined in: <http://www.utdallas.edu/deanofstudents/dishonesty/>.

Name: Yu Feng

Date: 9/23/2021

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3.2.3

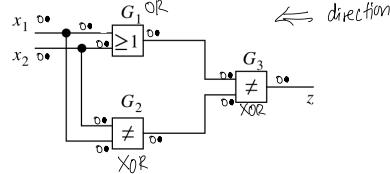
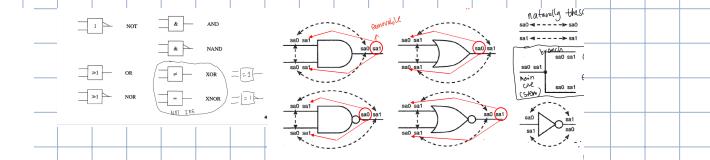
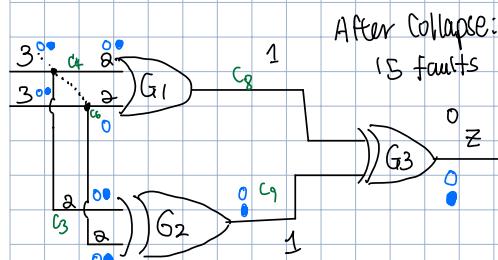
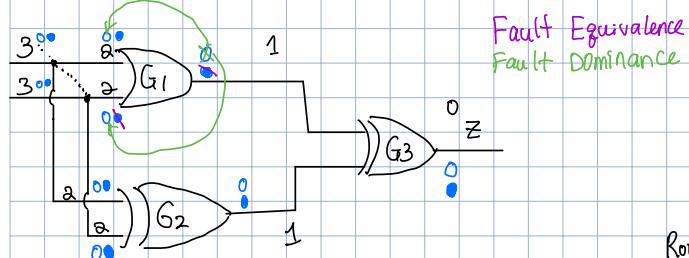
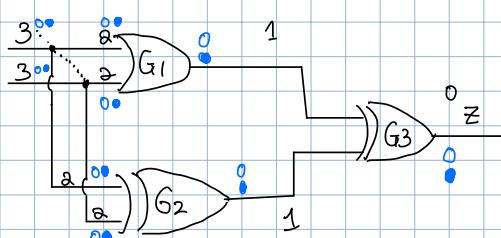
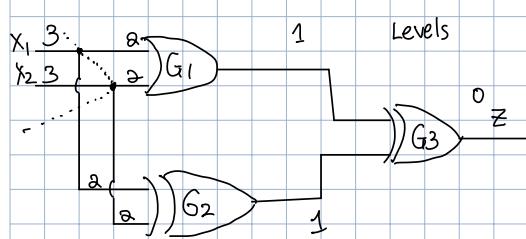
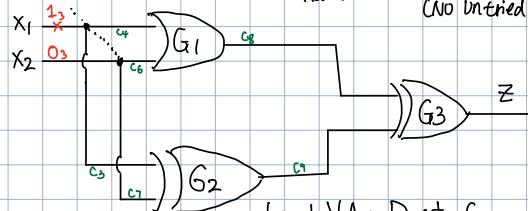


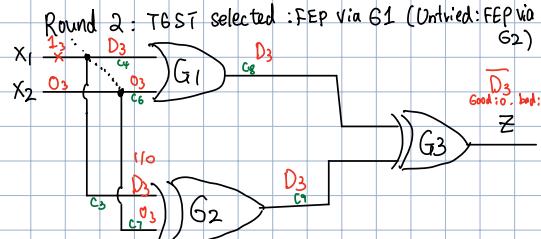
Figure 3.23 An example illustrating incompleteness of the equivalence and dominance relations



Test for  $X_1 = 1, X_2 = 0$   
Round 1: TGST Identified (No Untried)



$$\begin{aligned} D &= \{G_1, G_2\} \\ U &= \{\} \end{aligned}$$

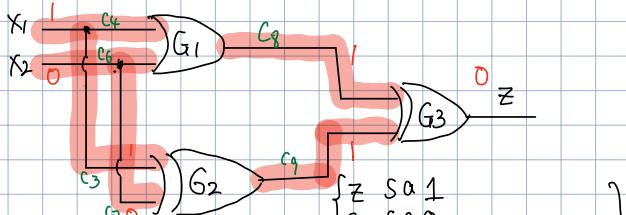


$$\begin{aligned} \text{Local VA: } & D_3 \text{ at } C_4 \\ & D_3 \text{ at } C_3 \\ D &= \{G_1, G_2\} \\ U &= \{\} \end{aligned}$$

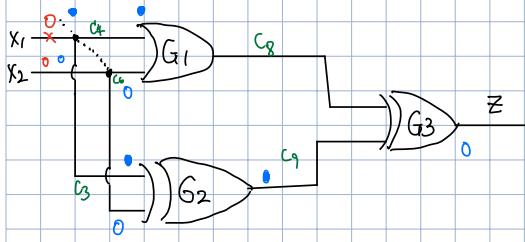
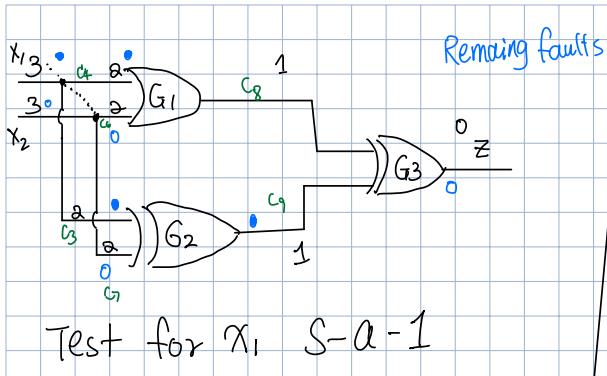
Round 3: TGST selected: FEP via G3 (Untried: FEP via G2)  
Local VA:  $\overline{D}_3$  at Z  
Untried Alternative: FEP via G2

$$\begin{aligned} D &= \{G_2\} \\ U &= \{\} \\ \therefore \text{Test pattern} &= \begin{cases} X_1 = 1 \\ X_2 = 0 \end{cases} \end{aligned}$$

Fault Simulation:



$$\text{Faults detectable by } \{1, 0\} = \begin{pmatrix} Z SA 1 \\ Z SA 0 \\ C3 SA 0 \\ C4 SA 0 X1 SA 0 \\ C4 SA 1 X2 SA 1 \\ G1 SA 1 \\ G2 SA 1 \end{pmatrix}$$



Round 1 : TGST Identified (No untried)

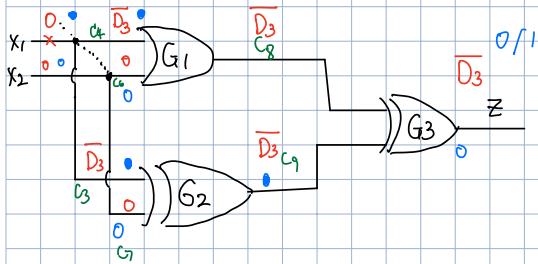
Local VA:  $\overline{D_3}$  at  $C_4$

$\overline{D_3}$  at  $C_3$

$$D = \{G_1, G_2\}$$

$$U = \{\}$$

Round 2 : TGST selected : FEP via G1 (Untried: FEP via G2)



Local VA:  $\overline{D_3}$  at  $C_8$

Untried Alternative: FEP via G2

$$D = \{G_3, G_2\}$$

$$U = \{\}$$

Round 3: TGST selected: FEP via G3 (Untried: FEP via G2)

Local VA:  $\overline{D_3}$  at  $Z$

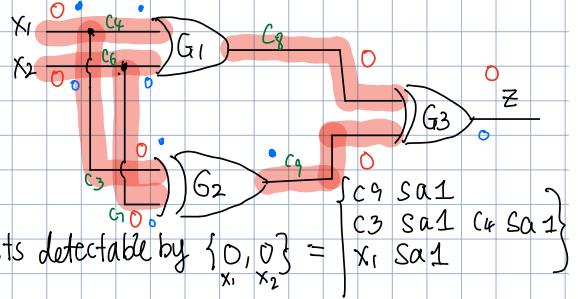
Untried Alternative: FEP via G2

$$D = \{G_2\}$$

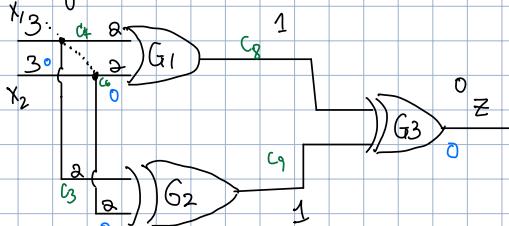
$$U = \{\}$$

$$\therefore \text{Test pattern} = X_1 = 0 \\ X_2 = 0$$

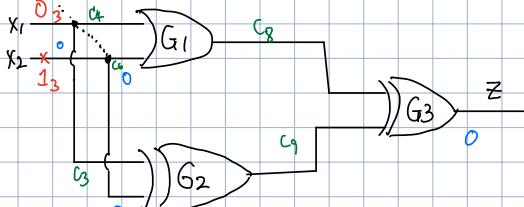
Fault Simulation:



Remaining faults:



Test for  $X_2 = 0$



Round 1 : TGST Identified (No untried)

Local VA:  $D_3$  at  $C_6$

$D_3$  at  $C_7$

$$D = \{G_1, G_2\}$$

$$U = \{\}$$

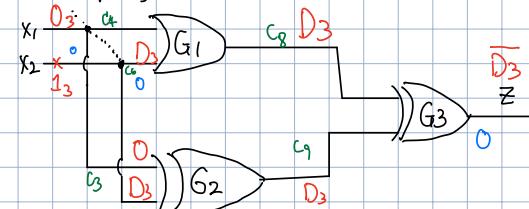
Round 2 : TGST selected : FEP via G1 (Untried: FEP via G2)

Local VA:  $D_3$  at  $C_8$

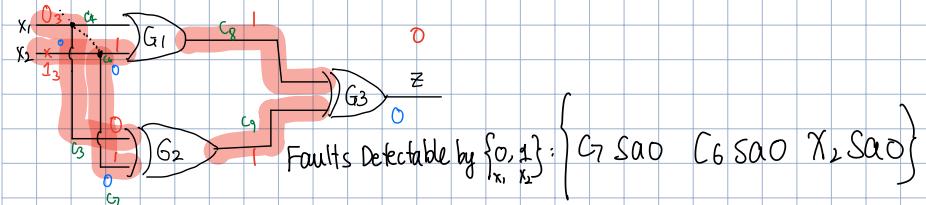
Untried Alternative: FEP via G2

$$D = \{G_3, G_2\}$$

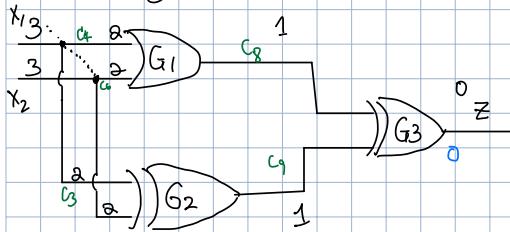
$$U = \{\}$$



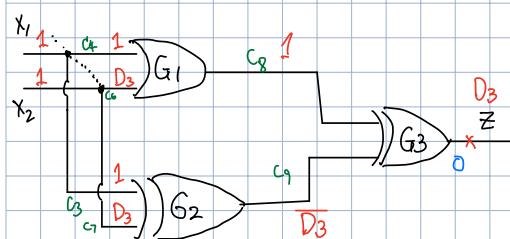
### Fault Simulation:



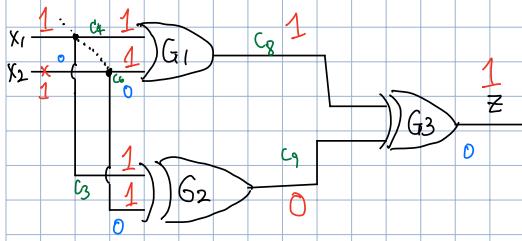
### Remaining faults



Test for  $Z \text{ SAO}$



Fault Simulation:



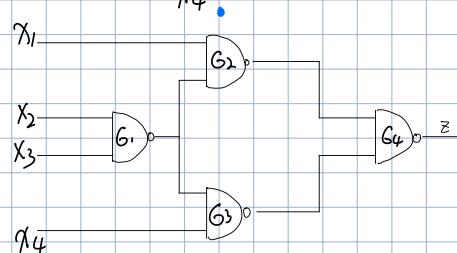
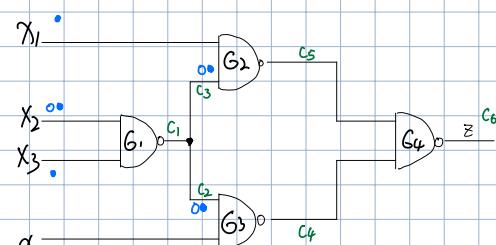
$$\text{Faults detectable by } \{1, 0\}_{x_1, x_2} = \begin{cases} Z \text{ SAO} \\ C_9 \text{ SAO} \\ C_3 \text{ SAO} \\ G \text{ SA1} \\ C_4 \text{ SA0 } X_1 \text{ SAO} \\ X_2 \text{ SA1} \end{cases}$$

$$\text{Faults detectable by } \{0, 0\}_{x_1, x_2} = \begin{cases} C_9 \text{ SA1} \\ C_3 \text{ SA1} \\ C_4 \text{ SA1} \\ X_1 \text{ SA1} \end{cases}$$

$$\text{Faults Detectable by } \{0, 1\}_{x_1, x_2}: \{C_7 \text{ SAO}, C_6 \text{ SAO}, X_2 \text{ SAO}\}$$

$$\text{Faults detectable by } \{1, 1\}: \{Z \text{ SAO}\}$$

All Faults are Covered.



NAND

0	0	1
0	1	1
1	0	1
1	1	0

For circuit 3.23, The schematic of which the VHDL represents can be seen in Figure 1. The VHDL code can be found in the 323 folder.

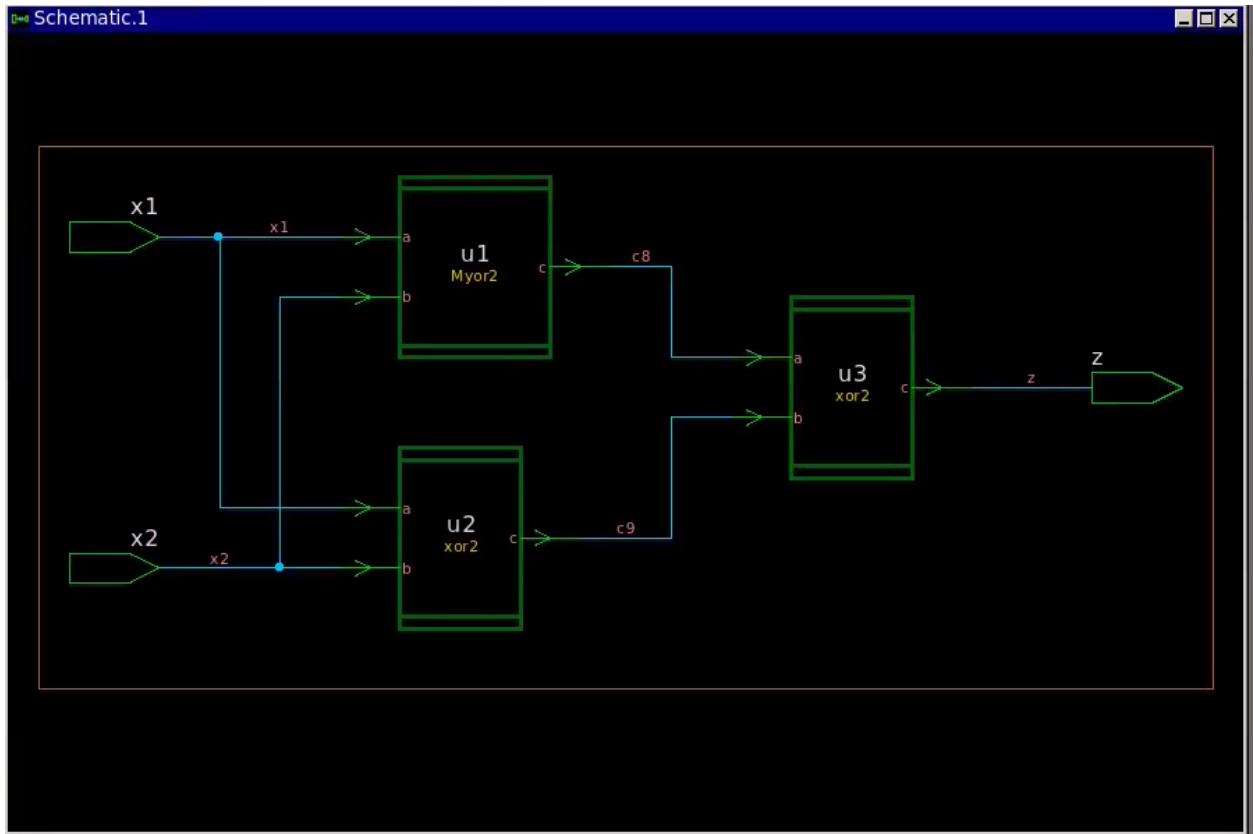


Figure 1 Schematic of circuit 3.23

Simulation waveform presented in Figure 2 shows that it functions the same as circuit 3.23.

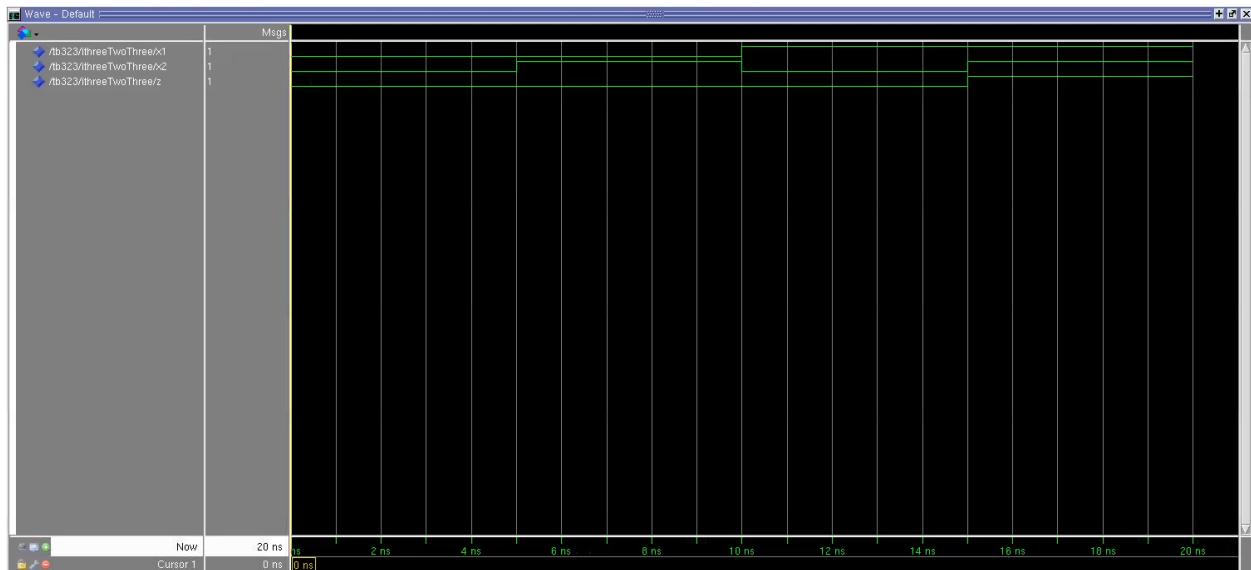


Figure 2 Waveform of VHDL Simulation

The synthesis result, which reports the timing and area, can be found in the threeTwoThree.report in 323 folder. The post-synthesis VHDL code can be found in the folder as well.

After importing the VHDL into TetraMax, shown in Figure 3, and build the ATPG model followed by the design rule check using the tool, one can see the schematic shown in TetraMax remains the same as Figure 1.

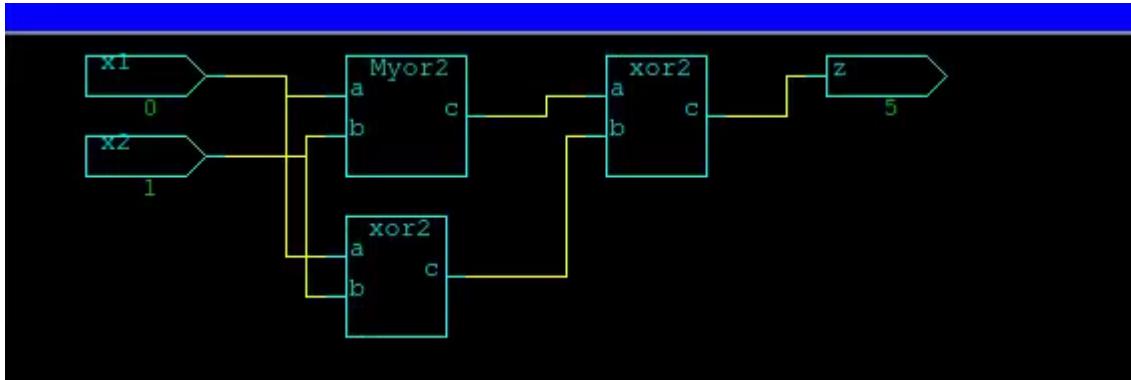


Figure 3 Schematic of 3.23 in TetraMax

All faults were able to be detected using ATPG. Since TetraMax sees faults on the same wire as different ones, 24 faults were detected before collapsing. Figure 4 shows the faults found, and Figure 5 shows the patterns used.

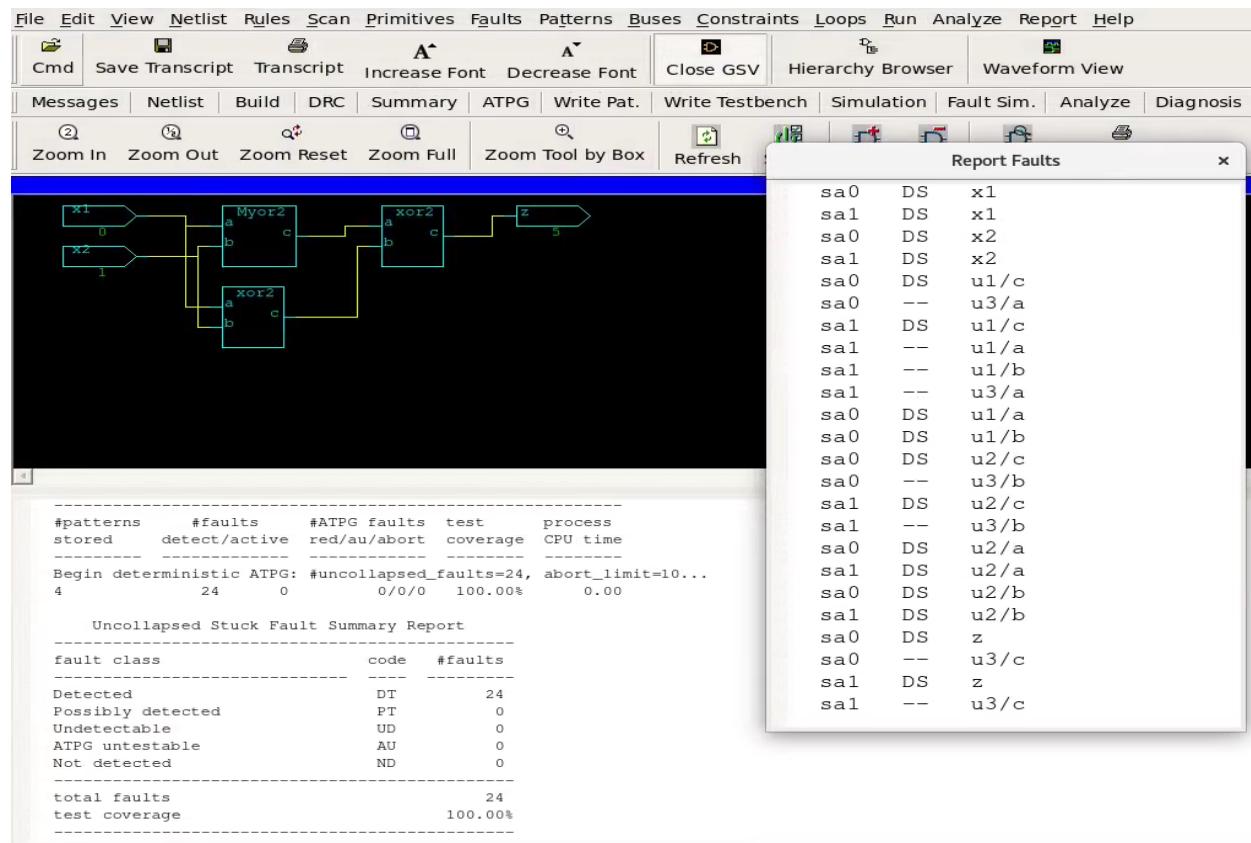


Figure 4 Faults in circuit 3.23

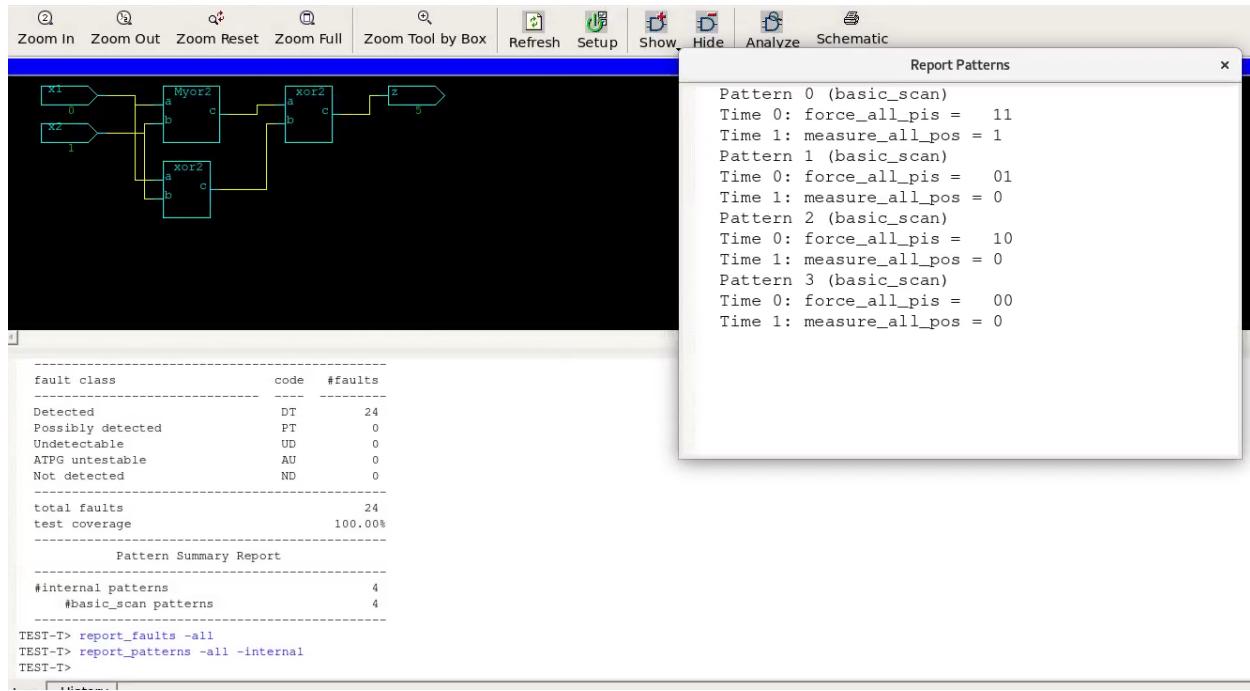
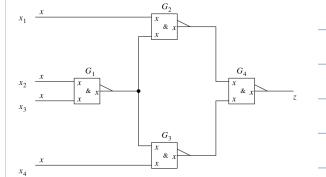


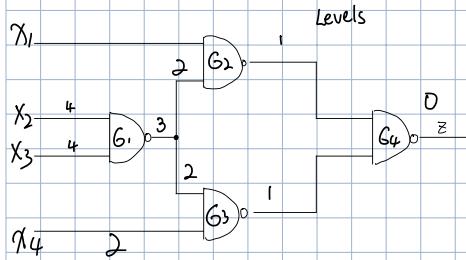
Figure 5 Patterns used in finding faults

As can be seen, the patterns used to test faults are the same as the hand-work analysis. The reason of discrepancy in fault count is fault collapsing using fault equivalence and fault dominance theory reduces the need to repeatedly examine faults that do not provide new knowledge.

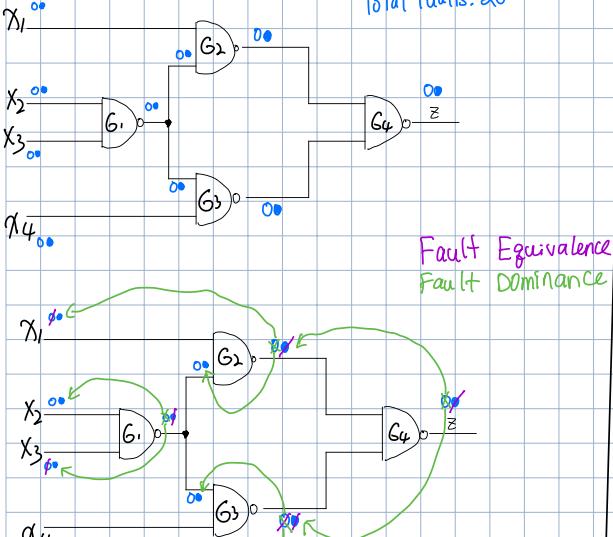
3.28



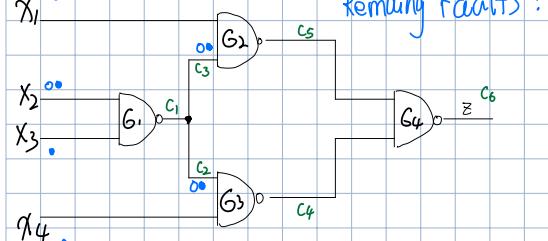
Levels



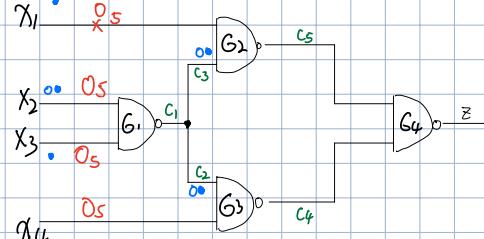
Total faults: 20



Remaining faults: 9



Test for  $x_1$ , SA1



Round 1: TGST Identified FEE

Local VA:  $D_5$  at  $x_1$

$$D = \{G_2\}$$

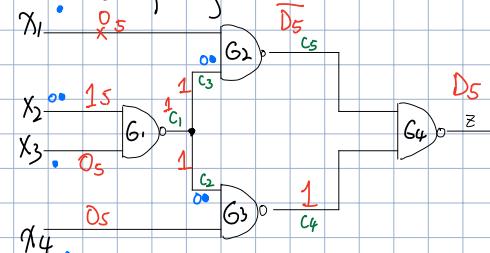
$$U = \{\}$$

Round 2: TGST selected: FEP via  $G_2$  (Untried: None)

Local VA:  $D_5$  at  $C_5$

$$D = \{G_4\}$$

$$U = \{\}$$



Round 3: TGST Selected: FEP via  $G_4$

(Untried: None)

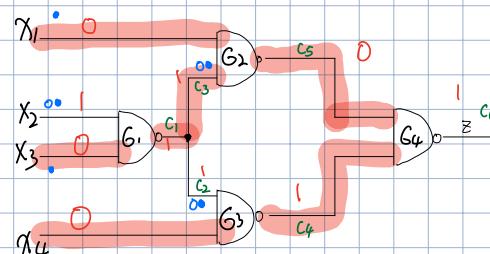
$$D = \{\}$$

$$U = \{\}$$

$\therefore$  Test pattern:  $x_1, x_2, x_3, x_4$

$$= \{0, 1, 0, 0\}$$

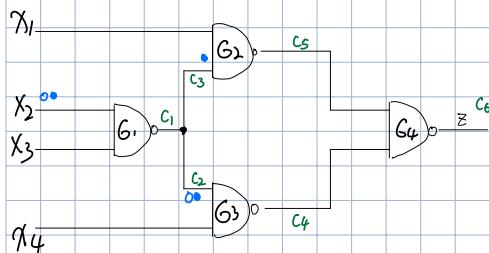
Fault Simulation:



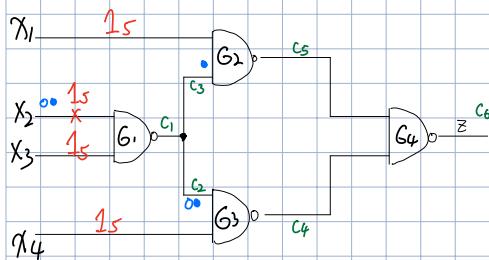
Faults detectable by  $\{0, 1, 0, 0\}$  are:

$$\begin{cases} x_1 \text{ SA1} \\ C_3 \text{ SA0} \\ x_3 \text{ SA1} \\ x_4 \text{ SA1} \end{cases}$$

Remaining Faults :



Testing for  $X_2$  SA0



Round 1 : TGST identified FEE

Local VA :  $D_5$  at  $X_2$

$$D = \{G_1\}$$

$$U = \{\}$$

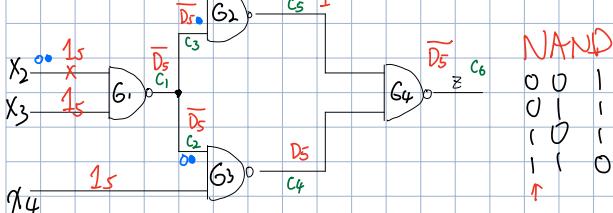
Round 2 : TGST selected : FEP via  $G_1$  (Untried : Nonl )

Local VA :  $D_5$  at  $C_2$ ,  $\overline{D}_5$  at  $C_3$

$$D = \{G_2, G_3\}$$

$$U = \{\}$$

$X_1$  0s



Round 3 : TGST selected : FEP via  $G_3$  ( Untried : FEP via  $G_2$  )

Local VA :  $D_5$  at  $C_4$

$$D = \{G_2\}$$

$$U = \{\}$$

Round 4 : TGST selected : FEP via  $G_4$

Local VA :  $\overline{D}_5$  at  $Z$

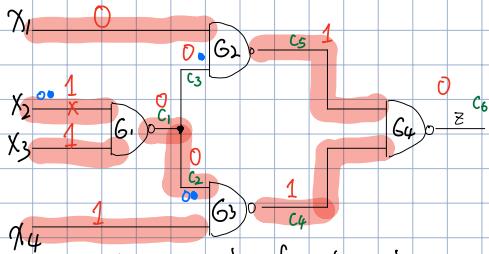
$$D = \{G_2\}$$

$$U = \{\}$$

∴ Test pattern

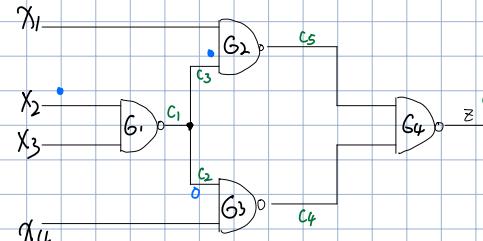
$$X_1 X_2 X_3 X_4 \{ 0, 1, 1, 1 \}$$

Fault Simulation:

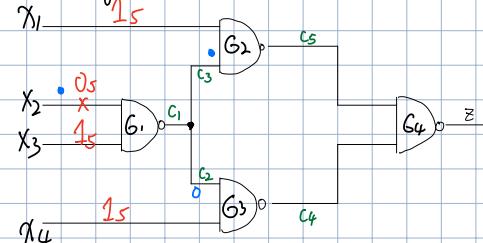


faults detectable by  $\{ 0, 1, 1, 1 \}$  are  
 $\{ G_2 \text{ Sa1} \}$   
 $\{ X_2 \text{ Ca0} \}$

Remaining Faults :



Testing for  $X_2$  Sa1



Round 1 : TGST identified FEE

Local VA :  $\overline{D}_5$  at  $X_2$

$$D = \{G_1\}$$

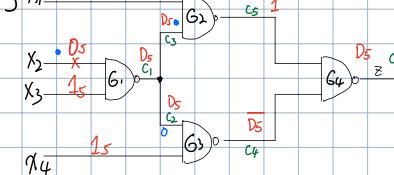
$$U = \{\}$$

Round 2 : TGST selected : FEP via  $G_1$  ( Untried : Nonl )

Local VA :  $D_5$  at  $C_2$ ,  $D_5$  at  $C_3$

$$D = \{G_2, G_3\}$$

$$U = \{ \}$$



Round 3 : TGST selected : FEP via  $G_3$  (Untried : FEP via  $G_2$ )

Local VA :  $D_5$  at  $C_4$

$$D = \{G_2\}$$

$$U = \{\}$$

Round 4 : TGST selected : FEP via  $G_4$

Local VA :  $D_5$  at  $Z$

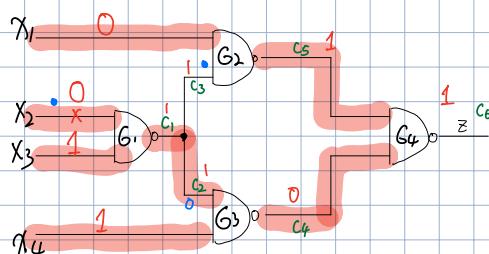
$$D = \{G_4\}$$

$$U = \{\}$$

$\therefore$  Test pattern

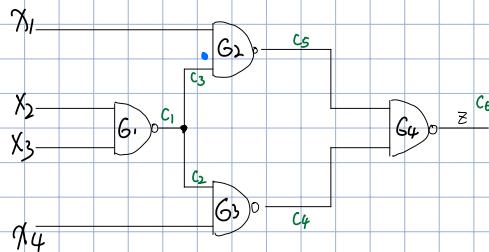
$$X_1, X_2, X_3, X_4 \in \{0, 0, 1, 1\}$$

Fault Simulation:

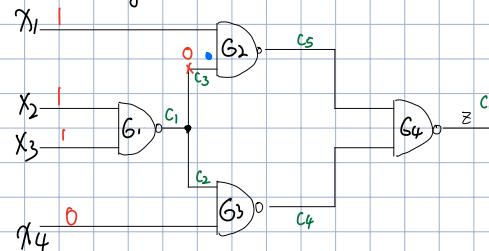


Faults detectable by  $\{0, 0, 1, 1\}$  are  
 $\{C_2 S_{A0}, C_2 S_{A1}\}$

Remaining Faults :



Testing for  $C_3 S_{A1}$



Round 1 : TGST Identified FEE

Local VA :  $\overline{D_5}$  at  $C_3$

$$D = \{G_2\}$$

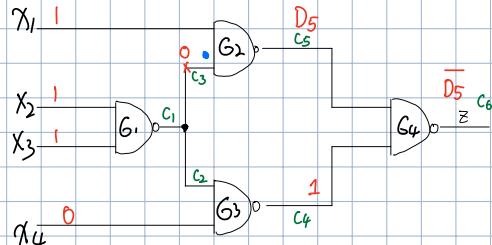
$$U = \{\}$$

Round 2 : TGST selected : FEP via  $G_2$  (Untried : None)

Local VA :  $D_5$  at  $C_3$

$$D = \{G_2\}$$

$$U = \{\}$$



Round 3 : TGST selected : FEP via  $G_4$  (Untried : None)

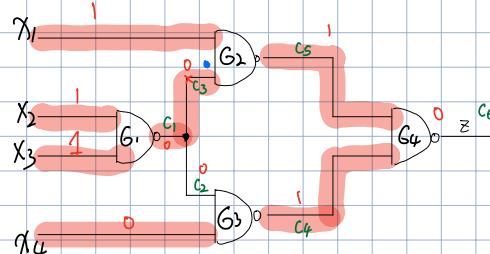
VA :  $\overline{D_5}$  at  $Z$

$$D = \{\}$$

$$U = \{\}$$

$\therefore$  Test pattern is  $\{1, 1, 1, 0\}$

Fault Simulation:



Faults detectable by  $\{1, 1, 1, 0\}$  is  
 $\{C_3 S_{A1}\}$

Faults detectable by  $\{0, 1, 0, 0\}$  are:

$$\{X_1 S_{A1}, C_3 S_{A0}, X_3 S_{A1}\}$$

Faults detectable by  $\{0, 1, 1, 1\}$  are

$$\{C_2 S_{A1}\}$$

Faults detectable by  $\{0, 0, 1, 1\}$  are

$$\{C_2 S_{A0}\}$$

Faults detectable by  $\{1, 1, 1, 0\}$  is  $\{C_3 S_{A1}\}$

All 9 faults are covered.

For circuit 3.28, The schematic of which the VHDL represents can be seen in Figure 7. The VHDL code can be found in the folder named 328. Figure 6 shows the simulation waveform, proving its correct functionality.

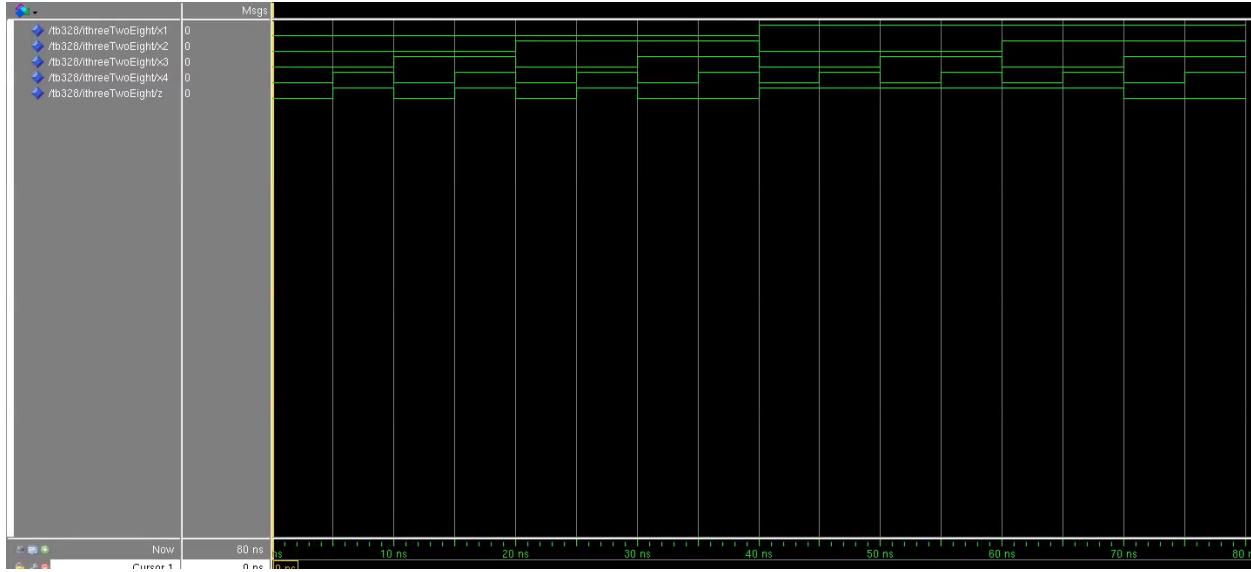


Figure 6 Waveform of Circuit 3.28

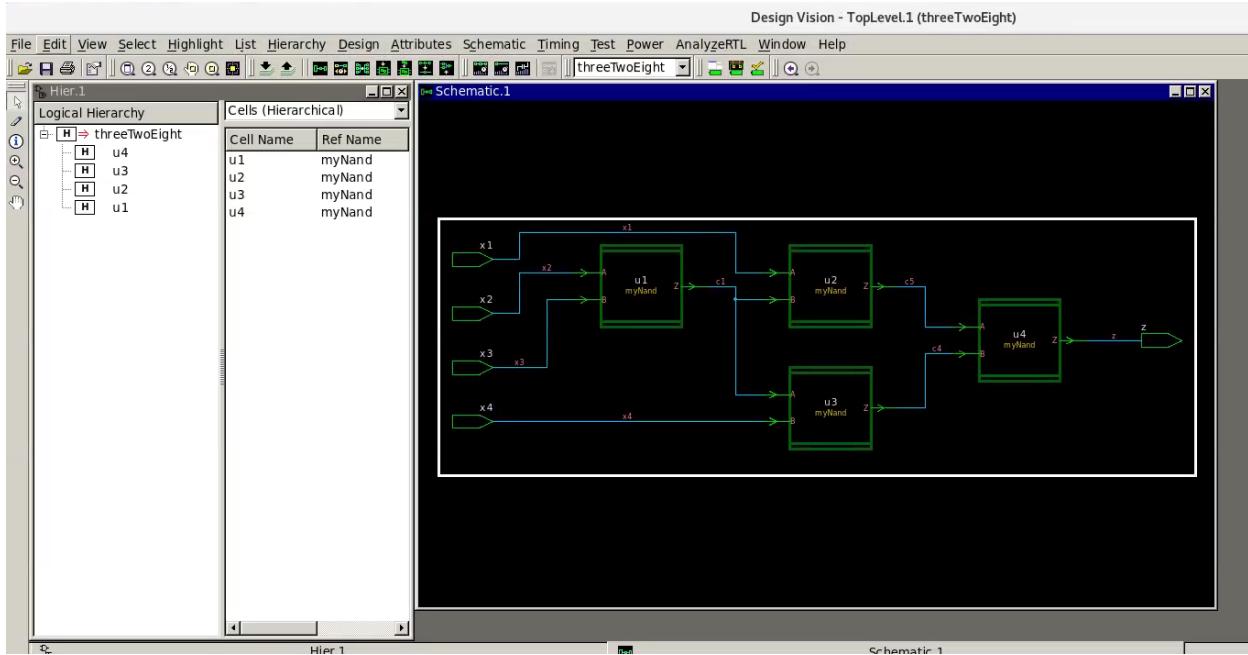


Figure 7 Schematic view of Circuit 3.28

The synthesis result, which reports the timing and area, can be found in the threeTwoEight.report in 328 folder. The post-synthesis VHDL code can be found in the folder as well.

After importing into TetraMax, and have ATPG model built followed by design rule checked, the same the schematic in Figure 8, presented by TetraMax, matches that of Figure 7.

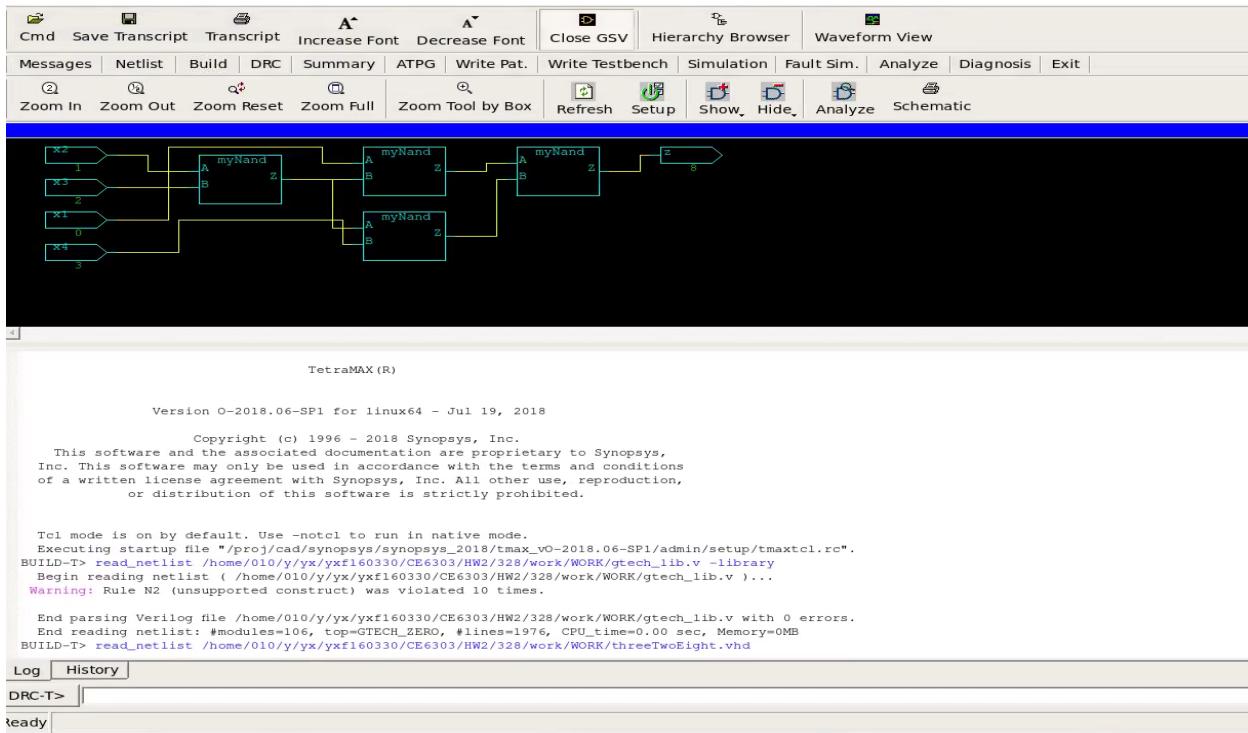


Figure 8 Schematic presented in TetraMax for Circuit 3.28

Thus, after running ATPG, faults can be reported as seen in Figure 9 and patterns used are reported in Figure 10.

The screenshot shows the TetraMAX (R) software interface with a transcript log on the left and a 'Report Faults' table on the right.

**Transcript Log (Left):**

```

File Edit View Netlist Rules Scan Primitives Faults Patterns Buses Constraints Loops Run Analyze Report Help
Cmd Save Transcript Transcript Increase Font Decrease Font Open GSV Hierarch
Messages Netlist Build DRC Summary ATPG Write Pat. Write Testbench S
Fast-sequential depth results: control=0(0), observe=0(0), detect=0(0), CPU time
DRC dependent learning completed, CPU time=0.00 sec.
-----
DRC Summary Report
No violations occurred during DRC process.
Design rules checking was successful, total CPU time=0.00 sec.
-----
TEST-T> remove_faults -all
0 faults were removed from the fault list.
TEST-T> add_faults -all
34 faults were added to fault list.
TEST-T> run_atpg -ndetects 1
ATPG performed for stuck fault model using internal pattern source.
-----
#patterns #faults #ATPG faults test process
stored detect/active red/au/abort coverage CPU time
-----
Begin deterministic ATPG: #uncollapsed_faults=34, abort_limit=10...
6 34 0 0/0/0 100.00% 0.00

Uncollapsed Stuck Fault Summary Report
-----
fault class code #faults
-----
Detected DT 34
Possibly detected PT 0
Undetectable UD 0
ATPG untestable AU 0
Not detected ND 0
-----
total faults 34
test coverage 100.00%
-----
Pattern Summary Report
-----
#internal patterns 6
#basic_scan patterns 6
-----
TEST-T> report_faults -all
TEST-T>

```

**Report Faults (Right):**

	Report Faults
sa0	-- u2/A
sa0	-- u2/B
sa0	-- x1
sal	-- u4/A
sal	DS x1
sal	-- u2/A
sal	DS u3/Z
sa0	-- u3/B
sa0	-- u3/A
sa0	-- x4
sal	-- u4/B
sal	DS x4
sal	-- u3/B
sal	DS z
sal	-- u4/Z
sa0	-- u4/A
sa0	-- u4/B
sa0	-- u2/Z
sa0	-- u3/Z
sal	DS u2/B
sal	DS u3/A
sa0	DS z
sa0	-- u4/Z
sal	DS u1/Z
sa0	-- u1/A
sa0	-- u1/B
sa0	-- x2
sa0	-- x3
sal	DS x2
sal	-- u1/A
sal	DS x3
sal	-- u1/B
sa0	DS u1/Z

Figure 9 Faults Report for 3.28

TetraMAX - Synopsys Inc.

**File Edit View Netlist Rules Scan Primitives Faults Patterns Buses Constraints Loops Run Analyze Report Help**

**Cmd Save Transcript Transcript Increase Font Decrease Font**

**Messages Netlist Build DRC Summary ATPG Write Report Patterns**

```

DRC dependent learning completed, CPU time=0.00 sec.
-----
DRC Summary Report
-----
No violations occurred during DRC process.
Design rules checking was successful, total CPU time=0.00
-----
TEST-T> remove_faults -all
0 faults were removed from the fault list.
TEST-T> add_faults -all
34 faults were added to fault list.
TEST-T> run_atpg -ndetects 1
ATPG performed for stuck fault model using internal pattern
-----
#patterns #faults #ATPG faults test process
stored detect/active red/au/abort coverage CPU tim
----- -----
Begin deterministic ATPG: #uncollapsed_faults=34, abort_l
6           34      0       0/0/0   100.00%    0.0

Uncollapsed Stuck Fault Summary Report
-----
fault class          code #faults
----- -----
Detected             DT    34
Possibly detected    PT    0
Undetectable         UD    0
ATPG untestable     AU    0
Not detected         ND    0
-----
total faults          34
test coverage        100.00%
-----
Pattern Summary Report
-----
#internal patterns      6
#basic_scan patterns    6
-----
TEST-T> report_faults -all
TEST-T> report_patterns -all -internal
TEST-T>

```

**Report Patterns**

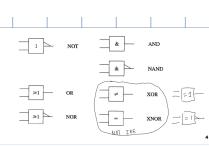
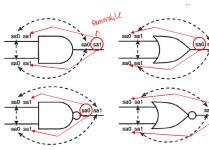
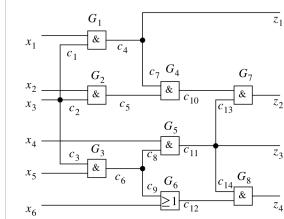
Time 0: force\_all\_pis = 1000  
Time 1: measure\_all\_pos = 1  
Pattern 1 (basic\_scan)  
Time 0: force\_all\_pis = 0111  
Time 1: measure\_all\_pos = 0  
Pattern 2 (basic\_scan)  
Time 0: force\_all\_pis = 1110  
Time 1: measure\_all\_pos = 0  
Pattern 3 (basic\_scan)  
Time 0: force\_all\_pis = 0010  
Time 1: measure\_all\_pos = 0  
Pattern 4 (basic\_scan)  
Time 0: force\_all\_pis = 0011  
Time 1: measure\_all\_pos = 1  
Pattern 5 (basic\_scan)  
Time 0: force\_all\_pis = 1100  
Time 1: measure\_all\_pos = 1

**Exit**

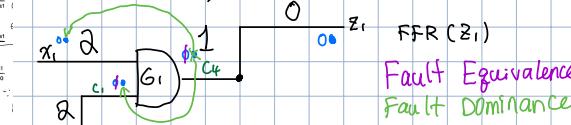
Figure 10 Pattern Report for 3.28

Due to the usage of fault collapsing and critical path tracing, hand-work uses less pattern to detect all faults than TetraMax, and less faults need to be analysed.

3.36



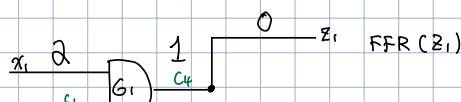
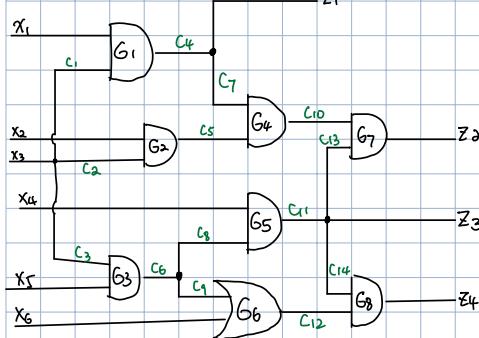
FOR FFR( $Z_1$ )



Fault Equivalence  
Fault Dominance

Remaining Faults: 5

FFR( $Z_1$ )



Test for  $x_1 = 0$

Round 1 : TGSF identified FEE

Local VA:  $D_7$  at  $x_1$

$$D = \{G_1\}$$

$$U = \{\}$$

Round 2 : TGSF selected : FEP via  $G_1$  (Untwisted : Nonl )

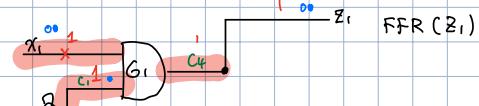
Local VA:  $D_7$  at  $Z_1$

$$D = \{ \}$$

$$U = \{ \}$$

$\therefore$  Test Pattern:  $x_1 x_2 x_3 x_4 x_5 x_6$   
 $= \{1, X, 1, X, X, X\}$

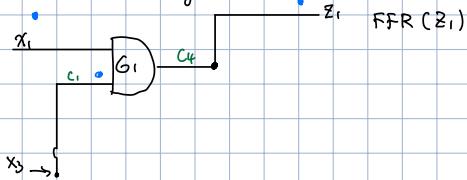
Fault Simulation:

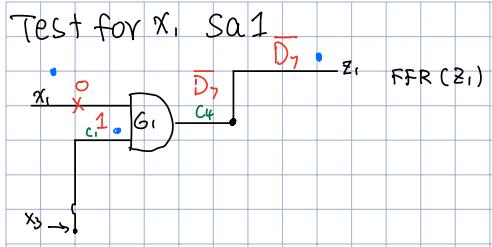


Faults detectable by  $\{1, X, 1, X, XX\}$

$$\begin{cases} Z_1 = 0 \\ X_1 = 0 \end{cases}$$

Remaining Faults:





Round 1 : TGST identified FEE

Local VA :  $\overline{D_7}$  at  $x_1$

$$D = \{G_1\}$$

$$U = \{\}$$

Round 2 : TGST selected : FEP via  $G_1$  (Untried : Nonl )

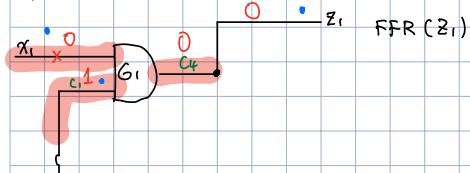
Local VA :  $\overline{D_7}$  at  $z_1$

$$D = \{\}$$

$$U = \{\}$$

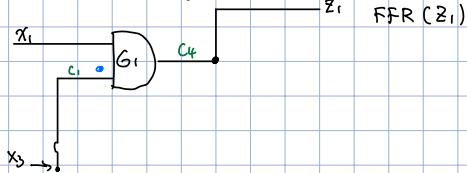
∴ Test Pattern :  $x_1, x_2, x_3, x_4, x_5, x_6$   
 $= \{0, X, 0, X, X, X\}$

Fault Simulation:

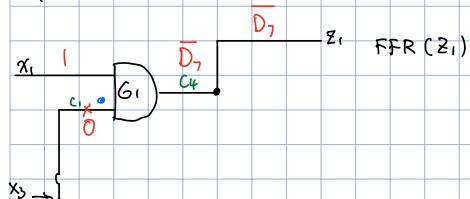


faults detectable by  $\{0, X, 1, X, XX\}$   
 $\{z_1, S_{a1}\}$   
 $\{x_1, S_{a1}\}$

Remaining Faults:



Test for  $C_1 S_{a1}$



Round 1 : TGST identified FEE

Local VA :  $\overline{D_7}$  at  $C_1$

$$D = \{G_1\}$$

$$U = \{\}$$

Round 2 : TGST selected : FEP via  $G_1$  ( Untried : Nonl )

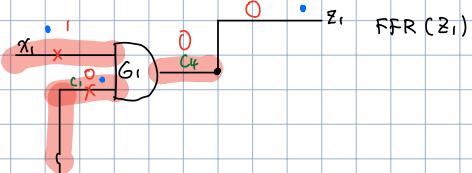
Local VA :  $D_7$  at  $z_1$

$$D = \{ \}$$

$$U = \{ \}$$

∴ Test Pattern :  $x_1, x_2, x_3, x_4, x_5, x_6$   
 $= \{1, X, 0, X, X, X\}$

Fault Simulation:

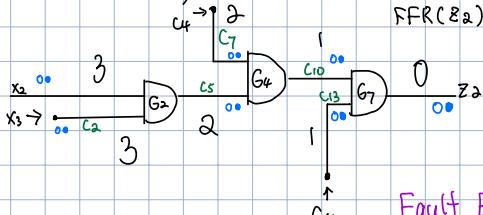


Fault detectable by  $\{1, X, 0, X, X, X\}$   
 $\{z_1, S_{a1}\}$   
 $\{x_1, S_{a1}\}$

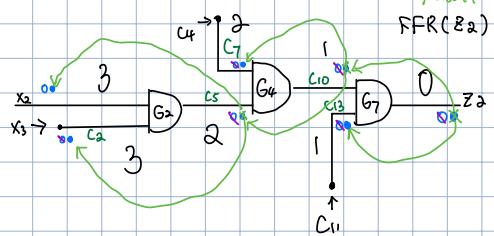
Faults detectable by  $\{0, X, 1, X, XX\}$   
 $\{z_1, S_{a1}\}$   
 $\{x_1, S_{a1}\}$

Fault detectable by  $\{1, X, 0, XX, X\}$   
 $\{C_1, S_{a1}\}$  ∵ All 9 faults have been covered in FFR( $z_1$ )

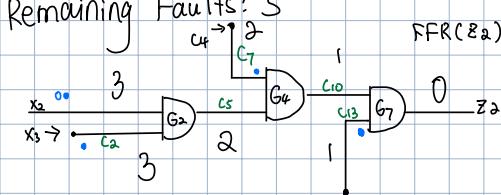
For FFR( $z_2$ )



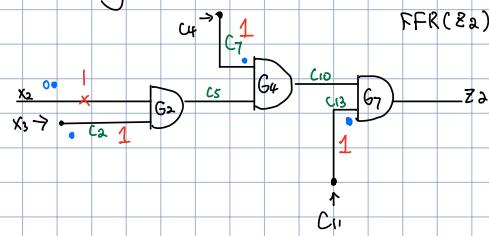
Fault Equivalence  
Fault Dominance



Remaining Faults: 5



Testing for  $X_2$  SAD



Round 1 : TGST Identified FEE

Local VA:  $D_7$  at  $X_2$

$$D = \{G_2\}$$

$$U = \{\}$$

Round 2 : TGST selected : FEP via  $G_2$  (Untried : Nonl)

Local VA:  $D_7$  at  $C_{10}$

$$D = \{G_4\}$$

$$U = \{\}$$

Round 3 : TGST selected : FEP via  $G_4$  (Untried : Nonl)

Local VA:  $D_7$  at  $C_{10}$

$$D = \{G_2\}$$

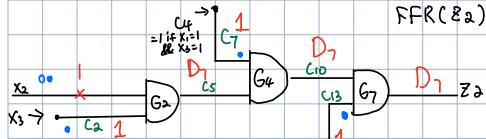
$$U = \{\}$$

Round 4 : TGST selected : FEP via  $G_7$  (Untried : Nonl)

Local VA:  $D_7$  at  $Z_2$

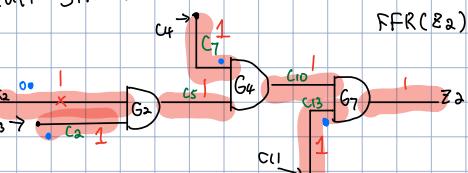
$$D = \{\}$$

$$U = \{\}$$



$\therefore$  Test Pattern:  $X_1, X_2, X_3, X_4, X_5, X_6$   
 $= \{1, 1, 1, 1, 1, X\}$

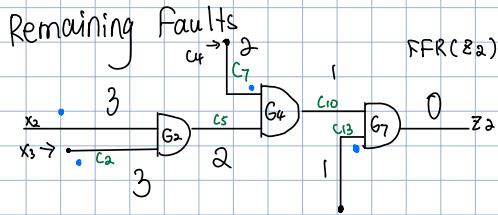
Fault Simulation:



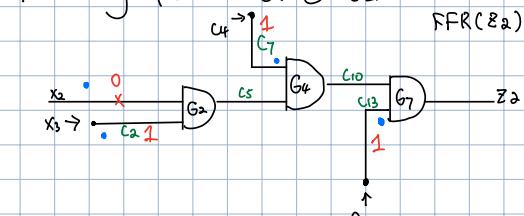
fault Detectable by  $\{1, 1, 1, 1, 1, X\}$

is  $\{X_2 \text{ SAD}\}$

Remaining Faults



Testing for  $X_2$  SA1



Round 1 : TGST Identified FEE

Local VA:  $D_7$  at  $X_2$

$$D = \{G_2\}$$

$$U = \{\}$$

Round 2 : TGST selected : FEP via  $G_2$  (Untried : Nonl)

Local VA:  $\overline{D_7}$  at  $C_{10}$

$$D = \{G_4\}$$

$$U = \{\}$$

Round 3 : TGST selected : FEP via  $G_4$  (Untried : Nonl)

Local VA:  $\overline{D_7}$  at  $C_{10}$

$$D = \{G_2\}$$

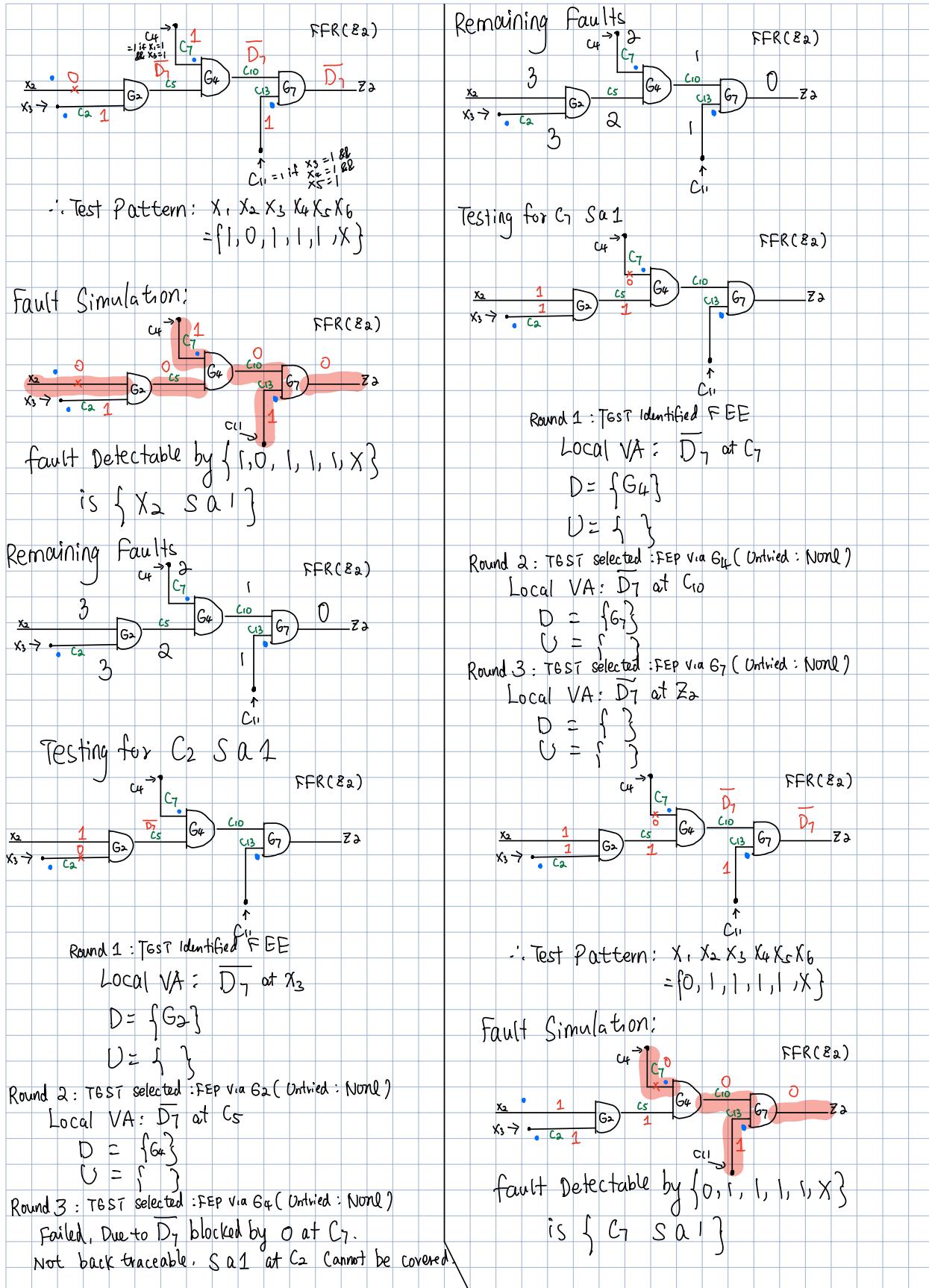
$$U = \{\}$$

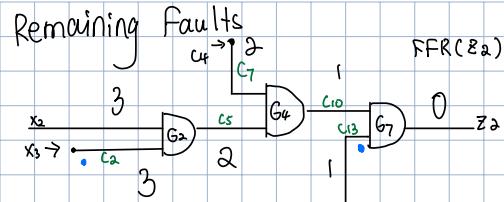
Round 4 : TGST selected : FEP via  $G_7$  (Untried : Nonl)

Local VA:  $\overline{D_7}$  at  $Z_2$

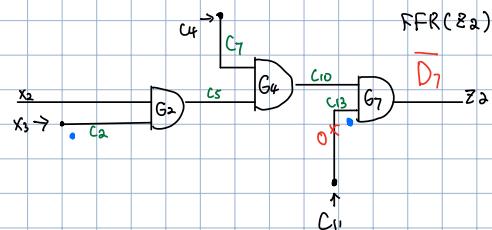
$$D = \{\}$$

$$U = \{\}$$





Testing for  $C_{13}$  SA 1



Round 1 : TGST Identified FEE

Local VA:  $\overline{D}_7$  at  $C_{13}$

$$D = \{G_7\}$$

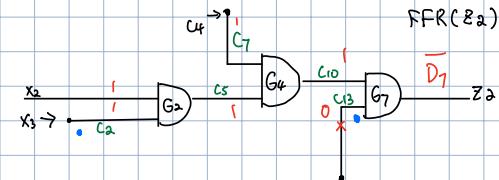
$$U = \{\}$$

Round 2 : TGST selected : FEP via  $G_7$  (Untried : Nonl)

Local VA:  $\overline{D}_7$  at  $Z_2$

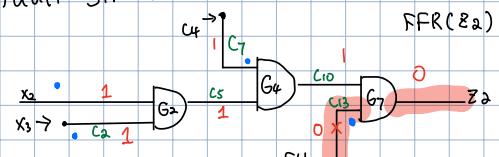
$$D = \{\}$$

$$U = \{\}$$



$$\therefore \text{Test Pattern: } X_1, X_2, X_3, X_4, X_5, X_6 \\ = \{1, 1, 1, 0, 1, X\}$$

Fault Simulation:



fault Detectable by  $\{1, 1, 1, 0, 1, X\}$   
is  $\{C_{13} \text{ SA 1}\}$

fault Detectable by  $\{1, 1, 1, 1, 1, X\}$

is  $\{X_2 \text{ SA 0}\}$

fault Detectable by  $\{1, 0, 1, 1, 1, X\}$

is  $\{X_2 \text{ SA 1}\}$

fault Detectable by  $\{0, 1, 1, 1, 1, X\}$

is  $\{C_7 \text{ SA 1}\}$

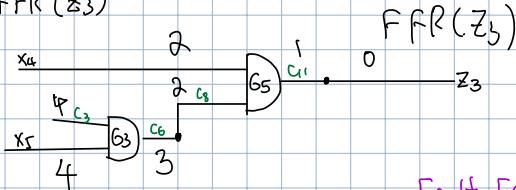
fault Detectable by  $\{1, 1, 1, 0, 1, X\}$

is  $\{C_6 \text{ SA 1}\}$

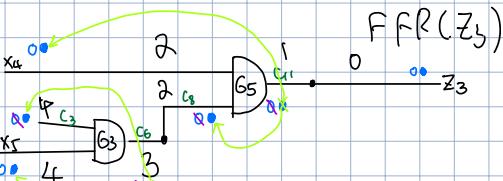
$C_2 \text{ SA 1}$  is not coverable.

4 / 5 faults are covered in  $\text{FFR}(Z_2)$

For  $\text{FFR}(Z_3)$



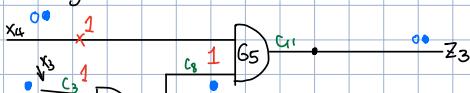
Fault Equivalence  
Fault Dominance



Remaining Faults : 8



Testing for  $X_4$  SA 0



Round 1 : TGST Identified FEE

Local VA:  $D_7$  at  $X_4$

$$D = \{G_5\}$$

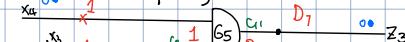
$$U = \{\}$$

Round 2 : TGST selected : FEP via  $G_5$  (Untried : Nonl)

Local VA:  $D_7$  at  $Z_3$

$$D = \{\}$$

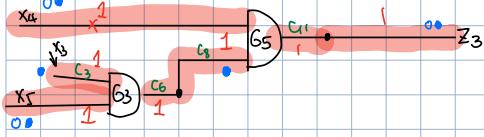
$$U = \{\}$$



$\therefore$  Test Pattern:  $X_1, X_2, X_3, X_4, X_5, X_6$

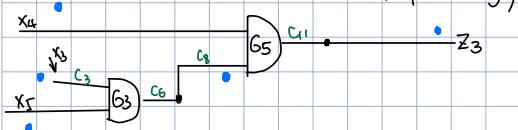
$$= \{X, X, 1, 1, 1, X\}$$

### Fault Simulation



faults Detectable by  $\{X_1, X_2, 1, 1, 1, X\}$   
are  $\{Z_3 \text{ SAI}\}$   
 $\{X_4 \text{ SAI}\}$   
 $\{X_5 \text{ SAI}\}$

### Remaining Faults



### Testing $X_4 \text{ SAI}$



Round 1 : TEST identified FEE  
Local VA:  $\overline{D}_7$  at  $X_4$   
 $D = \{G_5\}$   
 $U = \{\}$

Round 2 : TGST selected : FEP via  $G_5$  (Untried : None)

Local VA:  $D_7$  at  $Z_3$

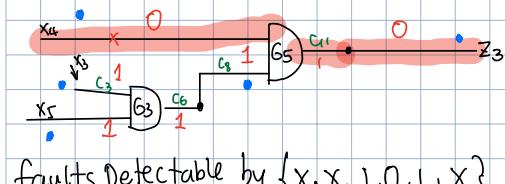
$D = \{\}$

$U = \{\}$



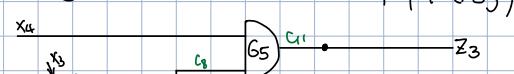
$\therefore$  Test Pattern:  $X_1, X_2, X_3, X_4, X_5, X_6$   
 $= \{X, X, 1, 0, 1, X\}$

### Fault Simulation



faults Detectable by  $\{X_1, X_2, 1, 0, 1, X\}$   
are  $\{Z_3 \text{ SAI}\}$   
 $\{X_4 \text{ SAI}\}$

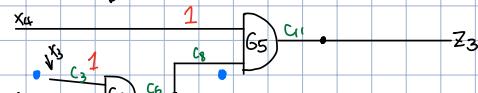
### Remaining Faults



### $FFR(Z_3)$



### Testing $X_5 \text{ SAI}$



Round 1 : TGST Identified FEE

Local VA:  $\overline{D}_7$  at  $X_5$

$D = \{G_3\}$

$U = \{\}$

Round 2 : TGST selected : FEP via  $G_3$  (Untried : None)

Local VA:  $\overline{D}_7$  at  $Z_3$

$D = \{G_5\}$

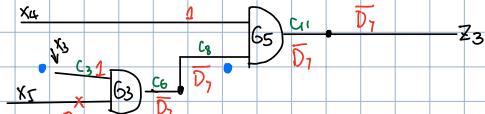
$U = \{\}$

Round 3 : TGS1 selected : FEP via  $G_5$  (Untried : None)

Local VA:  $\overline{D}_7$  at  $Z_3$

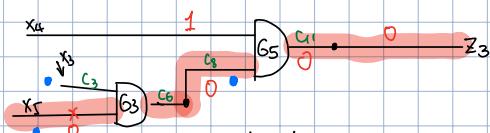
$D = \{\}$

$U = \{\}$



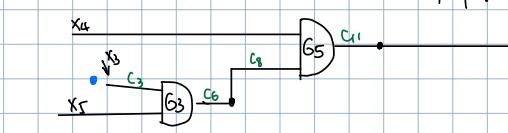
$\therefore$  Test Pattern:  $X_1, X_2, X_3, X_4, X_5, X_6$   
 $= \{X, X, 1, 1, 0, X\}$

### Fault Simulation

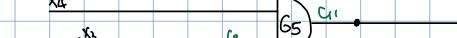


fault Detectable by  $\{X_1, X_2, 1, 1, 0, X\}$  are  
 $\{C_8 \text{ SAI}\}$   
 $\{X_5 \text{ SAI}\}$

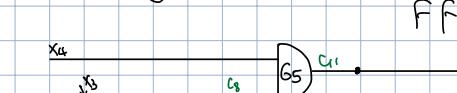
### Remaining Faults



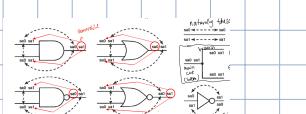
### $FFR(Z_3)$



### Testing $C_3 \text{ SAI}$



### $FFR(Z_3)$



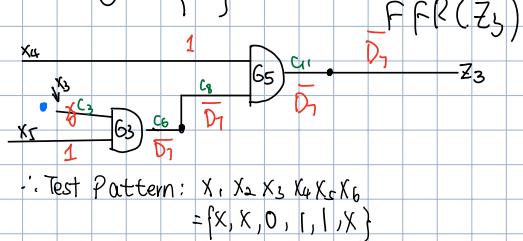
Round 1 : TGST Identified FEE  
 Local VA:  $\overline{D}_7$  at  $G_3$   
 $D = \{G_5\}$   
 $U = \{\}$

Round 2: TGST selected FEP via  $G_3$  (Untried: None)

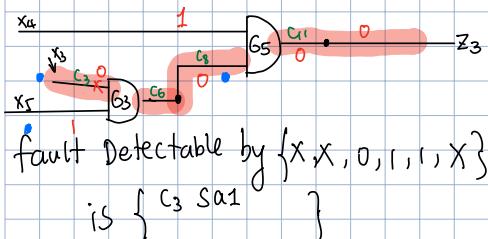
Local VA:  $D_7$  at  $G_3$   
 $D = \{G_5\}$   
 $U = \{\}$

Round 3: TGST selected FEP via  $G_5$  (Untried: None)

Local VA:  $D_7$  at  $Z$   
 $D = \{?\}$   
 $U = \{\}$



### Fault Simulation



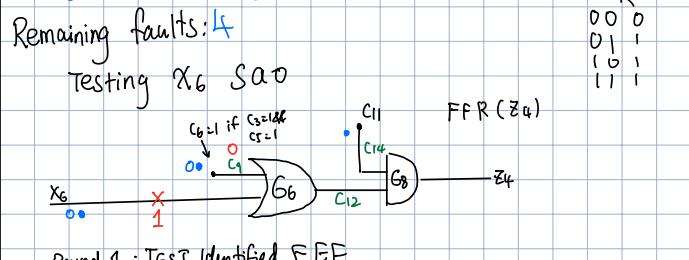
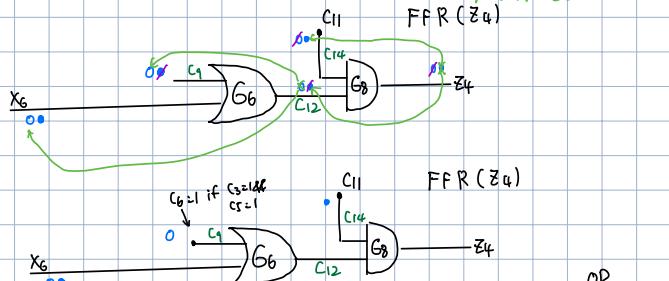
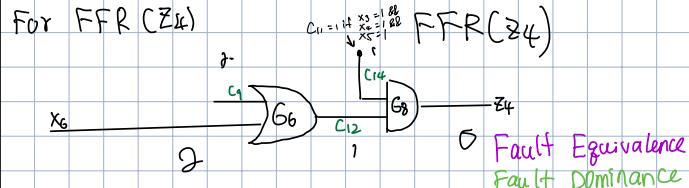
faults Detectable by  $\{X, X, 1, 1, 1, X\}$   
 are  $\{Z_3 \text{ SA0}\}$   
 $\{X_4 \text{ SA0}\}$   
 $\{X_5 \text{ SA0}\}$

faults Detectable by  $\{X, X, 1, 0, 1, X\}$   
 are  $\{Z_3 \text{ SA1}\}$   
 $\{X_4 \text{ SA1}\}$

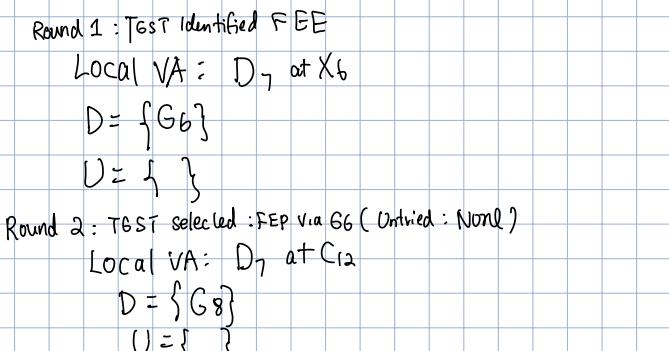
fault Detectable by  $\{X, X, 1, 1, 0, X\}$   
 are  $\{C_8 \text{ SA1}\}$   
 $\{X_5 \text{ SA1}\}$

fault Detectable by  $\{X, X, 0, 1, 1, X\}$   
 is  $\{C_3 \text{ SA1}\}$

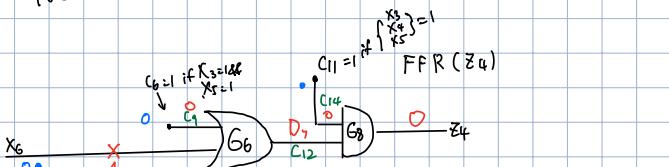
$\therefore$  All 8 faults are covered in  $\text{FFR}(Z_3)$



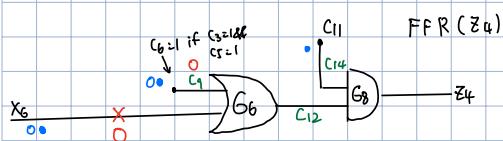
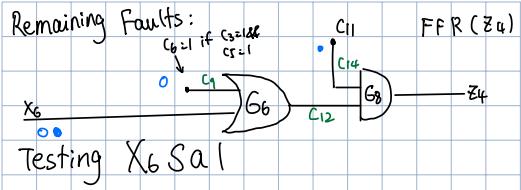
OR  
 00 0  
 01 1  
 10 1  
 11 1



Round 3: TGST selected FEP via  $G_8$  (Untried: None)  
 Failed. Due to  $D_7$  blocked by 0 at  $C_{14}$ .  
 No other alternative available.



$\therefore X_6 \text{ SA0 Cannot be covered.}$



Round 1 : TGST Identified FEE

Local VA:  $\overline{D}_7$  at  $X_6$

$$D = \{G_6\}$$

$$U = \{\}$$

Round 2 : TGST selected : FEP via G6 (Untried : None)

Local VA:  $D_7$  at  $C_{12}$

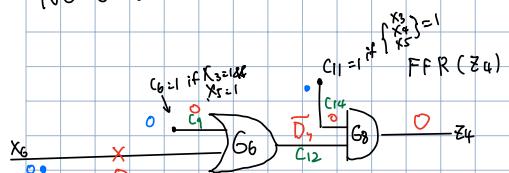
$$D = \{G_6\}$$

$$U = \{\}$$

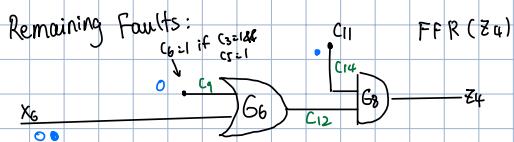
Round 3 : TGST selected: FEP via G8 (Untried: None)

Failed. Due to  $D_7$  blocked by 0 at  $C_{14}$ .

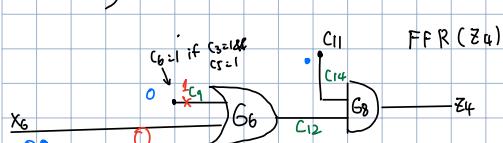
No other alternative available.



$\therefore X_6$  S a1 Cannot be covered.



Testing C9 Sa0



Round 1 : TGST Identified FEE

Local VA:  $D_7$  at  $C_9$

$$D = \{G_6\}$$

$$U = \{\}$$

Round 2 : TGST selected : FEP via G6 (Untried: None)

Local VA:  $D_7$  at  $C_{12}$

$$D = \{G_6\}$$

$$U = \{\}$$

Round 3 : TGST selected : FEP via G8 (Untried: None)

Local VA:  $D_7$  at  $Z_4$

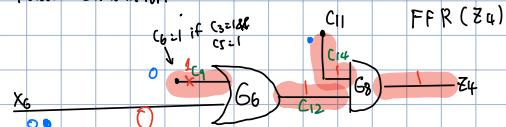
$$D = \{\}$$

$$U = \{\}$$

$\therefore$  Test pattern:  $X_1, X_2, X_3, X_4, X_5, X_6$

$$= \{X, X, 1, 1, 1, 0\}$$

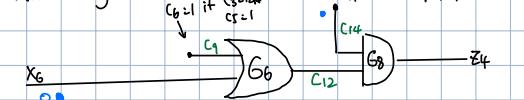
Fault Simulation:



fault Detectable by  $\{X, X, 1, 1, 1, 0\}$

$$\text{is } \{C_9 \text{ Sa0}\}$$

Remaining Faults:



Testing C14 Sa1



Round 1 : TGST Identified FEE

Local VA:  $\overline{D}_7$  at  $C_{14}$

$$D = \{G_6\}$$

$$U = \{\}$$

Round 2 : TGST selected : FEP via G8 (Untried: None)

Local VA:  $D_7$  at  $Z_4$

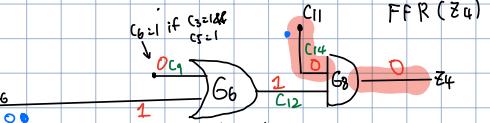
$$D = \{\}$$

$$U = \{\}$$

Test Pattern:  $X_1, X_2, X_3, X_4, X_5, X_6$

$$= \{X, X, 0, 0, 0, 1\}$$

Fault Simulation:



fault Detectable by  $\{X, X, 0, 0, 0, 1\}$

$$\text{is } \{C_{14} \text{ Sa1}\}$$

$\therefore$  fault Detectable by  $\{x, x, 1, 1, 1, 0\}$   
is  $\{c_9 s_{10}\}$

fault Detectable by  $\{x, x, 0, 0, 0, 1\}$   
is  $\{c_{14} s_{11}\}$

$\therefore$  2 out of 4 faults are covered in FFR(24)

$\therefore$  Overall, 3 faults cannot be covered in 3,36

For circuit 3.36, The schematic of which the VHDL represents can be seen in Figure 11. The VHDL code can be found in the folder named 336. Figure 12 shows the simulation waveform, proving its correct functionality.

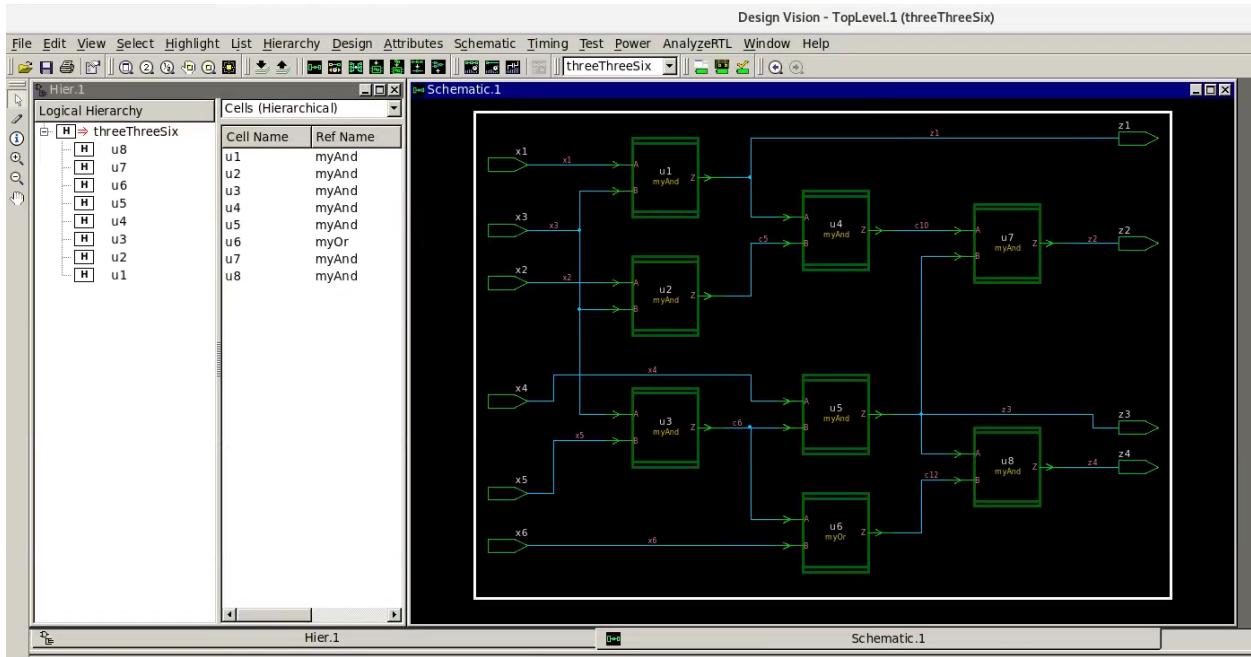


Figure 11 Schematic of 3.36

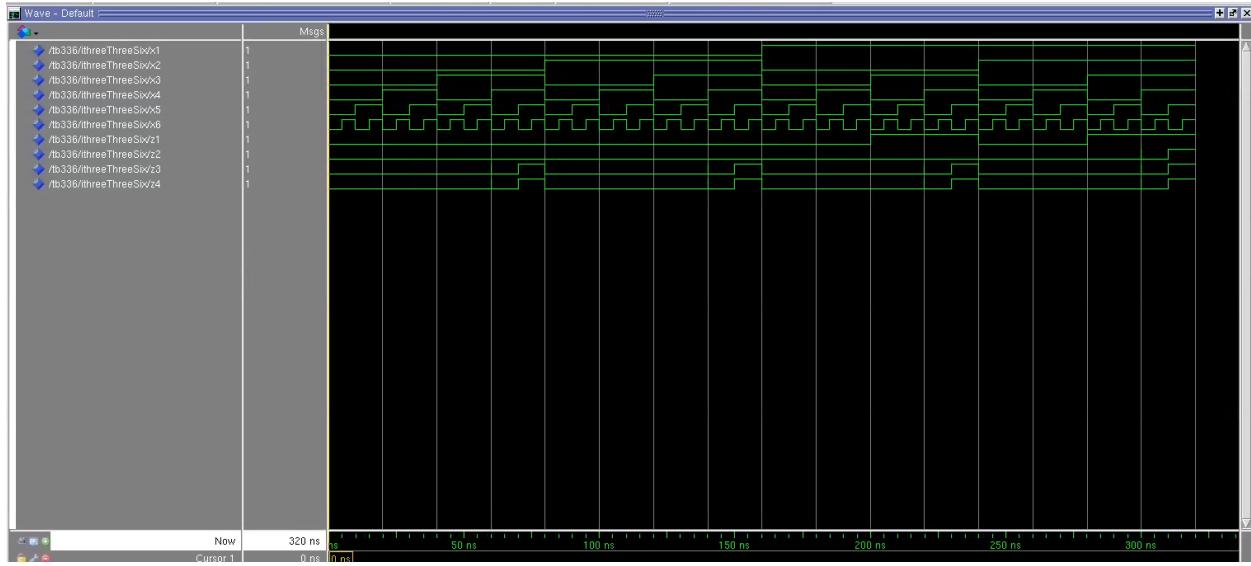


Figure 12 Simulation Waveform of 3.36

The synthesis result, which reports the timing and area, can be found in the threeThreeSix.report in 336 folder. The post-synthesis VHDL code can be found in the folder as well.

After importing into TetraMax, and have ATPG model built followed by design rule checked, the same the schematic in Figure 13, presented by TetraMax, matches that of Figure 12.

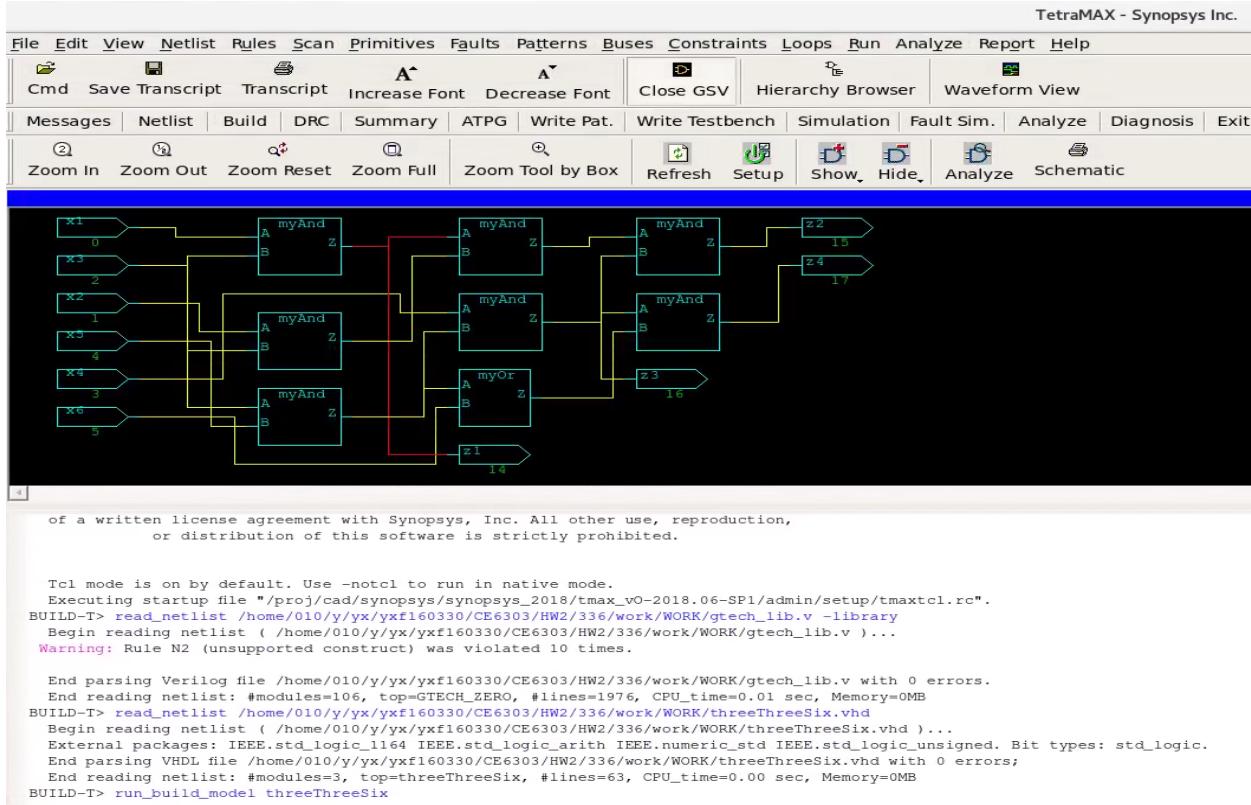


Figure 13 Schematic produced in TetraMax for 3.36

Thus, after running ATPG, faults can be reported as seen in Figure 14 a and b; and patterns used are reported in Figure 15.

Report Faults		
sal	UR	u2/B
sal	DS	x2
sal	--	u2/A
sal	DS	u2/Z
sal	--	u4/B
sal	DS	u4/Z
sal	--	u7/A
sal	DS	u4/A
sal	DS	z2
sal	--	u7/Z
sal	DS	u7/B
sa0	DS	z2
sa0	--	u7/Z
sa0	--	u7/A
sa0	--	u7/B
sa0	--	u4/Z
sa0	--	u4/A
sa0	--	u4/B
sa0	--	u2/Z
sa0	--	u2/A
sa0	--	u2/B
sa0	--	x2
sa0	UR	x6
sa0	--	u6/B
sa0	DS	z4
sa0	--	u8/Z
sa0	--	u8/A
sa0	--	u8/B
sa0	--	u6/Z
sa0	DS	u6/A
sal	DS	z4
sal	--	u8/Z
sal	DS	u8/A
sal	UR	u6/Z
sal	--	u6/B
sal	--	u6/A
sal	--	x6
sal	--	u8/B
sa0	DS	u1/Z
sa0	--	u1/A
sa0	--	u1/B

```

0 faults were removed from the fault list.
TEST-T> add_faults -all
68 faults were added to fault list.
TEST-T> run_atpg -ndetects 1
ATPG performed for stuck fault model using internal pattern source.

#patterns #faults #ATPG faults test process
stored detect/active red/au/abort coverage CPU time
-----
Begin deterministic ATPG: #uncollapsed_faults=68, abort_limit=10...
8 60 0 3/0/0 100.00% 0.00

Uncollapsed Stuck Fault Summary Report
-----
fault class code #faults
-----
Detected DT 60
Possibly detected PT 0
Undetectable UD 8
ATPG untestable AU 0
Not detected ND 0

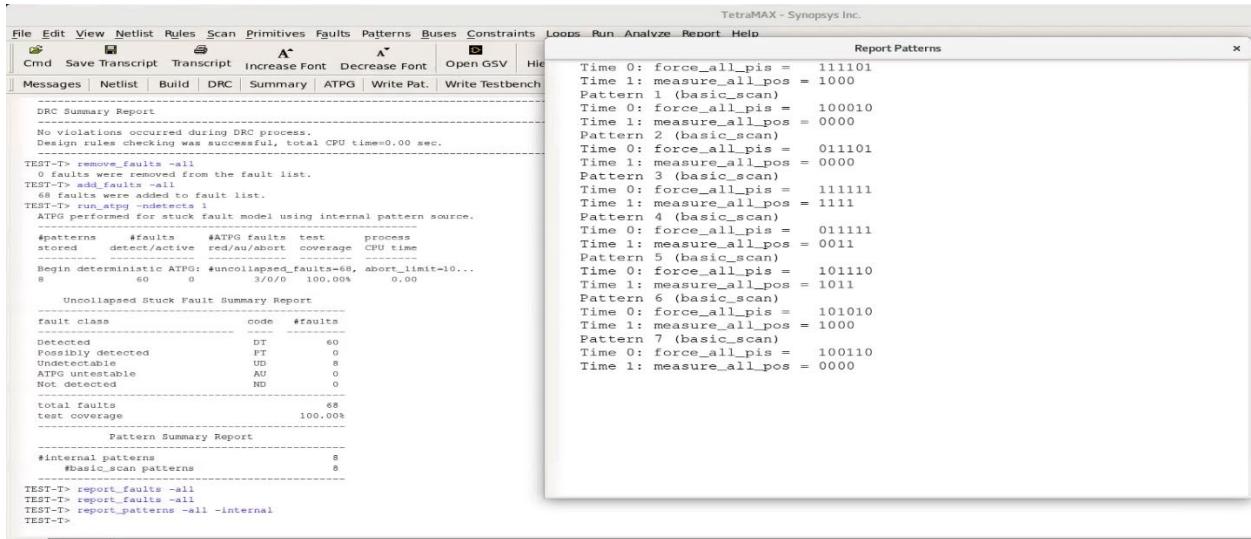
total faults 68
test coverage 100.00%
-----
Pattern Summary Report
-----
#internal patterns 8
#basic_scan patterns 8

TEST-T> report_faults -all
TEST-T> report_faults -all
TEST-T>

Log History
TEST-T>
Ready / work .synopsys_dc.setup (~/CE6303/H... Terminal Report Faults faultsFound.txt

```

Figure 14 a&b Faults found in 3.36



The screenshot shows the TetraMAX software interface. The menu bar includes File, Edit, View, Netlist, Rules, Scan, Primitives, Faults, Patterns, Buses, Constraints, Loops, Run, Analyze, Report, and Help. The toolbar includes Cmd, Save Transcript, Transcript, Increase Font, Decrease Font, Open GSV, and Help. The bottom status bar shows 'work .synopsys\_dc.setup (~/CE6303/H... Terminal Report Faults faultsFound.txt'.

```

File Edit View Netlist Rules Scan Primitives Faults Patterns Buses Constraints Loops Run Analyze Report Help
Cmd Save Transcript Transcript Increase Font Decrease Font Open GSV Help
Messages Netlist Build DRC Summary ATPG Write Pat. Write Testbench
DRC Summary Report
No violations occurred during DRC process.
Design rules checking was successful, total CPU time 0.00 sec.

TEST-T> add_faults -all
0 faults were removed from the fault list.
TEST-T> run_atpg -ndetects 1
ATPG performed for stuck fault model using internal pattern source.

#patterns #faults #ATPG faults test process
stored detect/active red/au/abort coverage CPU time
-----
Begin deterministic ATPG: #uncollapsed_faults=68, abort_limit=10...
8 60 0 3/0/0 100.00% 0.00

Uncollapsed Stuck Fault Summary Report
-----
fault class code #faults
-----
Detected DT 60
Possibly detected PT 0
Undetectable UD 8
ATPG untestable AU 0
Not detected ND 0

total faults 68
test coverage 100.00%
-----
Pattern Summary Report
-----
#internal patterns 8
#basic_scan patterns 8

TEST-T> report_faults -all
TEST-T> report_faults -all
TEST-T> report_patterns -all -internal
TEST-T>

```

Figure 15 Patterns used in fault testing for 3.36

As can be seen, not all faults can be detected and tested due to the fact that the circuit has multiple fanouts. In the hand-work, the circuit needs to be divided into 4 Fan-out-free Regions to perform fault analysis and critical path tracing. As a result, the analysed pattern and fault counts has discrepancies between each other.