3.

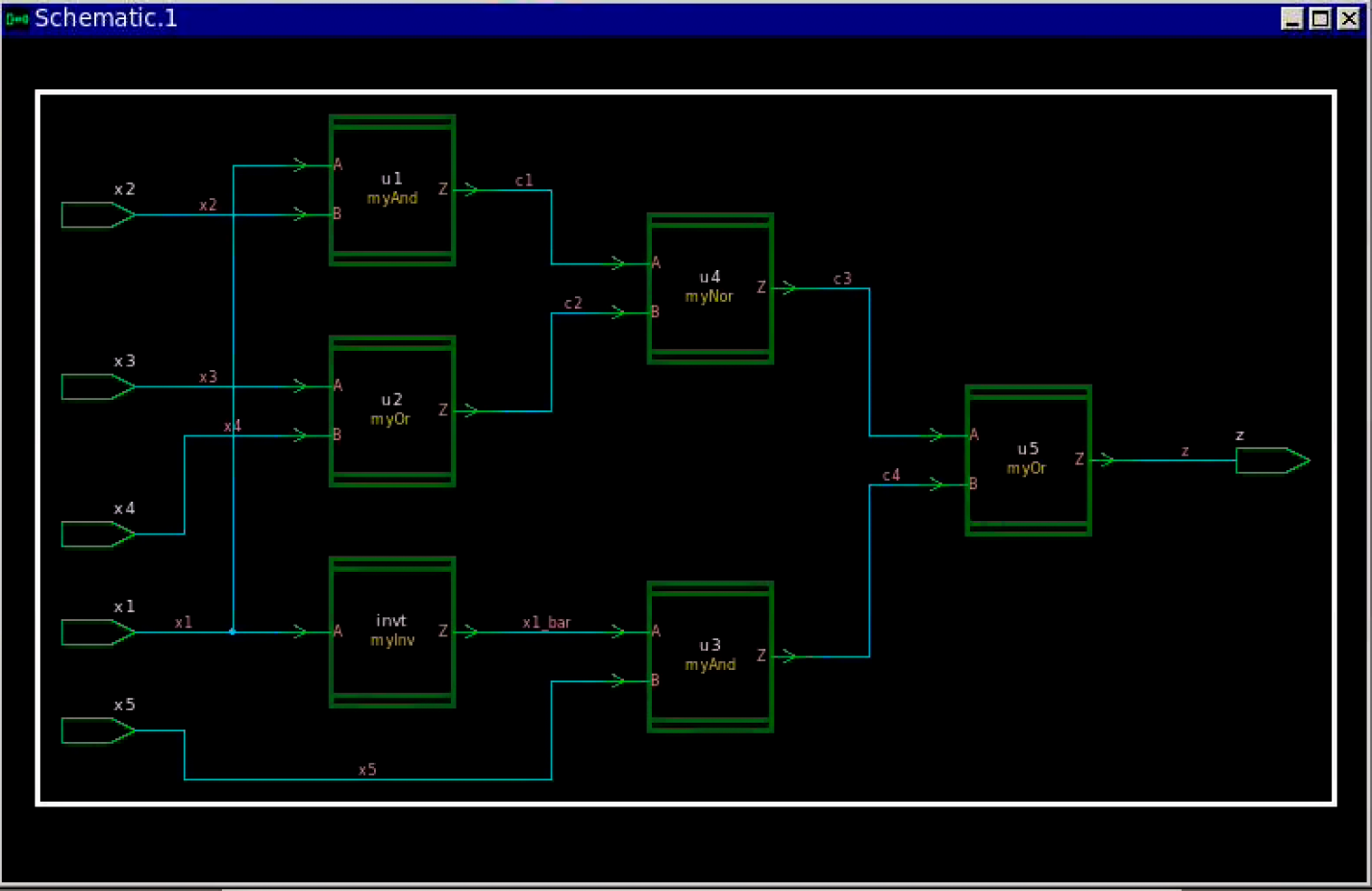
For the schematic shown in figure 8.13, the schematic in Figure 1 can be generated from VHDL. Its correctness is verified by the waveform as shown in Figure 2.

Figure Schematic of Figure 8.13

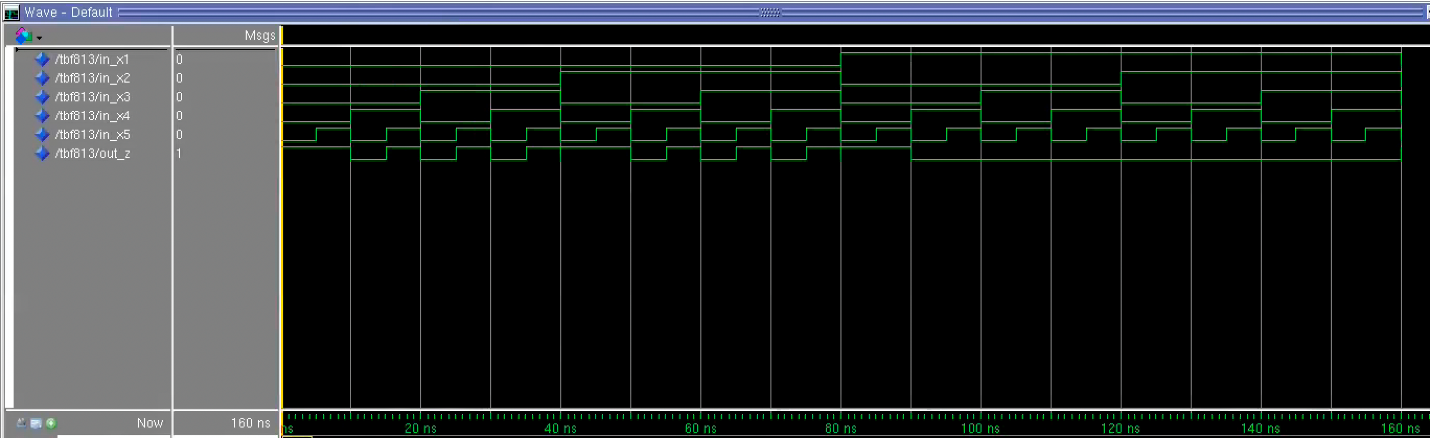


Figure Validation Waveform of Schematic

The delay path of i) and ii) is shown in the following figures. In Figure 4, the delay path analysed by the program have also determined the route through x1\_bar and x5 as delay path.

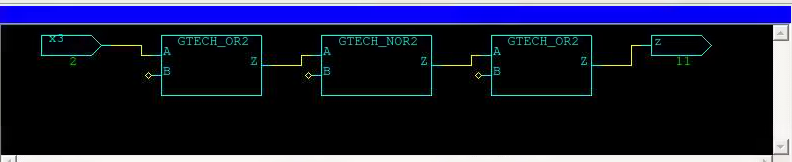


Figure Delay Path of i) and ii) of Q1

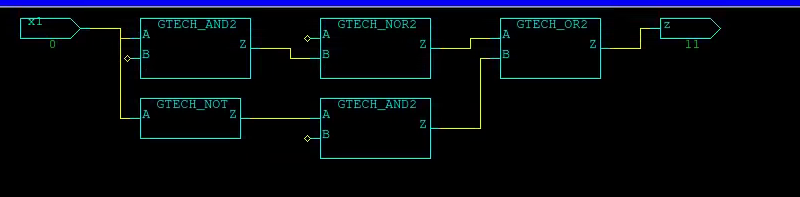


Figure Delay Path of iii) and iv) of Q1

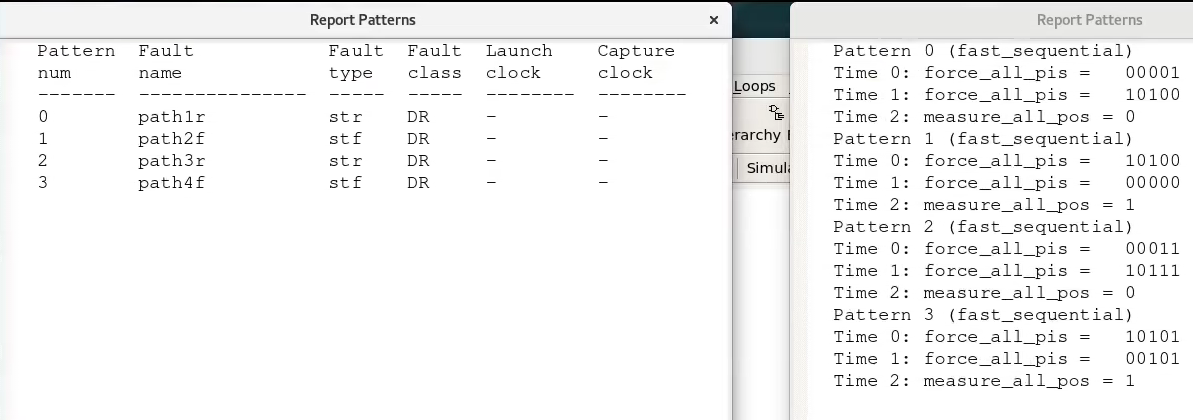
The following figures show the testing patterns for all delay paths. Figure 5 shows Robust test patterns and Figure shows non robust test pattern. Comparing to the manually obtained patterns, patterns generated by the program has no XX (Don’t care values) available. For this reason, pattern for i) is different to the result obtained by hand as I treated x2 input as XX instead of setting it to S0.

Figure Robust Test Patterns

In Figure 6, the same test pattern is used to test i) and iii) in non-robust test scenario. Since setting either gate of AND as don’t care results in the same output, the program chose to utilize x2 to save generation of another pattern.

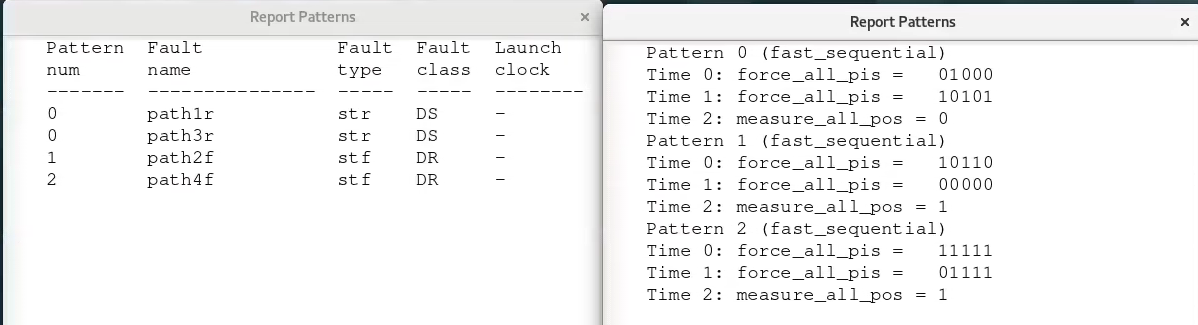


Figure Non-Robust Test Patterns

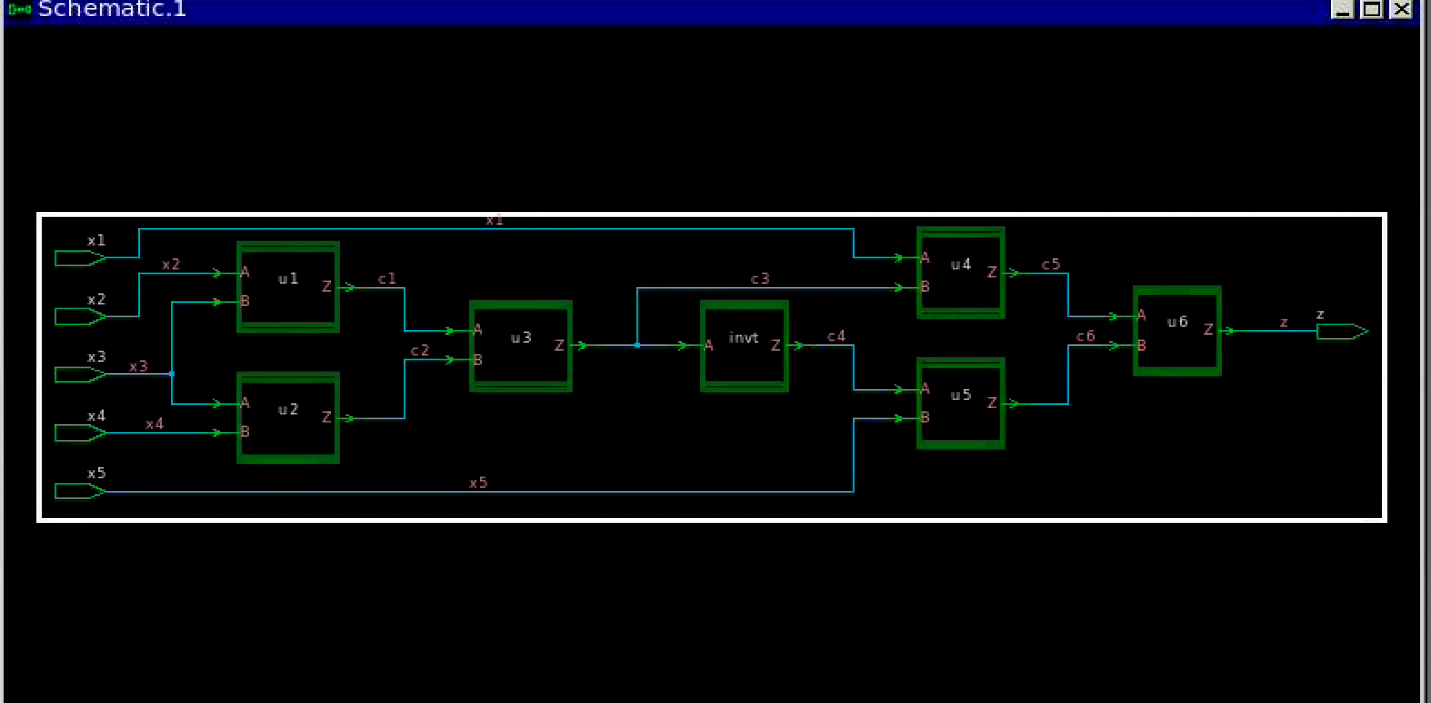
For figure 8.20, Figure 7 shows the schematic generated from VHDL. Its correctness is shown in the waveform in Figure 8.

Figure Schematic of Figure 8.20

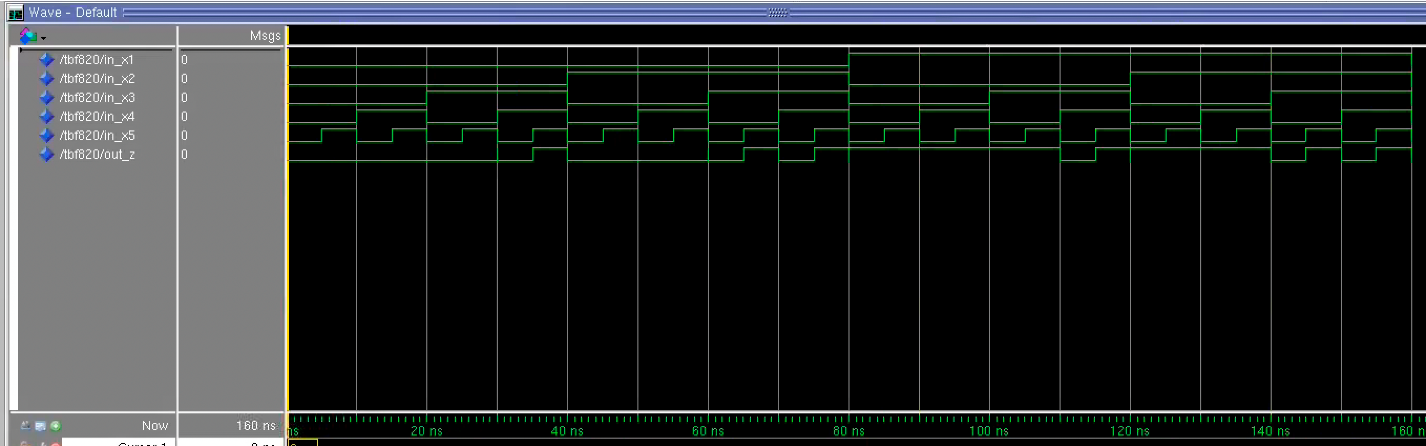


Figure Validation Waveform of Figure 8.20

The delay path from TetraMax is presented in Figure 9 and Figure 10.



Figure Delay path for i) and ii)

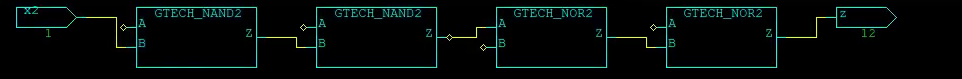


Figure Delay path for iii) and iv)

The result obtained from the program may be slightly different from that of by hand due to different choice of path.

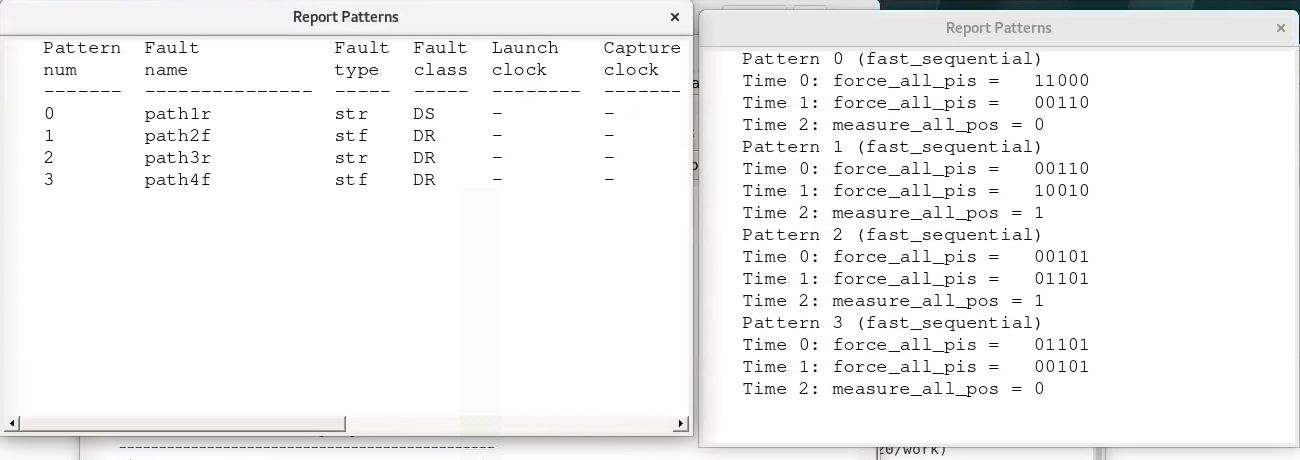


Figure Robust Test of Q2

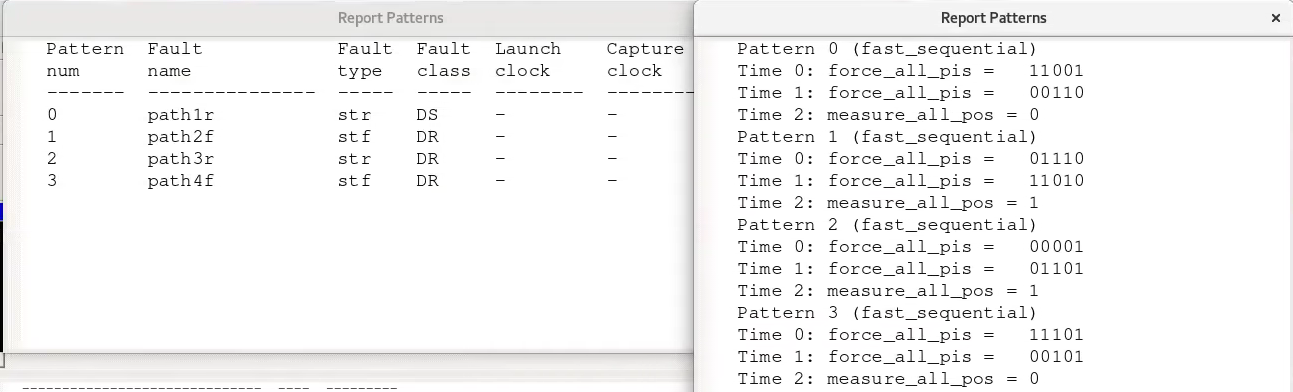


Figure non-Robust Test of Q2

7.

All test methods up to current detect faults that are not explainable using known FFMs. As a result, new FFMs need to be created so that it can not only compete in coverage with the industrial march test, but also allow new FFMs to be detectable. Since none of the industrial march test detect all realistic faults, March SS test is introduced in the article to cover all static simple FFMs.

To define “static simple FFM”, the article brought in the concept of fault primitives, which defines the set of targeted FFMs. Under the concept, a set of targeted FFMs is described in <S/F/R>, where S defines sensitizing operation sequence, F defines faulty behaviour, and R is the resultant value. Depending on ways of sensitisation, number of operations, and influence between faults, one can class a set of FFMs into single-port or multi-port, static or dynamic, simple or linked. A set of static simple FFM can then be defined as faults sensitised by performing at most 1 operation, and each fault cannot influence each other.

As the test is designed to test on RAM, functional fault models on RAM can be divided into single-cell FFMs and two-cell FFMs, according to number of cells the fault inpacts. Faults in single-cell FFMs include state fault (SF), transition fault (TF), write disturb faults (WDF), read destructive fault (RDF), deceptive read destructive fault (DRDF), and incorrect read fault (IRF). Faults in two-cell FFMs in clude state coupling fault (CFst), disturb coupling fault (CFds), transition coupling fault (CFtr), write destructive coupling fault (CFwd), read destructive coupling fault (CFrd), deceptive read destructive coupling fault (CFdrd), and incorrect read coupling fault (CFir).

By analysing the common fault primitives (<S/F/R>) across all the faults above, March SS is developed to cover all faults mentioned above to hit multiple birds in one stone. Since other March tests do not have the common fault primitive when designed, they cannot guarantee all faults above are covered. However, while March SS provides the best coverage, its test length of 22n is the longest in the table. It will depend on the application and desired fault coverage to judge whether it’s worthy to trade off long test time with higher coverage.