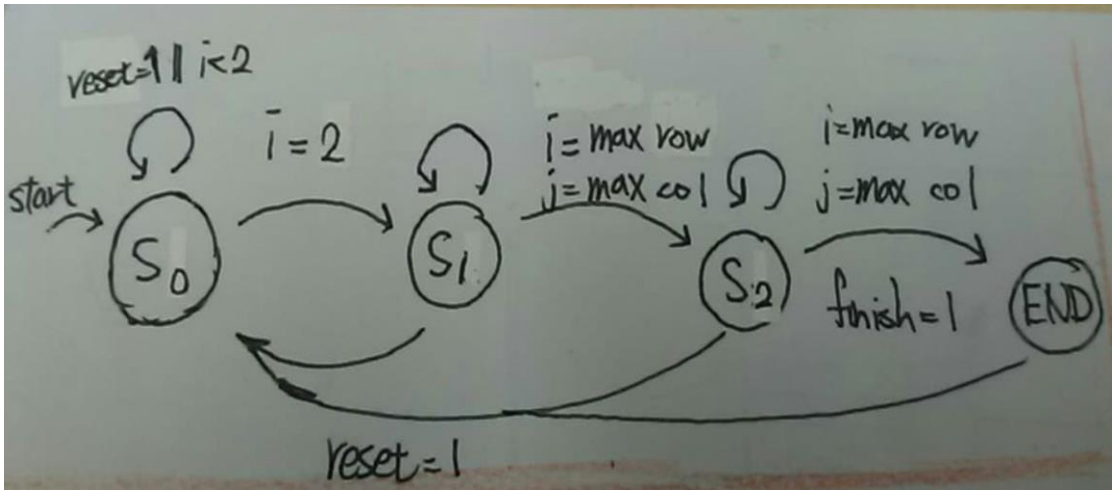
lab4_b123276353

1. State Transition Graph

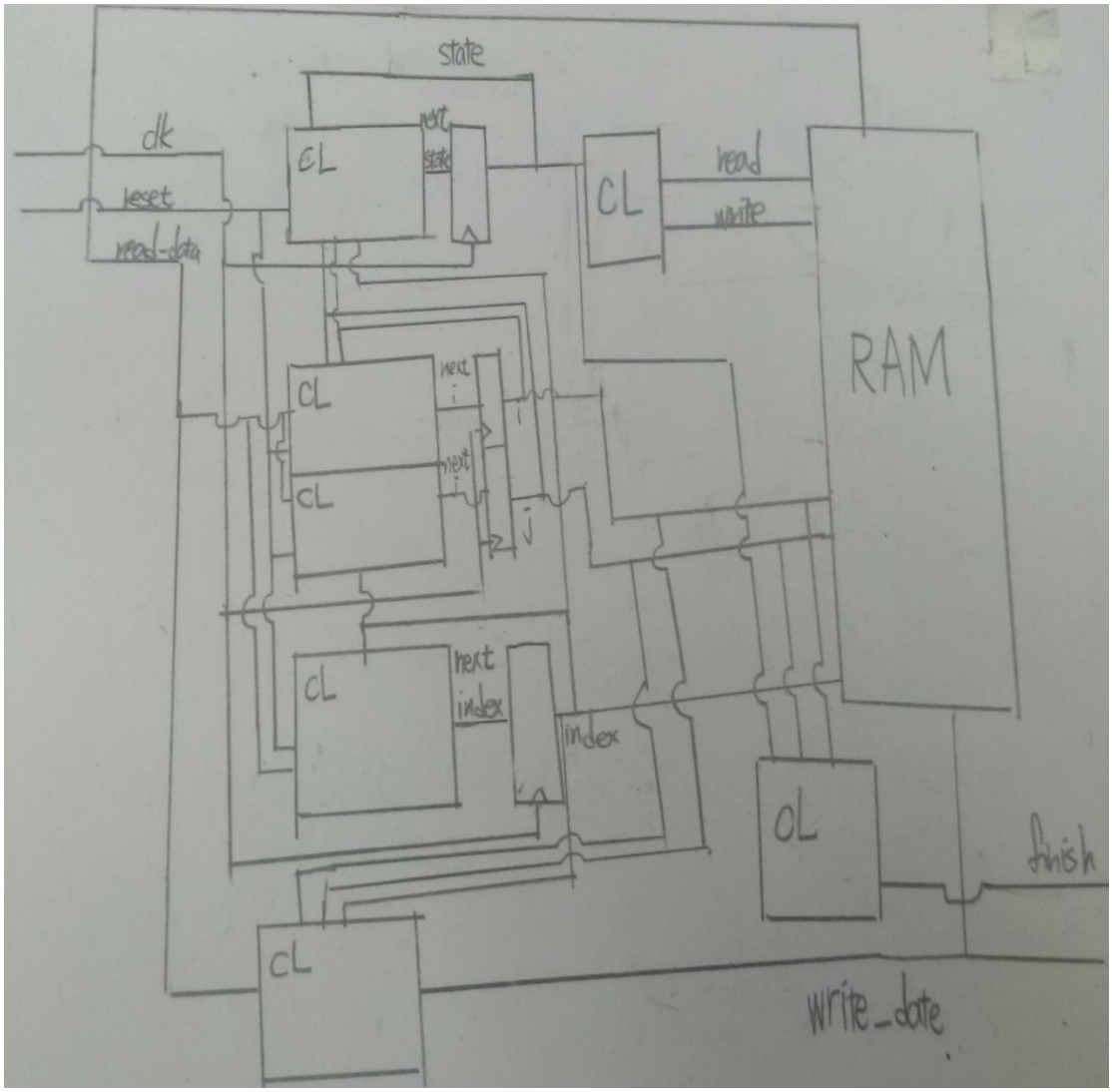


S_0:數據兩個矩陣的 col 和 row。
S_1:讀取矩陣每個位置的數值。
S_2:輸出矩陣乘法結果。

開始由 S_0 開始，進行讀取，i 到 2 的時候下一個 state 為 S_1。
S_1 主要進行讀檔，可以先進行運算，讀完之際(和 S_1 得到的大小相符)，下一個 state 為 S_2。
S_2 進行輸出，輸出完之際(和 S_1 得到的大小相符)即結束。
Reset=1 時全部狀態初始化(S0)。

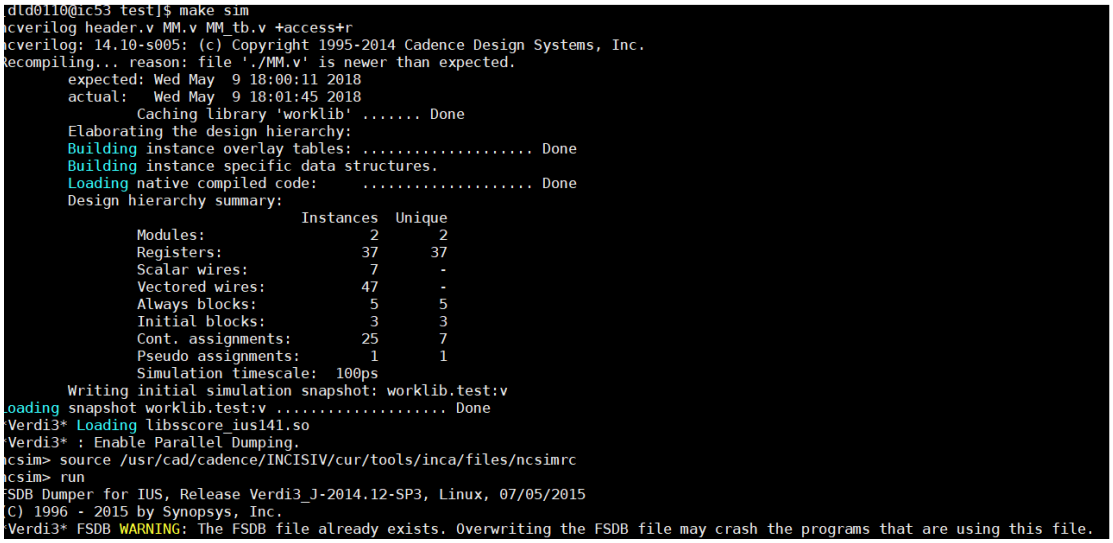
2.Block Diagram

如同下圖:



3.ncverilog 模擬結果 (sim + syn)

sim:



```
dld0110@ic53 test]$ make sim
ncverilog header.v MM.v MM_tb.v +access+r
ncverilog: 14.10-s005: (c) Copyright 1995-2014 Cadence Design Systems, Inc.
Recompiling... reason: file './MM.v' is newer than expected.
       expected: Wed May  9 18:00:11 2018
       actual:   Wed May  9 18:01:45 2018
                 Caching library 'worklib' ....... Done
       Elaborating the design hierarchy:
       Building instance overlay tables: .................... Done
       Building instance specific data structures.
       Loading native compiled code:     .................... Done
       Design hierarchy summary:
                                  Instances  Unique
                 Modules:                 2       2
                 Registers:              37      37
                 Scalar wires:            7       -
                 Vectored wires:         47       -
                 Always blocks:           5       5
                 Initial blocks:          3       3
                 Cont. assignments:      25       7
                 Pseudo assignments:      1       1
                 Simulation timescale:  100ps
       Writing initial simulation snapshot: worklib.test:v
Loading snapshot worklib.test:v ..................... Done
*Verdi3* Loading libsscore_ius141.so
*Verdi3* : Enable Parallel Dumping.
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
FSDB Dumper for IUS, Release Verdi3_J-2014.12-SP3, Linux, 07/05/2015
(C) 1996 - 2015 by Synopsys, Inc.
*Verdi3* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may crash the programs that are using this file.
```

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*Verdi3* : Create FSDB file 'MM.fsdb'
*Verdi3* : Begin traversing the scopes, layer (0).
*Verdi3* : End of traversing.
      2       3       3       4
      2       3       3       4
############################
Row:          0 Column:          0 is correct.
############################
############################
Row:          0 Column:          1 is correct.
############################
############################
Row:          0 Column:          2 is correct.
############################
############################
Row:          0 Column:          3 is correct.
############################
############################
Row:          1 Column:          0 is correct.
############################
############################
Row:          1 Column:          1 is correct.
############################
############################
Row:          1 Column:          2 is correct.
############################
############################
Row:          1 Column:          3 is correct.
############################
##################
#Congratulation!!!#
##################
Simulation complete via $finish(1) at time 3160 NS + 2
./MM_tb.v:118          $finish;
ncsim> exit
```

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syn:

```
ncsim> exit
[dld0110@ic53 test]$ make syn
ncverilog header.v MM_syn.v MM_tb.v -v /theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v +define+SDF +access+r
ncverilog: 14.10-s005: (c) Copyright 1995-2014 Cadence Design Systems, Inc.
file: MM_syn.v
        module worklib.MM:v
                errors: 0, warnings: 0
file: MM_tb.v
        module worklib.test:v
                errors: 0, warnings: 0
                Caching library 'tsmc13' ....... Done
                Caching library 'worklib' ....... Done
        Elaborating the design hierarchy:
  MM_DW01_cmp6_0 r2614 ( .A({1'b0, 1'b0, 1'b0, 1'b0, 1'b0, 1'b0, 1'b0, 1'b0,
                         |
ncelab: *W,CUVWSP (./MM_syn.v,25982|21): 4 output ports were not connected:
ncelab: (./MM_syn.v,340): GT
ncelab: (./MM_syn.v,340): LE
ncelab: (./MM_syn.v,340): GE
ncelab: (./MM_syn.v,340): NE

  MM_DW01_add_8 add_133_G10 ( .A({\add_data[9][39] , \add_data[9][38] ,
                            |
ncelab: *W,CUVWSP (./MM_syn.v,26029|26): 1 output port was not connected:
ncelab: (./MM_syn.v,1520): CO

  MM_DW01_add_7 add_133_G9 ( .A({\add_data[8][39] , \add_data[8][38] ,
                           |
ncelab: *W,CUVWSP (./MM_syn.v,26086|25): 1 output port was not connected:
ncelab: (./MM_syn.v,2559): CO

  MM_DW01_add_6 add_133_G8 ( .A({\add_data[7][39] , \add_data[7][38] ,
                           |
ncelab: *W,CUVWSP (./MM_syn.v,26142|25): 1 output port was not connected:
ncelab: (./MM_syn.v,3598): CO

  MM_DW01_add_5 add_133_G7 ( .A({\add_data[6][39] , \add_data[6][38] ,
                           |
ncelab: *W,CUVWSP (./MM_syn.v,26198|25): 1 output port was not connected:
ncelab: (./MM_syn.v,4637): CO

  MM_DW01_add_4 add_133_G6 ( .A({\add_data[5][39] , \add_data[5][38] ,
                           |
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ncelab: *W,CUVWSP (./MM_syn.v,28508|33): 1 output port was not connected:
ncelab: (/theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v,26199): QN

  TLATX1 \new_data_reg[18][3][12]  ( .G(N7298), .D(n32806), .Q(
                                   |
ncelab: *W,CUVWSP (./MM_syn.v,28510|33): 1 output port was not connected:
ncelab: (/theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v,26199): QN

  TLATX1 \new_data_reg[18][3][11]  ( .G(N7298), .D(n32760), .Q(
                                   |
ncelab: *W,CUVWSP (./MM_syn.v,28512|33): 1 output port was not connected:
ncelab: (/theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v,26199): QN

ncelab: *W,MXWARN: Reached maximum warning limit for 'CUVWSP'(1000).
        Reading SDF file from location "./MM.sdf"
        Annotating SDF timing data:
                Compiled SDF file:     MM.sdf.X
                Log file:
                Backannotation scope:  test.mmmmm
                Configuration file:
                MTM control:
                Scale factors:
                Scale type:
        Annotation completed successfully...
        SDF statistics: No. of Pathdelays = 263086  Annotated = 100.00% -- No. of Tchecks = 240985  Annotated = 100.00%
                                        Total      Annotated      Percentage
                 Path Delays          263086          263086          100.00
                      $width           48233           48233          100.00
                   $setuphold         192752          192752          100.00
  assign n5 = a[2];
      |
ncelab: *W,SDFNCAP (./MM_syn.v,10007|7): The interconnect source test.mmmmm.U29020.Y is separated by a unidirectional continuous assign from the destinat
ion test.mmmmm.mult_132.U151.A.  The port annotation will still occur.
  assign n66 = a[19];
      |
ncelab: *W,SDFNCAP (./MM_syn.v,10013|7): The interconnect source test.mmmmm.U52658.Y is separated by a unidirectional continuous assign from the destinat
ion test.mmmmm.mult_132.U854.A.  The port annotation will still occur.
  assign n5 = a[2];
      |
ncelab: *W,SDFNCAP (./MM_syn.v,10007|7): The interconnect source test.mmmmm.U29020.Y is separated by a unidirectional continuous assign from the destinat
ion test.mmmmm.mult_132.U857.A.  The port annotation will still occur.
  assign n66 = a[19];
      |
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ncelab: *W,SDFNCAP (./MM_syn.v,1696|7): The interconnect source test.mmmmm.U29047.Y is separated by a unidirectional continuous assign from the destinati
on test.mmmmm.mult_132_G9.U989.A.  The port annotation will still occur.
  assign n15 = a[5];
          |
ncelab: *W,SDFNCAP (./MM_syn.v,1696|7): The interconnect source test.mmmmm.U29047.Y is separated by a unidirectional continuous assign from the destinati
on test.mmmmm.mult_132_G9.U986.A.  The port annotation will still occur.
  assign n15 = a[5];
          |
ncelab: *W,SDFNCAP (./MM_syn.v,1696|7): The interconnect source test.mmmmm.U29047.Y is separated by a unidirectional continuous assign from the destinati
on test.mmmmm.mult_132_G9.U983.A.  The port annotation will still occur.
ncelab: *W,MXWARN: Reached maximum warning limit for 'SDFNCAP'(1000).
        Building instance overlay tables: .................... Done
        Generating native compiled code:
                worklib.MM:v <0x09d2b72f>
                        streams:   0, words:     0
                worklib.test:v <0x7a8f5c43>
                        streams:   7, words: 14182
        Loading native compiled code:     ..................... Done
        Building instance specific data structures.
        Design hierarchy summary:
                                    Instances  Unique
                Modules:                73345      86
                UDPs:                   32188       3
                Primitives:            259819       8
                Timing outputs:        107562      32
                Registers:              32202      21
                Scalar wires:          139836       -
                Expanded wires:            20       1
                Always blocks:              3       3
                Initial blocks:             3       3
                Cont. assignments:          0      71
                Pseudo assignments:         1       1
                Timing checks:         240985    4927
                Interconnect:          222240       -
                Delayed tcheck signals:   48210    3065
                Simulation timescale:       1ps
        Writing initial simulation snapshot: worklib.test:v
Loading snapshot worklib.test:v ..................... Done
*Verdi3* Loading libsscore_ius141.so
*Verdi3* : Enable Parallel Dumping.
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
```

```
ncsim> run
FSDB Dumper for IUS, Release Verdi3_J-2014.12-SP3, Linux, 07/05/2015
(C) 1996 - 2015 by Synopsys, Inc.
*Verdi3* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may crash the programs that are using this file.
*Verdi3* : Create FSDB file 'MM_syn.fsdb'
*Verdi3* : Begin traversing the scopes, layer (0).
*Verdi3* : End of traversing.
      2       3       3       4
      2       3       3       4
############################
Row:          0 Column:          0 is correct.
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Row:          0 Column:          2 is correct.
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############################
Row:          0 Column:          3 is correct.
############################
############################
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############################
############################
Row:          1 Column:          1 is correct.
############################
############################
Row:          1 Column:          2 is correct.
############################
############################
Row:          1 Column:          3 is correct.
############################
##################
#Congratulation!!!#
##################
Simulation complete via $finish(1) at time 3161121 PS + 0
./MM_tb.v:118           $finish;
ncsim> exit
```