YIFENG XIAO

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EDUCATION

University of Southern California (USC), Los Angeles, CA, U.S. Jan. 2021 - Present
Ph.D. in Ming Hsieh Department of Electrical and Computer Engineering

- GPA: 3.90/4.00; work with Prof. Pierluigi Nuzzo.
- Research interests: Design and verification of cyber-physical system (CPS), AI-based design automation.
- Relevant coursework: Machine Learning, Probability, Stochastic Process, Linear Algebra, Optimization, Nonlinear Control System, Analysis of Algorithms, Learning and Control for Safety-Critical Robotic Systems, etc.

Fudan University (FDU), Shanghai, China Aug. 2016 - Jul. 2020
B.E. in Microelectronic Science and Engineering

- GPA: 3.64/4.00; worked with Prof. Jianli Chen and Prof. Bei Yu.
- Research interests: Electronic design automation (EDA), Machine Learning.

University of Sudney (USYD), Sydney, Australia Feb. 2019 - Jun. 2019
Exchange Student in the Department of Information and Computer Engineering

PUBLICATION

Journal Papers

1. Zhu, Z., Li, Y., Su, M., Zhang, S., Su, H., Xiao, Y., ... & Chang, Y. W. (2024), "Subgraph Matching-Based Reference Placement for Printed Circuit Board Designs", The Journal of Supercomputing 2024. [LINK]

Conference Papers

1. Xiao, Y., Oh, C., Lora, M., & Nuzzo, P. (2023, Sep.), "Efficient Exploration of Cyber-Physical System Architectures Using Contracts and Subgraph Isomorphism", DATE 2024 (Best Paper Award). [LINK]
2. Su, M., Xiao, Y., Zhang, S., Su, H., Xu, J., He, H., ... & Chang, Y. W. (2022), "Late Breaking Results: Subgraph Matching Based Reference Placement for PCB Designs", DAC 2022. [LINK]
3. Xiao, Y., Su, M., Yang, H., Chen, J., Yu, J., & Yu, B. (2021, Dec.), "Low-Cost Lithography Hotspot Detection with Active Entropy Sampling and Model Calibration", DAC 2021. [LINK]
4. Ma, C., Xiao, Y., Wang, S., Yu, J., & Chen, J. (2021, Oct.), "CongestNN: A Bi-Directional Congestion Prediction Framework for Large-Scale Heterogeneous FPGAs", ASICON 2021. [LINK]

RESEARCH EXPERIENCE

Hardware and Mapping Co-Design for DNN Acceleration Using Reinforcement Learning Jun. 2024 - Sep. 2024
Project Leader, Advisor: Dr. Masood Mortazavi, Futurewei Technologies

- Proposed a framework for hardware and mapping strategies co-optimization using single-step RL.
- Sampled design points with joint probability distribution to reduce the output dimension of the agent.
- Developed an efficient decoding method based on scaling graphs and designed a certified reward function.

Efficient Exploration of CPS Architectures Using Contracts and Subgraph Isomorphism Oct. 2022 - Sep. 2023
Project Leader, Advisor: Prof. Pierluigi Nuzzo, Viterbi School of Engineering, USC

- Formulated design space exploration problem with mixed-integer linear program (MILP) coded in Gurobi.
- Formally modeled diverse design viewpoints using assume-guarantee (A/G) contracts and leveraged contract-based decomposition to enhance scalability.
- Conducted refinement checking and subgraph isomorphism to exclude infeasible architectures efficiently.

Machine Learning-Based Circuit Block Identification for Comparative Analysis May. 2023 - Aug. 2023
Project Leader, Supervisor: Kim-Fung Chan, Micron Technology

- Designed an efficient feature extraction method on layout images with the Sobel filter.

- Constructed an image segmentation model to identify functional circuit blocks achieving 90% accuracy.
- Computed area of different circuit blocks on layout images for comparative analysis.

Low-Cost Hotspot Detection with Active Entropy Sampling Dec. 2019 - Apr. 2020

Project Leader, Advisor: Bei Yu, Dept. of CSE, The Chinese University of Hong Kong (CUHK)

- Processed layout data into clips and performed feature extraction using principal component analysis.
- Developed an entropy-based selection technique combining model uncertainty with calibration and data diversity.
- Applied an active learning framework for hotspot detection to achieve higher accuracy and less overhead.

TEACHING AND INTERNSHIPS

Futurewei Technologies May 2024 - Aug. 2024

Machine Learning Research Intern

- Explored design space exploration methodology based on reinforcement learning.

USC Viterbi School of Engineering Jan. 2024 - Apr. 2024

Teaching Assistant for EE581: Mathematical Foundations for System Design: Modeling, Analysis, and Synthesis

Micron Technology May 2023 - Aug. 2023

Machine Learning Intern

- Cooperated with the analog team on circuit block identification for comparative analysis.

USC AutoDrive Lab Sep. 2021 - Present

Mentor for USC Viterbi Center for Undergraduate Research in Viterbi Engineering (CURVE) Program

- Build simulation-based and experimental testbeds to emulate realistic scenarios for self-driving vehicles.

DesCyPhy Lab Jun. 2022 - Jul. 2022

Mentor for 2022 USC Viterbi Summer High School Intensive in Next-Generation Engineering (SHINE) Program

- Conduct robustness verification for the traffic sign classification system with Z3.

USC Viterbi Graduate Mentorship Program Aug. 2022 - Nov. 2022

AWARD

2024 Best Paper Award, Design Automation and Test Conference in Europe 2024 (4/996)
2023 DAC Young Fellowship
2020 Outstanding Graduates of Shanghai (2nd place of 122)
2019 National IC Design Competition - First Prize for Undergraduate Group
2018 SCSK Corporation Scholarship (1/122)
2018 Undergraduate Excellence Scholarship of FDU

TECHNICAL SKILLS

Languages: English (Proficient), Chinese (Native)
Programming: Python, C/C++, Verilog, Java, Perl
Software & Platforms: Pytorch, Robot Operating System (ROS), MATLAB, Tensorflow, Gurobi, Z3, NuXMV, Simulink, LaTeX