

Tutorial: Design Compiler NXT

1 Introduction

This tutorial provides a step-by-step guide to using Synopsys Design compiler, one of the most widely used tools for logic synthesis in digital design. Synthesis is a crucial phase in digital design, transforming a high-level description of a circuit, typically written in HDL like Verilog, SystemVerilog or VHDL, into a gate-level netlist. A simple design is uploaded to brightspace, please download and import the design folder to fastX3.

Main steps in Synthesis Flow:

- Specify Libraries
- Read RTL
- Applying Timing Constraints
- Synthesize the Design
- Generate Reports
- Save the Results

2 Specify Libraries

1. Edit your `~/tcshrc_synopsys.local` file by changing the value of SYN_HOME to:

`/eda/synopsys/syn/W-2024.09-SP5-5`

Then add the following line at the bottom of the file:

`set path=($SYN_HOME/bin $path)`

2. Unzip the folder using the command: `unzip lab1.zip`. Change the directory to lab1. The `setup.tcl` file sources the `rm_setup/dc_setup.tcl` file which in turn sources the `rm_setup/common_setup.tcl` file.
3. Invoke the DC NXT in topographical mode using the command: `dcnxt_shell -topo -gui`
4. Execute the command from the same terminal you launched the tool or you can run these command from the input area at the bottom of the GUI: `source setup.tcl`

```
dcnxt_shell-topo> source setup.tcl
Information: Loading library file '/home/ds7860/lab1/TOP.dlib' (FILE-007)
Information: Loading library file '/ip/tsmc/tsmc16adfp/stdcell/NDM/N16ADFP_StdCell_physicalonly.ndm' (FILE-007)
Information: Using the 'open_lib' command has enabled NDM mode for the current Design Compiler NXT session. (DCT-294)

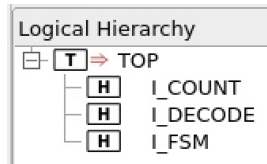
=====

Library Settings:
search_path:      . /eda/synopsys/syn/W-2024.09-SP5-5/libraries/syn /eda/synopsys/syn/W-2024.09-SP5-5/dw/syn_ver
link_library:     * N16ADFP_StdCelltt0p8v25c.db
target_library:   N16ADFP_StdCelltt0p8v25c.db
physical libraries: N16ADFP_StdCell_physicalonly.ndm
physical design library: TOP.dlib

=====
dcnxt_shell-topo>
```

3 Read RTL

- Depending on the type of file, specify the format as shown below (enter only one of the following):
 - `analyze -f verilog TOP.v`
 - `analyze -f vhd1 TOP.vhd`
- After reading the rtl file, elaborate the design by specifying the TOP module name: `elaborate TOP`
- Now you should be able to see the modules in the **Logical Hierarchy** pane at the upper-left of the GUI, there is a T icon called TOP, which is the top-level, and there are icons for the lower level hierarchical (H) instances as shown below:



- Use the following commands to list the libraries and designs:
 - `list_libs`
 - `list_designs`

```

dcnxt_shell-topo> list_libs
Logical Libraries:
-----
Library      File      Path
-----
N16ADFP_StdCelltt0p8v25c N16ADFP_StdCelltt0p8v25c.db /ip/tsmc/tsmc16adfp/stdcell/NLDM
gtech        gtech.db  /eda/synopsys/syn/W-2024.09-SP5-5/libraries/syn
standard.sldb standard.sldb /eda/synopsys/syn/W-2024.09-SP5-5/libraries/syn
1
dcnxt_shell-topo> list_designs
COUNT DECODE FSM TOP (*)
1
dcnxt_shell-topo>
  
```

- It is always a good practice to save the design as an unmapped ddc file at this step. Remember that we still haven't applied any constraints to our design. If we have applied the constraints, then we will save it to the mapped folder. For now execute this command: `write_file -hier -f ddc -output ./unmapped/TOP.ddc`

4 Apply Timing Constraints

- Verify that the current design is **TOP** by executing the following command: `current_design`
- Source the constraints to the design by sourcing the SDC file: `source TOP.con`

```

dcnxt_shell-topo> current_design
Current design is 'TOP'.
{TOP}
dcnxt_shell-topo> source TOP.con
Current design is 'TOP'.
Information: linking reference library : /ip/tsmc/tsmc16adfp/stdcell/NDM/N16ADFP_StdCell_physicalonly.ndm. (PSYN-878)

Linking design 'TOP'
Using the following designs and libraries:
-----
* (4 designs)                /home/ds7860/lab1/TOP.db, etc
N16ADFP_StdCelltt0p8v25c (library) /ip/tsmc/tsmc16adfp/stdcell/NLDM/N16ADFP_StdCelltt0p8v25c.db

Current design is 'TOP'.
dcnxt_shell-topo>
  
```

5 Synthesize the Design

1. Perform synthesis by entering the following command: `compile_ultra`
2. Watch the log by increasing the size of the terminal from which you launched the `dcnxt_shell`, you will see different warnings and errors. But you can also see **Library analysis succeeded**.

```
dcnxt_shell-topo> compile_ultra
Loading db file '/eda/synopsys/syn/W-2024.09-SP5-5/libraries/syn/dw_foundation.sldb'
Warning: DesignWare synthetic library dw_foundation.sldb is added to the synthetic_library in the current command. (UISN-40)
Information: Performing leakage power optimization. (PWR-850)
CPU Load: 2%, Ram Free: 750 GB, Swap Free: 255 GB, Work Disk Free: 232 GB, Tmp Disk Free: 9989 GB
Analyzing: "/ip/tsmc/tsmc16adfp/stdcell/NLDM/N16ADFP_StdCelltt0p8v25c.db"
Library analysis succeeded.
Warning: No TLUPlus file identified. (DCT-034)
Error: Layer 'M1' is missing the 'resistance' attribute. (PSYN-100)
Error: Layer 'M1' is missing the 'capacitance' attribute. (PSYN-100)
Warning: Layer 'M1' is missing the optional 'edge capacitance' attribute. (PSYN-101)
```

6 Generate Reports

1. Report all the violations by entering the following command: `report_constraints -all_violators`
2. Generate a more detailed timing report by entering the following command: `report_timing`
3. Generate an area report: `report_area`
4. You can update the clock period in **TOP.con** based on the timing violation and source the **TOP.con** file and run the synthesis again.
5. You can generate the power report using the command: `report_power`

7 Save the Results

1. Select **File - Save As - mapped**
2. Specify the file name as **TOP.ddc**
3. Make sure **Save all designs in the hierarchy** button is checked, this will save the entire design hierarchy into a single file and click **Open**
4. Alternatively we can save the design by running the command (similar to unmapped file at beginning):

```
write -hierarchy -format ddc -output lab1/mapped/TOP_netlist.ddc
```

5. If you want the output netlist in verilog format, run the following command:

```
write -format verilog -hierarchy -output TOP_netlist.v
```

6. If you are using Synopsys IIC2 for physical design, you can save the output as ASCII format:

```
write_icc2_files -output ./mapped/TOP_icc2
```

References

- Design Compiler NXT Tutorial from ECE-GY 6443: VLSI System and Architecture Design SPRING 2025