ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL

BANDGAP REFERENCE AND LOW DROPOUT VOLTAGE REGULATOR DESIGN FOR CAPSULE ENDOSCOPY SYSTEM

M.Sc. THESIS

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Department of Electronics and Communication Engineering

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KAPSÜL ENDOSKOPİ SİSTEMİ İÇİN BANT ARALIĞI REFERANS DEVRESİ ve DÜŞÜK GERİLİM DÜŞÜMLÜ DEVRE TASARIMI

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Benan Beril İNAM, a M.Sc. student of ITU Graduate School student ID 504191204, successfully defended the thesis entitled "BANDGAP REFERENCE AND LOW DROPOUT VOLTAGE REGULATOR DESIGN FOR CAPSULE ENDOSCOPY SYSTEM", which she prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

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FOREWORD

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ABBREVIATIONS

ADC	**:** Analog to Digital Converter
BJT	**:** Bipolar Junction Transistor
CTAT	**:** Complementary to Absolute Temperature
DC	**:** Direct Current
DTMOS	**:** Dynamic Threshold Metal Oxide Semiconductor
ESR	**:** Equivalent Series Resistor
GBW	**:** Gain Bandwidth Product
LHP	**:** Left Half Plane
LDO	**:** Low Dropout Regulator
MOS	**:** Metal Oxide Semiconductor
NMOS	**:** N-type Metal Oxide Semiconductor
OPAMP	**:** Operational Amplifier
OTA	**:** Operational Transconductance Amplifier
PMIC	**:** Power Management Integrated Circuit
PMOS	**:** P-type Metal Oxide Semiconductor
PMU	**:** Power Management Unit
PSR	**:** Power Supply Rejection
PSRR	**:** Power Supply Rejection Ratio
PTAT	**:** Proportional to Absolute Temperature
PVT	**:** Process Voltage Temperature
RHP	**:** Right Half Plane

SYMBOLS

$\mathbf{A_v}$	: Voltage Gain
$\mathbf{W}$	: MOSFET Channel Width
$\mathbf{L}$	: MOSFET Channel Length
$\mu_\mathbf{n}$	: Electron Mobility
$\mu_\mathbf{p}$	: Hole Mobility
$\mathbf{I_D}$	: MOSFET Drain Current
$\mathbf{V_{GS}}$	: MOSFET Gate-Source Voltage
$\mathbf{V_{DS}}$	: MOSFET Drain-Source Voltage
$\mathbf{V_{th}}$	: MOSFET Threshold Voltage
$\mathbf{V_{dd}}$	: Supply Voltage
$\mathbf{V_{in}}$	: Input Voltage
$\mathbf{V_T}$	: Thermal Voltage
$\mathbf{V_{do}}$	: Dropout Voltage

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BANDGAP REFERENCE AND LOW DROPOUT VOLTAGE REGULATOR DESIGN FOR CAPSULE ENDOSCOPY SYSTEM

SUMMARY

For the last 40 years, there have been many advancements in biomedical systems as there is a huge demand for them. A capsule endoscopy device is one of the biomedical systems which is used for the imaging of the gastrointestinal system. Endoscopic procedures require two operations because when the procedure starts from the esophagus it can only reach until duodenum, however imaging of the small bowel can be only accessed from the anal cavity. This operation is highly uncomfortable for the patient since the diagnosis of the entire gastrointestinal system requires two endoscopic procedures. To make this operation more comfortable for the patient, capsule endoscopy is developed.

The capsule endoscopy system includes a laser source and a laser driver to process the information coming from the source and a transmitter system to transmit the processed data. The transmitter involves an analog to digital converter, transimpedance amplifier, power amplifier, and a phase generator. A single battery is used to supply voltage for all of these mentioned circuits. The battery input voltage of the system decays with time and to increase the lifetime of the capsule it is essential to design a power management unit. This power management unit involves a regulator to create supply voltage for chip blocks and a reference generator to obtain process-voltage-temperature independent reference.

For the regulator, a low dropout regulator is chosen as they do not have ripple at the output voltage as in switching regulators which makes them less noisy. Noise is an important parameter because the input signal is low and any input voltage may affect the operation of the circuits. Traditional LDOs require a large off-chip capacitor at the output to create a right half plane zero and stabilize the circuit. However, the capsule is strictly limited in the area hence a cap-less LDO is designed. To enhance the transient performance after removing the output capacitor, a dynamic bias circuitry is added to the design. Output voltage only changes $\pm 6\%$ with process-temperature-voltage corners. Load and line transient results show that even though the input voltage or output load changes with time, the circuit can still regulate the output voltage.

To obtain reference voltages for the blocks, a bandgap reference voltage generator is designed. In this design, two different design structures are used to achieve temperature independence. Both MOS and bipolar transistors are employed for this purpose. Design with MOS transistors advantages from operating in the subthreshold region hence supporting lower supply voltages however it has a larger variation at the output due to threshold voltage change over corners. Bipolar transistors benefit from less

PVT variation however their performance degrades with lower supply voltages and high temperatures. To use two different characteristics of both designs, a system that switches to better performing structure is built. A comparator is designed to detect temperature and supply voltage. In this system, reference with bipolar transistors operates when the input voltage is higher than 2.8 V and at lower temperatures, and reference with MOS transistors starts to work when the input voltage is lower than 2.8 V and at higher temperatures. To further reduce the variation of the design with MOS trimming structure is implemented to the output resistor and variation decreased from 15% to 5%. The temperature coefficient of the reference generator is calculated as $75\ \mathrm{ppm}/^{\circ}C$.

A power management unit that involves a bandgap reference generator and a low dropout regulator is introduced and designed. Important performance parameters are extracted from the requirements of the capsule endoscopy transmitter. Hence, the layout area is designed to be small and output voltage variation is minimized over PVT corners. The layout of the system is designed and post-layout simulation results are reported in the study.

KAPSÜL ENDOSKOPİ SİSTEMİ İÇİN BANT ARALIĞI REFERANS DEVRESİ ve DÜŞÜK GERİLİM DÜŞÜMLÜ DEVRE TASARIMI

ÖZET

Geçtiğimiz son 40 yılda, biyomedikal sistemler sağlık endüstrisine yönelik ihtiyacın ve ilginin artmasıyla hızla gelişmiştir ve bu alanda birçok yenilik yapılmıştır. Bu yenilikler çok geniş ölçekli tümleştirme teknolojisinin(Very large scale integration) de ilerlemesiyle pekişmiştir. Biyomedikal alandaki gelişmeler sayesinde görüntüleme yapılarak hastanın kanser veya sağlıksız oluşumları önceden tespit edilebilebilmektedir ve bu sayede hayat kurtarıcı rol oynar. Bu cihazlardan bu çalışmada örnek olarak kullanılan kapsül endoskopi cihazı da önemli bir yere sahiptir. Kapsül endoskopi, sindirim sistemlerinde hasarlı dokuların tespitinde kullanılır. Endoskopi işlemi eğer yutaktan başlarsa ancak oniki parmak bağırsağına ulaşır, eğer ince bağırsak görüntülemesi yapılmak isteniyorsa anal görüntüleme yapılması gerekir. Bu yüzden, hastanın görüntülemesinin tek seferde yapılması mümkün değildir. Hastanın iki farklı operasyona girmesi ise hasta için fazlasıyla konforsuzdur. Bahsedilen operasyon tekrarını engellemek ve hastanın konforunu sağlamak adına kapsül endoskopi sistemi geliştirilmiştir.

Kapsül endoskopi sistemi içinde birçok elektronik devre barındırmaktadır. Bu devreler, dokulardan gelen bilginin işlenmesi için lazer kaynak ve lazer kaynağı süren lazer sürücü devresi, lazerden elde edilen sinyalleri işleyebilmek adına yapılan verici devresinde yer alan transempedans kuvvetlendiricisi, analogtan dijitale çevirici, faz üretici devre, frekans karıştırıcı devresi ve güç kuvvetlendiricisi olarak özetlenebilir. Sistemde ise bütün bu devreleri besleyebilmek adına tek bir pil bulunmaktadır. Fakat bu pil zamanla hızla azalan bir davranışa sahiptir. Dokulardan alınan bilginin doğru işlenebilmesi için devreler sabit bir gerilime ihtiyaç duyar fakat bataryanın geriliminin zamanla azalan bir eğriye sahip olması bu durumu zorlaştırmaktadır. Bunun için sistemde bataryanın davranışını optimize eden bir yapıya büyük bir ihtiyaç ortaya çıkar.

Kapsül endoskopinin batarya gerilimini optimize etmek ancak bir güç yönetimi(power management) sistemi ile sağlanabilir. Bu sistem sayesinde verici devresindeki bloklar daha düşük besleme gerilimi ve dolayısıyla daha düşük akım değerleriyle çalışabilir. Düşük akım çekilmesiyle bataryanın ömrü uzaması sağlanır ve sistemden alınan verim artar. Verici bloğuna gelen giriş sinyali oldukça zayıf bir sinyaldir ve bu sinyalin doğru işlenebilmesi için gürültü minimuma indirilmelidir. Gürültünün minimuma indirilmesi ancak akımın azaltılmasıyla sağlanır. Düşük besleme gerilimi kullanılmasıyla ise, devreler daha küçük boyutlarda istenilen performans parametrelerini yakalayabilir. Özellikle kapsül endoskopi alan konusunda oldukça limitlidir ve sistemin boyut

açısından optimize edilmesi sistemin gerçeklenebilmesi adına kritiktir. Bu açıklanan özellikleri sağlamak adına güç yönetimi devrelerinde regülatörler yer almaktadır.

Regülatörler çıkışta sabit gerilim elde edebilmek adına kullanılan devrelerdir. Regülatörlerin çıkışındaki gerilim değerleri giriş geriliminden daha yüksek veya daha düşük olabilir. Bu çalışmada gerilim düşüren regülatör devresi kullanılmıştır. Gerilim düşüren regülatöler, anahtarlamalı regülatörler ve lineer regülatörler olarak ikiye ayrılır. Anahtarlamalı regülatörler, diyot veya transistör veya enerji depolayan element olan indüktör ve kapasitörlerden oluşurlar. Çalışma prensipleri, indüktör üzerindeki akımın sürekli olarak anahtarlamayla değiştirilmesi ve bunun sonucunda kapasite üzerindeki gerilim değerinin anahtarlama frekansıyla hedeflenen gerilime ulaşması üzerinedir. Fakat elde edilen bu gerilim üzerinde, sürekli olarak kapasitenin dolup boşalması sonucunda, dalgalanma yer alır. Bu dalgalanma özellikle biyomedikal devrelerde tercih edilmez çünkü sistemde gürültüye sebep olur. Aynı zamanda, devredeki indüktör ve kapasitörler alanın artmasına sebep olur. Bunlardan kaçınabilmek adına lineer regülatörler tercih edilmiştir. Lineer regülatörler, referans gerilimi ile çıkışın gerilim bölücüden elde edilen sonucuyla karşılaştırılmasıyla elde edilmektedir. Çıkışta temiz ve sabit bir gerilim üretebilmek adına devrede referans ile gerilim bölücü arasında bir geri besleme dögüsü kurulmaktadır.

Sistemde en yaygın olarak kullanılan lineer regülatöre örnek olarak düşük gerilim düşümlü regülatör devresi kullanılmıştır. Düşük gerilim düşümlü regülatörler, giriş gerilimi ile çıkış gerilimi arasındaki fark çok küçük olduğunda dahi çıkışta sabit bir gerilim vermeye devam eder. Bu yüzden batarya ile çalışan sistemlerde, giriş gerilimini zamanla azalmasına rağmen, çıkışta regülasyonuna devam edebilmektedir. Bu devrenin dizaynında göz önünde bulundurulması gereken birçok parametre vardır. Bu parametrelerden ilki devredeki giriş ve çıkış arasında yer alan geçiş transistörünün uygun olarak boyutlandırılmasıdır. Bu sayede devre istenilen gerilim düşüm geriliminde maksimum akımın akmasını sağlar. Devrenin hat ve yük regülasyon parametreleri farklı giriş gerilimi veya yük akım değerlerinde, çıkıştaki gerilimi ne kadar sabit tutabildiğinin ölçüsüdür. Aynı zamanda, verici sisteminde yer alan analogtan dijitale çevirici ve lazer sürücü devreleri belirli zaman periyotlarında daha fazla akıma ihtiyaç duyarlar, bu yüzden hat ve yük üzerinde geçici sinyal analizleri yapmak bu durumu analiz edebilmek adına önemlidir. Bahsedilen parametreler arasında bir takas (trade off) ilişkisi bulunmaktadır, bu yüzden en iyi performansı yakalayabilmek dizayn sürecini zorlaştırmaktadır.

Açıklanan parametreler ve sistemin ihtiyaçları göz önünde bulundurularak, devrenin performans parametreleri tanımlanmıştır. Bu çalışma UMC 180nm teknolojisinde tasarlanmıştır. Genelde düşük gerilim düşümlü regülatörler, stabilize edebilmek için çıkışlarında büyük bir çip dışı (off-chip) kapasitöre ihtiyaç duyar ve bu kapasitör ve eşdeğer seri direnci (ESR) sağ yarım düzlemde sıfır getirir. Fakat, bu kadar büyük boyutta bir kapasitör çipte çok fazla alan kapladığı için özellikle kapsül endoskopide tercih edilmez. Tasarlanan devrede bu büyük kapasitör kaldırılmıştır ve bu devrenin kaldırılmasıyla oluşan geçici yük ve hat sinyallerinin kompanzasyonunu sağlamak adına dinamik bir besleme sistemi eklenmiştir.

Sistemde, verici bloğunun ihtiyaç duyduğu maksimum akım değeri 80 mA olarak hesaplanmıştır. Bu akım değerini sağlayabilmesi ve gerilim düşümünü minimum 200 mV değerinde tutabilmek için 800 μm genişlik, ve prosesin minimum olan kanal uzunluğu değeri olan 360 nm kullanılmıştır. Bu geçiş transistörü üzerinden akan akım değeri yüksek olduğu için prosesin elektromigrasyon (EM) kurallarına dikkat edilerek serimi tasarlanmıştır. Giriş geriliminin 3.3 V ve 2 V değerleri arasında devre çıkışta sabit gerilim sağlayabilmektedir. Devrede hat gerilimi ve yük akımı analizlerine bakıldığında çıkıştaki gerilim üzerindeki proses-gerilim-sıcaklık varyasyonu sonucu değişim yalnızca $\pm 6\%$ olarak elde edilmiştir. Özellikle devre dizaynında çıkıştaki gerilim değişiminin oldukça az olmasına özen gösterilmiştir. Devredeki geçici sinyal analizi sonucunda elde edilen en yüksek değişim değeri ise ± 8 mV olarak bulunmuştur. Devre bütün proses-gerilim-sıcaklık varyasyonlarında stabildir ve faz marjı 50 dereceden fazladır. Devrenin yük kaldırıldığında toplam tükettiği akım 45 μA'dır.

Verici sisteminde, analogtan dijitale çevirici, düşük gerilim düşümlü regülatör gibi devreler operasyonlarında aynı zamanda bir referans gerilim değerine ihtiyaç duyarlar. Bu referans değerinin proses-gerilim-sıcaklık varyasyonlarından etkilenmiyor olması önemlidir, gerilim değeri üzerinde bir hata oluştuğu takdirde devrenin güvenilirliği azalır ve çıkışta hatalı sonuçlar gözlenebilir. Bant aralığı referans devreleri, çıkışlarında sabit bir gerilim oluşturarak, birçok devrenin akım veya gerilim referansı olarak kullanılır. Bu devrelerin çalışma prensipleri, MOS ve bipolar transistörlerin, sıcaklık ile olan karakteristikleri üzerine kuruludur. Sıcaklıktan bağımsız bir gerilim elde etmek için sıcaklıkla doğru orantılı değişen ve ters orantılı değişen iki farklı akım transistorlerin I-V karakteristikleri kullanılarak elde edilir ve bu akım direnç üzerine düşürülür.

Dizayn edilen bant aralığı referans devresinin proses-gerilim-sıcaklık varyasyonunun olabilecek en düşük seviyede olması hedeflenmiştir. Bunun için sistemde iki farklı bant aralığı referans devresine yer verilmiştir. Bunlardan birinde sıcaklıktan bağımsız davranışı elde edebilmek için MOS transistörler diğerinde ise bipolar transistörler kullanılmıştır. MOS transistörlerin kullanıldığı topolojide, sıcaklıktan bağımsızlık bipolardan daha iyiyken, eşik gerilimi proses varyasyonlarında fazlasıyla değişmektedir, aynı zamanda devre eşik-altı bölgede çalıştırıldığı için besleme geriliminin düşük değerlerinde de doğru sonuç verebilmektedir. Bipolar transistörler ise proses varyasyonlarında daha iyi performansa sahiptirler fakat üstünde baz-emetör gerilimi proses ile sınırlı olduğu için besleme gerilimi belirli bir voltajın altına düştüğünde kesime girebilirler. Her iki yapının da avantajlarını kullabilmek adına bir sistem kurulmuştur. Bu sistemde devre oda şartlarında ve 2.8 üzerindeki gerilim değerlerinde bipolar transistörler ile opere ederken daha düşük gerilimlerde ve yüksek sıcaklıklarda MOS ile opere etmektedir. Bunun için bir karşılaştırıcı devresi tasarlanıp her iki karşılaştırma için kullanılmıştır. Sıcaklık ile karşılaştırabilmek adına ayrıca bir sıcaklıkla doğru orantılı değişen bir devre kurulup istenilen sıcaklıkta diğer yapıya geçmesi sağlanmıştır. Besleme gerilimini karşılaştırabilmek için ise bir direnç bölücüden geçirerek referans gerilimi ile karşılaştırarak elde edilmiştir. Devrenin az güç tüketmesi için bu yapılara anahtarlama yapılmıştır ve bu sayede kullanılmayan akım kolları kapatılmıştır. Bu devrenin doğru bir şekilde anahtarlanmasını sağlamak

için bir sayısal devre bloğu da eklenmiştir. MOS transistörlerin kullanıldığı yapıda anlatıldığı üzere proses varyasyonları çıkış geriliminin değişimine yol açmaktadır. Bu değişimi azaltmak adına prosesin bulunduğu koşula göre direnç değerinin azaltılması veya artırılması sağlanmıştır. Bu sayede proses varyasyonu %15'ten %5'e düşürülmüştür. Elde edilen devre proses-gerilim-sıcaklık varyasyonlarında sadece %5 değişime sahiptir. Sıcaklık katsayısı ise $75\ \mathrm{ppm}/^{\circ}C$ olarak hesaplanmıştır.

Bu çalışmada kapsül endoskopinin güç yönetim sistemi üzerine bant aralığı referans devresi ve düşük gerilim düşümlü regülatör dizaynı sunulmuştur. Yapılan dizaynlarda özellikle proses-gerilim-sıcaklık varyasyonunu azaltmaya özen gösterilip çipte az alan kaplaması hedeflenmiştir. Sistemin serim planları tasarlanmış ve serim sonrası sonuçları çalışmada raporlanmıştır.

1. INTRODUCTION

There is an increasing demand for battery-powered systems such as mobile devices, smartwatches, and medical instruments. Especially diagnostic systems in biomedical devices are part of this huge demand. Power management IC (PMIC) becomes one of the crucial parts of these devices to meet operation time and power consumption specifications. The power management system provides clean supply voltage and references voltages to blocks inside the chip. Generation of a supply voltage involves a voltage regulator to regulate the battery input. There are various approaches to designing a voltage regulator which include switching and linear regulators. Using a low dropout regulator (LDO) as a linear regulator is more suitable for biomedical devices as they occupy less area. Various specifications define the performance of the regulator such as transient response, stability, and current capability. Nevertheless, there are performance trade-offs between these parameters which makes it difficult to meet the specifications. LDOs and chip blocks also require a stable precise reference voltage. Bandgap reference circuits are widely used to accomplish this. These circuits generate an output voltage independent of the process-temperature-voltage (PVT) variations. The main idea of bandgap reference circuits is to compose two behaviors that are proportional to absolute temperature (PTAT) and complementary to absolute temperature (CTAT). For biomedical systems, variations in the output voltage become even more critical as the performance of the blocks depends on the stable noiseless reference.

1.1 Purpose of Thesis

Power management unit is crucial part of the biomedical systems as they generally include a battery device discharging with time. Biomedical systems such as capsular endoscopy, includes blocks which require a precise supply voltage and a reference

voltage. Any small variation on the input voltages of blocks such as phase generator or analog to digital converter reduces the performance of the circuit or even lead to incorrect results. To ensure reliable operation of system blocks, power management units are designed to be immune to variations, noise and process parameters.

Power management unit and the system level application example is demonstrated in Fig. 1.1. In this study, low dropout regulator is designed to regulate battery output and create supply voltage and bandgap reference generator circuit is designed to provide reference voltage to low dropout regulator and chip blocks. The system is designed in UMC 180 nm technology. Battery voltage in the system is 3.3 V and in the design MOSFET and bipolar transistor types are chosen to support battery voltage level. Design of both circuits is targeted to have the minimum variation as possible at the output voltage and keep the layout area small.

Designed bandgap reference circuit consists of two different voltage reference generation structures to further increase the performance. Conventional designs consists of only BJT or MOS based transistors to obtain temperature independent voltage. In this structure to achieve smaller variation, both bipolar and MOS transistors are employed for different operation modes. A system containing comparator, logic combination, switch and a trimming structure, is introduced to detect the operation modes to minimize the process variation and input voltage variations. There is a linear relation with the output of bandgap reference and LDO regulator, meaning any variation at the reference voltage affects the regulator output. This is the reason that bandgap reference must have small variation, to provide clean and stable supply voltage, it is essential to design reference voltage accordingly.

Capsular endoscopy is limited with area, however conventional low dropout regulator topologies contains a large off-chip capacitor. Off-chip capacitor can be removed by adding a dynamic biasing structure to compensate transient variations due to lack of capacitance at the output. In this thesis, bandgap reference voltage generation system is presented to minimize the variation, and cap-less LDO regulator is designed to optimize the layout area to satisfy necessary specifications for capsular endoscopy blocks.

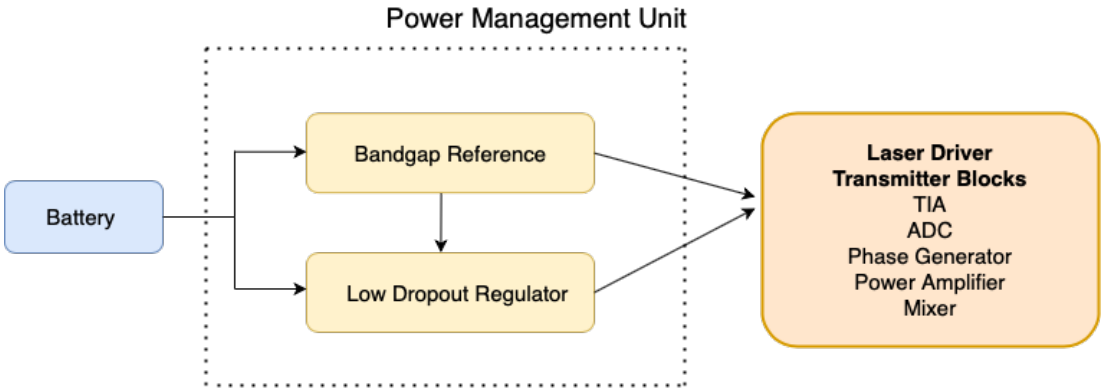

Figure 1.1 : Power Management System of the Capsular Endoscopy.

1.2 Literature Review

There are numerous works to obtain reference voltages for chip blocks aiming to meet various performance targets. The discovery of the bandgap reference circuits dates back to 1971, and it is introduced by Robert Widlar. Developments of the design are followed by Brokaw [1, 2]. Designs are based on the idea of creating Complementary to Absolute Temperature (CTAT) by using the negative temperature coefficient of pn junction voltage and Proportional to Absolute Temperature (PTAT) from the thermal voltage (V_T) as explained in the further sections. These designs allow having only 1.2 V reference voltage due to the summation of V_T and V_{be} can result in the bandgap of the silicon. However, with the advancements in technology scaling down, operating supply voltage is also reduced. Moreover, 1.2 V reference voltage, limits the design of subsequent blocks. Hence, further studies on the design of bandgap references have continued with the generation of sub-1 V references. The constraint of energy bandgap voltage has been overcome by scaling the output voltage through resistors in several studies [3, 4]. Another method is to use DTMOS (Dynamic Threshold MOS) devices, which results in a lower bandgap as the bulk potential is connected to a lower voltage [5, 6]. Further studies have included designs employing MOS transistors in the subthreshold region to make it more suitable for low-power designs [7].

Voltage regulators are one of the crucial blocks of power management systems. Regulators can be classified as switching and linear regulators. Linear regulators

are widely used in biomedical designs where the layout area needs to be smaller and they can provide cleaner output voltage than switching regulators. Linear regulators are mainly step-down converters, and a low dropout voltage regulator is the most popular used one. Most LDO designs include an off-chip capacitance for stability which occupies a large area in the layout [8, 9]. To optimize the area there are recent developments on the capacitor-less LDO topologies which employ additional biasing methods [10–12].

2. BANDGAP REFERENCE CIRCUIT

As mentioned before in earlier sections, blocks inside the capsule endoscopy such as ADC, and power amplifier need voltage reference as an input to operate. Voltage reference needs to be independent from the supply, process, and temperature variations so that blocks will be able to provide the desired accuracy at the output [13]. In addition to process-supply-temperature independence, for biomedical systems, power consumption becomes one of the important requirements to have durable battery management.

2.1 Theory of Bandgap Reference Generator

2.1.1 CTAT generation

As mentioned in the earlier sections, to obtain a temperature-independent voltage reference at the output, we need a CTAT voltage in the circuit. This can be easily achieved by using a device with a pn-junction as it has a negative temperature coefficient. For this purpose, a bipolar junction transistor can be employed as in the BiCMOS process it is only used in a parasitic diode connection.

Bipolar transistors' temperature characteristics can be detailed in the below formulations, as explained in [14]. The current of the bipolar transistor is:

$$V_{BE} = \frac{kT}{q} \ln \frac{I_c}{I_s}. \tag{2.1}$$

From this equation, it can be noticed that the current of BJT strongly depends on the I_s, saturation current. The relation of I_s with temperature is

$$I_s = bT^{(4+M)} \exp \frac{-E_g}{kT} \tag{2.2}$$

where E_g is the energy gap of the silicon, M is the temperature dependence and b is the proportionality factor. From this equation, we can derive the first order relation of temperature with V_{BE} voltage as given below:

$$\frac{dV_{BE}}{d_T} = \frac{V_{BE} - (4+M)V_T - V_G}{T}. \tag{2.3}$$

Finally we can see that bipolar transistors have a negative temperature coefficient of $dV_{BE}/dT = -1.5\ mV/K$ at $T = 300K$.

2.1.2 PTAT generation

There are various design techniques to generate PTAT voltage, which can be explained with the same working principle. As shown in Fig. 2.1, voltages V_1 and V_2 are equal to each other since MP0 and MP1 flow the same current and the voltage drops across MN0 and MN1 will be equal if they have the same sizes. Bipolar transistors are enforced to flow the same current by the current mirrors MP0 and MP1, and as explained before, by nature, they both have V_{BE} voltages decreasing with temperature. If we take the difference between these two V_{BE} voltages, where bipolar transistors are sized with different emitter areas, the resulting voltage has a positive TC characteristic. PTAT voltage is obtained from the linear relation of temperature and V_T, as described in Eq. 2.4-2.6 [14].

$$\Delta V_{BE} = V_{BE1} - V_{BE2} \tag{2.4}$$

$$\Delta V_{BE} = V_T \ln \frac{nI_0}{I_s} - V_T \ln \frac{I_0}{I_s} \tag{2.5}$$

$$\Delta V_{BE} = V_T \ln(n) \tag{2.6}$$

From this equation, it can be seen that the current flowing from MP1 is equal to $V_T \ln(n)/R_0$, and this current is mirrored to the output and summed up with CTAT

voltage V_{EB}. Finally, temperature independent voltage reference at the output can be written as

$$V_{REF} = \left(V_{EB} + \frac{R_1}{R_0} V_T \ln(n)\right). \tag{2.7}$$

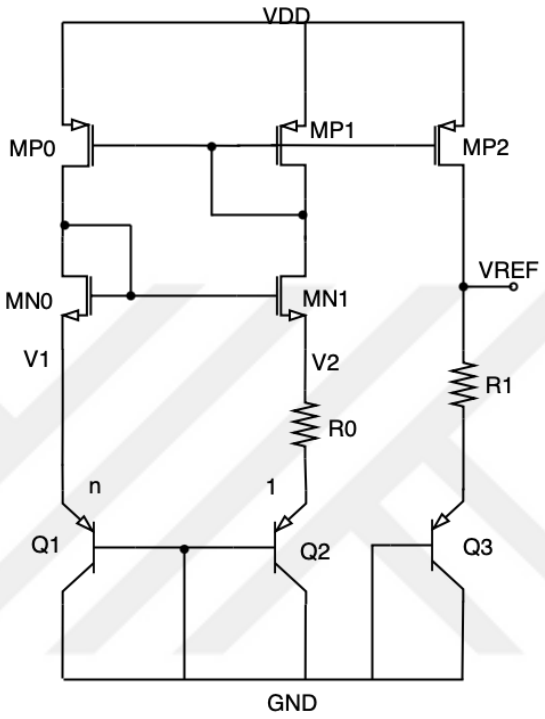

Figure 2.1 : Simple Implementation of Bandgap Reference Design.

2.1.3 Bandgap reference design using BJT

The previous conventional bandgap reference implementation used for the explanation of PTAT and CTAT generation suffers from variation due to many components that need to be matched throughout the design coming from the current mirrors, matching between bipolar transistors and resistors. To mitigate the error, a high gain error amplifier is introduced to the circuit.

Folded cascode amplifier shown in Fig. 2.4 is chosen for the error amplifier as it provides sufficient gain and the stabilization is not complicated as it is self-compensating [15, 16]. The gain of the amplifier can be detailed as follows:

$$A_v = g_{m,mn1}[(g_{m,mn5}r_{o,mn5}(r_{o,mn1}||r_{o,mn2})||(g_{m,mp5}r_{o,mp5}r_{o,mp4}))] \tag{2.8}$$

This amplifier can be divided into two parts, the first part is the differential stage, and input transistors are sized with a rather large width to obtain high gain and low noise from the first stage. The second part is where the voltage-to-current conversion is managed, in this stage lengths of the transistors are sized relatively large to obtain current matching between mirrors and high output impedance to achieve high gain. Input DC voltage of the amplifier is approximately 700 mV as they are tied to the collectors of the bipolar transistors. PMOS inputs are used in the design to obtain the necessary gate to source voltage to operate in saturation.Biasing of the second stage is achieved as shown in Fig. 2.5, by using diode-connected MOS transistors and keeping the transistors of the second part of the amplifier in either saturation or subthreshold regions over PVT corners. Vb0 is used to bias the PMOS current mirror and Vb1 and Vb2 are used for the NMOS current mirror of the cascode part. The Vp is used to bias the tail current of the input stage. To be able to have smaller currents, low-voltage biasing connections are implemented for Vb0 and Vb1. Although the biasing voltages change depending on process variations, they only affect the operation point. Furthermore, as long as the MOS transistors have sufficient gate-source voltages, the amplifier can still provide a high gain.

Bandgap reference with error amplifier is designed as shown in Fig. 2.3. PTAT generation in this circuit is achieved by taking the difference current flowing through the Q_1 and Q_2 over the resistance R_2. Generated PTAT current can be formulated as

$$I_{PTAT} = \frac{V_T \ln(n)}{R_2}. \tag{2.9}$$

Current flowing through the R_1 has CTAT characteristics since it is equal to V_{BE}/R_1. The reference voltage at the output is created by summing up PTAT and CTAT currents and it is copied onto the resistor R_{out} using current mirrors. Current mirrors are sized with large lengths to achieve better current matching. Current matching of temperature independent current is essential since it is dropped onto a resistor to create voltage and

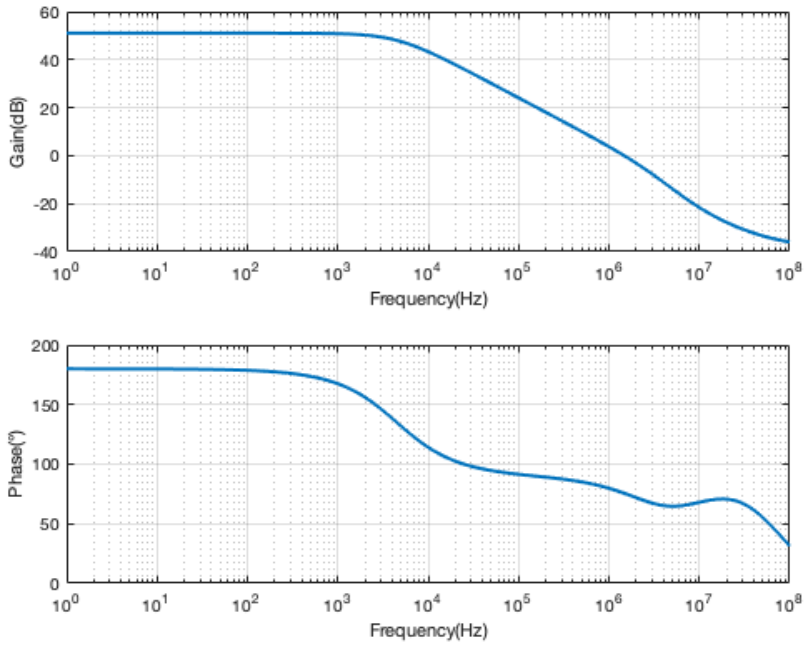

Figure 2.2 : Gain Phase Result of the Error Amplifier.

a small amount of mismatch can lead to an error over the voltage reference. The layout of the current mirrors is handled to have less process variance as possible, and interdigitated layout technique is employed for these transistors. The reference voltage at the output can be obtained as given in Eq. 2.10.

$$V_{REF} = \frac{R_{OUT}}{R_1}\left(V_{BE2} + \frac{R_1}{R_2} V_T \ln(n)\right) \tag{2.10}$$

In this design, value n which is the ratio between BJTs is chosen as 8 to obtain good matching between bipolar devices. The common centroid layout technique presented in Fig. 2.6 is adapted to achieve less process variation after the circuit is produced. Once the n value is selected, the resistor ratio is arranged according to the desired voltage at the output. Unit resistance value used is chosen as $133\ kOhms$ and the resistor ratio between R_1 and R_2 is chosen as 10.25 while the common centroid technique is further applied for the resistors.

The resulting design has a small variation over PVT as a result of using bipolar transistors. However, because the current mirrors and BJTs headroom voltage is

limited by the process, another circuit with MOS transistors is designed to achieve less error on the reference voltage over a wider range.

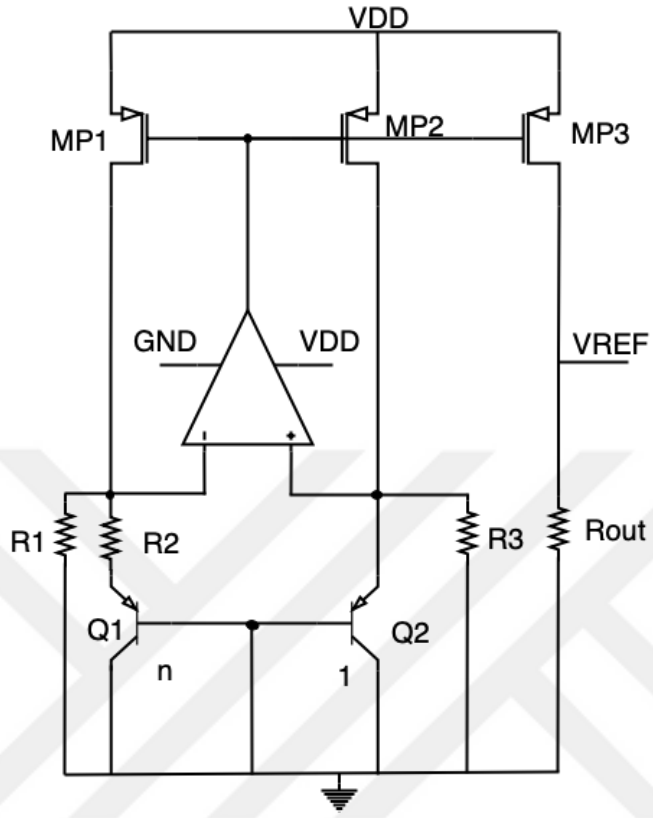

Figure 2.3 : Bandgap Reference with BJT.

2.1.4 Bandgap reference design using MOSFET

Biomedical devices and in this case the design is targeted for a capsular endoscopy system containing a battery that only operates for 2-3 hours and the voltage coming from the battery decays over time. Hence, it is crucial for the power management system to be able to work over a wide range of supply voltage and provide a stable voltage reference to feed the blocks inside the capsule. The aforementioned bandgap reference design with BJT is limited by the supply voltage as BJTs have a certain V_{BE} and once the supply voltage drops it will not be able to operate. This concern brings out the necessity of another bandgap reference design that works at a lower supply voltage. Although BJTs provide less variance over process corners, the performance of a design with BJT is defined by its certain parameters which cannot be modified. To overcome

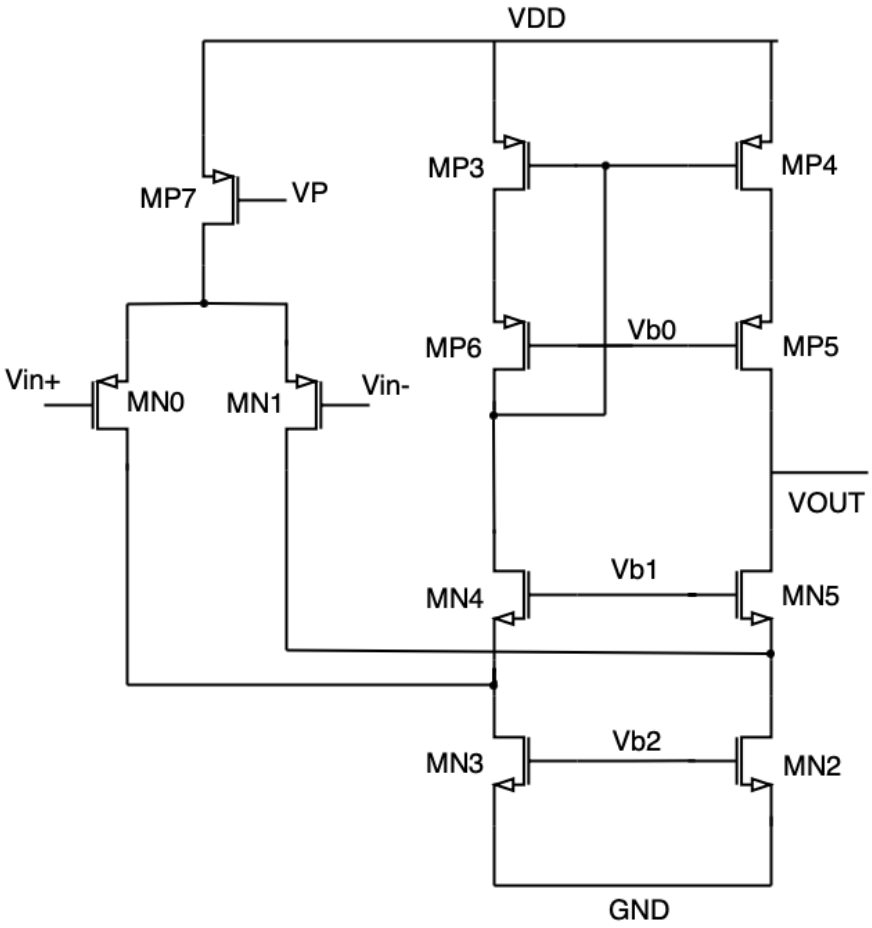

Figure 2.4 : Error Amplifier used for Bandgap Reference with BJT.

this issue, a topology with MOSFETs is embedded into the bandgap reference block, by judiciously choosing in a way that will still provide good performance over layout area and current consumption.

To obtain similar temperature characteristics as bipolar transistors, MOS transistors are used to operate in the subthreshold region (weak inversion). In the subthreshold region, the gate to source voltage is less than the threshold voltage, and as a result supply voltage can be lower because the transistor will need less headroom voltage to operate. Besides, the current flowing through will be significantly small resulting in better noise performance. In this region, MOSFET I-V equation can be given as follows [17]

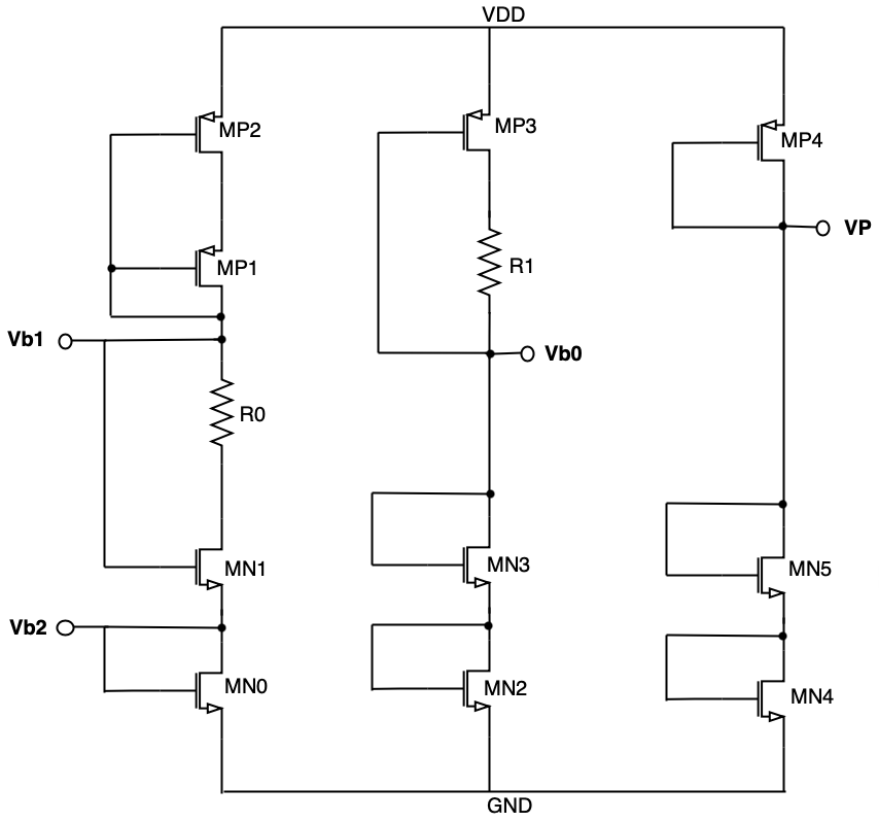

Figure 2.5 : Bias Circuit of Error Amplifier.

$$I_D = \mu_n C_{ox} \frac{W}{L} V_T^2 \exp\left(\frac{V_{GS} - V_{th}}{m V_T}\right) \left[1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right] \tag{2.11}$$

where C_{ox} is gate oxide capacitance, $\frac{W}{L}$ is transistor size ratio, μ_n electron mobility, V_T is kT/q where k is Boltzmann constant, q is electron charge and T is absolute temperature and m is the subthreshold slope parameter. From this equation V_{GS} can be extracted as [18]:

$$V_{GS} = V_{th} + m V_T \ln\left(\frac{I_D}{\mu_n C_{ox} \frac{W}{L} V_T^2}\right) \tag{2.12}$$

From this equation, it can be observed that the negative temperature dependency of the MOS transistor mostly comes from the threshold voltage [19]. Thus the temperature compensation in this topology is obtained by arranging V_{GS} by adjusting the sizes of transistors.

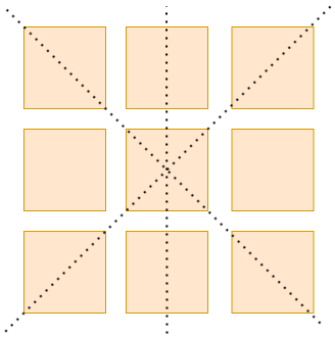

Figure 2.6 : BJT matching for layout.

MOS transistors in subthreshold are employed in the circuit as shown in Fig. 2.7. In this topology, reference voltage is created by summing up the PTAT and CTAT currents over a resistor branch. As described before, PTAT current is generated by equalizing the nodes V_1 and V_2. In order to equalize these nets, a different approach is adopted rather than using an OTA. M_{P0} and M_{P1} flow the same amount of current as they are connected to the cascoded tail currents and by making the gain larger and using wider length transistors current matching will be good enough to make V_1 and V_2 equal to each other. Consequently, PTAT current is generated over the M_{P3} whereas the voltage drop across the resistor is equal to the difference of gate-source voltages of M_{P1} and M_{P2}. V_{GS} drop of the M_{P2} results in a CTAT voltage node and this is used to create the PTAT current by connecting it to the resistor R_1. PTAT current is defined as follows

$$I_{PTAT} = \frac{mV_T \ln(n)}{R_1} \tag{2.13}$$

and by simply summing up the I_{PTAT} and I_{CTAT} currents which flows over the R_{out}, temperature independent voltage at the output can be achieved as given in below formulation

$$V_{REF} = \frac{R_{OUT}}{R_2}\left(V_{SG,MP2} + \frac{R_2}{R_1} mV_T \ln(n)\right). \tag{2.14}$$

The necessary supply voltage can be calculated from the output branch of the circuit and it is equal to the $V_{REF} + V_{DSN} + V_{SGP}$. At the output V_{REF} is defined as 1.2 V according to the necessary voltages for capsular endoscopy blocks and for LDO to provide stable voltage output supply can be used as low as 2 V.

In this design, MOS transistor ratio between M_{P0} and M_{P1} is chosen as 8:1, to achieve total number of 9 MOS pairs and in the layout these transistors are connected to make a square shape which leads to more homogeneous process variation. Once the n is chosen as 8, to obtain desired V_{REF} and temperature compensation resistor ratio between R_1 and R_2 is chosen as 3.7. To accomplish less process variation, resistors are divided into unit resistances of $133\ k\Omega$, and this value is used as well as in the bandgap reference with bipolar transistors mentioned before. The size of the resistors and MOSFET widths are quite large in order to keep MOS transistors in subthreshold region. As mentioned before, gate to source voltage of the MOS transistors are smaller than the threshold region and for that reason it is crucial to make sure the transistors are not changing its region to cutoff. To ensure this V_{DS} voltages of MOS pairs are checked if they are more than 100 mV over PVT corners, so that there is enough headroom voltage to keep them in subthreshold region. In addition, region of the transistors calculated from Cadence operating points are always monitored over corner. Current consumption is obtained as 3 μA which is quite small as a result of large resistors used in the block.

Even though, the bandgap reference design with MOS transistors benefits from lower supply voltage, reference voltage at the output has larger variation because the compensation is dominated by the threshold voltage which changes quite significantly over PVT corners. In order to mitigate this bandgap reference resistor is trimmed which is described in more detailed in later sections.

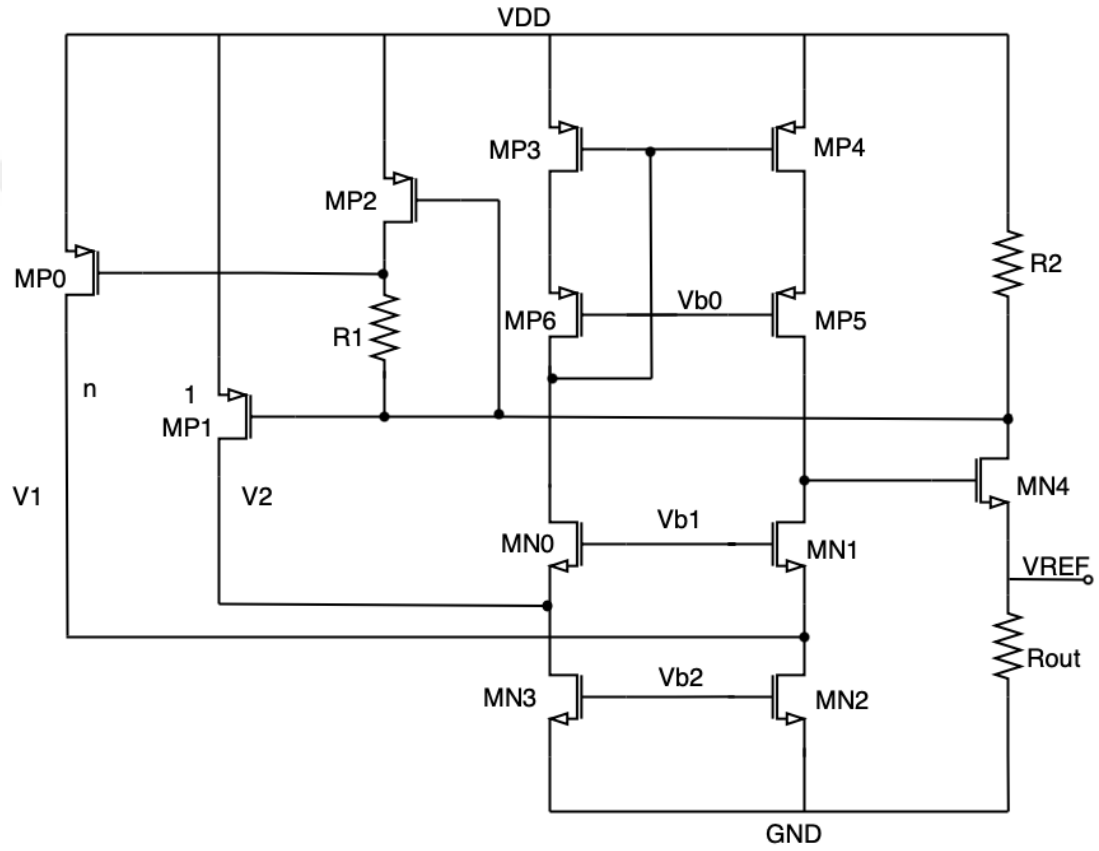

Figure 2.7 : Bandgap Reference with MOS Transistors.

2.2 Bandgap Reference Design employing both BJT and MOSFETs

As mentioned before, two types of bandgap reference circuit have been designed to take advantage of both the bipolar and the MOS transistor characteristics. Reference generation with a MOSFET-based design benefits from operating in a wide range of supply voltages and has a better performance at higher temperatures. Whereas bipolar transistors have the advantages of less process variation and less error on the output voltage. This reference voltage is used in the LDO regulator and a wide supply range is important to have sufficient line sweep and transient parameters. It is also important to have less variance at the output of the LDO regulator because it is crucial to have a stable supply voltage throughout the capsule endoscopy chip. The output voltage of the LDO regulator has a linear relation with the bandgap reference, which is explained in detail in later sections.

The design has initially evolved from the bandgap reference circuit with MOS transistors depicted in Fig. 2.7. After running corner simulations whose results are shown in Fig. 2.21, the circuit is redesigned using bipolar transistors, as presented in Fig. 2.8. In this design, the BJT collector is connected to the MOS tail transistors rather than the ground. However, the UMC180nm process only allows them to be connected to the ground, as these devices are only used for diode-type operation purposes and the collector should be connected to the substrate. In addition, the circuit also suffers from I_B (base current) of the bipolar transistors, which may appear as a leakage current and create error at the output voltage that may not be negligible. To sum up, MOS transistors used for temperature compensation cannot be replaced with bipolar ones altogether.

To introduce a compensation structure with bipolar transistors, the cascode structure in the previous design is further changed to folded cascode by adding a folded PMOS input stage. In this way, instead of designing a second amplifier from scratch and increasing the area even larger, the existing design is revised. Not only the amplifier

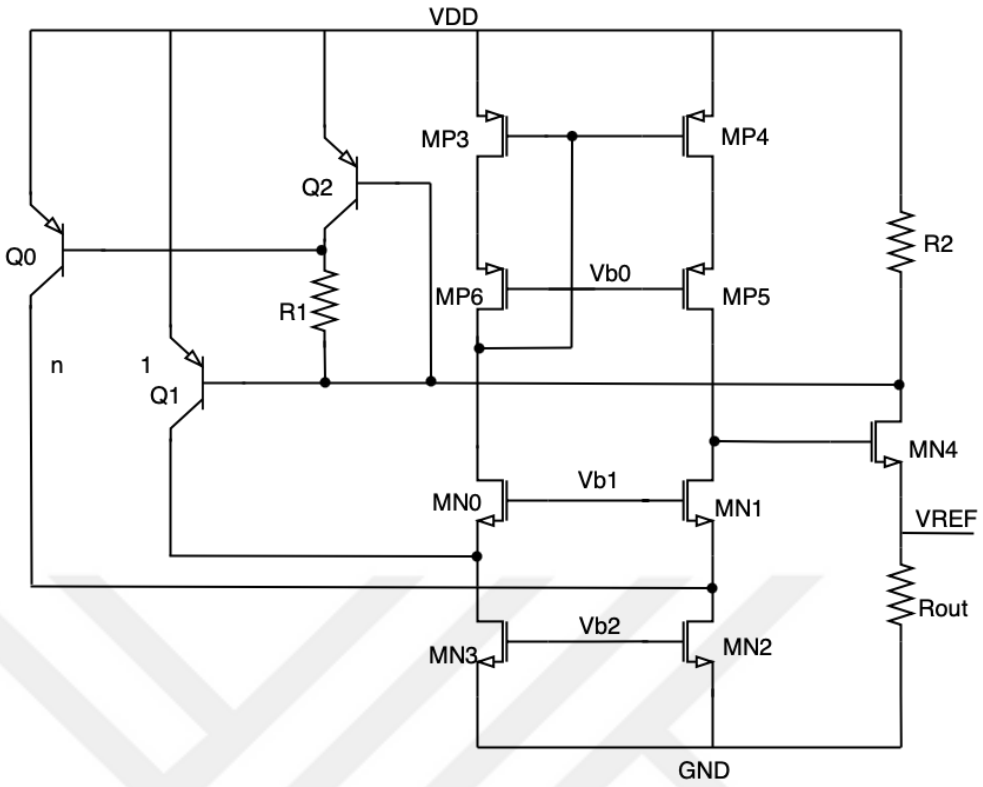

Figure 2.8 : Initial Bandgap Reference Design with BJT.

but also resistors at the output are used in common for both topologies and temperature is compensated by considering resistor values.

Since there are two different bandgap reference structures inside the circuit, keeping both of them in always-on condition would result in large current consumption. Hence, switches are added to the circuit, and MOS is only used when the temperature is higher than $80°C$ and the supply voltage is smaller than 2.8 V. $80°C$ is chosen as a threshold point because, it is observed from the results that, after $80°C$, bipolar transistors' DC value starts to decay, creating a larger variation and showing a temperature dependence. To be able to obtain temperature independence for a temperature range of $-40°C$ - $125°C$, and keep the variation less than 2 %, temperature comparison has been added.

For other conditions, which can be called nominal operation conditions where the supply is 3.3 V and temperature is $25°C$ design with BJT is operating. The operation of the implemented design is indicated in Fig. 2.9. Temperature and supply voltage threshold values are decided after running corner simulations and investigating which

design is more advantageous under defined conditions. Switches used to make this transition, are sized with $2W_{min}$ and L_{min} to optimize area and leakage current.

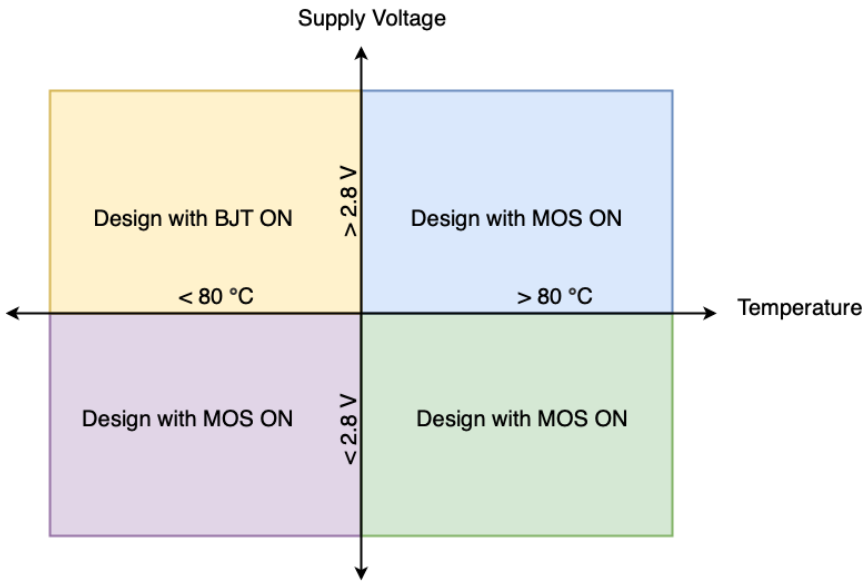

Figure 2.9 : Operating design according to condition.

As mentioned before, a bandgap with BJT and MOS will be used interchangeably depending on the condition, and to achieve this comparators are added to the circuit. Two comparators are used, and the designs are explained in more detail in section 2.2.1: one for the temperature comparison and another one for the supply voltage detection. To detect the supply voltage, since the voltage reference at the output will remain unchanged, it is compared to the proportion of the supply voltage using resistor division. For this resistor, the division ratio is chosen as 3.5 and compared with 800 mV output. Once the supply voltage is lower than 2.8 V, enable MOS signal is activated and all bipolar transistors are turned off. 2.8 V is chosen as a threshold for this application because comparison is done through output voltage reference, hence design with bipolar transistors is ensured to operate accurately with that supply and also have a margin of error. For temperature comparison, again the proportion of supply voltage after resistor division is compared with PTAT voltage generated from the circuit shown in Fig. 2.10.

PTAT generator circuit must stay always on in all conditions, hence the circuit is designed to have low current consumption (I_q), thus resistor value is chosen large. In

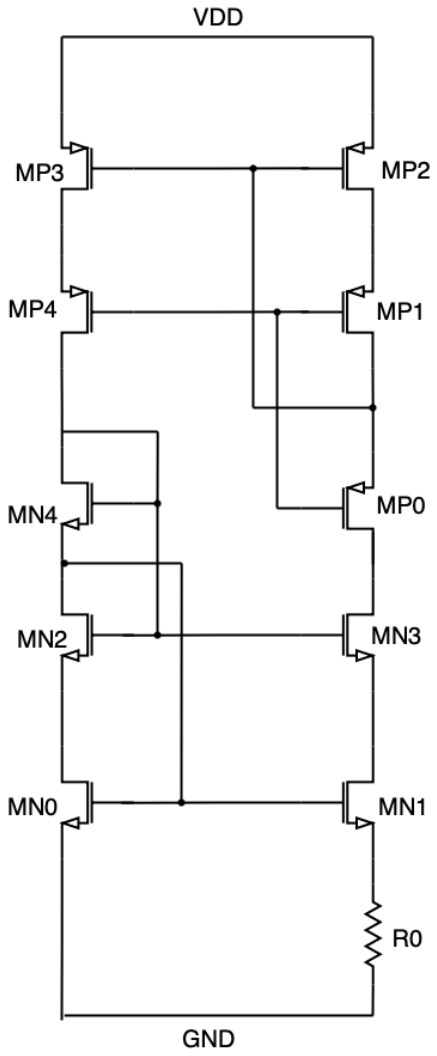

Figure 2.10 : PTAT Voltage Generation Circuit.

this conventional topology, PTAT voltage is generated by equalizing V_A and V_B with the help of current mirrors. Resulting voltage at the output is $V_{GS1} = V_{TH} + I_{PTAT}R_0$ and PTAT voltage is obtained by arranging I_{PTAT} and R_0 [20, 21]. Once, the PTAT voltage is obtained, it is compared with the voltage value where it clashes $80°C$ by using resistor division from the supply voltage.

Switching between BJT and MOS compensation transistors is performed using a logic block shown in Fig. 2.11. Comparator outputs of temperature and supply voltage are connected to the NOR gate. There are inverters at the outputs of the comparator, as inverters create a buffering from the analog output. Finally, the enabling signals go to the switches used for transition.

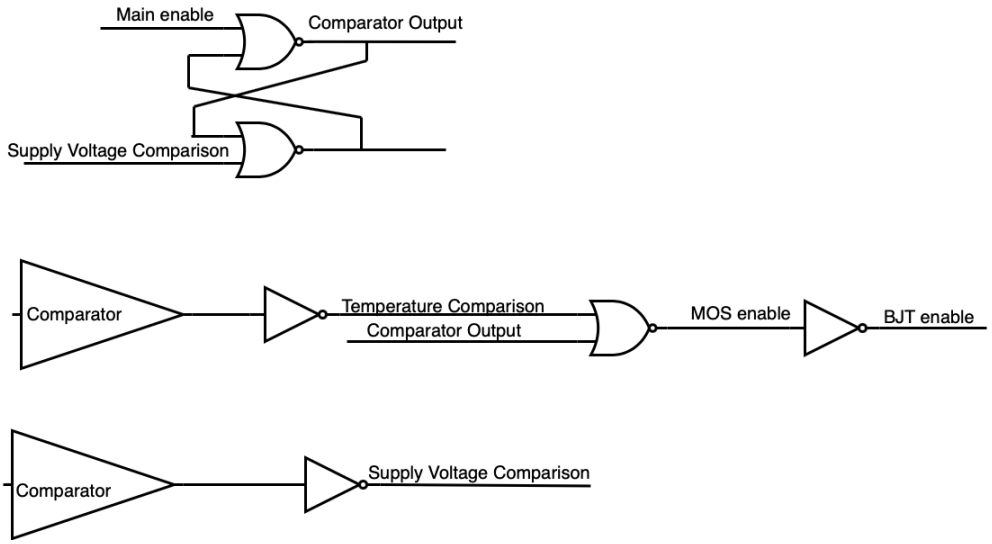

Figure 2.11 : Logic used for switching between MOS and BJT bandgap circuits.

As mentioned earlier, MOS transistors have more PVT variation than bipolar transistors. Once the output of the bandgap is connected to the LDO regulator, voltage variation at the output of LDO reaches 15% over the corner. To mitigate this error and create a more robust LDO, the bandgap circuit is trimmed for MOS transistors. Output resistors are trimmed to reduce resistor and V_{TH} variations. Switches are sized in the same manner explained earlier to balance leakage current and area consumption. The trimming procedure is interpreted in detail in section 2.2.2.

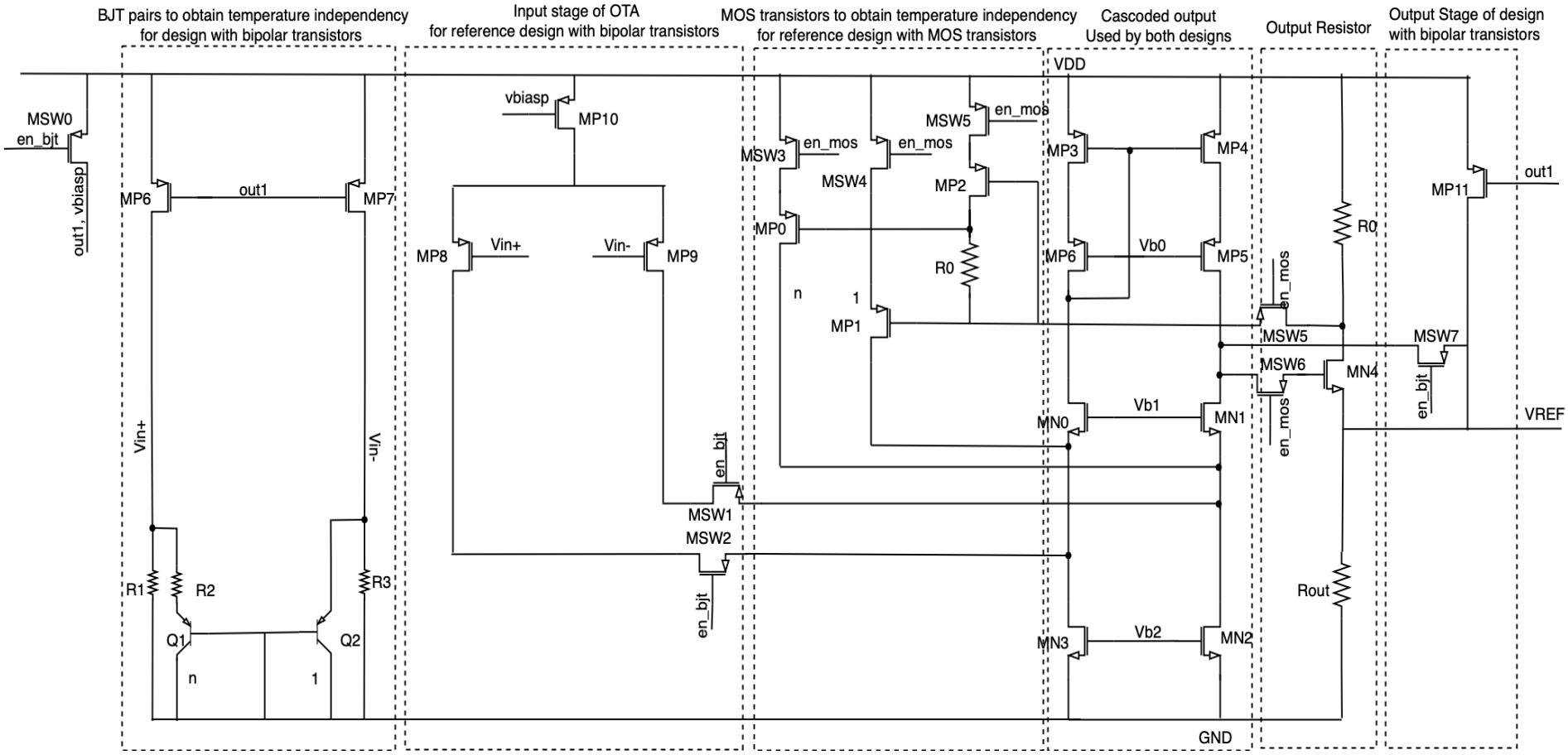

Figure 2.12 : Implemented design of Bandgap Reference.

2.2.1 Comparator design and results

As mentioned before, comparator is added to the circuit to employ both MOS and BJT type bandgap reference structures. One comparator design is used for both comparisons of temperature and supply voltage detection. Circuit aims to detect signal transition and according to the defined hysteresis point, at the output give a voltage either equal to supply or ground.

For this design, circuit shown in Fig. 2.14 is implemented. NMOS input stage is preferred as for the voltage and temperature detections inputs are 0.8 - 1.2 V levels and they are faster than PMOS inputs because of higher mobility. All transistors are sized with L_{min} to optimize layout area and to achieve faster speed by minimizing the gate capacitances. Current mirroring transistors are matched in the layout. As shown in Fig. 2.13, when the input crosses the reference input of 1.2 V, after 7 us of delay, output voltage is high. Since comparator is used for a circuit working in low-frequency system further complexity is not introduced. Comparator block uses total of 1.5 μA current.

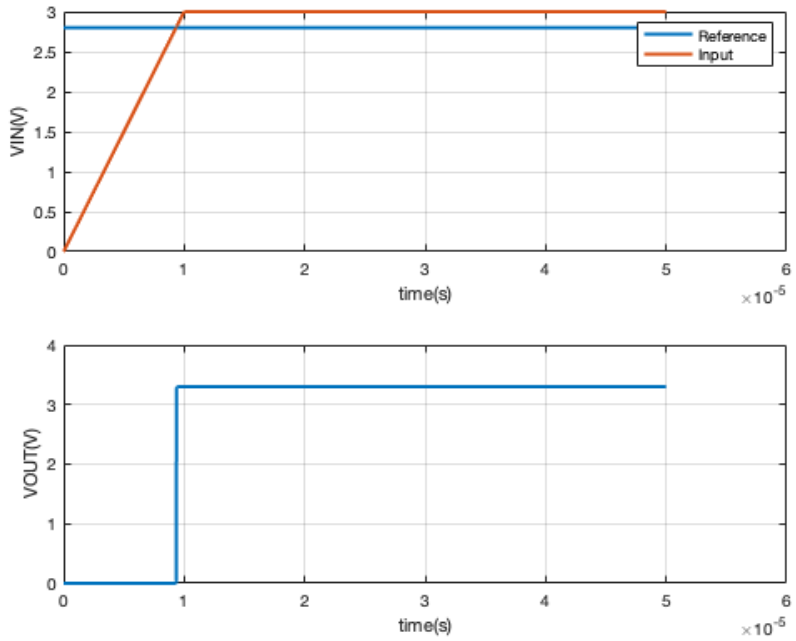

Figure 2.13 : Comparator Transient Signal Results.

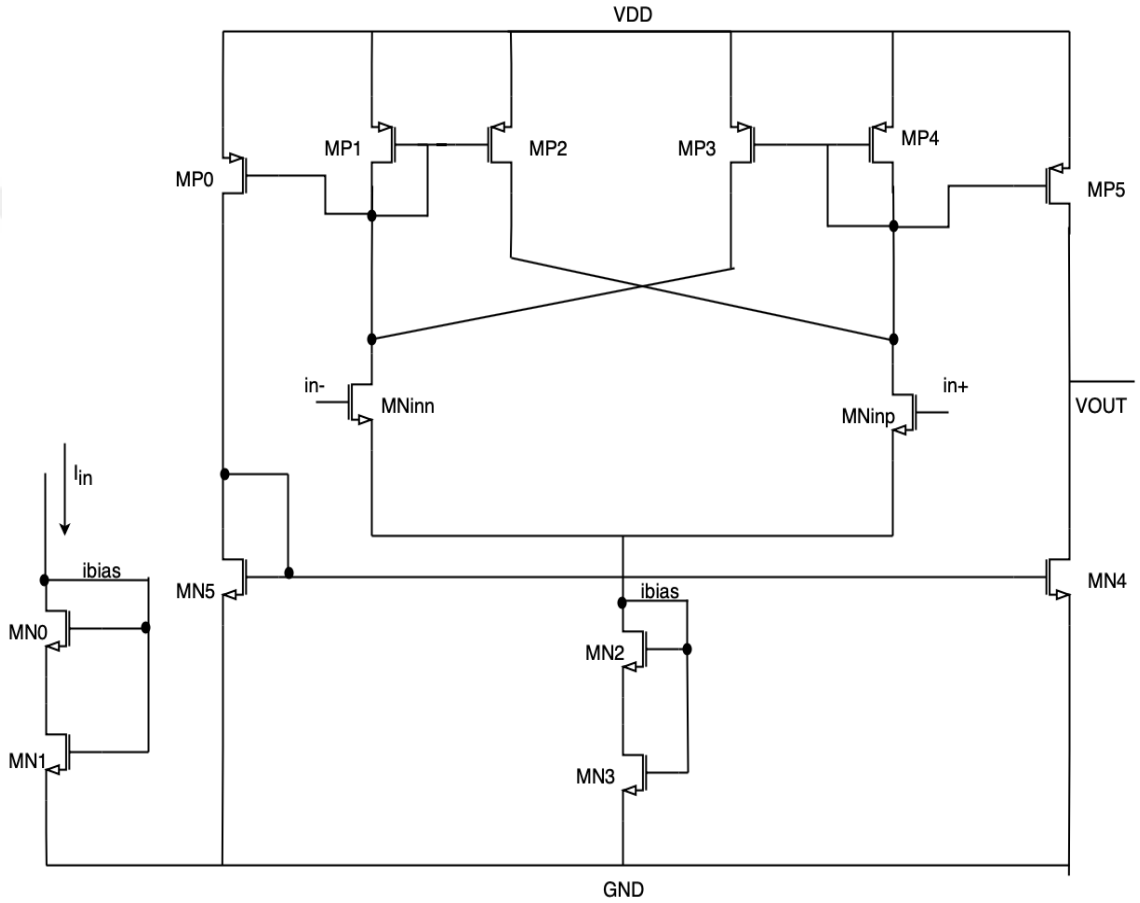

Figure 2.14 : Comparator Design.

2.2.2 Trimming

Results of a bandgap reference design with MOS transistors show that there is a large variation over MOSFET and resistor process corners. V_{th} of MOS transistors varies greatly at slow-slow and fast-fast corners and resistor changes at passive high and passive low corners. However, a large variation at the output of the bandgap increases at the voltage regulator output as the reference is scaled using resistors. To achieve the target performance of 5% variation at the output of the regulator, the bandgap reference design with MOS transistor is further trimmed. Since 5% target is already achieved with BJT, trimming is only done for a transistor with MOS design.

Trimming can only be done at room temperature at $27°C$ to compensate for process variations. Trim bits are decoded to take the input codes as thermometer coding. To achieve the target voltage resistor the output value is changed by adding switches and a logic combination. Using logic combination, 3-bit trimming code is inserted into the circuit. Using more trim codes means additional pads in the chip and it results in a larger layout area, hence 3-bit input is chosen to optimize the area. To find the correct trim code, Monte Carlo corners are run, and trim codes are swept. Once the circuit reaches the desired output voltage, the trim code is found and set. Corner simulations are done using the trim code extracted from the mentioned procedure. Finally, using the trim code output DC voltage is extracted, and trimming results are as shown in Table 2.1. PVT variation of design with MOS is reduced from 15% to 5% using trimming.

Table 2.1 : Reference Voltage post-layout Corner Results after trimming.

	Typ (mV)	Min (mV)	Max (mV)
V_{REF}	605	570	635

2.3 Bandgap Reference Simulation Results

Schematic simulation results of bandgap reference with only BJT are given in Figs 2.15, 2.16, and 2.17. Temperature is swept from $-40°C$ to $125°C$, process and input voltage corners are simulated. As it an be observed, output voltage starts to shift notably, due to characteristics of the design and this behaviour is adjusted with the help of design with MOS. Advantage of this design is that it has less process variation, because BJT has only two corners either slow or fast. Output voltage variation is 2% over corner. Corner results show a scattering to two different directions. This is due to resistor changes as low or high over corner and output voltage is higher when resistor value is at passive low (pass-lo) corner and it is low when resistor value is at passive high (pass-hi) corner.

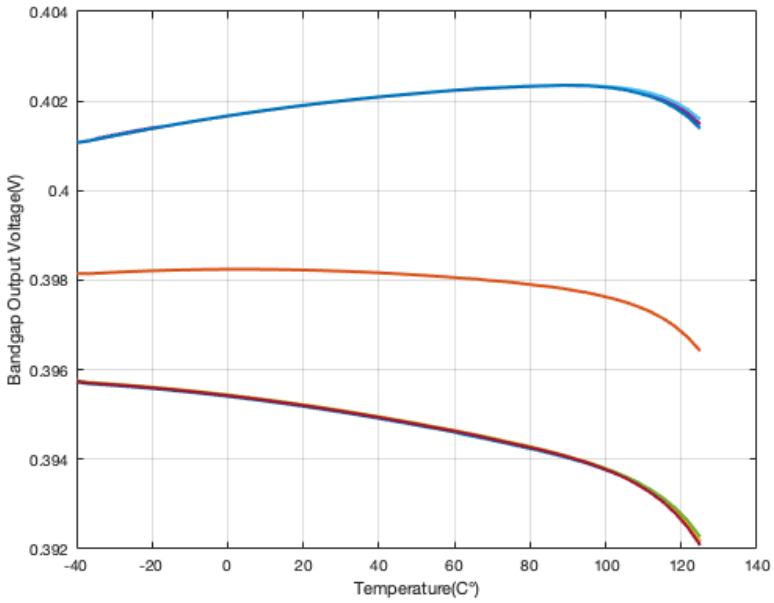

Figure 2.15 : Reference with BJT 400 mV Output Schematic Corner Results (Blue:Pass-lo corners, Red:Pass-hi corners, Orange:Typical corner).

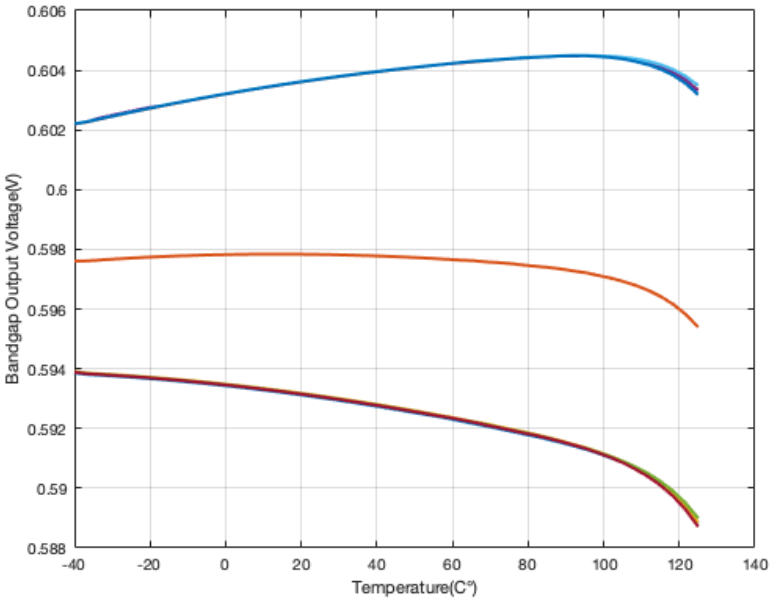

Figure 2.16 : Reference with BJT 600 mV Output Schematic Corner Results (Blue:Pass-lo corners, Red:Pass-hi corners, Orange:Typical corner).

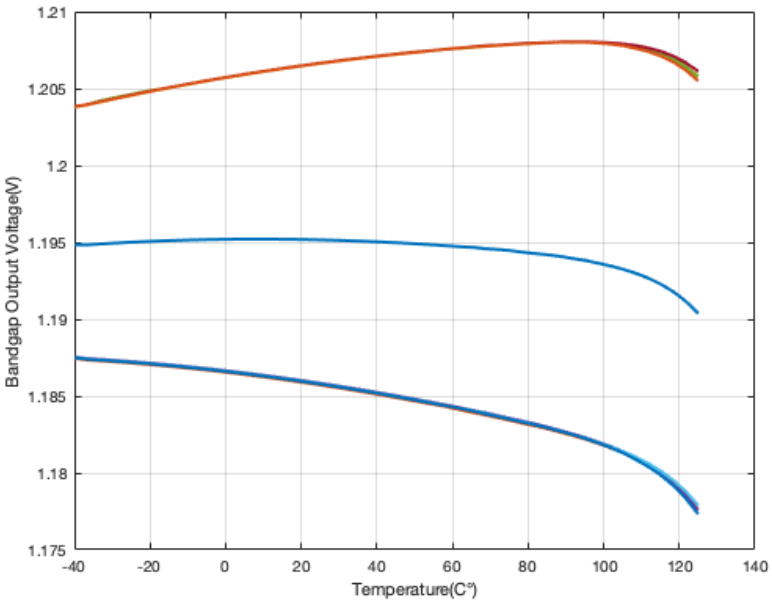

Figure 2.17 : Reference with BJT 1.2 V Output Schematic Corner Results (Orange:Pass-lo corners, Dark blue:Pass-hi corners, Blue:Typical corner).

Same simulation setup is run with post-layout extraction and results are given in Figs. 2.18, 2.19, and 2.20. Results are similar to schematic ones, which shows that components are well matched in the layout.

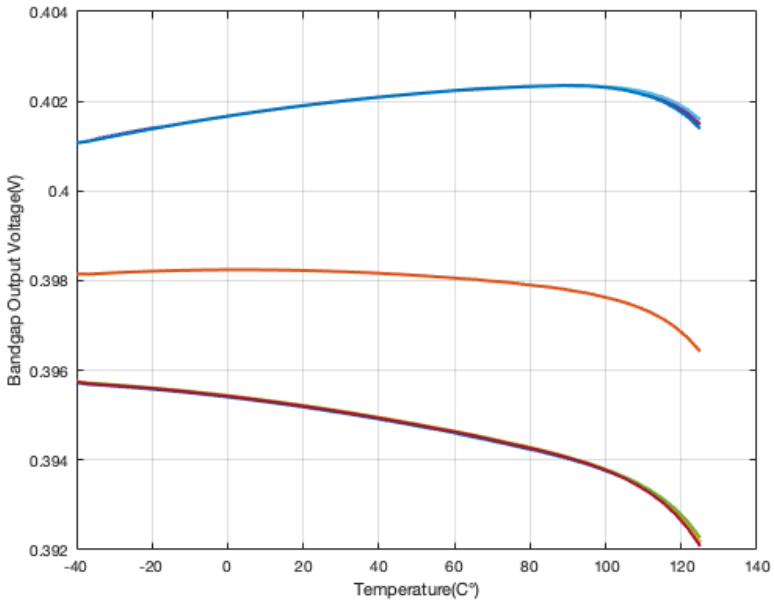

Figure 2.18 : Reference with BJT 400 mV Output RCX Corner Results (Blue:Pass-lo corners, Red:Pass-hi corners, Orange:Typical corner).

Schematic simulation results of bandgap reference with MOS transistor are given in Figs. 2.21, 2.22, and 2.23. Threshold voltage of the MOS transistors depends highly on the process and results also show that output changes with process voltage. However, temperature variation is less compared to design with bipolar transistors.

Post-layout simulation results of bandgap reference with MOS are demonstrated in Figs. 2.24, 2.25, and 2.26. Simulation results are similar to schematic. Output voltage variation is around 13 %.

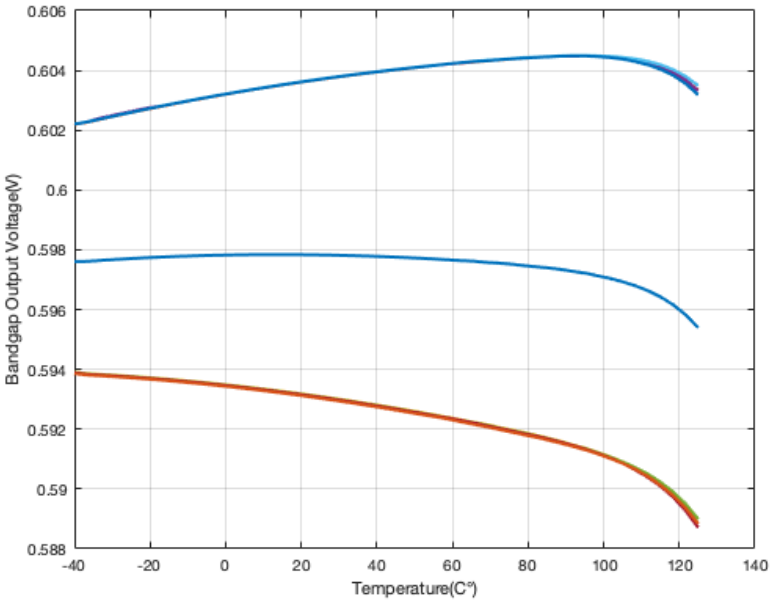

Figure 2.19 : Reference with BJT 600 mV Output RCX Corner Results (Dark Blue:Pass-lo corners, Orange:Pass-hi corners, Blue:Typical corner).

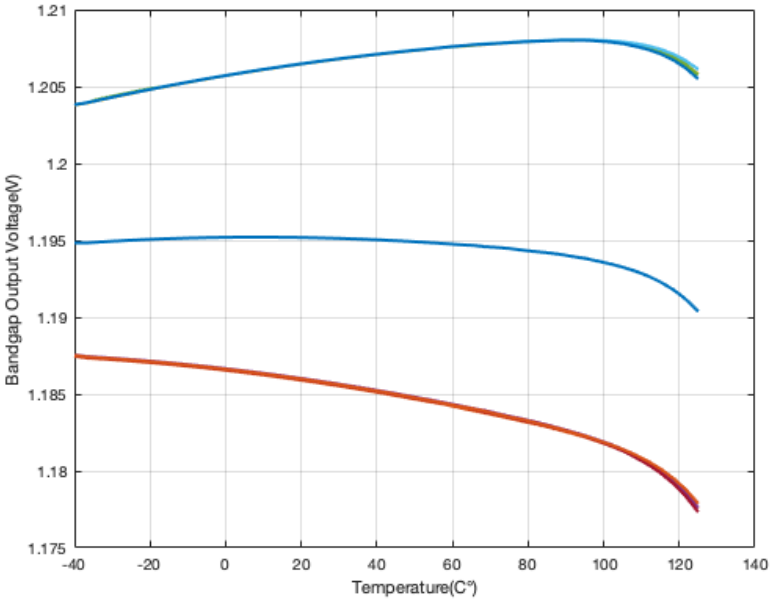

Figure 2.20 : Reference with BJT 1.2 V Output RCX Corner Results (Dark Blue:Pass-lo corners, Orange:Pass-hi corners, Blue:Typical corner).

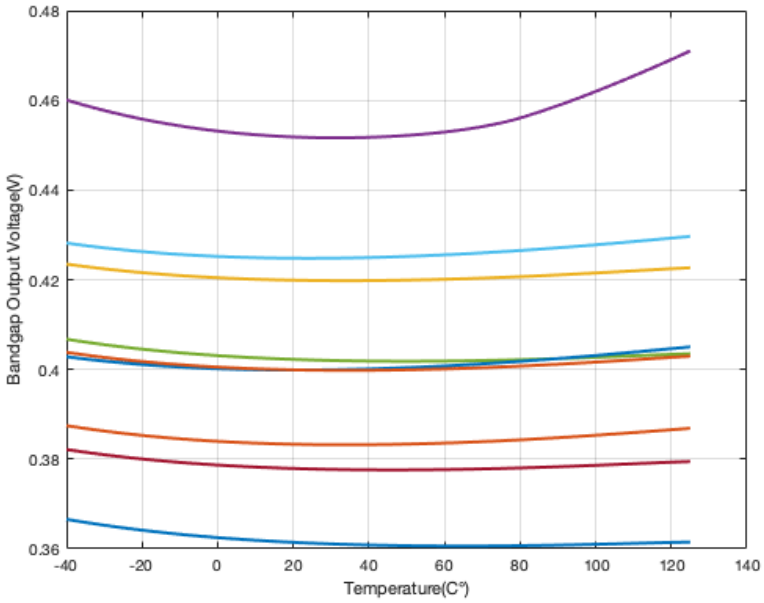

Figure 2.21 : Reference with MOS 400 mV Output Schematic Corner Results (Purple:Pass-lo corner, Blue:Pass-hi corners, Green:Typical corner).

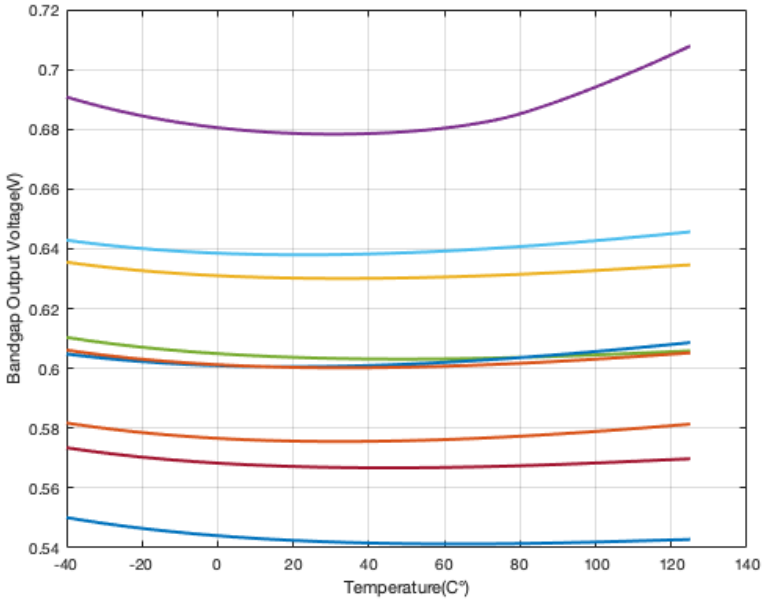

Figure 2.22 : Reference with MOS 600 mV Output Schematic Corner Results (Purple:Pass-lo corner, Blue:Pass-hi corners, Green:Typical corner).

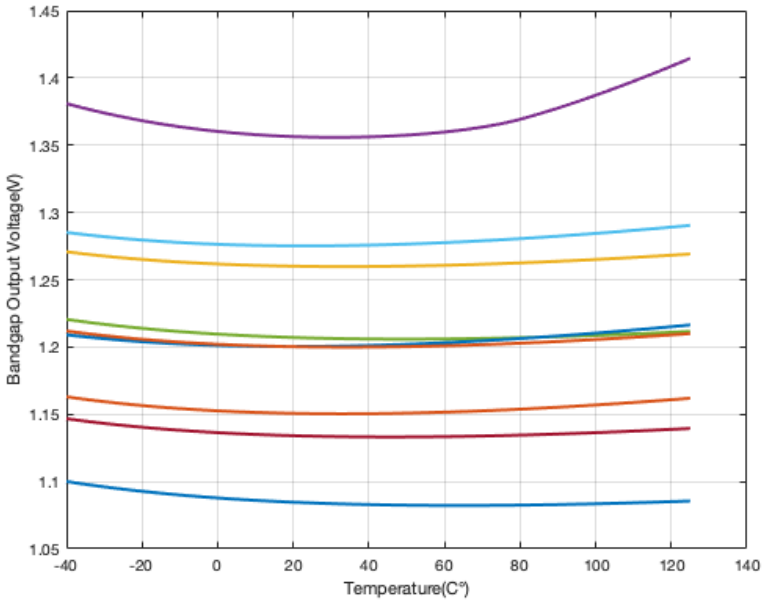

Figure 2.23 : Reference with MOS 1.2 V Output Schematic Corner Results (Purple:Pass-lo corner, Blue:Pass-hi corners, Green:Typical corner).

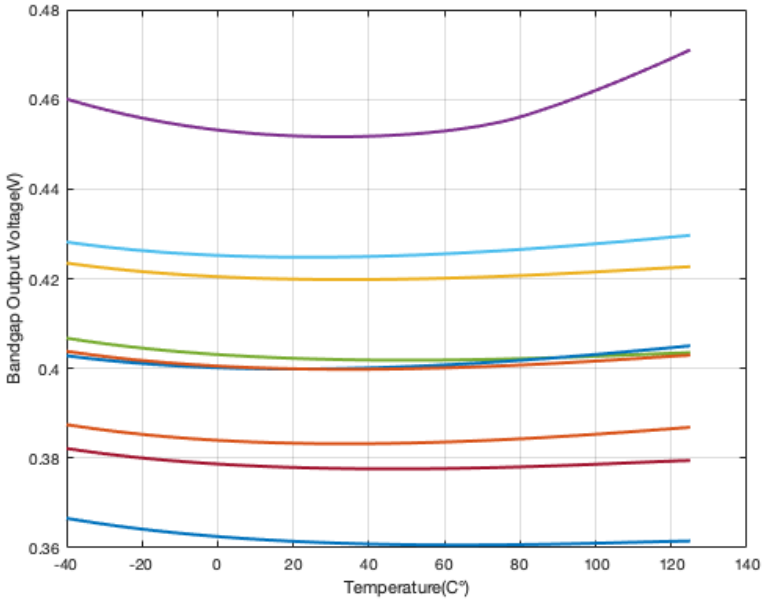

Figure 2.24 : Reference with MOS 400 mV Output RCX Corner Results (Purple:Pass-lo corner, Blue:Pass-hi corners, Green:Typical corner).

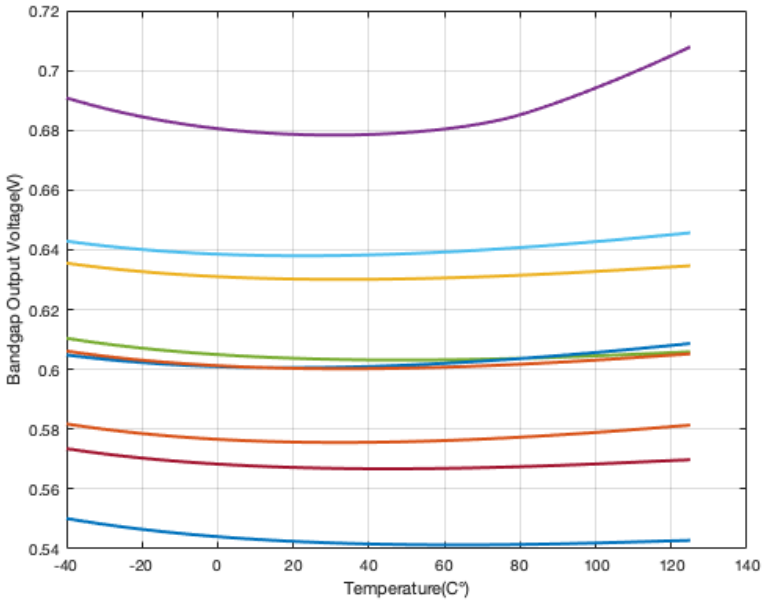

Figure 2.25 : Reference with MOS 600 mV Output RCX Corner Results (Purple:Pass-lo corner, Blue:Pass-hi corners, Green:Typical corner).

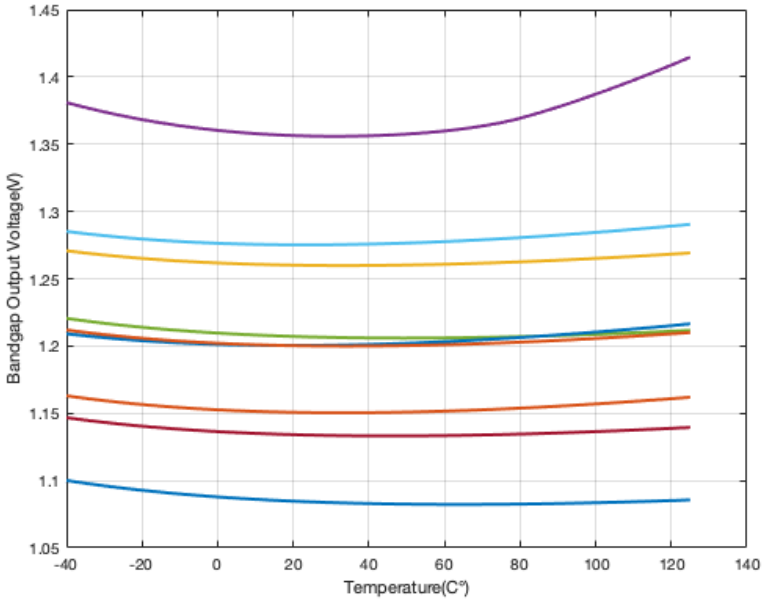

Figure 2.26 : Reference with MOS 1.2 V Output RCX Corner Results (Purple:Pass-lo corner, Blue:Pass-hi corners, Green:Typical corner).

Finally, results of implemented design including both structures with MOS and bipolar transistors are presented in Figs. 2.18, 2.19, and 2.20. It can be seen that when the temperature is higher than $60°C$, design with MOS transistor is operating while lower temperatures bipolar one is working. Process variations are shown in the section 2.2.2, and it is only 5 % after trimming. Due to switching between MOS and bipolar, there is a jump however, temperature variation is limited with 1.3 % and behaviour of the switch does not degrade the performance. Temperature coefficient of the final design is calculated as $75\ \mathrm{ppm}/°C$.

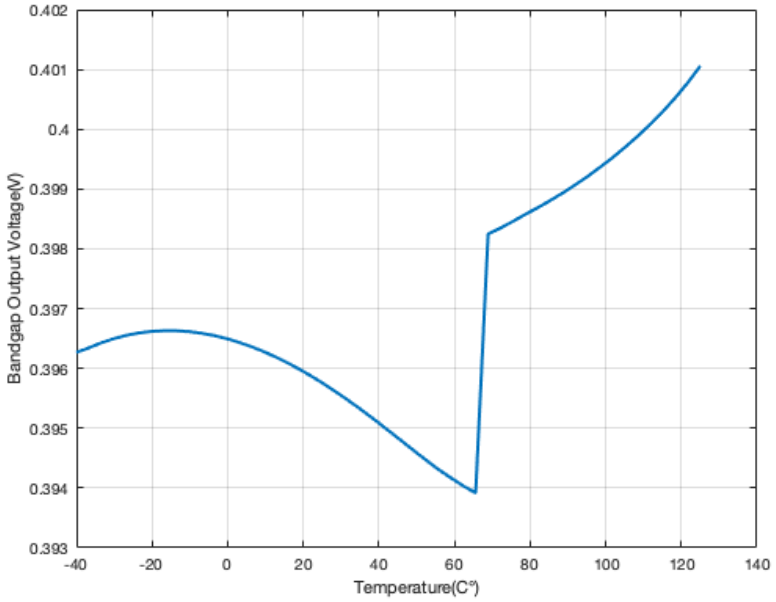

Figure 2.27 : Reference with implemented design 400 mV Output

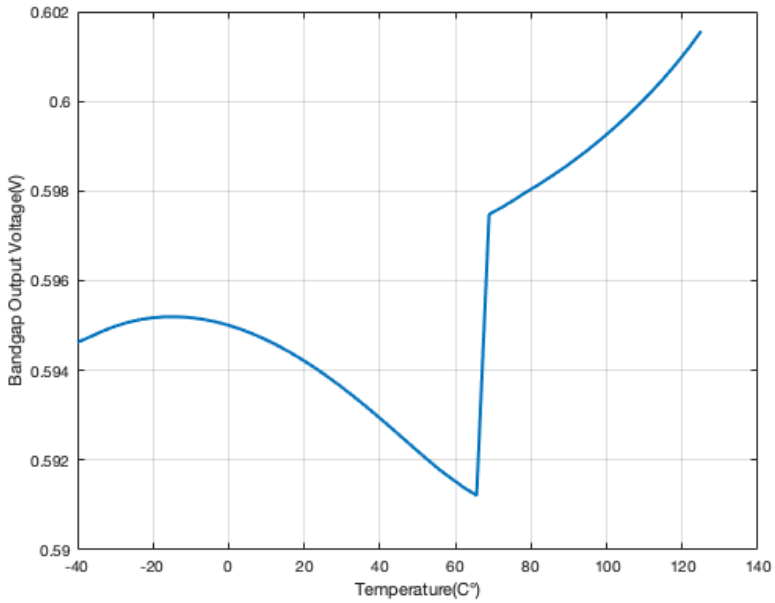

Figure 2.28 : Reference with implemented design 600 mV Output.

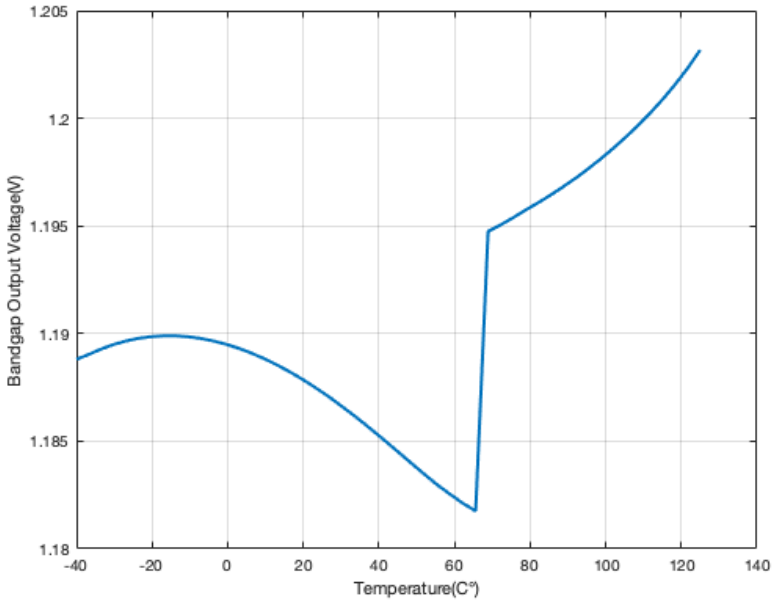

Figure 2.29 : Reference with implemented design 1.2 V Output.

2.3.1 Monte Carlo results

Monte Carlo simulation tool is used to observe the effects of mismatch and process variation. Output voltage variations are obtained using 500 number of yield and at room temperature. Standard deviation is obtained as $\pm 2.55\ mV$ and the output voltage variation is $\pm 1.2\%$ at 3 sigma variation and $\pm 1.7\%$ at 4 sigma variation. Post-layout simulations give $\pm 1.13\%$ at 3 sigma variation and $\pm 1.68\%$ at 4 sigma variation. This proves that good matching performance is achieved in the layout.

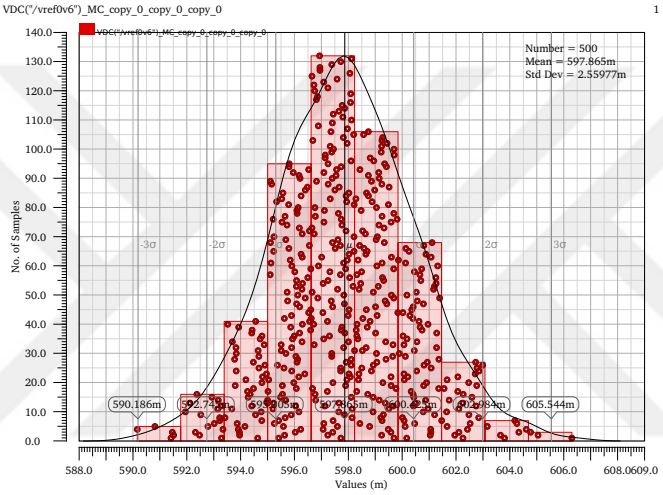

Figure 2.30 : Monte Carlo schematic results of reference with implemented design.

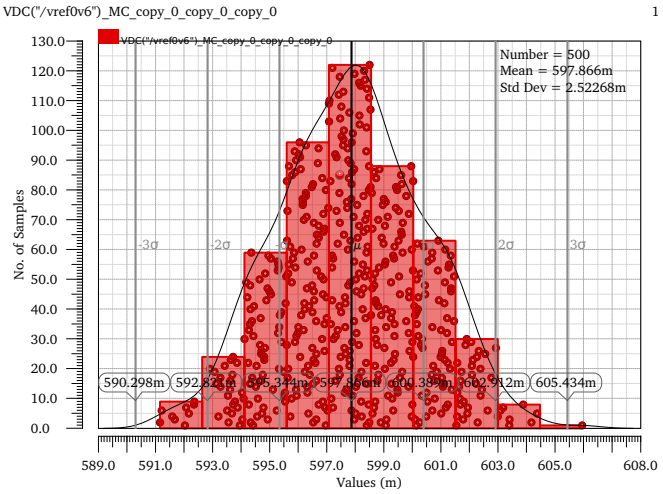

Figure 2.31 : Monte Carlo RCX results of reference with implemented design.

2.3.2 Noise simulation results

Output noise simulation results are given in Figs. 2.32 and 2.33. At 1 Hz, in both schematic and post-layout results equivalent output noise is 9 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$. The main contribution to noise comes from the resistors in the form of thermal noise because they are sized large to have less current. Contribution of the flicker noise is decreased by sizing the width and lengths of the transistors large. The post-layout result is highly similar to the schematic, it starts to differ from the schematic after 1 MHz and the reason is the capacitor parasitics start to affect the circuit at high frequencies. However, since this circuit only works in low-frequency, it does not cause performance degradation.

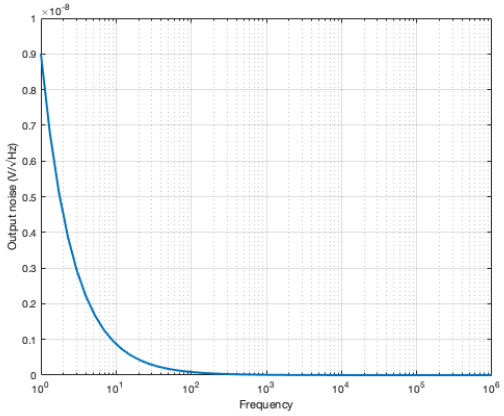

Figure 2.32 : Noise simulation schematic results.

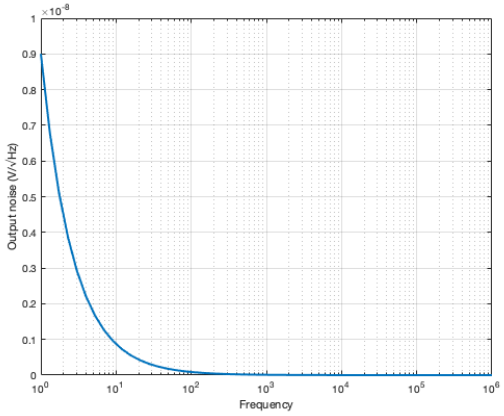

Figure 2.33 : Noise simulation RCX results.

2.3.3 Transient simulation results

Battery voltage can have small disturbances due to switching operations of ADC. It may reduce or increase for a brief time and then settle back to its initial voltage. To emulate this behavior, the supply voltage is changed from 2.8 V to 2.7 V and then back to 2.8 V with 5 μs rise and fall times. Voltage values around 2.8 V are chosen because this is the threshold where the comparator gives the flag for enabling the MOS transistors and the comparator response can be monitored with this simulation. The transient simulation result is given in Figs. 2.34 and 2.35 show that after total of overshoot and undershoot of 4 mV it settles back to its desired reference value.

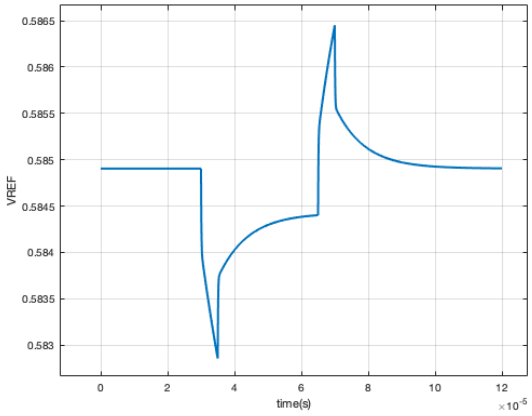

Figure 2.34 : Schematic result of transient response of bandgap reference.

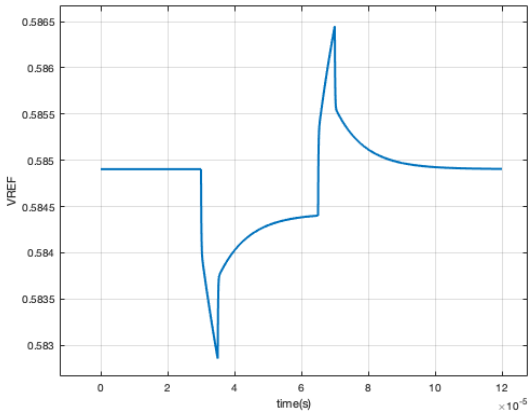

Figure 2.35 : RCX result of transient response of bandgap reference.

3. VOLTAGE REGULATORS

Capsular endoscopy is targeted to have a battery with a 3.3 V supply with 80 mA current capability, however, this voltage rating and current delivery decay over time. To increase the lifetime, biomedical devices such as capsular endoscopy needs a voltage regulator. Voltage regulators differ from the aforementioned voltage references as they can have a load current. While they both can be used for biasing, voltage regulators are generally used to supply voltage and current to the chip.

There are two types of voltage regulators: switching and linear regulators. Switching regulators have high efficiency and as an example of switching regulators, boost and buck converters or buck-boost converters. Switching converters' working principle depends on the charging and discharging of passive elements. Since passive elements are used in this structure, they consume larger areas and have a slower transient response, what is more, the compensation of switching converters is more complex than linear regulators. They also contain switching noise over the output voltage. For these reasons, to supply voltage, a linear voltage regulator is preferred in this study as it is a part of a biomedical device that has a hard limit on die size and is less noisy.

Linear regulators provide a stable voltage at the output lower than the input voltage which is the battery voltage in this study. The working principle of the linear regulators is shown in the block diagram Fig. 3.1. Battery voltage is dropped onto the element called the pass device, and to obtain the desired voltage at the output a feedback loop is created by using an error amplifier that takes the reference voltage as an input. This topology is called a low dropout regulator because the voltage drop at the pass device is small.

LDO regulators are widely used in power management units. They are usually preferred with battery-supplied topologies as they consume less area, and do not suffer from ripple noise as switching converters. Power management units in IoT

or biomedical devices have certain limits when it comes to noise, and mitigation of it from the supply voltage is essential. The output of the battery has nonidealities since it comes from a power delivery network containing many parasitic resistors, inductors, etc, or the supply could simply be a switching converter's output having a large ripple noise at the output. This is why one of the most important specifications of LDO is the power supply rejection ratio (PSRR), to obtain clean output voltage suppressing battery or supply noise is crucial. To obtain this, there are several studies focused on the methods of suppressing AC noise components and achieving high PSRR [22–24]. Another important specification of the LDO is the fast transient behavior. Chip blocks that are connected to the load of the regulator can flow higher current on specific cycles, and the supply voltage needs to be stable over these disturbances. Researchers proposed various methods to enhance transient response which mostly include increasing current consumption and the slew rate [25–27]. In addition to these specifications, most designs usually require an off-chip capacitance for stability [8, 9]. However, most studies propose new design techniques to eliminate the huge capacitor at the output and reduce the layout area spectacularly. Most capacitor-free designs employ a structure with a dynamic or adaptive biasing method to boost the current capability at the output and enhance the slew rate [10–12].

From mentioned previous studies on LDO regulators, there are various methods to achieve good performance over noise, transient, and area parameters. However, there is a trade-off between these performance parameters makes it a complex task to design. In this study, as it will be a part of capsular endoscopy, to fit inside the limited area, a capacitor-less regulator is designed. Furthermore, fast transient response is targeted because endoscopy blocks such as ADC require higher current supplied into the circuit during specific working periods. Also, reference voltage coming from the bandgap circuit is designed to be more accurate over PVT variations, to have less error at the output of LDO.

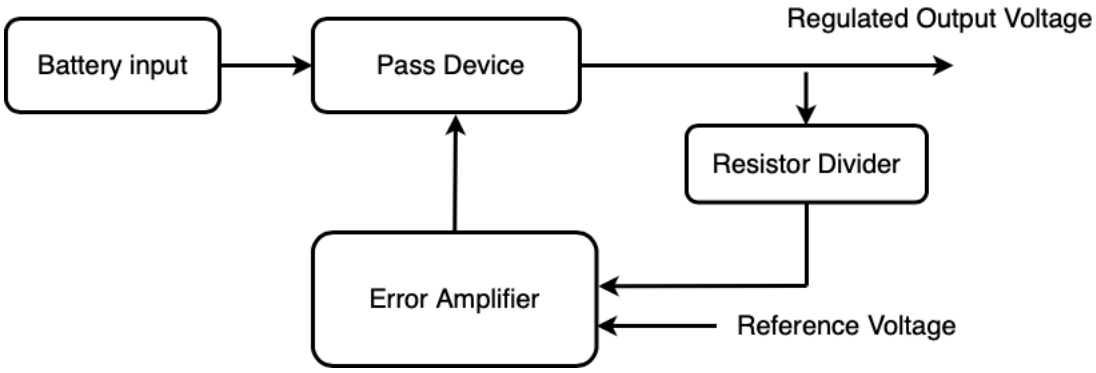

Figure 3.1 : Block Diagram of a Linear Regulator.

3.1 LDO Design Specifications

LDO consists of three main elements: error amplifier, feedback network, and pass device. The output voltage is generated by the negative feedback loop created by the resistor divider. As shown in Fig. 3.2, the error amplifier takes two inputs which are reference voltage coming from the bandgap reference and resistor divider scaling the output voltage. The output voltage is obtained at the desired value once the resistor division ratio is chosen. In this feedback loop, the error amplifier compares these two inputs and drives the pass device creating a clean and stable voltage at the output. The feedback loop can be written as follows

$$V_{out} = V_{ref} \frac{Ao}{1 + KAo} \tag{3.1}$$

where K is the feedback factor and V_{out} can be approximated to Eq. 3.2 if the loop gain (A_o) is sufficient.

$$V_{out} \approx V_{ref} \frac{1}{K} \tag{3.2}$$

As the feedback factor is the resistor division of R_1/(R_1+R_2), V_{out} voltage can be formulated as given in Eq. 3.3. From this equation it can be seen that any inaccuracy in V_{ref} will affect the output voltage directly.

$$V_{out} = V_{ref}\left[1 + \frac{R_2}{R_1}\right] \tag{3.3}$$

There are few parameters that define the performance and design specifications of LDO regulator. Most important specifications are described in more detailed as follows.

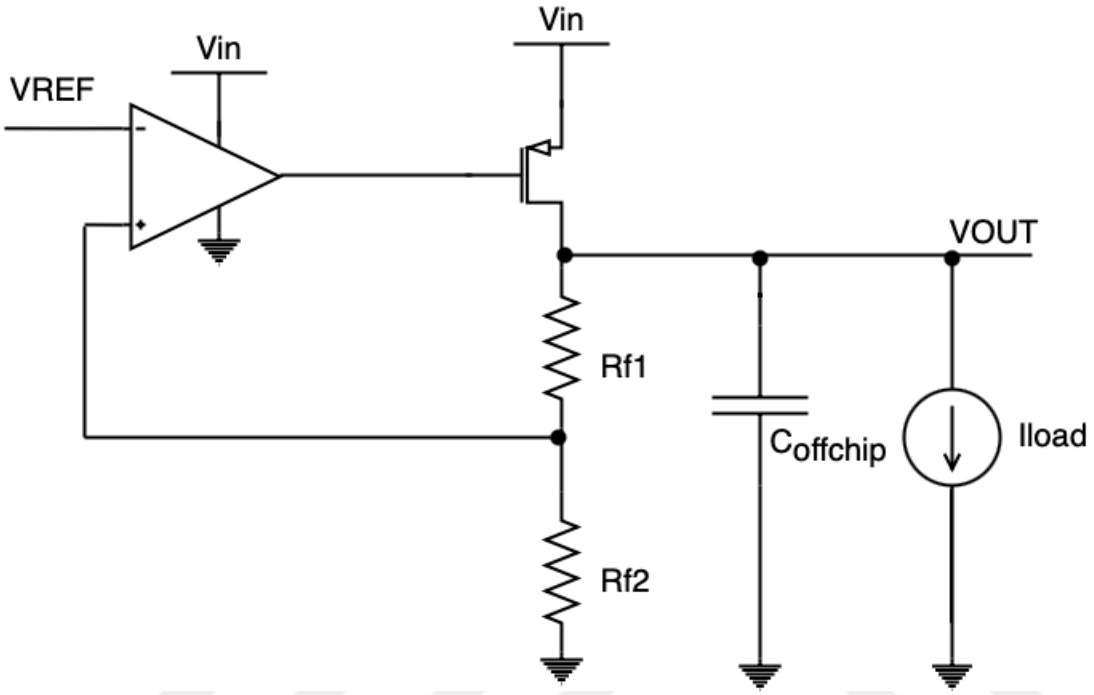

Figure 3.2 : Block Diagram of Conventional LDO.

3.1.1 Pass device and dropout voltage

Dropout voltage is defined as the difference of input and output voltage and it is one of the critical parameter as it defines the efficiency. LDO Regulators are step-down converters thus efficiency will be high when the output voltage is closest to the input voltage, this is why LDO should have a low dropout voltage.

Pass device parameters defines the dropout voltage. Pass device sizing is decided upon the maximum load current and minimum desired dropout voltage. When the pass device is in low dropout region, PMOS behaves like a resistor and it operates in triode region. This resistor value, R_{on} is derived in below Eqs. (3.4)-(3.6) [6].

$$I_D = \mu_n C_{ox} \cdot \left(\frac{W}{L}\right) \cdot \left[\left(V_{GS} - V_{TH}\right) V_{DS} - \frac{1}{2} V_{DS}^2\right] \tag{3.4}$$

when $V_{DS} \ll 2\,(V_{GS} - V_{TH})$

$$I_D \approx \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{TH})\, V_{DS} \tag{3.5}$$

$$R_{on} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{TH})} \tag{3.6}$$

Finally, dropout voltage can be formulated as below from the derived equations where I_L is the load current.

$$V_{do} = I_L \times R_{on} = \frac{I_L}{\mu_n C_{ox} (\frac{W}{L})(V_{GS} - V_{TH})} \tag{3.7}$$

3.1.2 Line regulation

Line regulation can be defined as the output voltage changes caused by the input voltage variation and it is formulated in Eq. 3.8. As defined earlier input voltage is a non-ideal source and this parameter defines the circuits ability to maintain output voltage.

$$R_{line} = \frac{\Delta V_{out}}{\Delta V_{in}} \tag{3.8}$$

As shown in Fig. 3.3, the circuit starts with a stable output over the changing input voltage however, after a certain threshold it is not able to operate as a regulator and output voltage decays linearly with input, this type of behavior is observed generally in systems operating with battery.

3.1.3 Load regulation

Load regulation can be defined as the ability to maintain stable output voltage over a changing load current. This parameter can be derived as in Eq. 3.9, and as it can be understood from the equation load regulation strongly depends on the open loop gain (A_o). This specification improves with high error amplifier gain and low load current. This parameter can be treated as a resistance at the output as it can be recognized from the equation.

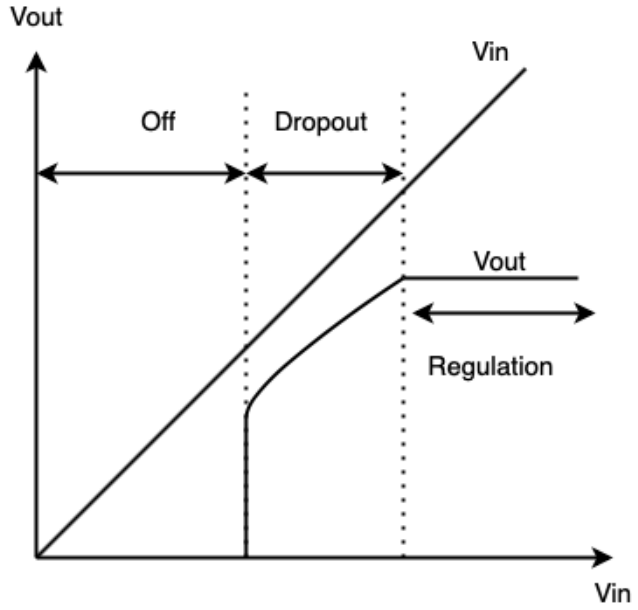

Figure 3.3 : Line Regulation Response.

$$R_{load} = \frac{\Delta V_{out}}{\Delta I_{load}} = \frac{R_{on}}{1 + A_o K} \tag{3.9}$$

3.1.4 Transient response

As mentioned in earlier sections, there could be abrupt changes in the load current. Output voltage must remain stable even when there is a large change in the load current. Transient response is defined by the value of the output capacitance, slew rate of the regulator, and the ESR resistance if exists. Voltage variation when there is a transient load current can be described as in Eq. 3.10, where C_{out} is the total output capacitance, t_1 is the loop bandwidth and V_{ESR} is the voltage on the ESR resistance.

$$\Delta V_{out} = \frac{I_{load}}{C_{out}} \Delta t_1 + \Delta V_{ESR} \tag{3.10}$$

Capacitor-less LDOs does not contain any ESR resistance, however this does not make an improvement as the capacitor at the output plays a significant role on the compensation of abrupt transient disturbances. This parameter depends on the bandwidth and slew rate, hence increasing those could improve the response. Nonetheless, increasing bandwidth means more power consumption as a trade-off.

3.1.5 Temperature dependence

Reference voltage of the LDO comes from the bandgap reference circuit. Subsequently, temperature variance at the output depends highly on the performance of the bandgap reference circuit, inaccuracies at the output of reference voltage will be scaled with resistor division ratio and may cause a large error at the output voltage.

3.1.6 Quiescent current

Quiescent current is the difference of input and output currents. It is the necessary current amount to supply to internal blocks such as error amplifier, bandgap reference, feedback network. Load current is not included in quiescent current and it is defined as the equation below.

$$I_q = I_{input} - I_{output} \tag{3.11}$$

3.1.7 Efficiency

Efficiency of the LDO regulator depends on the load current, input and output voltage and quiescent current. As mentioned before, dropout voltage has a high impact on the efficiency, since efficiency improves when the input and output voltage difference is minimum.

$$\eta = \frac{V_{out} I_{load}}{(I_q + I_{load}) V_{in}} \tag{3.12}$$

From the Eq. 3.12, it can be observed that efficiency is affected by the quiescent current. In most designs quiescent current is much smaller than the load current however, it can become prominent in small load currents.

3.1.8 Power supply rejection ratio (PSRR)

Input voltage usually contains ripple and AC noise elements. PSRR is the parameter that defines how well the circuit suppresses input voltage. It is essential to have good

noise rejection in order to obtain clear output voltage. PSRR can be formulated with disturbances on the input and output voltage as given in Eq. 3.13.

$$\mathrm{PSRR} = 20\log\left(\frac{V_{in}}{V_{out}}\right) \tag{3.13}$$

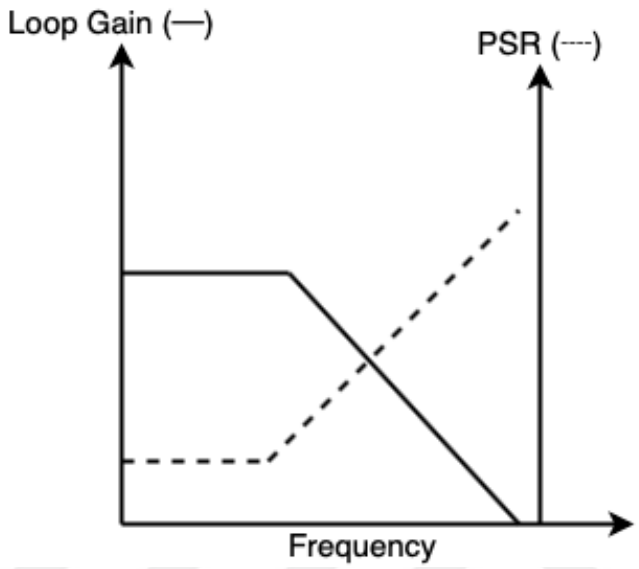

Figure 3.4 : Power Supply Rejection Ratio Response.

Supply noise may contain more noise on specific frequencies if there is a switching inside the block which could cause a voltage ripple. Whereas, PSRR performance varies with frequency. Elements inside the LDO such as error amplifier, bandgap reference and pass device affect PSRR performance and how well the output is regulated. Especially gain and frequency response of the error amplifier has a large impact on the PSRR.

Relation between the loop gain and PSRR is demonstrated in Fig. 3.4. PSRR and loop gain has a similar trend, PSRR is high before the 3-dB roll-off point of the loop gain then starts to decrease with 20 dB/decade. From depicted figure and equation, it can be understood that increasing the gain-bandwidth of LDO improves the PSRR performance [28].

3.2 LDO Regulator Design

Conventional LDO design as shown in Fig. 3.2, consists of error amplifier, pass device, bandgap reference and a large output capacitance. Large output capacitance is included into the LDO loop in order to achieve certain stability conditions. Stability condition simply comes from the Barkhausen's criteria, loop should have always phase shift of less than 180 degrees when loop reaches unity gain. Choosing the size of the output capacitor depends on the frequency of poles in the loop. Since, the output capacitor is large, it is off-chip meaning it comes with an ESR.

First pole which is the dominant pole of the LDO comes from the large pass device resistance (R_{on}), output capacitor and its ESR value. Second pole comes from the output resistance of the error amplifier and the parasitic capacitance of the pass device.

$$f_{p1} = \frac{1}{2\pi(R_{on} + R_{ESR})C_{load}} \tag{3.14}$$

$$f_{p2} = \frac{1}{2\pi R_{out,amp} C_{par}} \tag{3.15}$$

To obtain sufficient phase margin, by using an off-chip capacitor, left half plane zero is introduced to the loop in conventional LDOs.

$$f_{z1} = \frac{1}{2\pi R_{ESR} C_{load}} \tag{3.16}$$

Dominant pole given in Eq. 3.14, highly depends on the load current as the resistor value of pass device changes. Output capacitor and ESR value is chosen in order to cancel the second pole. Conventional LDOs have the advantage of having a good transient response since output capacitor helps with fast current path flowing through the load. However, the output capacitor consumes a large space, and this is why capacitor-less design is chosen in this study.

Capacitor-less LDO structure shown in Fig. 3.5, does not contain any ESR resistor at the output thus there is not any LHP zero and the system contains two poles mention in Eq. 3.14 and 3.15. Stability of the capacitor-less LDO degrades greatly at lower load conditions as the dominant poles is at low-frequency. For this reason, to maintain stability at low load conditions additional slewing detection structure is added into the loop.

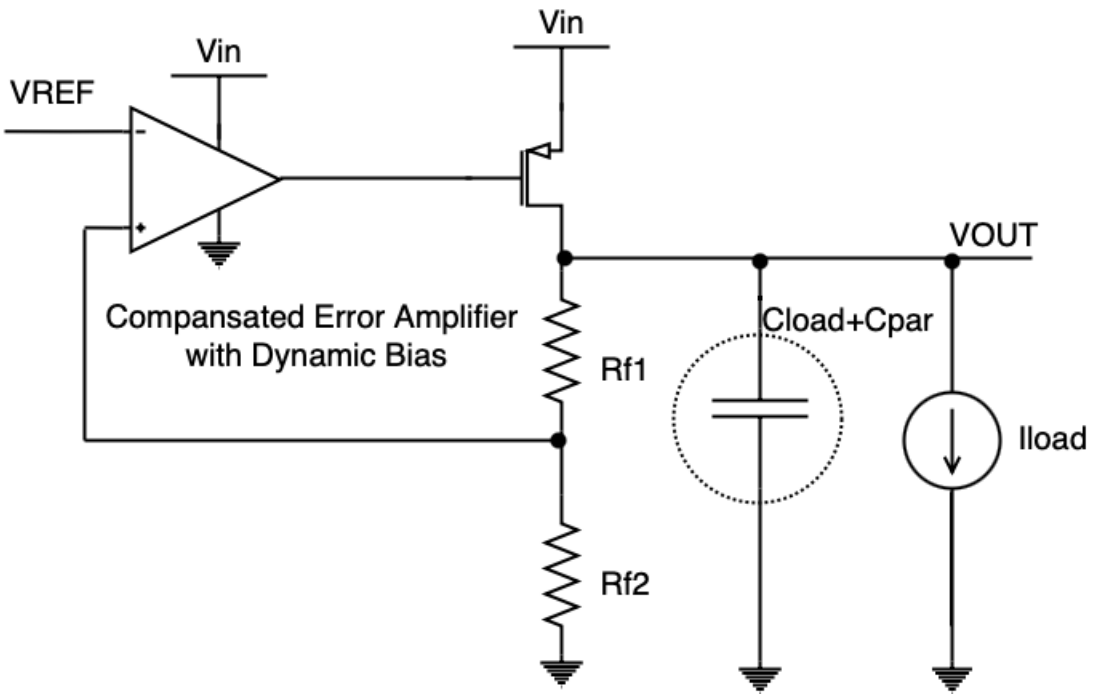

Figure 3.5 : Capacitor-less LDO topology.

3.2.1 Pass transistor design

As described in the earlier sections, the pass device defines the dropout voltage of the LDO regulator. The first pole of the LDO regulator is defined by the resistance of the pass device thus it plays a great role in the compensation of the regulator. Furthermore, the parasitic capacitance of the pass device determines the transient response.

For pass devices, most designs use NMOS or PMOS transistors depending on the LDO regulator's specifications. Since NMOS transistors have higher mobility than PMOS, they are sized smaller. However, using an NMOS requires an additional bias circuit which is usually a charge pump because the gate voltage of NMOS should be higher

than the output voltage. In this design, the PMOS pass device is chosen since error amplifier output can easily drive the gate of PMOS and it does not require a charge pump circuit which introduces complexity to the design.

The sizing of the pass device is straightforward once the dropout voltage and maximum load current are decided. From the MOSFET current equation, there is square relation between the W/L ratio of the device and drain-source voltage which is given in Eq. 3.17 and W/L is derived as Eq. 3.18.

$$V_{do} = \sqrt{\frac{2I_{load,max}}{\mu c_{ox} W/L}} \tag{3.17}$$

$$\frac{W}{L} = \frac{2I_{load,max}}{\mu c_{ox} V_{do}^2} \tag{3.18}$$

In this design, the dropout voltage is targeted to be 200 mV. The maximum load current specification comes from the required current for capsular endoscopy blocks, and the analysis shows that 80 mA is necessary. The width and length values of the pass device are chosen as in Table 3.1.

Table 3.1 : Width and length values for pass device.

	Total Width(μm)	Finger Width(μm)	Multiplier	Length(nm)
M_{pass}	800	10	8	360

Pass transistor size is quite large to have the high current capability and low resistance hence low dropout voltage. Length is chosen minimum to not increase width further. Transistor width is divided into many fingers because there is a large current flowing through from the pass device to the load, and there should not be a huge current flowing from the metal connection of the source/drain. Furthermore, electromigration (EM) rules of the process are reviewed during layout.

3.2.2 Error amplifier

LDO parameters are mostly defined by the performance of the error amplifier. It dominates LDO loop gain, PSRR, and line regulation. For this purpose, an operational transconductance (OTA) with a high gain and good frequency response is designed.

To design a circuit with a high gain single stage amplifier is not suitable even though stability analysis of it is quite straightforward. Miller OTAs are commonly used in most designs as an error amplifier, as they provide good gain-bandwidth. Nevertheless, they require a large compensation capacitor to create an LHP zero for stabilization. Most of the current spent for bandwidth, is used for driving the compensation capacitor. To mitigate the compensation capacitor, the current mirror OTA is designed. Diode-connected transistors in the design create a low impedance node and further frequency compensation is not needed.

Error amplifier consists of two parts, first part is the input stage, it takes a differential input and noise is suppressed because of the symmetry. For input transistors split length devices are used and the input transistors are matched in the layout. Using split length devices create a low impedance node, improving the stability. It also increases the offset performance as the output resistances will be larger creating a better matching between inputs. The second part of the amplifier is the output stage which is a push-pull amplifier. By using current mirrors, the input current is scaled to the output. For better current mirroring lengths are chosen larger and the transistors are matched in the layout.

Voltage gain in this topology can be derived as in Eq. 3.20. In this topology, mirroring ratio (B) is chosen as 2.

$$A_{EA} = g_{m,mn1} B (r_{o,mp3} || r_{o,mn7}) \tag{3.19}$$

Bandwidth of this circuit is equal to

$$f_{BW} = \frac{g_{m,mn1}}{2\pi C_L}. \tag{3.20}$$

There is a non-dominant pole coming from the node A, in order to achieve a sufficient margin, non-dominant pole should occur at 3 times the gain-bandwidth (GBW) frequency. To meet this criteria, MN6 and MN7 transistors are sized accordingly.

3.2.3 Feedback network

Feedback network consists of resistor dividers at the output to scale the voltage. Resistors are chosen quite large to reduce power consumption. Conventional LDOs involves a large capacitor at the output and a ESR equivalent of the capacitor. In this study, to optimize the area off-chip capacitor is removed. Removal of the off-chip capacitor results in a performance degradation in transient response. Capsular endoscopy contains an ADC, a switching circuit, hence it is essential for LDO to give fast response and keep the output voltage stable. Slewing detection and dynamic biasing is added at the output to improve the transient behaviour.

During operation of LDO, output load current may have abrupt changes and the feedback loop should still be able to provide a stable voltage. If there is an abrupt change at the load current, output voltage is affected by this change. Consequently input voltage of the error amplifier changes and creates an unbalance at the input. Error amplifier current mirror bias nodes notated as V_A and V_B changes with input voltage variation. To improve the transient behavior, firstly transient behaviour on the nodes must be tracked. For this purpose, slewing detection is introduced to the circuit as shown in Fig. 3.7. Voltages at the V_A and V_B are connected to this detection circuit and these voltages are defined by the amplifier. According to bias voltages, V_{hi} is closer to V_{dd} and V_{lo} is closer to ground in the steady condition. Positive slew is observed when there is a rise at the output voltage. In order to flow more current, node V_A decreases to build large source-gate voltage. Hence, V_{hi} voltage becomes closer to supply voltage and V_{lo} is also pulled up enabling a supply to ground swing at the output. When negative slewing is detected similar behaviour is observed, V_{hi} and V_{lo} voltages are pulled down in this case and transient response is improved.

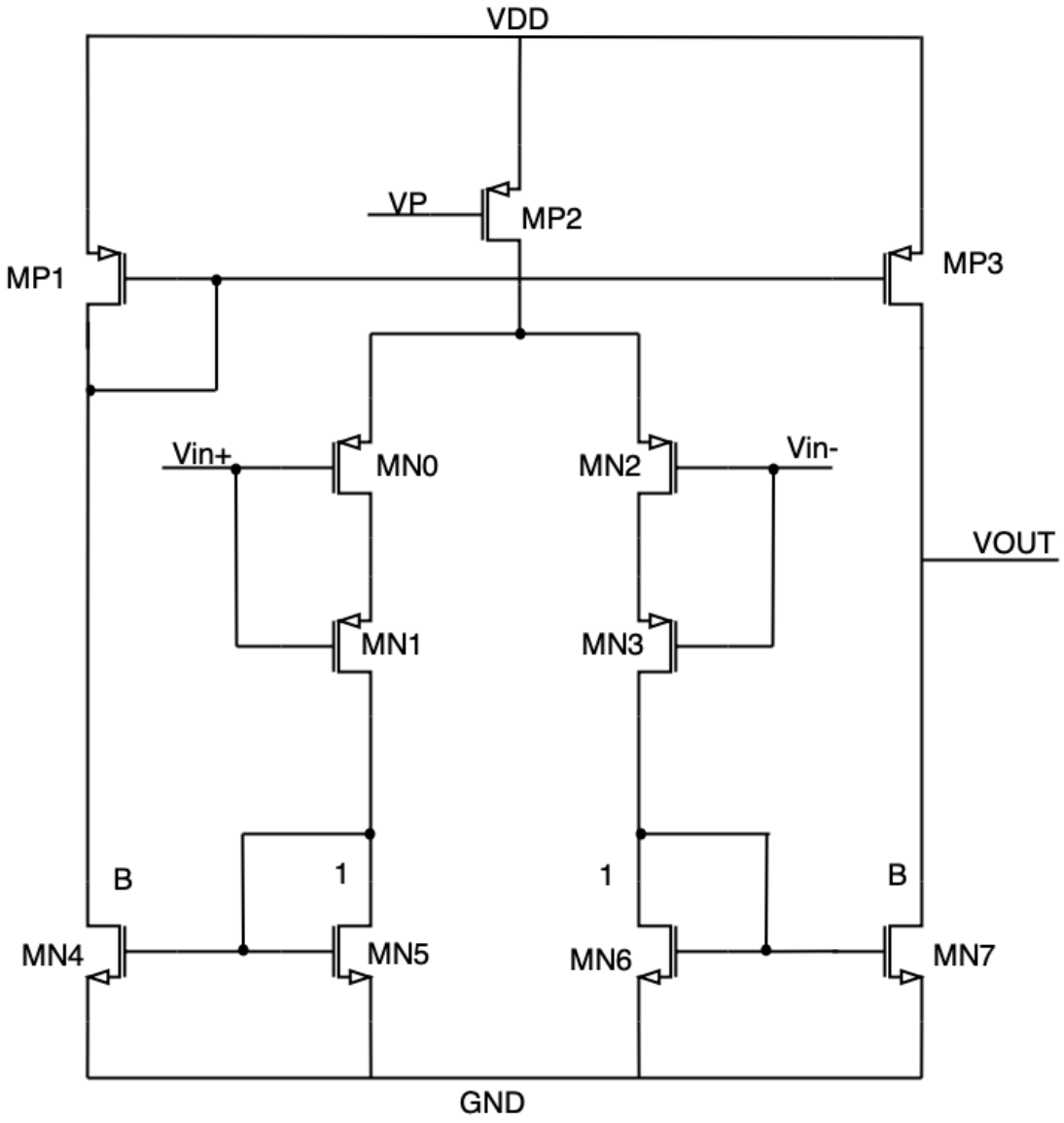

Figure 3.6 : Error Amplifier Design for LDO.

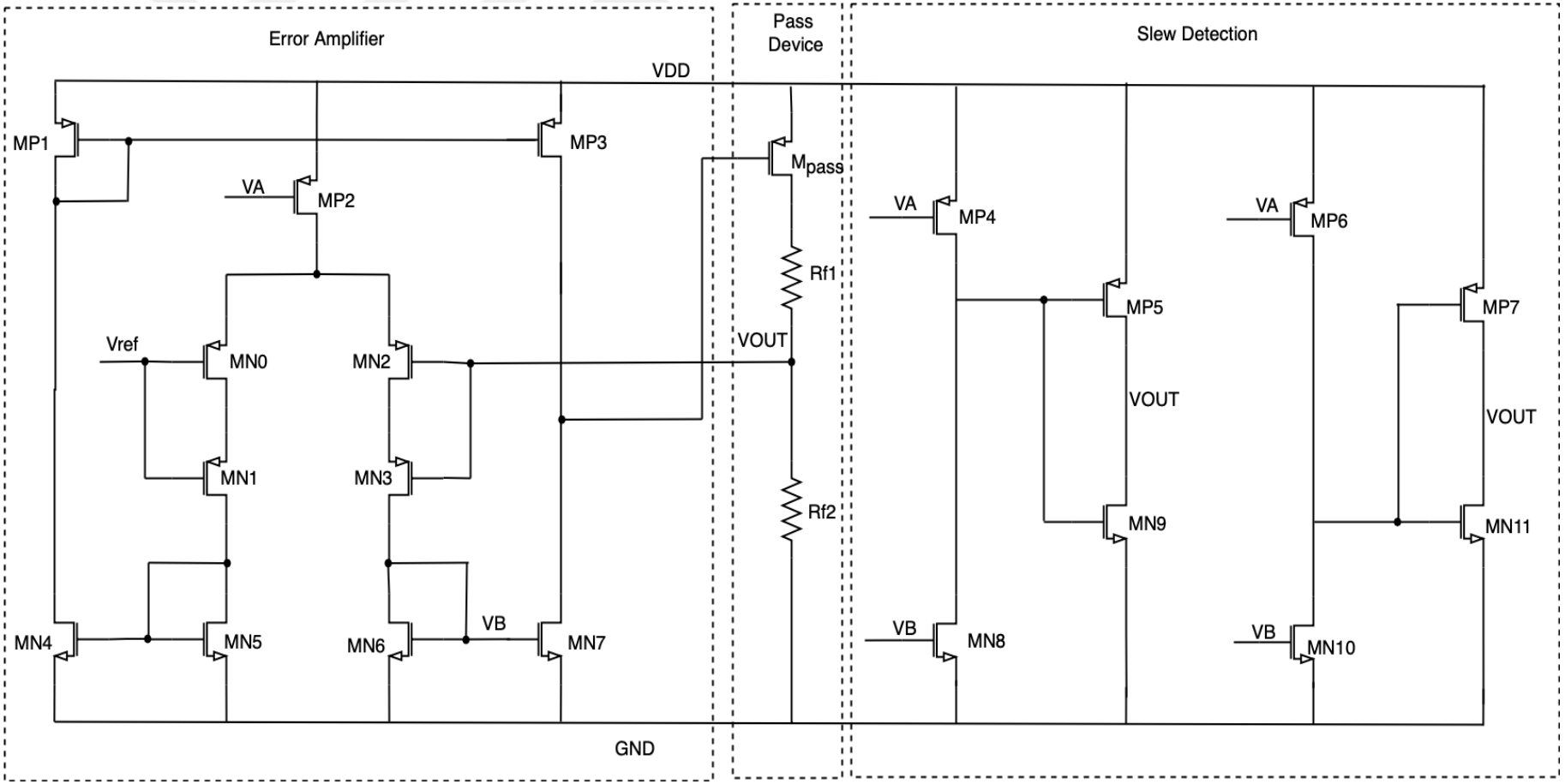

Figure 3.7 : Implemented design of LDO.

3.3 Results

In this section, LDO simulation results are provided for schematic and post-layout extracted simulations(RCX). Corner simulations are included in the results. For corners, the temperature is swept between -40 °C and 125 °C. MOS corners are fast-fast (ff), fast-slow (fs), slow-fast (sf), slow-slow (ss) and BJT corners slow-slow (ss) and fast-fast (ff) are simulated. For input voltage corners, 3.3 V and 2 V are used as a minimum and maximum points.

3.3.1 Load sweep results

For load regulation, the load resistance is swept between 1000 Ω and 10 Ω. Sweeping the load resistance means that load current is changed, since the output voltage is at 1.8 V, load current changes between 1.8 mA and 180 mA. Output voltage stays stable until 20 Ω and then it drastically reduces. This means that LDO can provide stable voltage at the output of up to 90 mA static current. It can be seen from the post-layout simulations that the variation from target output voltage is similar to schematic results and it is $\pm 5\%$ in the worst case.

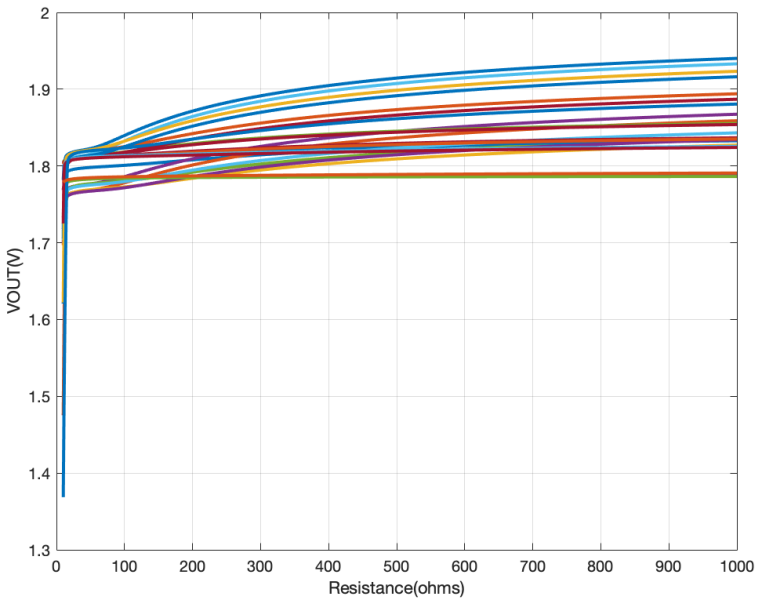

Figure 3.8 : Load Sweep Schematic Results.

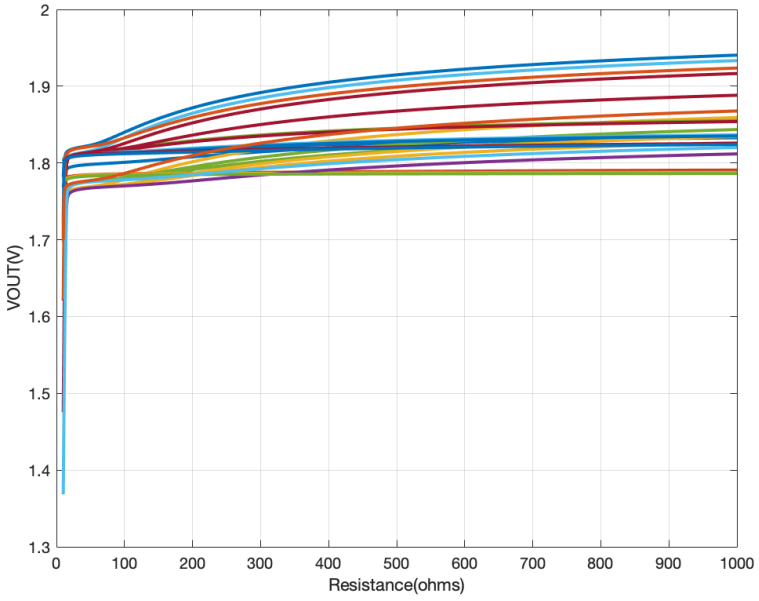

Figure 3.9 : Load Sweep RCX Results.

3.3.2 Line sweep results

For line regulation, input is swept from 3.3 V to 1.8 V. As shown in below figures, circuit can provide 1.8 V when the input voltage decreases to 2 V and it is the used minimum target voltage for pass device sizing. As it can be observed from the corner results, at lower loads regulator maintains stable output voltage when input is as low as 1.9 V leaving a 100 mV dropout voltage to the pass device. The reason as the load current decreases, resistor of the pass device also decreases, hence the dropout voltage is lower. Post-layout simulations shows that, the behaviour is highly similar with schematic results.

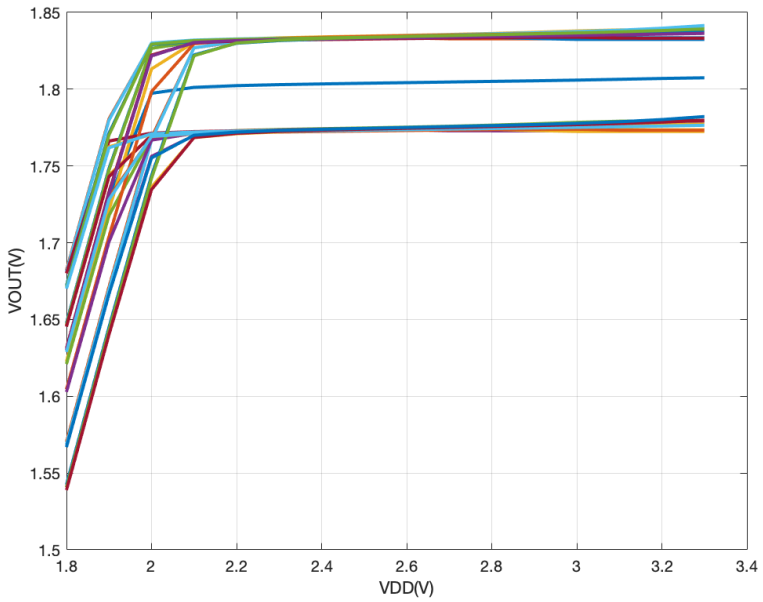

Figure 3.10 : Line sweep schematic results at 80 mA load.

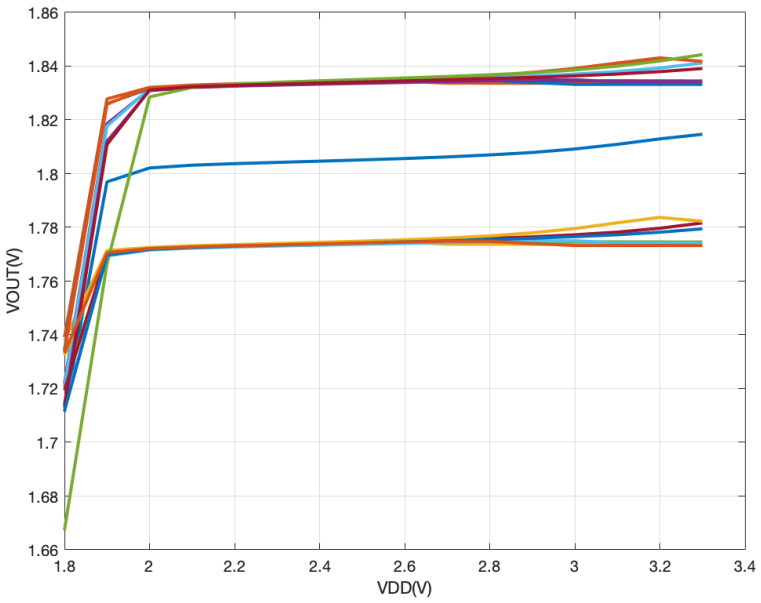

Figure 3.11 : Line sweep schematic results at 1 mA load.

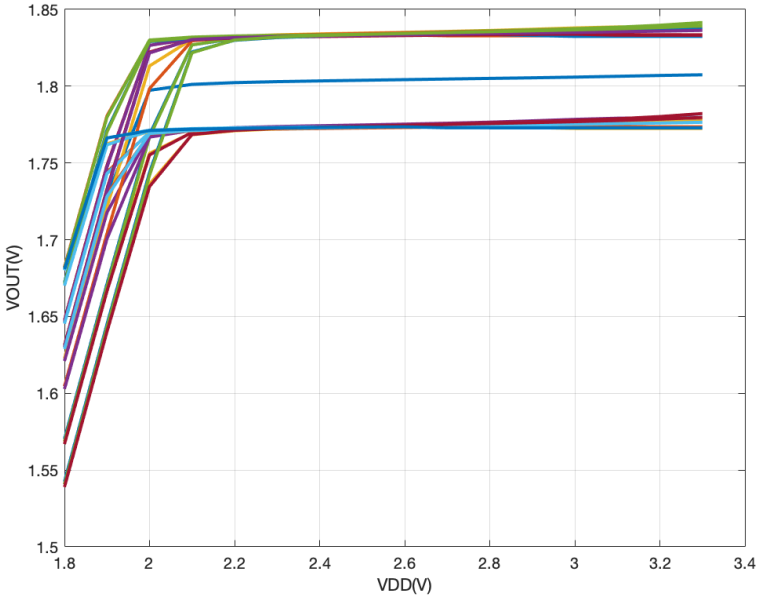

Figure 3.12 : Line sweep RCX results at 80 mA load.

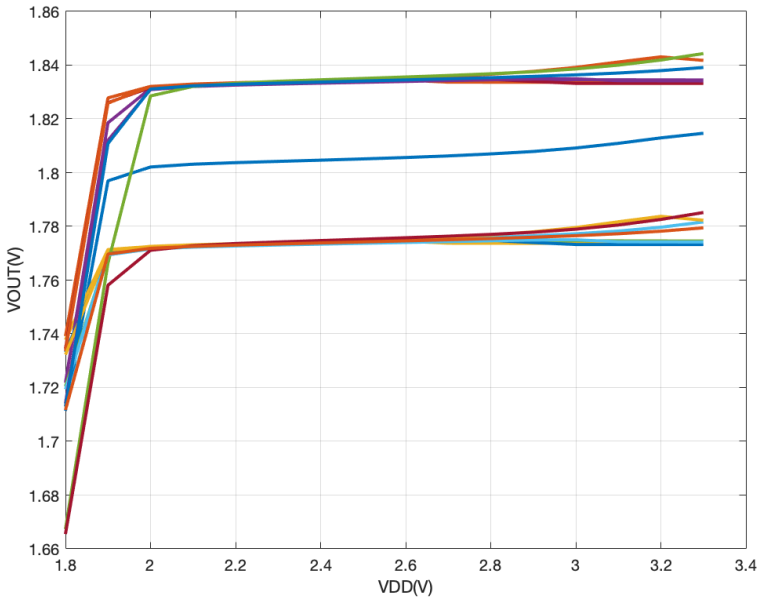

Figure 3.13 : Line sweep RCX results at 1 mA load.

3.3.3 Line transient results

Battery voltage inside the capsular endoscopy is connected to the driver blocks. When there is a switching in a driver block or any variance on the supply voltage over a certain period, regulator output should be able to provide a stable voltage. For line transient, input voltage is given as a transient pulse from 2 V to 3.3 V and for rise and fall times 5 μs is used. Results show that at the output circuit is capable of regulating after overshoot and undershooting. Overshoot is around 19.5 mV and undershoot is 23 mV in schematic results and around 20.5 mV and undershoot is 23.7 mV in post-layout simulation results.

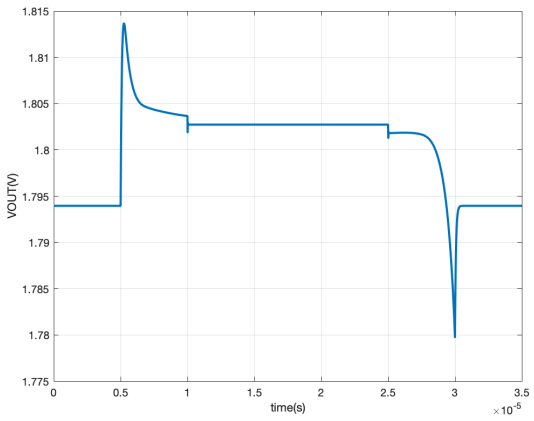

Figure 3.14 : Line Transient Schematic Results.

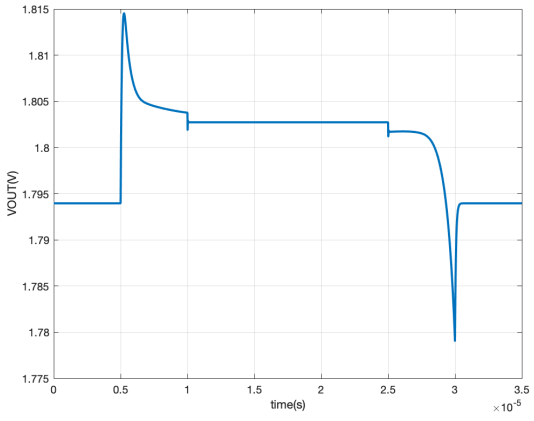

Figure 3.15 : Line Transient RCX Results.

3.3.4 Load transient results

Output of the regulator is connected to the blocks of capsular endoscopy and according to the design requirements, load current changes during specific period. The reason is that analog to digital converter and laser driver circuits demands higher values of current. In order to replicate this behaviour, load current is changed from 40 mA to 80 mA and as rise and fall time 5 μs is chosen. Similar to line transient behaviour overshoot and undershoot is observed at the output voltage.

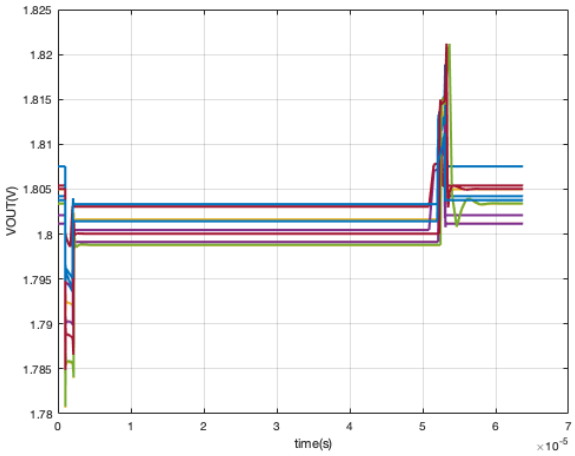

Figure 3.16 : Load Transient Schematic Results.

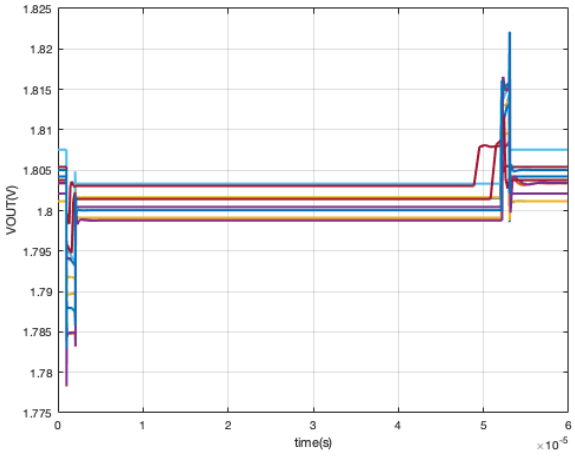

Figure 3.17 : Load Transient RCX Results.

3.3.5 Stability results

Gain characteristics of LDO is important as it effects most of the specifications. For stability measurements, loop is broken from the resistor feedback. It is crucial to make sure stability is ensured for all load conditions, hence for load minimum and maximum currents are defined as 1 mA and 80 mA. As shown in below figures, sufficient phase margin is checked for all corners and current min and max points.

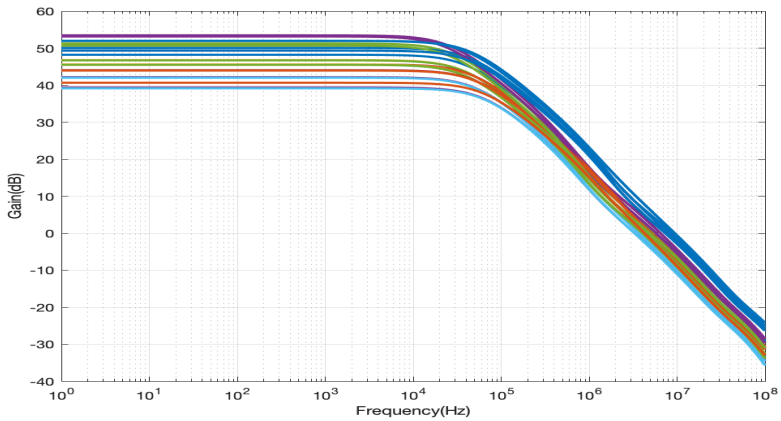

Figure 3.18 : Gain Schematic Results at 80 mA load.

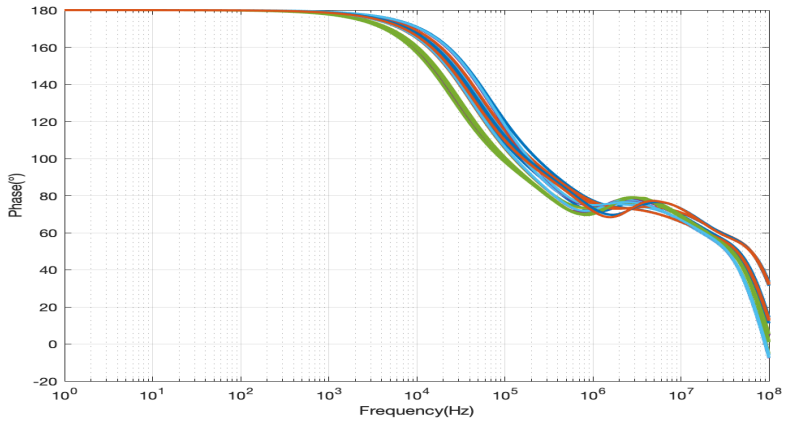

Figure 3.19 : Phase Schematic Results at 80 mA load.

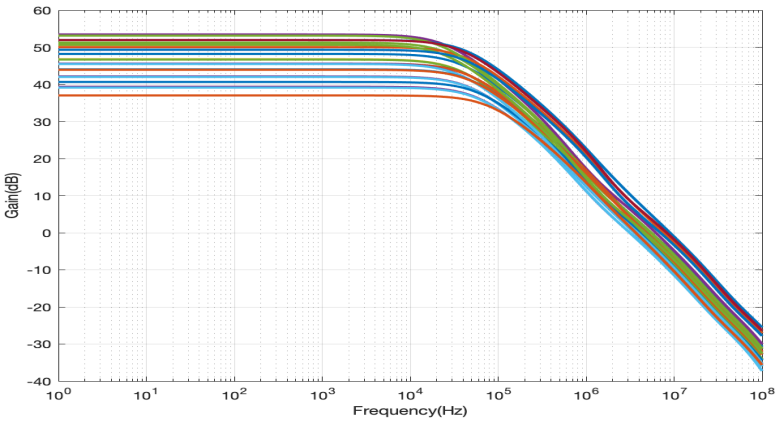

Figure 3.20 : Gain Schematic Results at 1mA load.

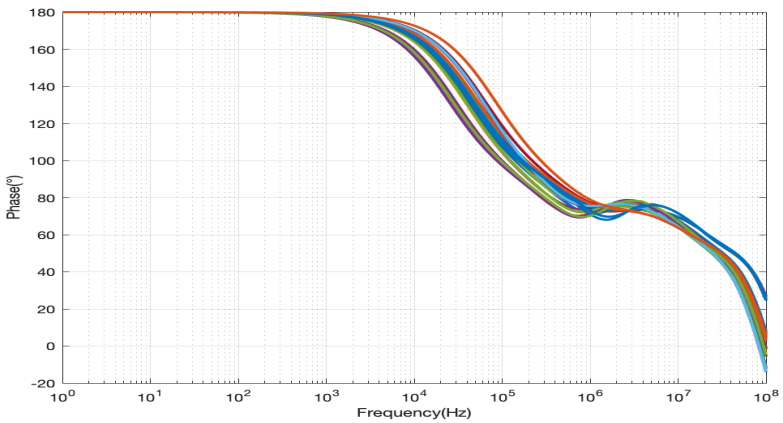

Figure 3.21 : Phase Schematic Results at 1mA load.

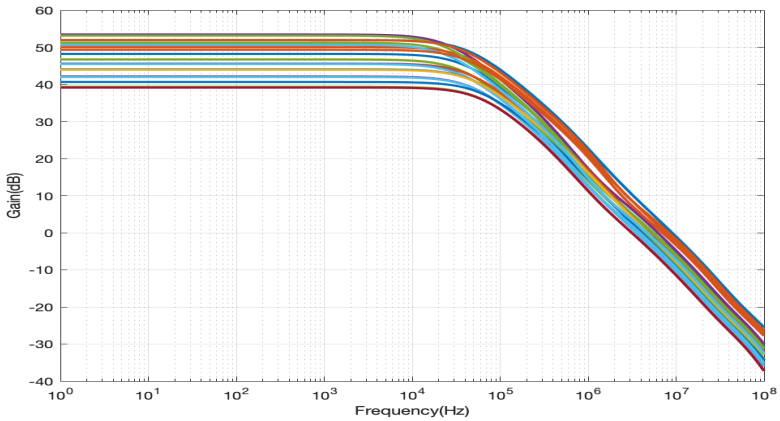

Figure 3.22 : Gain RCX Results at 80 mA load.

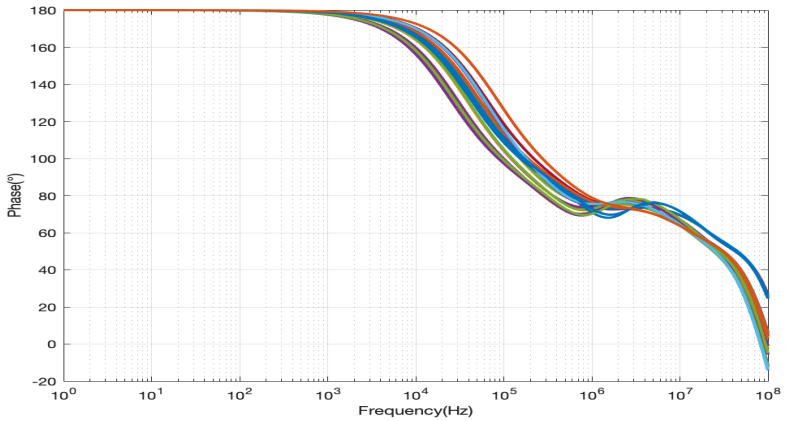

Figure 3.23 : Phase RCX Results at 80 mA load.

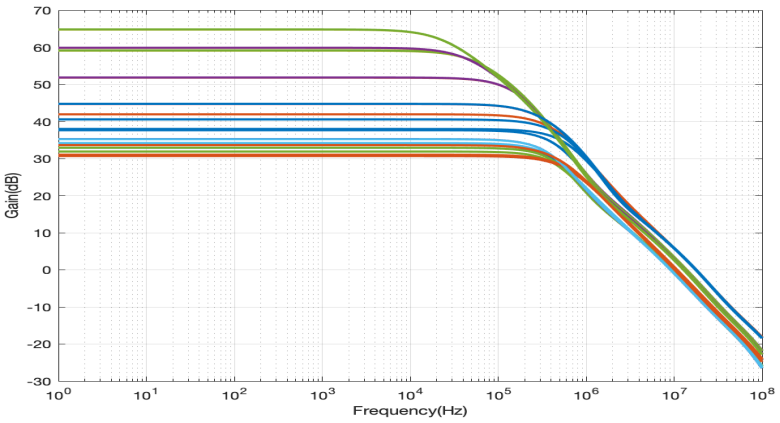

Figure 3.24 : Gain RCX Results at 1mA load.

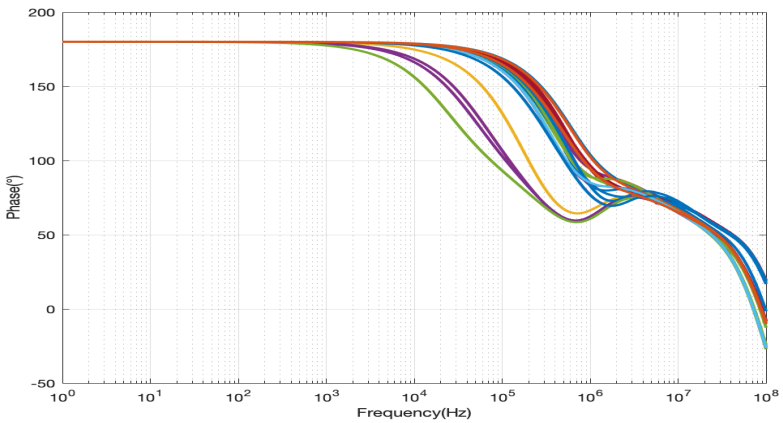

Figure 3.25 : Phase RCX Results at 1mA load.

3.3.6 Monte Carlo results

Monte Carlo simulations are run to observe the effects of mismatch and process variations. Output DC voltage variations are presented using 200 number of yield and at room temperature. As shown in Figs 3.26 and 3.27, mean of the output voltage is centered at 1.8 V. 3 sigma variation at the output voltage is $\pm 7\%$ and 4 sigma variation is $\pm 9.5\%$. Post-layout results are highly similar to schematic showing that transistors are well matched in the layout.

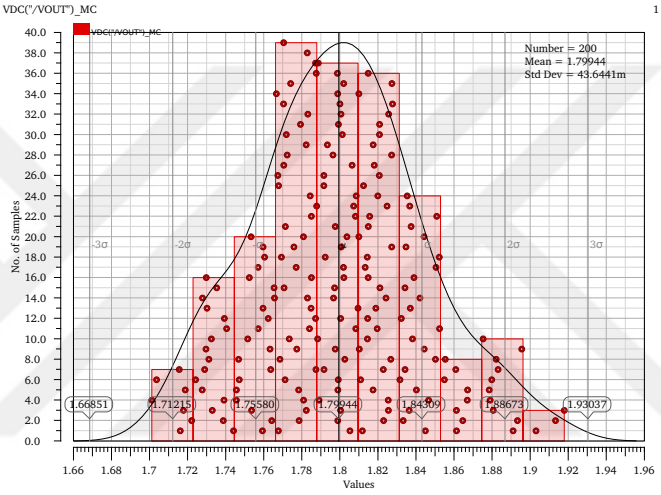

Figure 3.26 : LDO Monte Carlo Schematic Results.

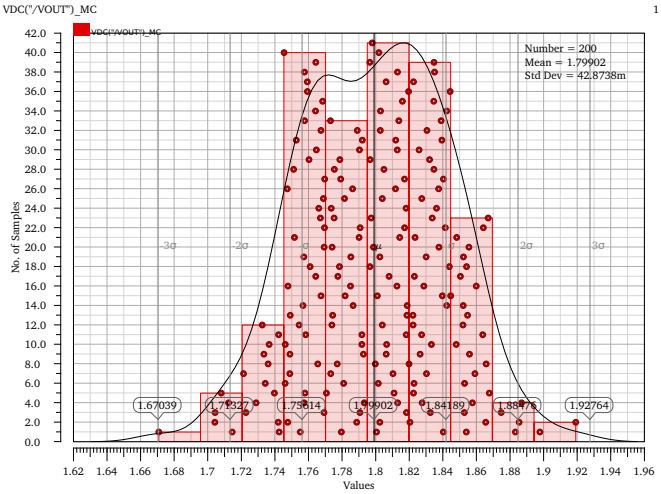

Figure 3.27 : LDO Monte Carlo RCX Results.

3.3.7 PSRR results

As mentioned before, V_{out} must be isolated from V_{in} sufficiently to ensure any ripple or noise at the input is not affecting the output. To plot this parameter, supply voltage is given as AC signal and at the output PSR is formulated as $20\log(\frac{V_{out}}{V_{in}})$. From the simulation results, it can be observed schematic and post-layout results are very similar, minimum point of PSR is same only frequency behaviour changes.

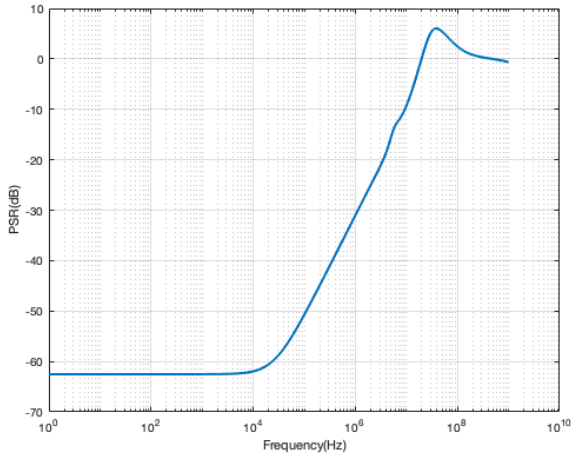

Figure 3.28 : LDO PSR Schematic Results.

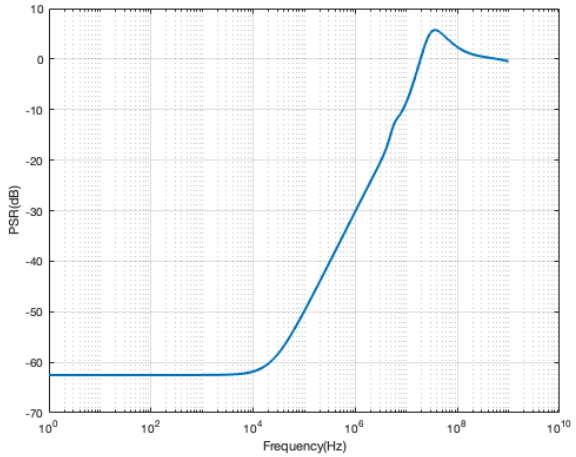

Figure 3.29 : LDO PSR RCX Results.

3.4 Specifications Table

Results achieved for various specifications are given in Table 3.2. Line and load sweep results are the same as the variation and dominated by the bandgap reference output variations. Stability is simulated over PVT corners, and in the table typical result is reported. Load and line transient variation results are obtained from the maximum overshoot and minimum undershoot points of the output voltage. Current consumption parameter is the quiescent current of low dropout regulator core and load current is not included. Feasibility studies on the capsule endoscopy system showed that maximum necessary current is 80 mA and LDO is designed to satisfy this specification. This is why all LDO simulations are tested with 80 mA load current.

Table 3.2 : Low Dropout Regulator Specifications Table.

Specification	Result
Dropout Voltage	200 mV
Maximum Load Current	80 mA
Load Sweep Variation	$\pm$ 6 %
Line Sweep Variation	$\pm$ 6 %
Load Transient Variation	$\pm$ 23 mV
Line Transient Variation	$\pm$ 21 mV
Current Consumption	45 μA
Power Consumption	90 - 148.5 μW
Gain	45 dB
Phase	67°
PSR@100 kHz	$-$52 dB

4. LAYOUT OF THE POWER MANAGEMENT SYSTEM

General layout rules are followed throughout the design. Current mirrors and input transistors are matched in the layout and dummy transistors are added next to them. Dummy transistors are necessary to ensure matching device parameters are homogeneous and symmetric when the circuit is etched in silicon. The operation of the MOS transistors is affected by where its bulk potential voltage is. To ensure the charge profile of bulk connections, they must be connected to supply voltage which is an n-well, and ground which is a p-well. This is achieved by including guard rings in the layout. Guard rings also mitigate latchup and protect the transistors from high leakage currents. Bandgap reference consists of a large resistance unit string and in the layout, they are placed carefully, so that over process corners all unit resistors will be exposed to the same amount of parameter change and resistor division is preserved. Bandgap reference consists of nine BJT transistors and they are placed symmetrically. As shown in Fig. 4.1, the metal connection of load is large, because at load current can be as high as 80 mA, and the parasitic resistance of the metal must be small. To satisfy the EM rules of the process, metal 3 layer with 15 μm width is used. Pass device transistor is divided into many fingers to increase the current capability for higher loads. The layout occupies 210 μm x185 μm area without including the pad connections. Layout with pad connections is shown in Fig. 4.2, and the layout size is 725 μm x650 μm. Most of the area is occupied by pads, metal connection to pads are wide to decrease parasitics and increase current capability of the connections.

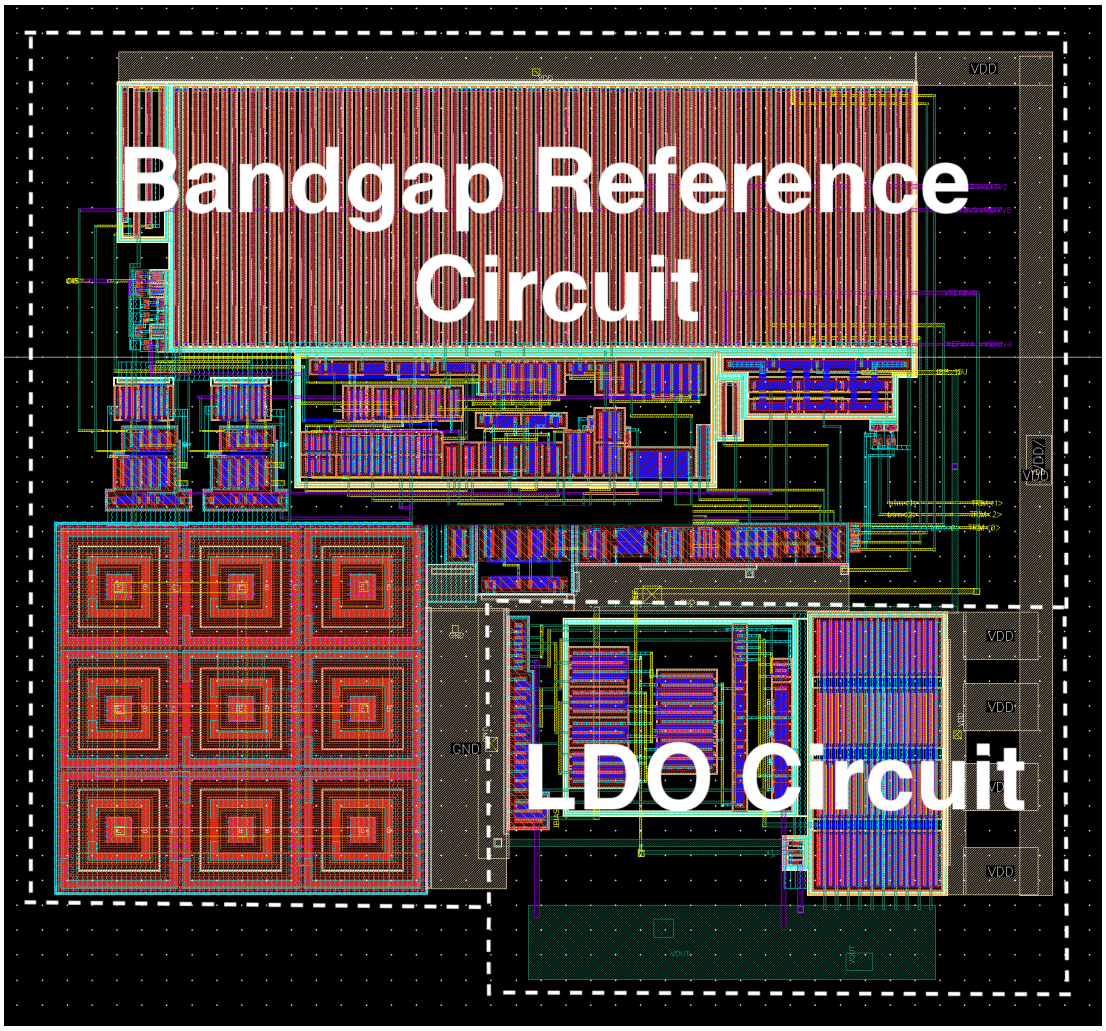

Figure 4.1 : Layout view of the system.

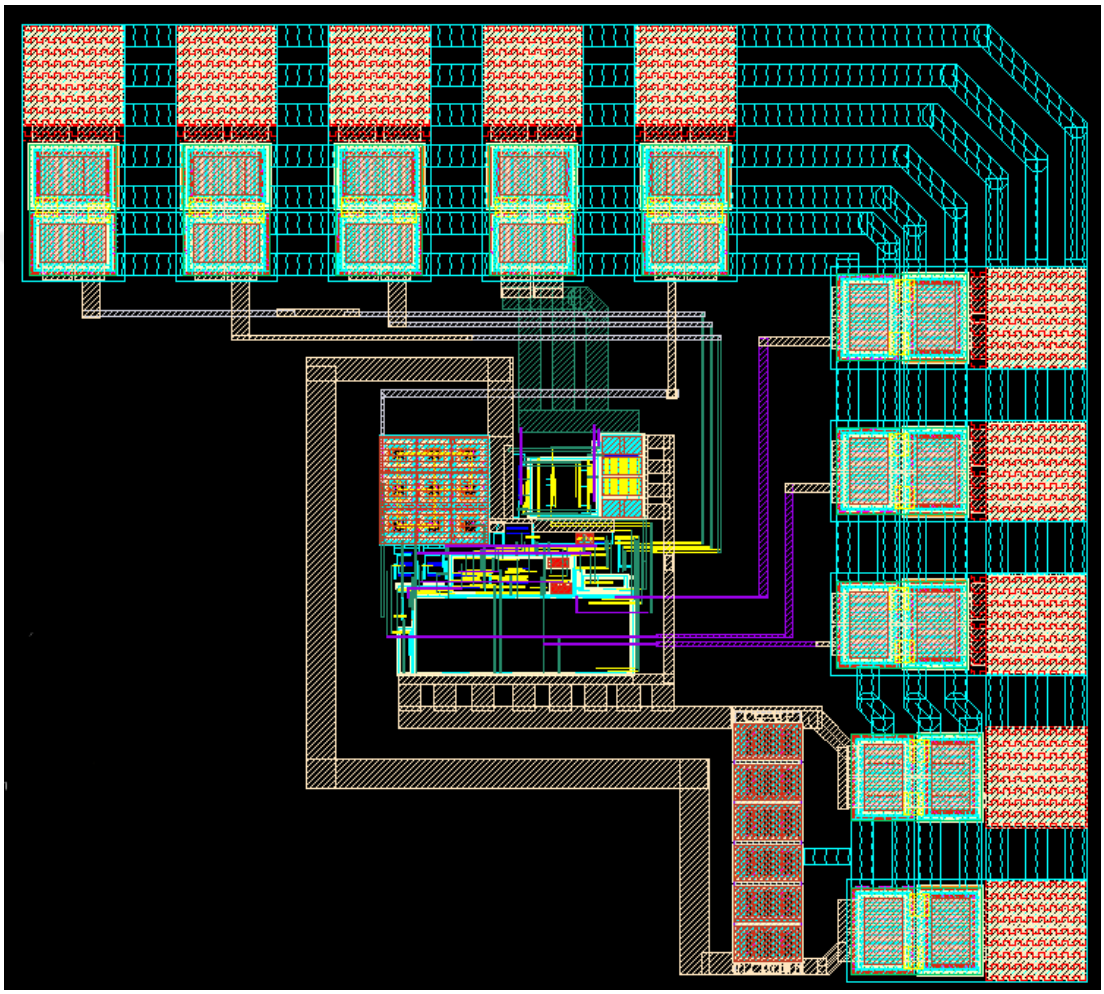

Figure 4.2 : Layout view of the system with pad connections.

5. CONCLUSION

In this study, a power management unit design for biomedical applications especially for capsular endoscopy is introduced. Hence, major design concerns include layout area, PVT variations, and current consumption. The system is designed using UMC 180nm technology. The proposed bandgap reference generator provides 0.4 V, 0.6 V, 0.8 V, and 1.2 V outputs with only 5 % voltage variation at the output. A novel design employing both MOS and BJT temperature characteristics is proposed. A system is built to use their advantages of them and includes a comparator, logic blocks, and a trimming structure. Monte Carlo results give ± 10.2 mV 4 sigma variation at the output of 600 mV and temperature coefficient is calculated as $75\ \mathrm{ppm}/^{\circ}C$.

A cap-less LDO is designed to reduce the layout area of the chip. Since LDO takes bandgap reference as input the voltage variation at the output is 5 %. Specification on voltage variation is kept tight as it is essential to have a stable supply voltage for blocks such as ADC and phase generator. To improve the transient performance dynamic biasing is added to the circuit. LDO is designed to be stable over the load current of 1 mA and 80 mA. The layout is designed for both circuits. Post layout extraction results are highly similar to schematic results and they satisfy the specifications. Table 5.1 presents comparison of LDO specifications with three different designs. In this work, because of the capsule endoscopy requirements, LDO can operate with 80 mA load current which is higher than in other studies.

Table 5.1 : Comparison Table for LDOs.

	[29]	[30]	[31]	This Work
Process	CMOS 0.13	CMOS 0.18	CMOS 0.18	CMOS 0.18
V_{do}	0.2 V	0.2 V	0.2 V	0.2 V
V_{out}	1 V	1.6 V	1.6 V	1.8 V
I_{max}	50 mA	50 mA	50 mA	80 mA
I_q	37.3 μA	55 μA	18 μA	45 μA
PSR @100kHz	-38 dB	-50 dB	-55 dB	-52 dB

REFERENCES

[1] **Brokaw, A.** (1974). A simple three-terminal IC bandgap reference, *1974 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, volumeXVII, pp.188–189.

[2] **Widlar, R.** (1971). New developments in IC voltage regulators, *IEEE Journal of Solid-State Circuits*, *6*(1), 2–7.

[3] **Banba, H.**, **Shiga, H.**, **Umezawa, A.**, **Miyaba, T.**, **Tanzawa, T.**, **Atsumi, S. and Sakui, K.** (1999). A CMOS bandgap reference circuit with sub-1-V operation, *IEEE Journal of Solid-State Circuits*, *34*(5), 670–674.

[4] **Neuteboom, H.**, **Kup, B. and Janssens, M.** (1997). A DSP-based hearing instrument IC, *IEEE Journal of Solid-State Circuits*, *32*(11), 1790–1806.

[5] **Annema, A.J.** (1999). Low-power bandgap references featuring DTMOSTs, *IEEE Journal of Solid-State Circuits*, *34*(7), 949–955.

[6] **Kayihan, H.I.**, **Inam, B.B.**, **Dogan, B. and Yelten, M.B.** (2020). A wide-temperature range (77–400K) CMOS low-dropout voltage regulator system - Analog Integrated Circuits and Signal Processing, *Springer*.

[7] **Basyurt, P.B.**, **Bonizzoni, E.**, **Maloberti, F. and Aksin, D.Y.** (2017). A low-power low-noise CMOS voltage reference with improved PSR for wearable sensor systems, *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp.1–4.

[8] **Mannama, V.**, **Sabolotny, R. and Strik, V.** (2006). Ultra low noise low power LDO design, *2006 International Biennial Baltic Electronics Conference*, pp.1–4.

[9] **Sunil, B.**, **Kulkarni, N.B.**, **Pradeep, P.**, **Praveen, P.K.**, **Singh, B.K. and Chippalkatti, V.** (2020). Design of Low Noise and Low Power LDO for Sensor Application, *2020 International Conference on Smart Technologies in Computing, Electrical and Electronics (ICSTCEE)*, pp.284–287.

[10] **Ho, M. and Leung, K.N.** (2011). Dynamic Bias-Current Boosting Technique for Ultralow-Power Low-Dropout Regulator in Biomedical Applications, *IEEE Transactions on Circuits and Systems II: Express Briefs*, *58*(3), 174–178.

[11] **Ahmed, F.U.**, **Sandhie, Z.T. and Chowdhury, M.H.** (2020). An Implementation of External Capacitor-less Low-DropOut Voltage Regulator in 45nm Technology with Output Voltage Ranging from 0.4V-1.2V, *2020 IEEE 38th International Conference on Computer Design (ICCD)*, pp.453–456.

[12] **Ho, E.N.Y. and Mok, P.K.T.** (2010). A Capacitor-Less CMOS Active Feedback Low-Dropout Regulator With Slew-Rate Enhancement for Portable On-Chip Application, *IEEE Transactions on Circuits and Systems II: Express Briefs*, *57*(2), 80–84.

[13] **Berk, M.S.**, **İnam, B.B. and Yelten, M.B.** (2021). An ISM-Band Multi-Phase Injection-Locked Ring Oscillator, *2021 IEEE 12th Latin America Symposium on Circuits and System (LASCAS)*, pp.1–4.

[14] **Razavi, B.** (2001). *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, first edition.

[15] **Rezaee-Dehsorkh, H.**, **Ravanshad, N.**, **Lotfi, R. and Mafinezhad, K.** (2009). Modified Model for Settling Behavior of Operational Amplifiers in Nanoscale CMOS, *IEEE Transactions on Circuits and Systems II: Express Briefs*, *56*(5), 384–388.

[16] **Nath, S.**, **Laskar, N.**, **Chanda, S. and Baishnab, K.** (2017). A High Gain, Low Power Two Stage OpAmp using Self Cascoding technique for Low Frequency Application.

[17] **Magnelli, L.**, **Crupi, F.**, **Corsonello, P.**, **Pace, C. and Iannaccone, G.** (2011). A 2.6 nW, 0.45 V Temperature-Compensated Subthreshold CMOS Voltage Reference, *IEEE Journal of Solid-State Circuits*, *46*(2), 465–474.

[18] **Ramasamy, S.**, **Venkataramani, B. and Meenatchisundaram, P.** (2008). A low power programmable band gap reference circuit with subthreshold MOSFETs, *TENCON 2008 - 2008 IEEE Region 10 Conference*, pp.1–6.

[19] **Giustolisi, G.**, **Palumbo, G.**, **Criscione, M. and Cutri, F.** (2003). A low-voltage low-power voltage reference based on subthreshold MOSFETs, *IEEE Journal of Solid-State Circuits*, *38*(1), 151–154.

[20] **Prasad, G. and Shama, K.** (2020). A 167.18 ppm/°C temperature coefficient, area efficient voltage reference using only MOS transistors, *Serbian Journal of Electrical Engineering*, *17*, 31–40.

[21] **Rossi, C. and Aguirre, P.** (2005). Ultra-low Power CMOS Cells for Temperature Sensors, *2005 18th Symposium on Integrated Circuits and Systems Design*, pp.202–206.

[22] **Wong, K. and Evans, D.** (2006). A 150mA Low Noise, High PSRR Low-Dropout Linear Regulator in 0.13m Technology for RF SoC Applications, *2006 Proceedings of the 32nd European Solid-State Circuits Conference*, pp.532–535.

[23] **Bautista, M.G.**, **Jilluh, Q.I.**, **Heimlich, M.**, **Dutkiewicz, E. and Pasco, J.** (2015). Design of low power, high PSRR low drop-out voltage regulator, *2015 International Conference on Humanoid, Nanotechnology, Information Technology,Communication and Control, Environment and Management (HNICEM)*, pp.1–5.

[24] **Yang, Y.**, **Yuan, Y.**, **Wu, L. and Zhang, X.** (2018). A High PSRR Low Drop-out Linear Regulator without Output Capacitor, *2018 IEEE International Conference on Electron Devices and Solid State Circuits (EDSSC)*, pp.1–2.

[25] **Tong, X. and Wei, K.** (2017). A Fully Integrated Fast-Response LDO Voltage Regulator with Adaptive Transient Current Distribution, *2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp.651–654.

[26] **Amayreh, M.**, **Leicht, J. and Manoli, Y.** (2016). A 200ns settling time fully integrated low power LDO regulator with comparators as transient enhancement, *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp.494–497.

[27] **Alapati, S.**, **SrihariRao, P.**, **Krishna Prasad, K.S.R. and Dixit, S.** (2014). A Transient-Enhanced Capacitorless LDO Regulator with improved Error Amplifier, *2014 IEEE Computer Society Annual Symposium on VLSI*, pp.89–93.

[28] **Morita, G.** (2014). Analog Dialogue, *Understand Low-Dropout Regulator (LDO) Concepts to Achieve Optimal Designs*, *48*(12).

[29] **Ho, E.N.Y. and Mok, P.K.T.** (2012). Wide-Loading-Range Fully Integrated LDR With a Power-Supply Ripple Injection Filter, *IEEE Transactions on Circuits and Systems II: Express Briefs*, *59*(6), 356–360.

[30] **Park, C.J.**, **Onabajo, M. and Silva-Martinez, J.** (2014). External Capacitor-Less Low Drop-Out Regulator With 25 dB Superior Power Supply Rejection in the 0.4–4 MHz Range, *IEEE Journal of Solid-State Circuits*, *49*(2), 486–501.

[31] **Ganta, S.**, **Park, C.J.**, **Gitzel, D.**, **Rivera, R. and Silva-Martinez, J.** (2013). An external capacitor-less low drop-out regulator with superior PSR and fast transient response, *2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp.137–140.

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PUBLICATIONS

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- - M. S. Berk, B. B. İnam and M. B. Yelten, "An ISM-Band Multi-Phase Injection-Locked Ring Oscillator," 2021 IEEE 12th Latin America Symposium on Circuits and System (LASCAS), (2021)
- - F. B. Gencer, X. Xhafa, B. B. İnam and M. B. Yelten, "Design and validation of an artificial neural network based on analog circuits," Analog Integr Circ Sig Process 106, (2021)
- - F. B. Gencer, X. Xhafa, B. B. İnam and M. B. Yelten, "Design of An Analog Circuit-Based Artificial Neural Network," 2019 11th International Conference on Electrical and Electronics Engineering (ELECO), Bursa, Turkey, (2019)