INTEGRATION, the VLSI journal 90 (2023) 81–89

Contents lists available at ScienceDirect

Integration, the VLSI Journal

journal homepage: www.elsevier.com/locate/vlsi

Radiation-aware analog circuit design via fully-automated simulation environment

Omer Yusuf Muhikanci [a], Kemal Ozanoglu [a,*], Engin Afacan [b], Mustafa Berke Yelten [c], Günhan Dündar [a]

[a] Department of Electrical and Electronics Engineering, Boğaziçi University, Turkey
[b] Department of Electronics Engineering, Gebze Technical University, Turkey
[c] Department of Electronics and Communications Engineering, Istanbul Technical University, Turkey

ARTICLE INFO

Keywords:
Space
Radiation
Analog
SET
TID
Sensitivity
Temperature
CAD

ABSTRACT

As a result of increased interest in space applications, radiation-aware circuit design has become a major concern to guarantee the safe operation of electronic systems operating under extreme space conditions. As the first step, several ad-hoc simulation approaches have been developed in analog and digital domains to estimate the functional behavior of circuits exposed to high radiation. However, most of these tools are application specific and stand-alone (not integrated into the simulation tools). Also, several commercial CAD solutions exist; however, access to these tools is limited due to security measures. To this end, we have developed a well-equipped, SPICE-integrated, and free-to-access simulation tool, RadiSPICE, capable of running statistical radiation simulations and performing extended temperature and sensitivity analyses. By using RadiSPICE, one can readily predict the functional behavior of circuits after long-term or short-term radiation effects. Moreover, the sensitivity analysis reveals vulnerabilities of the design against radiation and provides valuable design hints to the designer to make circuits radiation-hardened. To demonstrate the proposed tool, we have performed several experiments on two analog building blocks with different topologies (bandgap reference and comparator circuits) using RadiSPICE and discussed the robustness of the designs in detail.

1. Introduction

Research investments in space technologies have recently become more widespread mainly due to curiosity about the beginning of life, the construction of novel satellite communication systems, and exploration plans for the planets of the solar system and outer space. Electronic devices are located at the heart of these challenging missions, used in almost every part of the entire system. Performance-oriented circuit design for space applications is not different from the conventional design flow. However, one further problem appears with space applications: *radiation*. Radiation is transmission of energy or particles from a source through space. Most electronic devices used in space applications are exposed to highly energized particles (cosmic rays) such as protons and electrons arising from the charge trapped in the magnetosphere, solar radiation, and cosmic radiation [1]. These unexpected charges caused by radiation may interfere with the nominal operation of circuits, cause either permanent or temporary irregular behaviors, and ultimately result in a circuit malfunction. The story of the first communication satellite, Telstar-1, is a dramatic example of radiation-induced malfunction. The satellite failed just after the launch due to excessive high-energy electrons in the radiation belts caused by an exoatmospheric nuclear weapon test [2]. Furthermore, aggressive scaling of CMOS technology has increased the possibility of radiation-induced errors since smaller devices have a higher sensitivity to radiation events. So, even a very small amount of charge trapped in the channel or dielectric may alter the electrical properties of devices, leading to detrimental operational failures. Considering the catastrophic effects of radiation on the circuits and its results on critical space missions, researchers have extended their scope to avoid undesirable radiation-induced errors and ensure reliable operation.

Radiation-induced failures of CMOS transistors originate from two different phenomena: Total Ionization Dose (TID) and Single Event Effects (SEE) [3–5]. TID is a permanent result of radiation, which occurs after either hard and short-term or soft and long-term radiation stress of devices. As a result of TID, radiation-induced charges are captured in the Si–SiO_2 interface of transistors, leading to a shift in the device threshold voltage and resulting in dramatic performance losses. In contrast to TID, SET is a temporary phenomenon, which is the traveling of a single-highly energized particle through transistors [6].

* Corresponding author.
E-mail address: kemal.ozanoglu@boun.edu.tr (K. Ozanoglu).

https://doi.org/10.1016/j.vlsi.2023.01.009
Received 10 October 2022; Received in revised form 4 January 2023; Accepted 11 January 2023
Available online 16 January 2023

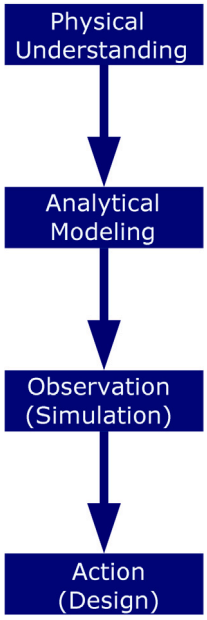

Fig. 1. Reliability-aware design steps.

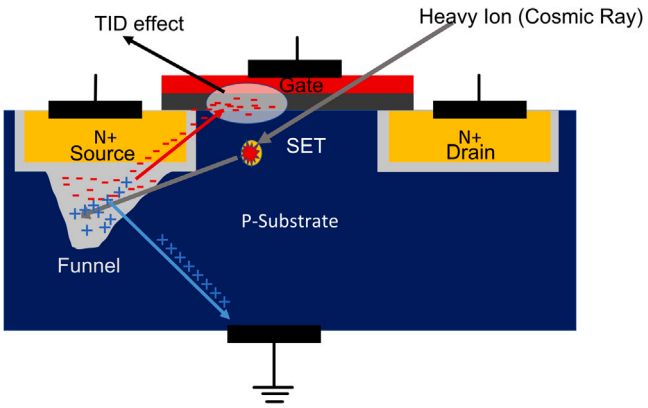

Fig. 2. Illustration of TID and SET on the cross-sectional view of a transistor.

SET does not cause any permanent change in any electrical parameter of the transistor; instead, it creates an instant charge transient at circuit nodes, thereby possibly impairing the operation of the circuit.

A general flow for reliability-aware circuit design is given in Fig. 1, where the design flow consists of four major steps: physical understanding, modeling, observation, and action. This flow is also valid for the radiation-aware circuit design. Radiation phenomena have been studied for a long time, and a certain background on underlying physical mechanisms has already been established. Modeling and simulation of radiation events are the priority to simulate the effects on the circuit performance (observation). The modeling of radiation-induced events has been successfully addressed in the literature [7]. Since TID causes considerable changes in the threshold voltage and leakage current, the models for TID have been developed to emulate these changes [8–10]. On the other side, SET is modeled as a double-exponential source to implement the charge collected by any node [11]. There are also different physical or behavioral models available in the literature [12,13]. The reported models are quite successful and applicable at both behavioral and transistor levels. Once reliable models are obtained, the next step is to observe the effect of radiation events on circuit performance by using the models in simulations. Prior work has focused on modeling radiation effects at transistor level [14–18]. Most of the reported work on the radiation effects simulation is application-specific. Even though simulation flows have been proposed for several applications, they cannot easily be generalized since they need relatively tedious preliminary work to re-construct the simulation framework for each circuit under test. Besides, a few commercialized simulation tools are available; however, they are expensive and have limited accessibility. To meet this deficiency, we present a well-appointed, free-to-access, and fully-integrated simulation tool: RadiSPICE. RadiSPICE is capable of statistical simulation of radiation events. It also incorporates an extended simulation temperature range utilizing models from cryogenic temperatures ($T < -150$ °C) to above-military-range ($T > 125$ °C) high temperatures. Furthermore, RadiSPICE can also perform sensitivity analysis to reveal the most sensitive parts of the circuit under test, hence facilitating the radiation-aware design process. We have designed a bandgap reference (BGR) and a comparator to demonstrate the proposed tool, analyzed them via RadiSPICE, and discussed the actions to make them more robust against radiation phenomena. The remainder of the paper is organized as follows. A brief background on SET and TID and utilized models is provided in Section 2. Section 3 describes the proposed tool in detail. In Section 4, the demonstration circuits are provided, where radiation-aware design techniques are also discussed. Finally, in Section 5 we present the conclusions.

2. Background: Physical mechanisms

Conventionally, there are two underlying radiation-induced degradation mechanisms in CMOS ICs: TID and SET. Fig. 2 illustrates these events on the cross-sectional view of a CMOS device.

TID is a phenomenon that appears due to the cumulative effect of radiation and represents permanent changes in the electrical parameters of transistors. As a result of radiation, energetic charges bombard Si, generating electron–hole pairs during the transition through the material. Some of those charges get captured by the traps existing in the Si–SiO_2 interface, inducing the build-up of charge, and altering the device threshold voltage [19]. As a result, they cause a considerable shift in the bias currents changing the circuit operation points and circuit specifications [18,20].

In contrast to TID, SET causes a temporary change in the circuit performance. As depicted in Fig. 2, SET is associated with cosmic rays (high energy protons and heavy particles) [21]. When an energized particle hits the circuit, it induces unexpected charges on the device. Consequently, it may cause a failure at any instant of circuit operation [2]. SET mostly affects off-transistors and leads to an increase in leakage current or voltage on the corresponding node. Conventionally, SET-originated failures are called ‘soft failures’ and do not cause detrimental permanent damage to devices. However, the instant change in voltage/current may disrupt the circuit transient response and result in reliability problems during the operation period [22–27]. Typically, a double exponential current pulse as illustrated in Fig. 4 mimics SET [28].

$$Q_{tot} = I_{peak}\left[t_1 + t_2 + (td_2 - td_1) - t_1 e^{-(td_2 - td_1)/td_1}\right] \quad (1)$$

The amplitude of the injected charge due to SET can be calculated using Eq. (1), where t_{d1} is the onset of the rise current, t_{d2} is the onset of the fall current, t_1 is the rise time constant, t_2 is the fall time constant, I_{peak} is the peak current amplitude, and Q_{tot} is the total charge delivered by the current pulse [11]. The value of the ionizing charge is estimated as a Gaussian distribution ($\mu = 0.25$ pC, $\sigma = 0.02$ pC). The rise time is kept as 1 ns while the fall time is four times slower than the rise time. [22].

3. RadiSPICE: A fully automated radiation simulation environment

A general flow for the proposed simulation environment is given in Fig. 3. RadiSPICE [29] is run on MATLAB® with a user-friendly

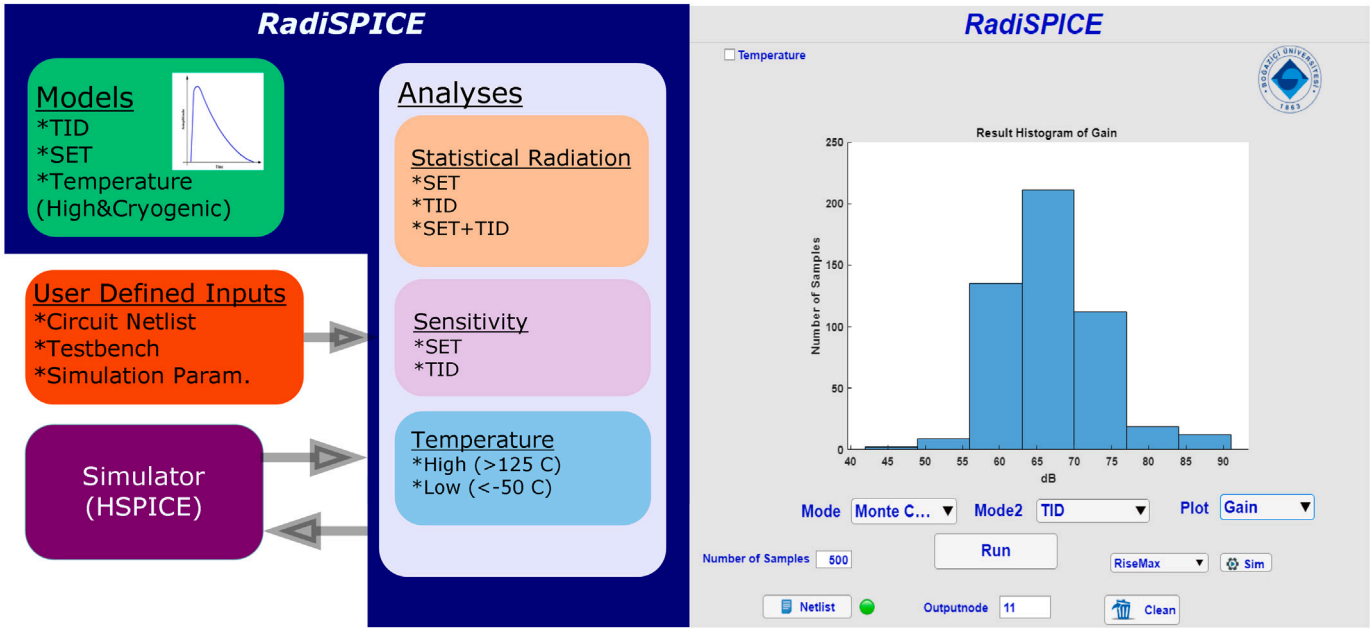

Fig. 3. A general flow and the user interface of RadiSPICE.

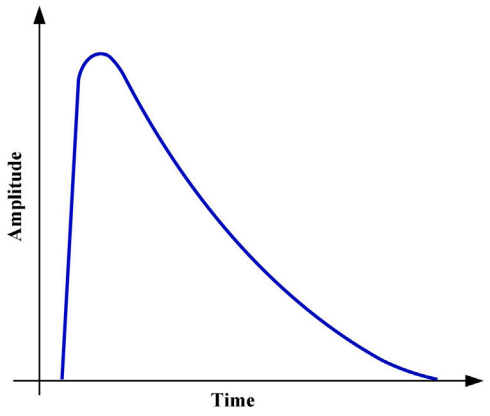

Fig. 4. Double exponential response for SET modeling.

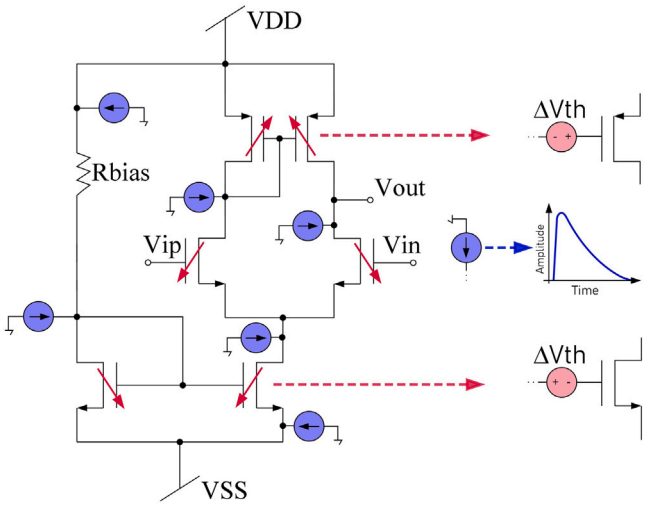

Fig. 5. Manipulated schematic for statistical radiation simulation, where the voltage sources represent V_{th} changes due to TID while the current sources represent the instant loading effects due to SET.

interface. The tool is fully integrated with SPICE, where HSPICE® and CosmosScope® are used as the simulator and the waveform viewer, respectively. The aforementioned radiation-induced effects (TID and SET) are accounted for via embedded models. Furthermore, extended temperature analysis is also available for very high temperatures and cryogenic conditions. The radiation and temperature analysis models can be readily modified or changed by the user. The tool receives the netlist of the design-under-test (DUT) circuit and manipulates it to simulate the statistical radiation events (TID and SET), conducts sensitivity analysis providing the individual effects of each transistor or node for TID and SET, respectively. Since TID and SET are both random events, radiation simulations are based on performing Monte Carlo iterations. During statistical simulations, SET, TID, and combined SET & TID simulations can be performed. The user selects the type of simulation from the environment interface (Fig. 3).

RadiSPICE offers an extended temperature analysis to investigate the circuit performance under extreme conditions. Here, the user can set the number of simulation points and the maximum and minimum temperature limits. The tool uses the BSIM models for temperatures between −55 °C and −125 °C. However, BSIM models do not support extreme temperatures, and particular models are needed to conduct simulations for either cryogenic or high temperatures [30].

In the SET simulation option, the user can run Monte Carlo simulations for single events, where the simulation temperature and the number of samples can be set. A current injection-based method is used to mimic the SET impact. Namely, current sources are randomly added to each node in the circuit, as shown in Fig. 5, since the event particle may incidentally hit any point on the die. During the analysis, one of those current sources is only activated to inject the charge, as given in Fig. 5. The event duration and amplitude are also varied in each sample. Once the analysis is completed, the tool reports the maximum and minimum changes on the selected circuit specifications. The environment also exhibits a scope option so the user can observe the simulation results on a waveform viewer.

To examine the SET effects, a D-latch circuit (Fig. 6) has been designed and simulated on RadiSPICE. The nominal and SET-affected simulation results are provided in Fig. 7. As can be seen from the results, a glitch and bit flips occur at the output node. Triple Modular

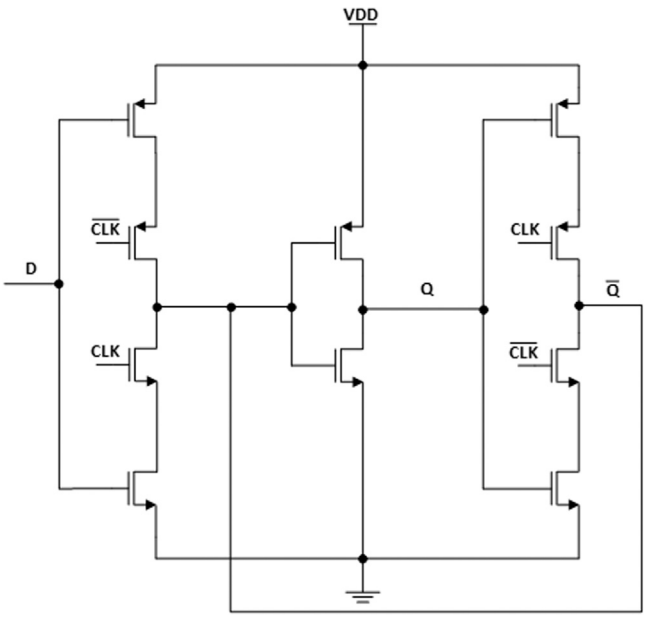

Fig. 6. Schematic of the D-latch.

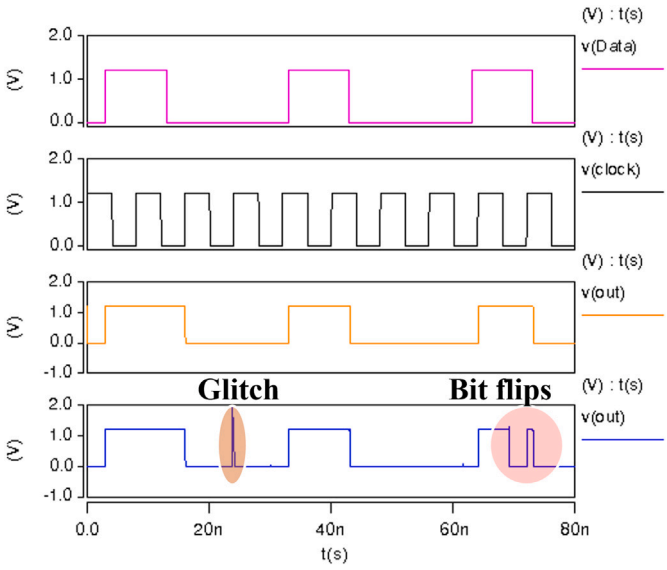

Fig. 7. Transient simulation output with and without SET.

Redundancy (TMR) is widely employed in digital circuits to avoid such catastrophic errors [31].

As shown in Fig. 5, a variable DC voltage source is connected to the gates of transistors in the DUT to emulate the TID-induced threshold voltage degradation, where the amplitude of the source is varied through the MC analysis. Contrary to SET, TID causes permanent damage to devices, so it is not necessary to observe the transient behavior of the circuit under investigation. Instead, RadiSPICE provides the histogram plot for the corresponding performance metric.

Another simulation option in RadiSPICE is sensitivity analysis, which reveals the component sensitivities to radiation effects. Similar to SET and TID analyses, a current source to every node and a voltage source to the gates are added to emulate SET and TID, respectively. In contrast to MC analysis, simulations are performed one by one in order to obtain the individual contributions of both nodes and transistors exposed to radiation. As a result of sensitivity analysis, the tool yields

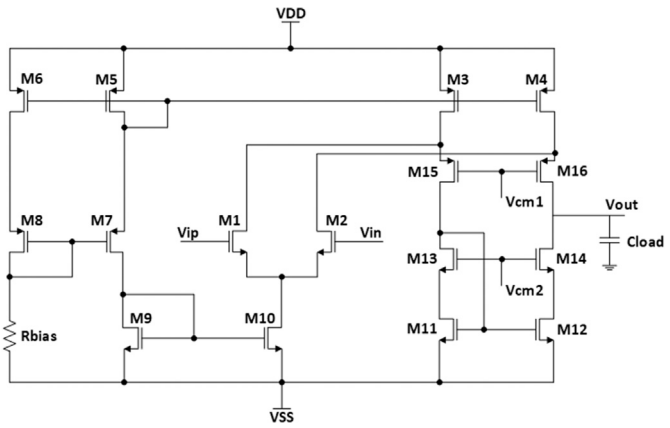

Fig. 8. Schematic of the simulated FCA.

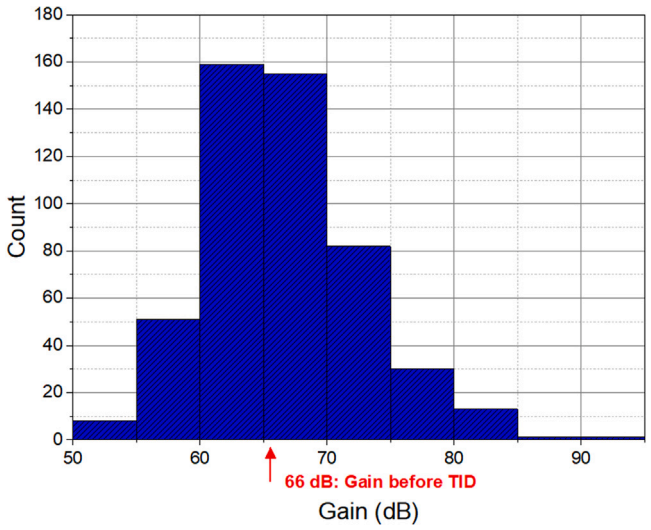

Fig. 9. TID effect on the gain of the FCA circuit.

a sensitivity matrix listing all sensitivities. The first column of the matrix consists of relative sensitivity values, where the most sensitive device/node is fixed to 100. The second and third columns represent the changes in the specified performance metrics.

To demonstrate both TID and sensitivity analyses, a folded cascode amplifier (FCA) given in Fig. 8 has been designed. The sample size for the MC analysis was selected as 500, where RadiSPICE monitors the change in the amplifier specifications such as gain, power, and gain-bandwidth product. Fig. 9 provides the histogram plot of the change in DC gain of the amplifier exposed to TID. As evident in Fig. 9, the gain of FCA varies considerably (42 dB to 91 dB) due to TID, where the nominal value was around 60 dB. The results of sensitivity analysis are tabulated in Table 1. According to the results, M3 and M4 are the most sensitive transistors to TID effects, so the designer should focus on these devices to mitigate the radiation effects.

4. Radiation-hardened circuit design via RadiSPICE

This section aims to give examples of how RadiSPICE can be utilized to validate the design of radiation-aware circuits. For that purpose, two different circuit topologies, the bandgap reference circuit and the dynamic comparator will be investigated for several vulnerability mechanisms due to space radiation.

Table 1
TID Sensitivities of the transistors in the FCA.

Transistor	Relative sensitivity	Gain change (%)	Output voltage change (%)
M3	100	6.10	0.022
M4	83.44	5.09	0.026
M11	72.73	4.44	0.015
M10	61.65	3.76	1.356
M9	33.09	2.02	1.377
M16	26.41	1.61	0.361
M12	22.67	1.38	0.002
M6	18.99	1.16	2.326
M5	13.93	0.85	2.319
M13	10.15	0.62	0.001
M2	3.25	0.20	2.025
M1	2.27	0.14	2.026
M15	0.61	0.03	0.355
M14	0.07	0.004	0.0001
M8	0.05	0.003	0.010
M7	0.03	0.002	0.003

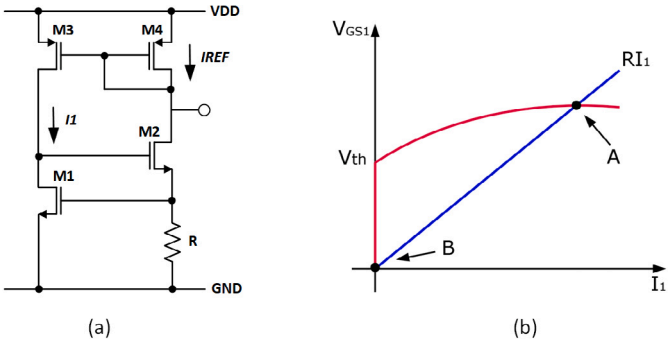

Fig. 10. A self-biased current reference example.

4.1. Reference circuits

The reference voltage and current generators are commonly used in analog integrated circuits to provide reliable bias currents and target voltages to the design; thus, they play a crucial role in system operation. Reference circuits are typically self-biased, having more than one stable operation point. A simple example of a self-biased current Ref. [32] is given in Fig. 10. This circuit may have two different operation points. In the first case, if there is adequate current flowing from both branches, the loop forms such that the voltage drop on the resistor is equal to the V_{GS} of M_1, and the circuit converges to the operation point A and generates a bias current, as shown in Fig. 10(b). In the second case, another operation point exists if no current flows from both branches. In this case, the voltage drop on the resistor and the V_{GS} of M_1 are both zero volts, which is called the *zero current condition*. Ideally, the designer does not consider this case; however, the circuit may get stuck at operation point B after some undesired processes (process variation, aging, radiation, etc.) To eliminate this problem and sustain a proper operation of reference circuits, startup circuits [32] are employed with the intention that the circuit operates away from operation point B.

Conventionally, startup circuits can be classified into two groups: dynamic startup circuits and static startup circuits. Dynamic startup circuits operate only during the power-up of the circuit. Then, they release their hold on the circuit operation; thus, consuming no additional power afterward. Conversely, static startup circuits continuously track the branch currents and interfere with circuit operation if the circuit operation shifts towards operation point B. The main drawback of using a static startup circuit is its continuous static power dissipation. Ideally, using a dynamic startup is encouraged to minimize the power consumption. However, the case would be different for the radiation-hardened circuits, where reliability becomes a major concern.

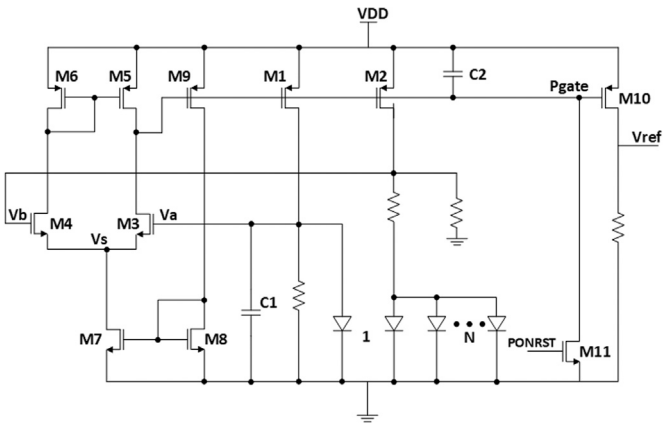

Fig. 11. A low-voltage bandgap reference circuit.

To investigate this problem, a popular self-biased bandgap reference (BGR) circuit [33] has been designed with dynamic and static startup circuits using the 180 nm CMOS process and analyzed via RadiSPICE. The schematic of the bandgap reference with dynamic startup circuit is given in Fig. 11. The differential amplifier at the left-hand side equalizes the voltages V_a and V_b and forms the bandgap loop, thus achieving the reference voltage V_{ref} at the output node. The amplifier itself is also biased with a mirrored replica of the generated branch currents. The dynamic startup circuit is formed with a switch controlled by power-on reset *(PONRST)* signal. When the circuit is powered, it pulls the gates of the current mirror down, thus initiating the loop and forcing the circuit away from the *zero current condition*. After *PONRST* signal becomes low, the circuit maintains the active state, and the output reference voltage preserves its value as long as the bandgap voltage loop is kept. This circuit is regularly used in many applications without any reported issues.

To explore the effect of radiation on the dynamic bandgap reference circuit, first, SET analysis was performed by RadiSPICE. Fig. 12 shows the transient simulation scenario where a negatively charged particle hits node V_a. Due to this unexpected charge, the amplifier input voltage becomes negative, and the output hits the positive supply rail. Thereby, the bias currents, including the bias current of the amplifier, decrease to zero, and the bandgap loop ceases, resulting in a *zero current condition*. Similar failure mechanisms are also reported in [34–36].

The TID sensitivity analysis, demonstrated in Table 2, supports the result obtained from the SET analysis. The table presents a sorted list of bandgap output current and bandgap reference voltage sensitivities. A detailed analysis of the table reveals that transistors with negative sensitivity to output current are more prone to initiate an operation failure, as in the event of radiation exposure, reduction in the bias current will shift the bandgap operation to the direction of *zero current condition*. In addition, other failure mechanisms could also be pointed out, such as a positively charged particle hitting node *Pgate* possibly initiating a similar *zero current condition* failure mechanism.

The obvious result of the SET analysis is that the bandgap reference with a dynamic startup may drastically fail when a heavy ion hits the circuit. As a remedy, the dynamic startup is replaced by a static one, as shown in Fig. 13. The underlying idea is leveraging the static startup behavior, where the bias current is continuously monitored. Hence, the startup transistor M_{12} pulls the gate of the PMOS current sources down in the case of current cease, forcing the circuit away from the *zero current condition*. This mechanism also avoids any SET-induced failure. To verify this hypothesis, the same SET event sequence is applied to the new circuit configuration. Fig. 14 shows the SET analysis of the modified bandgap reference. Thanks to the continuous monitoring property of static startup circuitry, the bandgap voltage V_{ref} recovers after the SET event sequence.

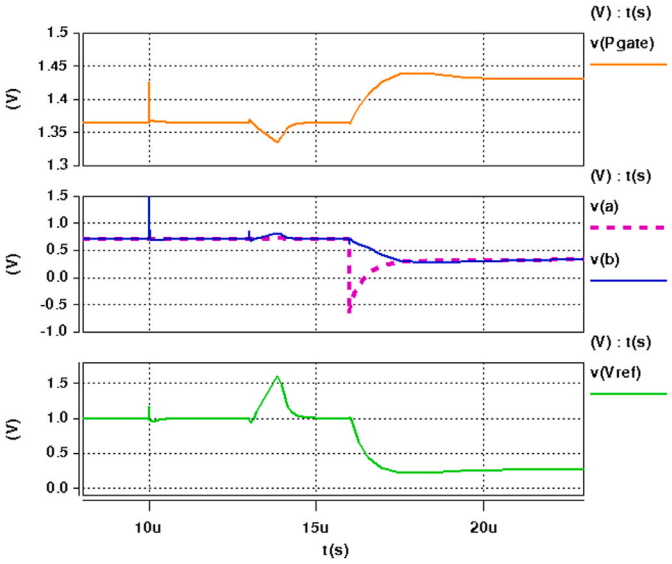

Fig. 12. BGR transient simulation output with reference voltage collapse after SET.

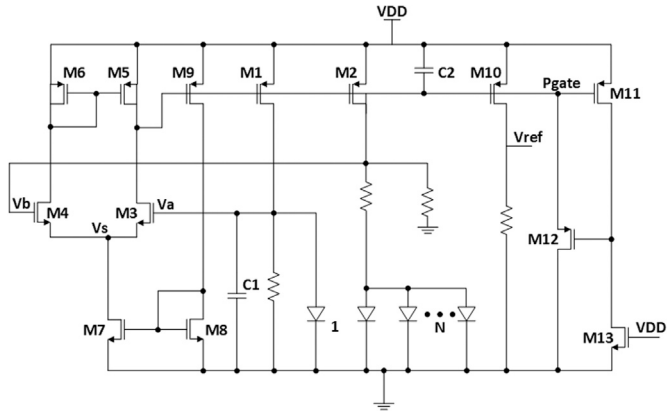

Fig. 13. Updated bandgap reference circuit employing static startup.

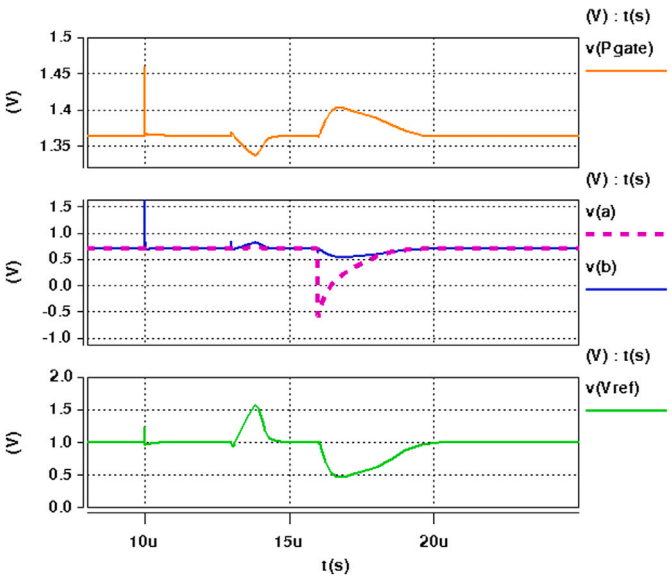

Fig. 14. BGR SET analysis results, showing reference voltage recovery.

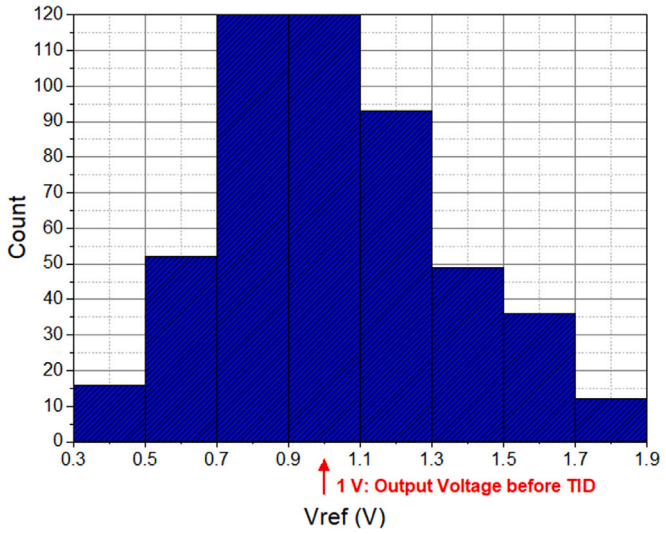

Fig. 15. TID effect on the bandgap reference voltage.

Table 2
Bandgap reference circuit TID sensitivity table.

Transistor	Relative sensitivity	Current change (%)	Output voltage change (%)
M2	100	−4.21	−12.32
M5	82.3	−3.47	−3.21
M3	82.1	−3.46	−3.2
M4	81.6	3.44	3.17
M6	81.1	3.42	3.15
M1	80.6	3.4	3.13
M9	0.93	0.04	0.04
M8	0.73	0.03	0.03
M7	0.64	−0.02	−0.02
M10	0.03	−0.001	9.3

A further radiation exposure effect on the bandgap circuit is the increase in the error of the reference voltage output due to the TID effect. Therefore, TID analysis has been carried out via RadiSPICE, and the results are shown in Fig. 15. The variation in the output reference voltage can spread substantially to $\sigma = 0.313$ V due to radiation exposure. The shift amount exceeds the expected process and device mismatch limits, thus necessitating updated ranges for trimming circuits and periodic self-trimming procedures.

4.2. Dynamic comparators

As a second demonstration example, two comparator circuits in different topologies have been designed using 65 nm CMOS technology under similar design constraints for a fair comparison, and the radiation tolerances of the circuits have been investigated.

The schematic of the first comparator is given in Fig. 16, which is the CMOS static latched comparator [37], employing two cross-coupled pairs for maintaining the latched voltage while the *CLK* signal is logic low. The comparator output voltage is expected to toggle when V_{in} crosses V_{ref}. Conventionally, this circuit operates properly even after PVT effects. However, the TID simulation performed with RadiSPICE reveals that radiation-induced mismatch on MOS transistors can result in a substantial comparator offset. As shown in Fig. 17, the comparator has an offset of $\sigma = 26.9$ mV, which is significantly higher than the tolerable limits of process-induced mismatch.

A transient simulation of SET event analysis performed on the static latched comparator and results are provided in Fig. 18. According to the SET analysis, the comparator also tends to generate false logic outputs in the presence of charged particle transition events. The

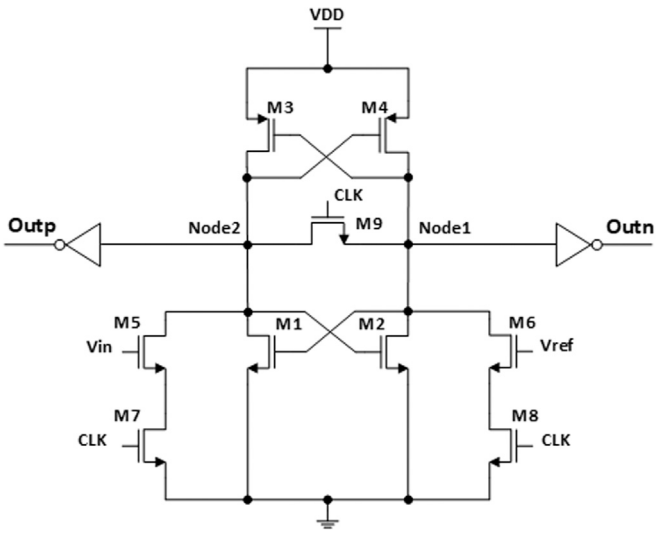

Fig. 16. CMOS static latched comparator.

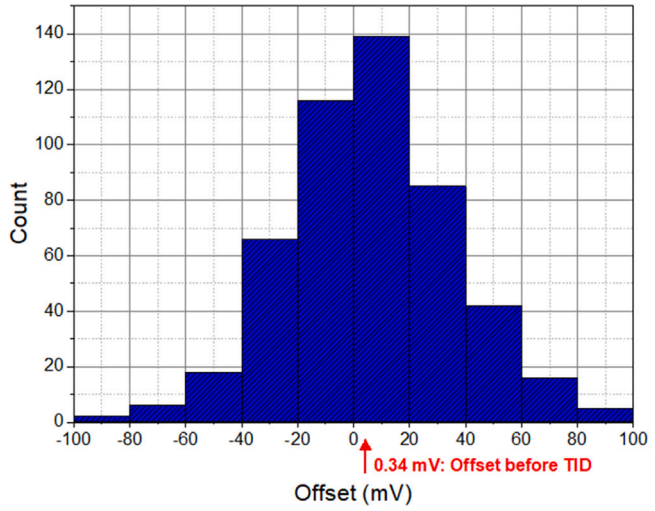

Fig. 17. TID effect on static latched comparator offset.

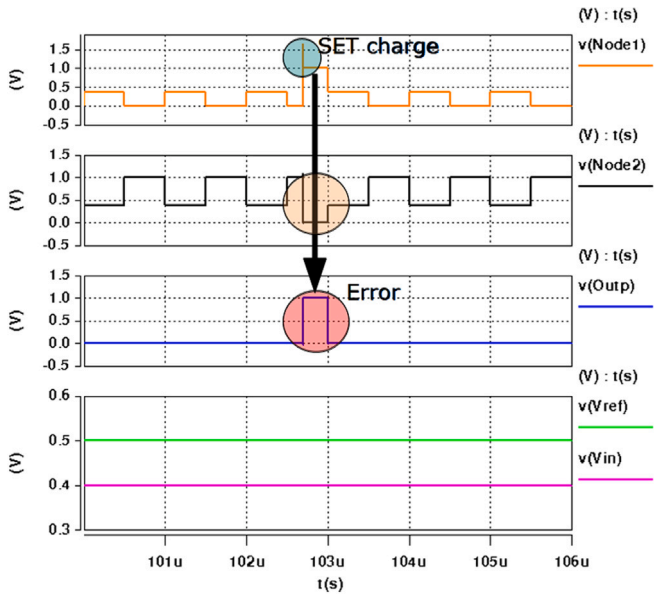

Fig. 18. SET analysis results of the static latched comparator.

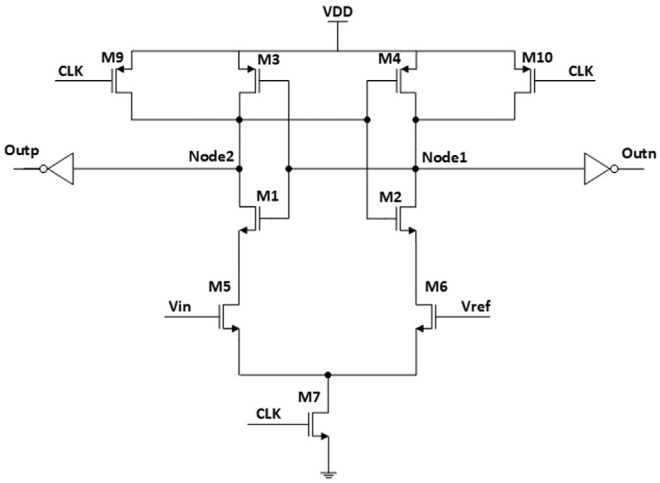

Fig. 19. Strong Arm Latch Comparator.

comparator output can erroneously reach logic high value, even if V_{in} is considerably lower (100 mV) than V_{ref}.

The second comparator under test is a CMOS dynamic latched comparator without static current, also called the *Strong ARM Latch Comparator* [38]. As can be seen from the circuit schematic given in Fig. 19, the circuit employs two cross-coupled pairs for maintaining the latched voltage while the *CLK* signal is logic high. The comparator output voltage is expected to toggle when V_{in} crosses V_{ref}. To examine the circuit behavior under the TID event, statistical simulation was performed via RadiSPICE. According to the results provided in Fig. 20, radiation-induced mismatch on the MOS transistors can dramatically increase the comparator offset up to $\sigma = 14.7$ mV. It can be concluded that this circuit is more robust than the former one. However, it is worth noting that the amount of variation, which is still beyond the acceptable limits for reliable operation.

A transient simulation of SET event analysis performed on the Strong Arm Latch Comparator shows that the comparator can also generate false logic outputs in the presence of charged particle transition events. Shown in Fig. 21, even when V_{in} is 100 mV lower than V_{ref}, comparator output can be at logic high value. This result is in line with the expectation that SET mostly affects off-transistors; hence, the Strong Arm Latch Comparator (not consuming static quiescent current) reveals substantial sensitivity to SET events.

The sensitivity tables for both comparator components to comparator input referred offset are given in Tables 3 and 4. In the tables, a negative sensitivity denotes a comparator offset in the reverse direction. As expected, the input differential pairs show 100% sensitivity. The cross-coupled transistors M_1–M_4 show higher sensitivity in the static latched comparator design as these transistors are continuously ON, affecting the decision process. For the Strong Arm Latch Comparator topology, the cross-coupled transistors M_1–M_4 show less sensitivity as these transistors are not continuously ON and thus have less impact on the decision process. The switch transistors connected to the *CLK* signal have a negligible effect on offset sensitivity for both topologies.

According to the simulation results, it can be concluded that for similarly sized comparator circuits, a TID exposure analysis with RadiSPICE reveals that the static latched comparator exhibits higher deviation on the comparator input offset voltage (σ = 26.9 mV) with respect to the Strong Arm Latch Comparator (σ = 14.7 mV). The TID sensitivity tables provide a deeper perspective on the design, revealing the list of offset-sensitive transistors to radiation exposure. As the static

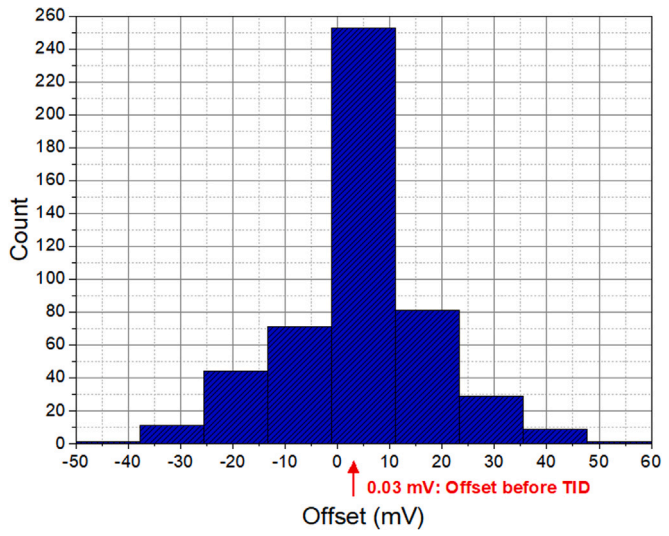

Fig. 20. TID effect on the Strong Arm Latched Comparator offset.

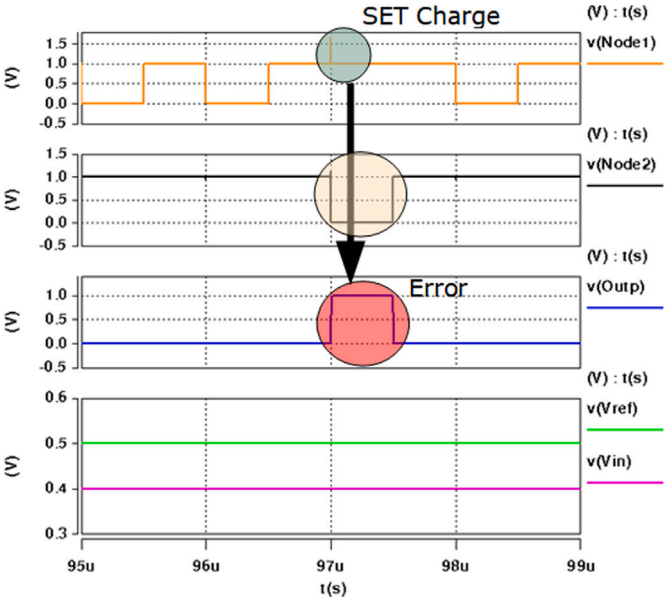

Fig. 21. SET analysis results of the Strong Arm Latched Comparator.

latched comparator branch currents are continuously ON, the cross-coupled transistors add to the overall comparator offset, increasing the offset deviation. Both topologies show weakness to SET events resulting in transient output logic failures, although the Strong Arm Latch Comparator is expected to exhibit more sensitivity to SET events due to employing high impedance nodes. Depending on the comparator requirements, these analysis results might necessitate additional offset-cancellation and TMR circuitry to be embedded in the design.

5. Conclusion

The radiation-hardened circuit design has become a major concern in sustaining a reliable operation during long-term space missions, where radiation effects may deteriorate devices resulting in catastrophic operational failures. Simulation of radiation effects at the design phase is one of the major steps in radiation-aware circuit design. This paper proposes a sophisticated, SPICE-integrated, free-to-access radiation simulation framework. It also exhibits an extended temperature analysis for very high and cryogenic ambient. Two analog building blocks (bandgap reference and comparator circuits) with diverse topologies have been designed, analyzed, and compared to demonstrate the proposed tool via RadiSPICE. The presented tool provides a useful, reliable, comprehensive circuit radiation exposure analysis. Also, it yields design insights pointing to topology weaknesses, paving the way to the option of a required topology update. As future work, we are planning to upgrade the tool such that process variability and time-dependent degradation analyses can also be performed as well.

Table 3
TID sensitivities of the static latched comparator transistors.

Transistor	Relative sensitivity (%)	Offset sensitivity (%)
M3	100	143.2
M4	97.21	−139.2
M2	81.01	−116
M1	80.45	115.2
M5	69.83	100
M6	69.83	−100
M7	15.64	22.4
M8	13.97	−20
M9	0.56	0.8

Table 4
TID Sensitivities of the Strong Arm Latch Comparator transistors.

Transistor	Relative sensitivity (%)	Offset sensitivity (%)
M5	100	100
M6	99.2	−99.2
M3	22.4	22.4
M4	21.6	−21.6
M1	5.6	5.6
M2	4.8	−4.8
M10	1.6	1.6
M7	0.8	0.8
M9	0.8	−0.8

CRediT authorship contribution statement

Omer Yusuf Muhikanci: Software, Validation, Investigation, Acquisition of data. **Kemal Ozanoglu:** Methodology, Investigation, Analysis and interpretation of data, Drafting. **Engin Afacan:** Methodology, Investigation, Analysis and/or interpretation of data, Drafting. **Mustafa Berke Yelten:** Resources, Methodology. **Günhan Dündar:** Conceptualization, Design of study, Methodology.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

Acknowledgment

The authors would like to thank Atakan Turker for his dedicated support in providing valuable simulation data.

References

[1] C.M. Whitney, et al., Radiation effects on a potential scintillation-based solid-state spectrometer prototype for compact monitoring of space radiation/weather satellite conditions, IEEE Trans. Nuclear Sci. 58 (6) (2011) 3095–3102.
[2] D.M. Fleetwood, P.S. Winokur, Radiation effects in the space telecommunications environment, in: 2000 22nd International Conference on Microelectronics. Proceedings (Cat. No. 00TH8400), Vol. 1, IEEE, 2000, pp. 43–49.

[3] P. Dodd, M. Shaneyfelt, J. Schwank, J. Felix, Current and future challenges in radiation effects on CMOS electronics, IEEE Trans. Nucl. Sci. 57 (4) (2010) 1747–1763.
[4] J.R. Schwank, M.R. Shaneyfelt, P.E. Dodd, Radiation hardness assurance testing of microelectronic devices and integrated circuits: Radiation environments, physical mechanisms, and foundations for hardness assurance, IEEE Trans. Nucl. Sci. 60 (3) (2013) 2074–2100.
[5] O. Schrape, M. Andjelković, A. Breitenreiter, S. Zeidler, A. Balashov, M. Krstić, Design and evaluation of radiation-hardened standard cell flip-flops, IEEE Trans. Circuits Syst. I. Regul. Pap. 68 (11) (2021) 4796–4809.
[6] R.C. Baumann, Radiation-induced soft errors in advanced semiconductor technologies, IEEE Trans. Device Mater. Reliab. 5 (3) (2005) 305–316.
[7] M.B. Yelten, Holistic device modeling: Toward a unified MOSFET model including variability, aging, and extreme operating conditions, IEEE Trans. Circuits Syst. II 69 (6) (2022) 2635–2640.
[8] S. Jagannathan, D.R. Herbison, W.T. Holman, L.W. Massengill, Behavioral modeling technique for TID degradation of complex analog circuits, IEEE Trans. Nucl. Sci. 57 (6) (2010) 3708–3715.
[9] G.I. Zebrev, V.V. Orlov, M.S. Gorbunov, M.G. Drosdetsky, Physics-based modeling of TID induced global static leakage in different CMOS circuits, Microelectron. Reliab. 84 (2018) 181–186.
[10] S. Xi, Q. Zheng, W. Lu, J. Cui, Y. Wei, Q. Guo, Modeling of TID-induced leakage current in ultra-deep submicron SOI NMOSFETs, Microelectron. J. 102 (2020) 104829.
[11] D.A. Black, et al., Modeling of single event transients with dual double-exponential current sources: Implications for logic cell characterization, IEEE Trans. Nuclear Sci. 62 (4) (2015) 1540–1549.
[12] A. Francis, M. Turowski, J. Holmes, H. Mantooth, Efficient modeling of single event transients directly in compact device models, in: 2007 IEEE International Behavioral Modeling and Simulation Workshop, IEEE, 2007, pp. 73–77.
[13] L. Artola, M. Gaillardin, G. Hubert, M. Raine, P. Paillet, Modeling single event transients in advanced devices and ICs, IEEE Trans. Nucl. Sci. 62 (4) (2015) 1528–1539.
[14] S. İlik, et al., Modeling of total ionizing dose degradation on 180-nm n-MOSFETs using BSIM3, IEEE Trans. Electron Dev. 66 (11) (2019) 4617–4622.
[15] G. Bozzola, et al., Improvement of radiation tolerance in CMOS ICs through layout-oriented simulation, in: 2016 5th International Conference on Modern Circuits and Systems Technologies (MOCAST), IEEE, 2016, pp. 1–4.
[16] K.O. Petrosyants, et al., Fault simulation in radiation-hardened SOI CMOS VLSIs using universal compact MOSFET model, in: 2016 17th Latin-American Test Symposium (LATS), IEEE, 2016, pp. 117–122.
[17] Fernandez-Martinez, et al., Simulation methods for ionizing radiation single event effects evaluation, in: 2009 Spanish Conference on Electron Devices, IEEE, 2009, pp. 144–147.
[18] S. Redant, et al., Radiation test results on first silicon in the design against radiation effects (DARE) library, IEEE Trans. Nuclear Sci. 52 (5) (2005) 1550–1554.
[19] S. Bala, R. Kumar, A. Kumar, Total ionization dose (TID) effects on 2D MOS devices, Trans. Electr. Electron. Mater. 22 (1) (2021) 1–9.
[20] R.D. Schrimpf, Warren, et al., Multi-scale simulation of radiation effects in electronic devices, IEEE Trans. Nuclear Sci. 55 (4) (2008) 1891–1902.
[21] A. Samaras, Protons single event transients test report, 2012, https://escies.org/download/webDocumentFile?id=60116, [Online; accessed 29-September-2022].
[22] Q. Zhou, K. Mohanram, Gate sizing to radiation harden combinational logic, IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst. 25 (1) (2005) 155–166.
[23] H.T. Nguyen, et al., Chip-level soft error estimation method, IEEE Trans. Dev. Mater. Reliab. 5 (3) (2005) 365–381.
[24] N. Seifert, Soft error rates of hardened sequentials utilizing local redundancy, in: 2008 14th IEEE International on-Line Testing Symposium, IEEE, 2008, pp. 49–50.
[25] D. Limbrick, et al., Impact of synthesis constraints on error propagation probability of digital circuits, in: 2011 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems, IEEE, 2011, pp. 103–111.
[26] W.H. Robinson, et al., Soft error considerations for multicore microprocessor design, in: 2007 IEEE International Conference on Integrated Circuit Design and Technology, IEEE, 2007, pp. 1–4.
[27] R.C. Harrington, Models for Characterizing Single-Event Effects in Advanced Technology Circuits (Ph.D. thesis), Vanderbilt University, 2019.
[28] G. Messenger, Collection of charge on junction nodes from ion tracks, IEEE Trans. Nuclear Sci. 29 (6) (1982) 2024–2031.
[29] Ö.Y. Muhikanci, K. Ozanoglu, E. Afacan, M.B. Yelten, G. Dündar, A simulation tool for space applications: Radispice, in: 2022 18th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design, SMACD, IEEE, 2022, pp. 1–4.
[30] A. Kabaoğlu, et al., Statistical MOSFET modeling methodology for cryogenic conditions, IEEE Trans. Electron Dev. 66 (1) (2018) 66–72.
[31] R.E. Lyons, W. Vanderkulk, The use of triple-modular redundancy to improve computer reliability, IBM J. Res. Dev. 6 (2) (1962) 200–209.
[32] F. Maloberti, Analog Design for CMOS VLSI Systems, Vol. 646, Springer Science & Business Media, 2006.
[33] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, K. Sakui, A CMOS bandgap reference circuit with sub-1-V operation, IEEE J. Solid-State Circuits 34 (5) (1999) 670–674.
[34] G.B. Hamad, S.R. Hasan, O.A. Mohamed, Y. Savaria, New insights into the single event transient propagation through static and TSPC logic, IEEE Trans. Nucl. Sci. 61 (4) (2014) 1618–1627.
[35] M. Tali, Single-event radiation effects in hardened and state-of-the-art components for space and high-energy accelerator applications, JYU Dissertations, 2019.
[36] C.M. Andreou, A. Javanainen, A. Rominski, A. Virtanen, V. Liberali, C. Calligaro, A.V. Prokofiev, S. Gerardin, M. Bagatin, A. Paccagnella, et al., Single event transients and pulse quenching effects in bandgap reference topologies for space applications, IEEE Trans. Nucl. Sci. 63 (6) (2016) 2950–2961.
[37] P.M. Figueiredo, J.C. Vital, Kickback noise reduction techniques for CMOS latched comparators, IEEE Trans. Circuits Syst. II 53 (7) (2006) 541–545.
[38] T. Kobayashi, K. Nogami, T. Shirotori, Y. Fujimoto, A current-controlled latch sense amplifier and a static power-saving input buffer for low-power architecture, IEICE Trans. Electron. 76 (5) (1993) 863–867.