Radiation Effects on MOSFETs

Deepkumar R. Shah

***Abstract*— Electronic devices contain numerous types of oxides and insulator materials. When these devices are brought in the space environment, significant charge build-up in the oxides and insulators induced because of the ionizing radiation can cause device degradation and failure. Electrons, protons, alpha-particles, etc. in the space can lead to radiation-induced total ionizing dose effects and Single Event Effects (SEEs). Moreover, heavy ions in the space can also cause degradation in oxides through different mechanisms like Single Event Gate Rupture, Oxide Breakdown, Displacement Damage, etc. This effects can alter the electrical properties of the devices. This review paper discusses the various radiation effects on MOSFETs, electrical properties that are altered by this radiation effects and the need for radiation hardening.**

***Index Terms*— MOSFETs, radiation effects, SEEs, total-dose effects**

I. Introduction

Since various kinds of radiation particles are present in the space and other radiation environments, electronic radiation hardening parts are used in the space applications. There are basically two types of radiation: particle radiation and photon radiation [1]. Particle radiation consists of charged as well as neutral particles such as protons, electrons, ions, alpha particles and neutrons. On the other hand, photon radiation consists of high energy x-rays and gamma rays. Different units for both types of radiation when dealing with their radiation effects. When dealing with photon radiation, the unit used is *rad*. A rad is the amount of photon radiation which deposits 100 ergs of energy per gram of a given material. When dealing with particle radiation, the units are flux (number/cm^{2}s) and fluence (number/cm^2). The parameters of the radiation particles such as particle mass, particle energy, particle species, target temperature, total dose and flux/fluence can give effect to the amount of radiation damage by the radiation [2]. This can affect the electrical, mechanical, optical, magnetic and superconducting properties of the material.

Oxides and insulators are the key components of all electronic devices from MOSFETs to bipolar ICs. Charge build up in the oxides and insulators due to ionizing radiation can lead to device degradation and failure. In harsh radiation environments, exposure to high energy photons and electrons can significantly reduce the life-time of the system due to total dose effects. Also, there are some single event effects that are short term. TID is a long term effect which permanently damages the device while SEEs are short term single event effects. SEEs appear for a very small interval of time and cause momentary change in the properties or function of the device. Examples of SEEs include Single Event Transients (SETs), Single Event Upsets (SEUs), Single Event Functional Interrupts (SEFIs), etc. In this paper, we discuss the effects of radiation on oxide-induced device degradation and failure, radiation-induced charge build up, heavy ion induced mechanisms and properties, TID effects, SEEs, degradation of electrical properties of the MOSFETs and need for radiation hardening.

II. Total Ionizing Dose Effects

A. Overview

High energy electrons (like the ones present in the environment or photon generated secondary electrons) and protons can ionize the atoms and generate electron-hole pairs. Until the electrons and holes generated by these particles have energy greater than the minimum energy required to generate electron-hole pairs, additional electron-hole pairs will be generated by them. In this way, a single high energy particle or photon can generate thousands of electron-hole pairs.

When MOSFETs are subjected to such high energy radiation particles, electron-hole pairs are generated in the oxide. This electron-hole pair generation in the oxide is the prime reason that leads to almost all TID effects. Charge build up induces in the oxide that can cause device failure. The mechanism of charge build up and device degradation is shown in Fig. 1. Fig. 1 is a plot of the energy band diagram for a MOSFET with p-substrate, n-channel and positive gate bias. As soon as the electron-hole pairs are created, the electrons will drift towards the gate and the holes will move towards the oxide-Si interface due to the presence of positive gate bias. However, some of the electrons will recombine with holes. The fraction of electron-hole pairs that escape recombination is called the charge yield. On the other hand, those holes which escape "initial" recombination will transport through the oxide toward the Si/oxide interface by hopping through localized states in the oxide. As the holes approach the Si/oxide interface, some fraction of the holes will be trapped, forming a positive oxide-trap charge. It is believed that protons (hydrogen ions) are likely released as holes "hop" through the oxide or as they are trapped near the Si/oxide interface. The hydrogen ions can also drift to the Si/oxide interface where they may react to form interface traps. At threshold, the interface traps are predominantly positively charged for p-channel MOSFETs and negatively charged for n-channel MOSFETs.

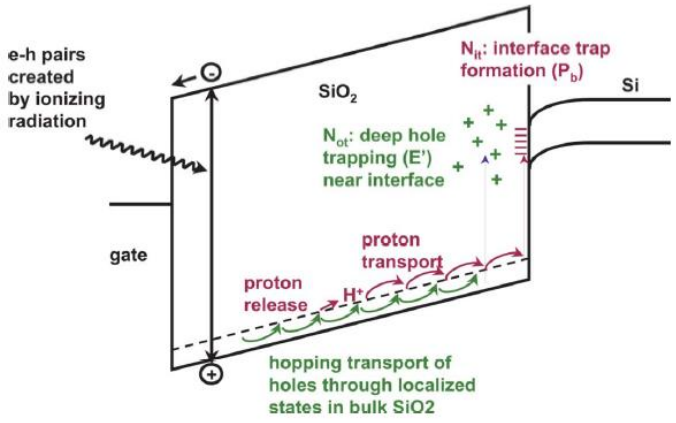

Fig. 1. Band Diagram of a MOS Capacitor with a positive gate bias. The main processes for radiation-induced charge generation are illustrated [3]

In addition to the oxide-trapped charge and interface-trap charge build-up in gate oxides, charge build-up will also occur in other oxides including the field oxides and alternate dielectrics. The radiation-induced charge build-up in these dielectrics can cause device degradation and circuit failure. Positive charge trapping in the gate oxide inverts the channel interface causing leakage current to flow in the "Off" state condition. This results in an increase in the static power supply current of the IC and may also cause IC failure. In a similar fashion, positive charge build-up in the field oxides causes large increases in IC static power supply leakage current. In fact, for advanced ICs with ultra-thin gate oxides, radiation-induced charge build-up in field oxides normally dominates the radiation-induced degradation of ICs. Large concentrations of interface-trap charge decreases the mobility of carriers and increases the threshold voltage of n-channel MOS transistors. These effects tend to decrease the drive of transistors which in turn degrades the timing parameters of an IC.

B. Charge Yield

If there is an electrical field existing across the oxide of a MOSFET, electrons in the conduction band and holes in the valence band will immediately transport in the opposite directions. Electrons are highly mobile in the oxide and are easily swept out of the oxide. Still, before leaving the oxide, some fraction of the electrons recombine with the holes of the valence band. This is called initial recombination. This initial recombination is dependent on the electric field in the oxide and the energy/type of the incident radiation particle [4]. In short, strongly ionizing particles form dense columns of charge and thus, the recombination rate is higher. On the other hand, weakly ionizing particles generate isolated charge pairs and thus, the recombination rate is lower. In terms of strength of the electric field, as the strength of the electric field increases, the recombination probability of the hole decreases. The fraction of un-recombined holes increases. According to [5], the total number of holes generated in the oxide that escape the initial recombination N_h is given by,

$$N_h = f(E_{ox})g_0 D t_{ox} \quad (1)$$

Here, $f(E_{ox})$ is the hole yield as a function of the electric field, g_0 is a material-dependent parameter that gives the initial charge pair density per rad of dose, D is the dose and t_{ox} is the oxide thickness.

C. Oxide Traps

The mobility of holes is less than that of electrons. In the presence of an electric field, the generated holes can travel to gate/oxide interface (negative bias) or oxide/Si interface (positive bias). Due to its positive charge, as a hole moves along in the oxide, it causes a distortion of the potential field of the oxide. This potential distortion increases the trap depth at the site and tends to trap itself at that site. Hence, the hole tries to trap itself at the localized site.

When a positive gate bias is applied, holes transport to the oxide/Si interface. Near the interface there are a large number of oxygen vacancies because of the "out-diffusion" of oxygen in the oxide and lattice mismatch at the surface [3]. These oxygen vacancies can act as trapping centres. Some fraction of the holes will be trapped as holes approach the interface. The number of holes that are trapped is given by the capture cross-section area near the interface. This is dependent on the applied field (gate bias) and is highly device fabrication dependent, with only a few percent of the holes being trapped in hardened oxides to as much as 50-100% for soft oxides [3]. The positive charge associated with trapped holes causes a negative threshold-voltage shift in both nMOS and pMOS transistors.

D. Interface Traps

Now, in addition to the formation of oxide traps, radiation also leads to the formation of interface traps. These interface traps can be positive, negative or neutral. Also, they exist within the silicon band gap, at the interface. Because of the presence of these traps at the interface, its charge can be easily changed by applying a specific gate bias. Traps in the lower portion of the band gap donate an electron to silicon and are thus, donors. Therefore, for pMOS transistor, the interface traps are positively charged which cause negative threshold voltage shifts. On the other hand, traps in the upper portion of the band gap accept an electron from silicon and are thus, acceptors. Therefore, for nMOS transistor, the interface traps are negatively charged which cause positive threshold voltage shifts. For interface traps at the mid-gap, they are approximately neutral. As the oxide trap charge is positive for both nMOS and pMOS transistors, interface trap charge and oxide trap charge compensate each other for nMOS transistors and add together for pMOS transistors [3].

E. Field Isolation Leakage

As the thickness of the gate oxide has kept on decreasing with the scaling of CMOS technology, less charge can be trapped in this thin oxide. This trapped charge can be easily

neutralized by thermal emission and electron tunnelling [6]. Because of this, charge trapping in the thicker field isolation oxide has become a grave concern for modern CMOS technology as compared to the charge trapping in gate oxide. Due to charge trapping in the field oxide, there is a leakage current that flows between transistors which can cause transistor cross-talk and thus, device failure or functional failure. This is not particularly a transistor effect of radiation but an IC effect.

F. Particle Micro-dose Effects

When total dose effects are caused by individual energetic particles, they are called micro-dose effects. These are nothing but an intersection of total dose effects and SEEs [7]. It can be also called Single Event Total Dose (SETD). These are total dose effects occurring as a single event and causing total dose failure of a single transistor. Such single energetic particle can cause device failure and thus, were studied independently from total dose effects. To mitigate unexpected failures of MOS devices in proton-rich or other charged-particle-rich space environments and to avoid underestimation of radiation-induced degradation by gamma ray testing of devices, particle micro dose effects are studied. This provided device reliability assurance for charge-rich space environments.

III. DEGRADATION IN ELECTRICAL PROPERTIES OF MOSFETS

A. Threshold Voltage Shifts

Threshold voltage for both nMOS and pMOS transistors shift due to radiation induced oxide trapped charge (N_{ot}) and interface trapped charge (N_{it}). The contributions of N_{it} and N_{ot} are additive for pMOS transistors and subtractive for nMOS transistors as discussed earlier. Both types of charges change with the post-irradiation time, temperature and electrical conditions. This is turn varies the threshold voltage as well. TID threshold voltage shifts depend on the thickness of the oxide (t) according to a power law (t^n), where n can be between 1 and 2 or 2 or 3 depending on the electrical biasing effects and processing [8]. The caveat to this is that the oxides with thickness less than 10 nm show almost no radiation-induced threshold voltage shifts. Figures 2 and 3 show the variation in the threshold voltage due to TID.

B. Sub-Threshold Slope

Radiation-induced sub-threshold slope is affected by both trapped interface charge (N_{it}) and lateral non-uniformity of trapped oxide charge (N_{ot}) [8]. Lateral non-uniformity of N_{ot} can be caused by a non-uniform deposition of charge or by a non-uniform distribution of traps. These effects degrade the device performance by increasing leakage currents.

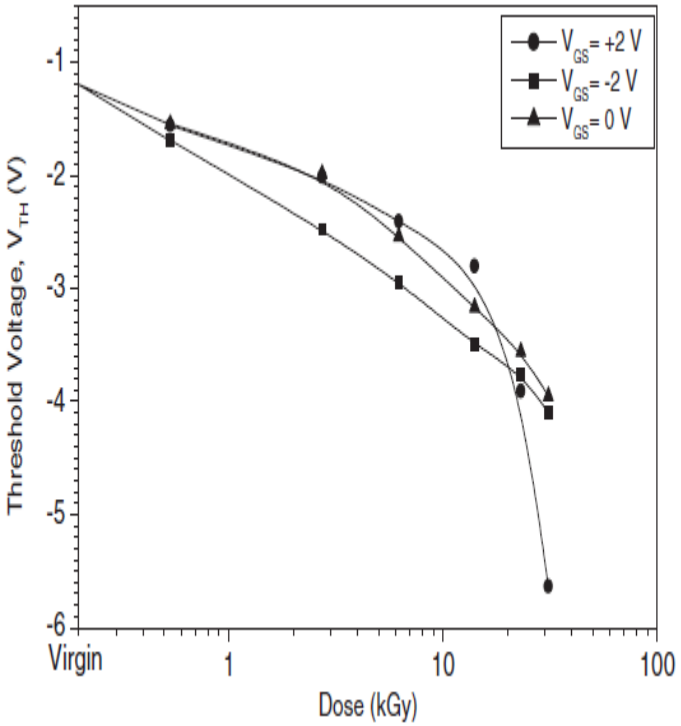

Fig. 2. Variation in the threshold voltage, V_{TH} after 8 MeV electron irradiation [9]

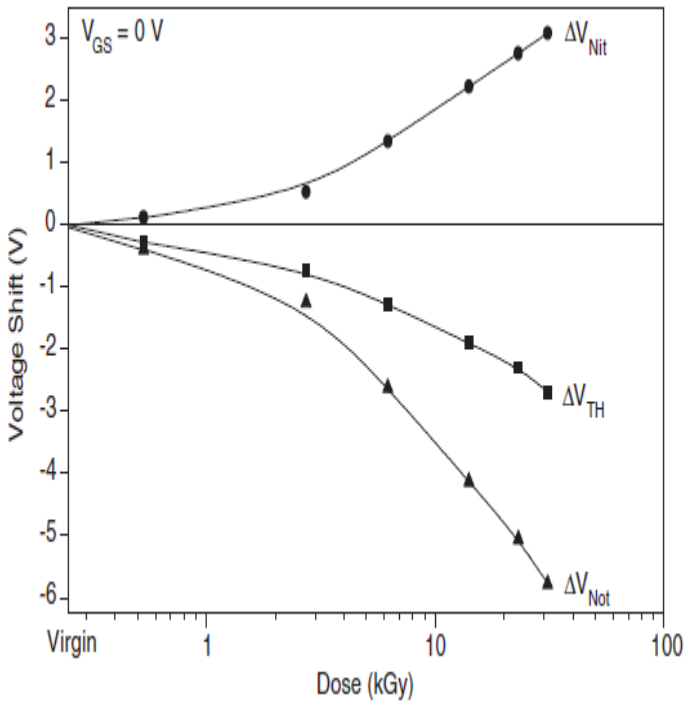

Fig. 3. Net threshold voltage shift and contributions to that shift due to interface traps and trapped-oxide charge for 8 MeV electron irradiated MOSFET. [9]

C. Transconductance

The Transconductance (g_m) of the MOS transistor is decreased by radiation-induced reduction in carrier mobility (μ) in the device channel caused by charges trapped at, or very

close to, the Si/oxide interface [8]. Transconductance also can be reduced by increase in surface resistivity such as would be caused in a MOSFET with Lightly Doped Drain (LDD) regions intended to reduce hot carrier reliability effects. Radiation-induced trapped charge in the field/spacer oxide, used to fabricate the LDD region, has been found to deplete p-type LDDs, increasing the resistivity and causing degradation in Transconductance without affecting the mobility (μ). Transconductance affects the speed and output drive of the MOSFET. Any change in the value of g_m affects the performance of the transistor. Figures 4 and 5 show the change in g_m and peak value of g_m due to TID.

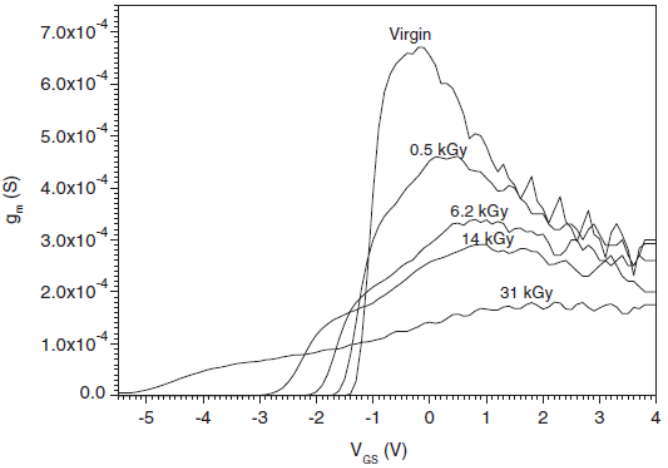

Fig. 4. Variation in g_m after 8 MeV electron irradiation (at V_{DS} = 0.1 V) [9]

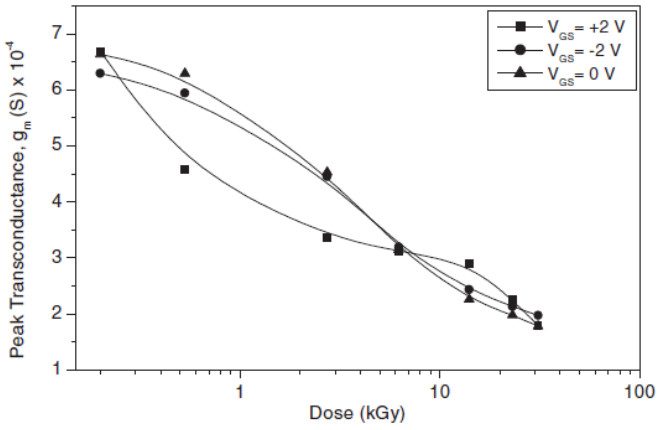

Fig. 5. Variation in g_{mPeak} after 8 MeV electron irradiation [9]

D. Channel and Junction Leakage Current

GIDL (Gate-Induced Drain Leakage) current is increased by Total Ionizing Dose (TID) [8]. Trapped charge build-up in lateral oxide isolation regions (i.e. field oxide structures) increases transistor edge leakage current and changes the junction breakdown voltage (degradation in nMOS transistors and enhancement in pMOS transistors).

E. 1/f Noise

Flicker noise or 1/f noise increases because of TID. This is correlated to the presence of oxide trapped charges and interface trapped charges in the oxides [8]. An increase in the flicker noise is detrimental to the phase noise of high frequency transceiver front-end circuits (e.g. mixers and VCOs i.e. Voltage Controlled Oscillators) as well as base band communications applications such as data converters and filters [10].

F. Gate Oxide Stability and Breakdown

We know that radiation induced trapped charges affect the oxide leakage current but these charges also affect the breakdown voltage of oxides. It has been observed that the trapped charges increase the oxide leakage current and reduce the oxide breakdown voltage. This occurs due to electron trap assisted tunnelling for total dose irradiations greater than 1 Mrad (Si) [8].

G. Mobility

Mobility of the carriers in the channel of a MOSFET can be determined from the value of g_m and peak value of g_m. With the change in the value of Transconductance due to TID, the mobility of the MOSFET also changes. This affects the speed of the MOSFET device. The relation between g_m and μ is given by

$$g_m = (Z\mu C_{ox}/L)V_{DS} \quad (2)$$

Here, Z is the width of the device, L is the length of the device, μ is the mobility of the device and C_{ox} is the oxide capacitance per unit area. Figures 6 and 7 show the variation in device mobility due to TID and also as a function of the interface trapped charge.

IV. SINGLE EVENT EFFECTS OVERVIEW

While TID effects are long term effects, SEEs are short term effects. The charge deposited by a single ionizing particle can produce a wide range of SEEs, including Single-Event Upsets (SEU), Single-Event Transients (SET), Single-Event Dielectric Ruptures (SEDR), Single-Event Functional Interrupts (SEFI), Single-Event Latchups (SEL), etc. SEEs can be produced by direct ionization (primary charged particles) or by secondary particles resulting from elastic collisions or nuclear reactions. High-speed ICs exhibit increased vulnerabilities to SEEs, including multiple-bit upsets that result from aggressive scaling, and large enhancements relative to ion-strike angle that are much greater than for earlier generations of technology [11]. SEUs are responsible for device soft failure. SETs do not directly cause upsets but may propagate through the logic. SEFIs can cause functional failure and needs device reconfiguration or power reset for recovery. As SEEs affect the circuit as a whole and not the MOSFET, SEEs are not discussed in detail here. Detailed explanation of

various SEEs is given in [7].

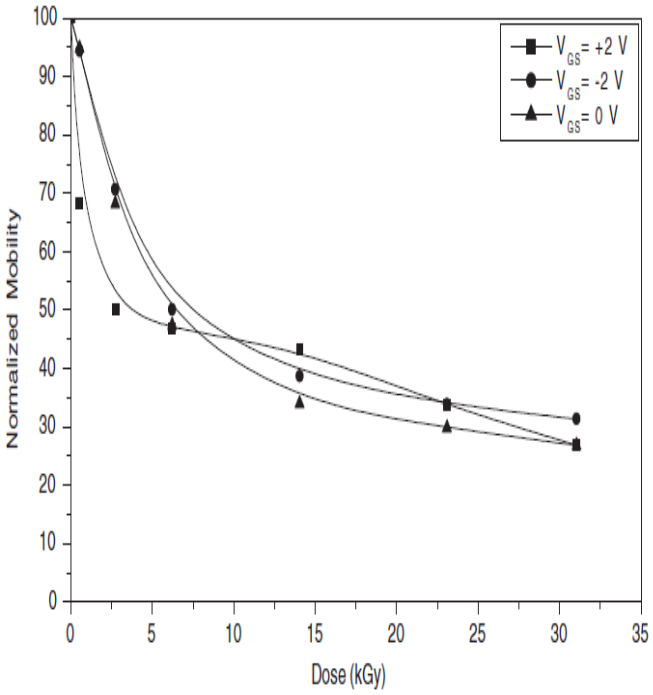

Fig. 6. Variation in normalized mobility after 8 MeV electron irradiation [9]

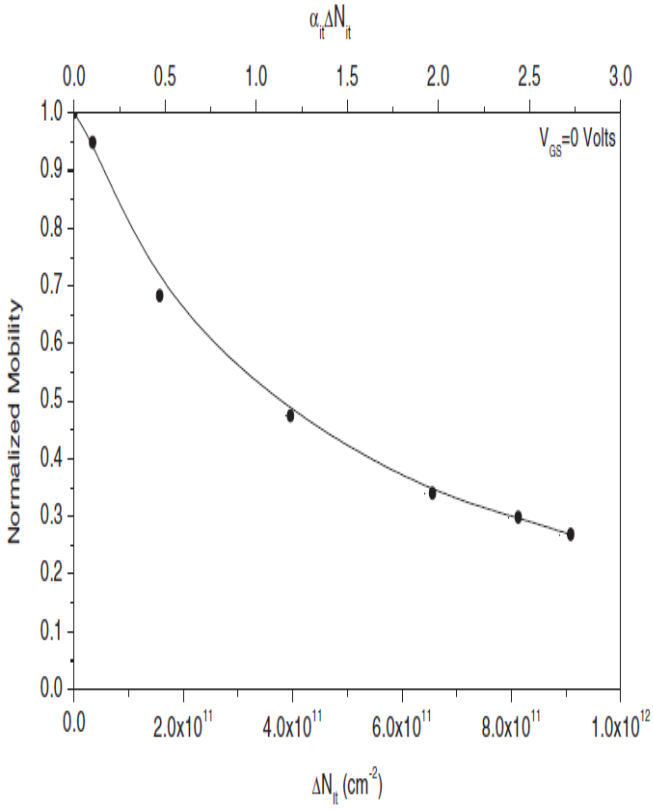

Fig. 7. Normalized mobility degradation during irradiation as a function of interface trapped charge N_{it} [9]

V. IMPORTANCE OF RADIATION HARDENING

Radiation hardening of MOS devices and circuits require specialized design, layout and/or processing steps. There are two types of radiation hardening: Radiation Hardening by Design (RHBD) and Radiation Hardening by Process (RHBP). RHBD deals with hardening by adding more transistors at circuit level and redundancy along with a majority voter circuit at system level [12]. Some techniques even use the concept of feedback and delay elements to mitigate SETs. RHBP deals with specific techniques to reduce the number of traps/recombination centres in the oxide [8]. As RHBP requires additional processing steps, it is costlier than RHBD. With more and more number of transistors being able to fit in the same size of an IC through scaling, adding more transistors than necessary, to reduce radiation effects has gained more importance.

VI. CONCLUSION

To sum up, it is very important to study radiation effects to make reliable space electronics. Various properties of the materials are varied in the space environment due to TID and SEEs. To mitigate these effects, RHBP and RHBD are used extensively for space applications.

REFERENCES

[1] Y. H. Lho, K. Y. Kim, "Radiation Effects on the Power MOSFET for Space Applications," *ETRI Journal*, vol. 27, no. 4, Aug. 2005, pp. 449-452. DOI: 10.4218/etrij.05.0205.0031

[2] H. F. A. Amir, F. P. Chee, S. Salleh, "Effects of High Energy Neutrons and Resulting Secondary Charged Particles on the Operation of MOSFETs," *Computational Science and Technology (ICCST), 2014 International Conference*, pp. 1-6, 2014.

[3] J. R. Schwank, M. R. Shaneyfelt, D. M. Fleetwood, et al., "Radiation Effects in MOS Oxides," *IEEE Trans. Nuclear Science*, Vol. 55, no. 4, pp. 1833-1853, 2008.

[4] F. B. McLean, H. E. Boesch Jr., and T. R. Oldham, "Electron-hole generation, transport, and trapping in SiO_2," in *Ionizing Radiation Effects in MOS Devices and Circuits*, T. P. Ma and P. V. Dressendorfer, Eds. New York: Wiley, 1989, pp. 87–192.

[5] F. B. McLean and T. R. Oldham, "Basic Mechanisms of Radiation Effects in Electronic Materials and Devices," Harry Diamond Laboratory, Tech. Rep. HDL-TR-2129, 1987.

[6] P. J. McWhorter, S. L.Miller, and W. M. Miller, "Modeling the anneal of radiation-induced trapped holes in a varying thermal environment," *IEEE Trans. Nuclear Science*, vol. 37, no. 6, pp. 1682–1689, Dec. 1990.

[7] P. E. Dodd, M. R. Shaneyfelt, J. R. Schwank, J. A. Felix, "Current and Future Challenges in Radiation Effects on CMOS Electronics," *IEEE Trans. Nuclear Science*, vol. 57, no. 4, pp. 1747-1763, 2010.

[8] H. L. Hughes, J. M. Benedetto, "Radiation Effects and Hardening of MOS Technology: Devices and Circuits," *IEEE Trans. Nuclear Science*, vol. 50, no. 3, pp. 500-521, 2003.

[9] Prakash, AP Gnana, S. C. Ke, and K. Siddappa. "High-energy radiation effects on subthreshold characteristics, transconductance and mobility of n-channel MOSFETs," *Semiconductor science and technology*, vol. 18, no.12, pp. 1037-1042, 2003.

[10] K. W. Chew, K. S. Yeo, and S. F. Chu, "Impact of technology scaling on the 1/f noise of thin and thick gate oxide deep submicron NMOS transistors," *IEE Proc. Circuits Devices Syst.*, vol. 151, pp. 415–421, 2004.

[11] R. D. Schrimpf, K. M. Warren, R. A. Weller, R. A. Reed, et al., "Reliability And Radiation Effects in IC Technologies," *2008 IEEE International Reliability Physics Symposium*, pp. 97-106, 2008.

[12] T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron CMOS technology," *IEEE Trans. Nuclear Science*, vol. 43, no. 6, pp. 2874–2878, Dec. 1996.