

# Heterogeneous 3-D Sequential CFETs With Ge (110) Nanosheet p-FETs on Si (100) Bulk n-FETs

Seong Kwang Kim, *Member, IEEE*, Hyeong-Rak Lim, Jaejoong Jeong, Seung Woo Lee, Ho Jin Jeong, Juhyuk Park, Joon Pyo Kim, Jaeyong Jeong, *Graduate Student Member, IEEE*, Bong Ho Kim<sup>✉</sup>, *Graduate Student Member, IEEE*, Seung-Yeop Ahn, Youngkeun Park<sup>✉</sup>, Dae-Myoung Geum, *Member, IEEE*, Younghyun Kim<sup>✉</sup>, *Member, IEEE*, Yongku Baek, Byung Jin Cho, *Senior Member, IEEE*, and Sanghyeon Kim<sup>✉</sup>, *Member, IEEE*

**Abstract**—In this study, we report on the fabrication and characterization of 3-D sequential complementary field-effect-transistors (CFETs) using the direct wafer bonding (DWB) technology and a low-temperature process for monolithic 3-D (M3D) integration. The device features a high-performance top Ge (110)/(110) channel on a bottom Si CMOS. To ensure high performance without causing damage to the bottom Si n-FETs, the maximum thermal budget during the fabrication of the top Ge p-FETs was limited to 400 °C. We systematically investigated the mobility enhancement of the thin Ge (110) nanosheet (NS) channel p-FETs as a function of channel orientation. Our results demonstrate that the low effective hole mass along the ⟨110⟩ direction on Ge (110) wafer provides record-high mobility of 400 cm<sup>2</sup>/V·s (corresponding to 760 cm<sup>2</sup>/V·s when normalized by footprint) at room temperature, which is the highest reported among the Ge p-FETs with similar channel thicknesses.

**Index Terms**—Complementary field-effect-transistors (CFETs), Ge-OI, monolithic 3-dimensional (M3D), MOSFETs, wafer bonding.

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Seong Kwang Kim, Hyeong-Rak Lim, Jaejoong Jeong, Seung Woo Lee, Ho Jin Jeong, Juhyuk Park, Joon Pyo Kim, Jaeyong Jeong, Bong Ho Kim, Seung-Yeop Ahn, Youngkeun Park, Yongku Baek, Byung Jin Cho, and Sanghyeon Kim are with the School of Electrical Engineering, KAIST, Daejeon 34141, South Korea (e-mail: shkim.ee@kaist.ac.kr).

Dae-Myoung Geum is with the School of Electronics Engineering, Chungbuk National University, Cheongju-si, Chungcheongbuk-do 28644, South Korea.

Younghyun Kim is with the Department of Photonics and Nanoelectronics, Hanyang University ERICA, Ansan, Gyeonggi-do 15588, South Korea.

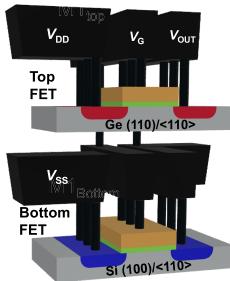
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## I. INTRODUCTION

MONOLITHIC 3-dimensional (M3D) integration technology has become a topic of great interest in recent years due to its potential to revolutionize the semiconductor industry. In conventional two-dimensional (2-D) integrated circuits, transistors are fabricated on a single layer of silicon, and interconnections are made between different blocks using metal wires. However, as the density of transistors and interconnects increases, power consumption and delay time become significant challenges. M3D integration technology is a promising solution to overcome these limitations by vertically stacking multiple layers of transistors, resulting in a significant reduction in wire length. This minimizes various parasitic resistance and capacitance and reduces power consumption by the short metal wires. In this line, the international roadmap for devices and systems (IRDSs) has proposed a new device architecture of 3-D very large scale integration (VLSI) circuits, involving sequential integration/fine-pitch stacking of logic, memory, non-volatile memory (NVM), analog, input/output (IO), and RF sensors [1]. The IRDS suggests two technologies for pursuing long-term alternative solutions to the technology addressed in more-than-Moore. These are extending the functionality of the CMOS platform through 3-D integration or stimulating the invention of new information processing paradigms [2]. In this respect, many researchers have actively developed vertically stacked devices, such as M3D integrated photonic devices, RF devices, and logic applications [3], [4], [5], [6].

Especially, for logic application, recent studies have reported outstanding performance of 3-D sequential complementary field-effect-transistors (CFETs) using a Si/Ge hybrid channel, outperforming all-Si channel devices [7], [8]. The 3-D sequential CFETs offer several advantages over conventional 2-D CMOS chips. First, the shorter interconnection length results in reduced power consumption and delay time. Second, the smaller form factor and higher integration density of devices lead to a significant reduction in chip area and cost, as shown in Fig. 1. A recent study reported that 3-D sequential CFETs can decrease the chip area and cost by 45% and 50%, respectively, compared to 2-D CMOS chips [9]. To realize the



● **Advantage of M3D Sequential CFET**

- Shorter interconnecting wires
- Less power consumption
- Less interconnection delay
- Less chip area and cost

● **Requirement of top devices**

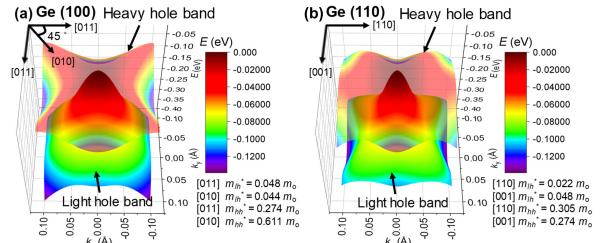
- Single crystal channel
- Low temperature channel formation
- Low temperature fabrication process
- Good performance

**Fig. 1.** Schematic of the heterogeneous 3-D sequential CFETs using Ge (110) nanosheet as top-tier channel and Si (100) as bottom-tier channel for high performance.

3-D sequential CFETs with these advantages, an appropriate channel transfer technique for a single crystal channel must be used to guarantee small device-to-device variation and high performance. Furthermore, a low-temperature process ( $<500^{\circ}\text{C}$ ) is necessary to achieve high performance in top-tier devices and prevent performance degradation in bottom-tier devices. In this respect, Ge is expected to be one of the most attractive channel materials for the next-generation p-FETs in 3-D sequential CFETs, due to its excellent carrier transport properties and low-temperature fabrication ( $<400^{\circ}\text{C}$ ), which have been proven by other studies using Ge (100) channel [6], [8].

Moreover, hole mobility is a critical parameter in determining the performance of logic applications due to its being three-times lower than electron mobility in Si. One of the primary factors that affects hole mobility in Si substrates is the surface orientation. Especially, the (110) surface orientation has received significant attention due to its valence band anisotropy with small effective mass ( $m^*$ ) at (110) channel orientation [10], [11], [12], [13], [14], [15], [16]. This circumstance has the same effect on Ge, where the (110) channel orientation in the (110) surface orientation has been shown to have a small  $m^*$  due to the anisotropic shape of the valence band [17]. Using the characteristics of Ge, we expect a further increase in hole mobility to minimize the gap with electron mobility. Dissanayake et al. [18] systematically analyzed the hole mobility according to channel orientations on the Ge (110) surface orientation using a condensation technology for the formation of the Ge (110) channel. While this technology is effective for obtaining pure Ge, its high process temperature of up to  $1100^{\circ}\text{C}$  makes it unsuitable for the fabrication of 3-D integrated devices [19].

Therefore, in this work, we focused on 3-D integration to pursue future CMOS platforms by transferring high-quality Ge (110) channel layer onto the bottom-tier CMOS wafer using heteroepitaxy and wafer bonding technology at low temperatures to avoid thermal damage. Especially, 3-D sequential CFETs with top Ge p-FETs and bottom Si n-FETs have a strong advantage for high carrier mobility to introduce heterogeneous integration of individually optimized surface and channel orientation for higher electron and hole mobility at the Si and Ge channels. It also has the strong advantage of maximizing the electrical characteristics by applying individually optimized fabrication processes. Finally, we first demonstrated Ge (110)/<110> on Si (100)/<110> heterogeneous channels for 3-D sequential CFETs by direct wafer bonding (DWB) technology using low-temperature process.



**Fig. 2.** Calculated valence band structure of (a) Ge (001) and (b) (110) surface orientation with 3-D band structure of HH and LH.

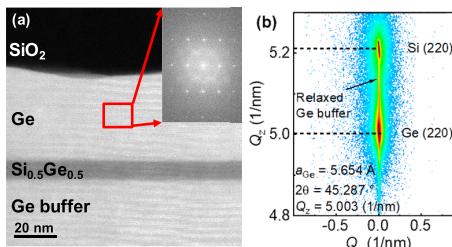
## II. MOTIVATION OF GE (110) CHANNEL

First, we calculated the valence band shape of (100) and (110) surfaces in Ge to evaluate the degree of valence band anisotropy with respect to direction using  $6 \times 6$  Hamiltonian-based  $k \cdot p$  method. Fig. 2(a) and (b) shows the 3-D valence band structure of Ge (001) and (110) substrates, respectively, revealing a sharper light hole (LH) band of Ge (110) substrate compared to the Ge (001) substrate. For intuitive observation, the LH band of the Ge (001) substrate has almost uniform LH effective mass ( $m_{lh}^*$ ) in all transport directions, whereas the energy band of LH in the Ge (110) substrate has a lighter  $m_{lh}^*$  in the transport direction of [110] compared to [001]. Additionally,  $m_{lh}^*$  in Ge (110)/[110] is 2 times smaller than that in Ge (100), while  $m_{lh}^*$  in (100) and that in Ge (110)/[001] are comparable. Fig. 2(e) and (f) shows the top-view images of the heavy hole (HH) band in Ge (001) and (110) substrates, respectively, showing HH effective mass ( $m_{hh}^*$ ) with no significant difference. These results strongly suggest that optimizing the carrier transport direction, where LH mass becomes smaller, can potentially improve mobility for high-performance logic applications. Therefore, the introduction of Ge (110)/[110] channel p-FETs in the top-tier could provide the optimal combination for high-performance 3-D sequential CFETs with Si (100)/[110] channel of the bottom-tier n-FETs, which are presently used in the industry.

## III. CHARACTERIZATION OF GE (110)-OI WAFERS

There are several techniques to fabricate thin Ge-on-insulator (-OI) structures, such as Smart cut [20], Ge condensation [21], liquid-phase epitaxy [22], and DWB [23]. Among these techniques, the DWB technology is particularly advantageous for top-tier channel formation in M3D since it enables the transfer of high-quality Ge films without implantation damage or high thermal budget. Furthermore, the DWB technology has the benefit of enabling back interface engineering, which can help reduce mobility degradation in a thin channel thickness. Ge (110) on CMOS wafer was fabricated by DWB. Epitaxial layers were grown Ge (45 nm)/Si<sub>0.5</sub>Ge<sub>0.5</sub>(10 nm)/Ge (900 nm) on Si wafer. Here, the top Ge serves as a channel layer, the Si<sub>0.5</sub>Ge<sub>0.5</sub> acts as an etching stop layer for the back substrate etching process, and the bottom Ge layer plays a role as a relaxed buffer layer to reduce defect density near the surface. To evaluate the film quality, we measured scanning transmission electron microscopy (STEM) for the epitaxially grown Ge on Si wafer.

Fig. 3(a) showed the cross-sectional STEM images of as-grown Ge (110) substrate, showing the intended Ge/Si<sub>0.5</sub>Ge<sub>0.5</sub>/Ge buffer structure. The inset of Fig. 3(a) clearly



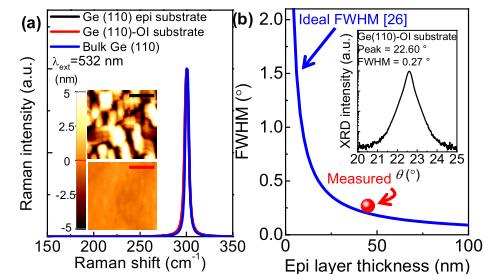
**Fig. 3.** (a) Cross-sectional STEM image of Ge (110) epitaxial grown wafer, which inset shows the diffraction pattern of Ge (110) channel and epi. (b) XRD RSM image of Ge (110) grown on Si (110) substrate, which clearly shows the peaks of Ge (220) and Si (220).

showed the diffraction pattern of the Ge channel. Moreover, Fig. 3(b) showed X-ray diffraction (XRD) reciprocal space map (RSM) image of Ge (110) grown on a Si (110) wafer, which indicates that the grown Ge buffer layer was fully relaxed and its lattice matched the lattice constant of Ge. Based on the obtained lattice constant, the calculated Ge lattice constant of 5.654 Å at the maximum peak point of Ge (220) was almost the same as the ideal lattice constant of 5.66 Å, indicating that the growth on Si (110) substrate was successful, and a high-quality channel of Ge (110) had grown well on Si (110) substrate.

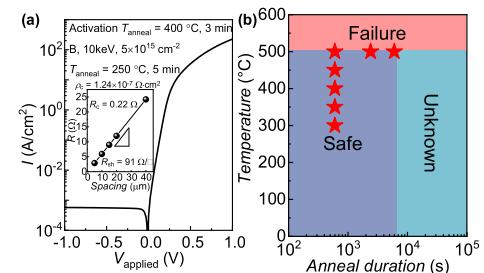
After bonding between epitaxially grown Ge on Si and CMOS wafer, we performed etch process using an ammonia peroxide mixture with a remarkable selectivity ratio of 400:1 between Ge and  $\text{Si}_{0.5}\text{Ge}_{0.5}$  [24]. More details for the fabrication process of Ge on CMOS wafer can be found in [25]. To evaluate the quality of the transferred Ge (110) channel, Raman spectra were measured for the bulk (110) wafer, Ge (110) grown on Si wafer, and Ge (110)-OI wafer, as shown in Fig. 4(a). The inset of Fig. 4(a) shows the atomic force microscopy (AFM) images of top-channel surface for Ge (110) epitaxial substrate and Ge (110)-OI substrate with  $R_{\text{RMS}}$  of 3.24 and 0.25 nm, respectively. In the future, to introduce a gate-all-around channel structure, there is a need to further optimize Ge channel growth technology to mitigate surface roughness. The transferred Ge (110) layer and Ge (110) grown on the Si (110) wafer exhibited a sharp peak and no peak shift from the bulk Ge (110) wafer, indicating no strain in the Ge (110) layer after the transfer. Furthermore, we obtained a sharp peak of Ge (110)-OI wafer at 22.6°, confirming the high-quality growth of the Ge layer with (110) surface orientation, as shown in the inset of Fig. 4(b). In addition, Fig. 4(b) showed that the full-width half-maximum (FWHM) of the Ge (110) peak was measured, and the measured FWHM from the Ge (110)-OI wafer was plotted with the ideal FWHM from the Scherrer equation of the Ge (110) layer as a function of the thickness [26], which indicates nearly perfect layer quality of the transferred Ge (110) layer using the DWB technology.

#### IV. CHARACTERIZATION OF GE (110)-OI p-FETs WITH CHANNEL ORIENTATION AND TEMPERATURE DEPENDENCE

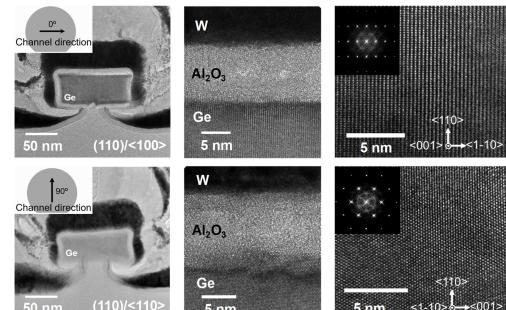
More details for the fabrication process of Ge (110)-OI p-FETs can be found in [25]. We achieved a useful level of contact resistance of  $1.24 \times 10^{-7} \Omega \cdot \text{cm}^2$ , as shown in the inset of Fig. 5(a). Prior to device stacking, we evaluated the



**Fig. 4.** (a) Raman spectra of bulk Ge (110), Ge (110)-OI wafer, and Ge (110) epitaxial wafer. Inset shows the AFM images of the Ge (110) channel surface before and after wafer bonding with  $R_{\text{RMS}}$  of 3.24 and 0.25 nm, respectively. (b) Comparison between ideal FWHM and measured FWHM, which inset shows XRD spectra of fabricated Ge (110)-OI wafer.



**Fig. 5.** (a)  $I$ - $V$  characteristics of  $p^+$ - $n$  diode with activation process at  $400^\circ\text{C}$ . (b) Process window of bottom-tier devices by rapid thermal annealing equipment.

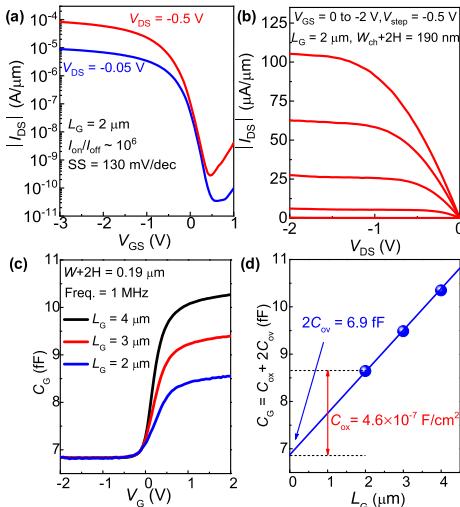


**Fig. 6.** TEM images of fabricated Ge (110)-OI p-FETs. It shows gate-stack clearly.

potential for thermal degradation of the bottom-tier devices with poly-Si/SiON/Si as the gate-stack and CoSi silicide as the S/D at the process temperature of top-tier devices in the rapid thermal annealing (RTA). The investigation allowed us to establish a process window for the thermal stability of the bottom devices, as depicted in Fig. 5(b). Our finding indicates that the bottom devices can withstand thermal annealing up to  $500^\circ\text{C}$  for 60 min without any significant degradation by thermal damage.

The cross-sectional transmission electron microscopy (TEM) images showed Ge (110)-OI p-FETs with the nanosheet (NS) channel, as shown in Fig. 6. The images clearly confirmed the distinction between the gate metal, oxide, and Ge (110) channel.

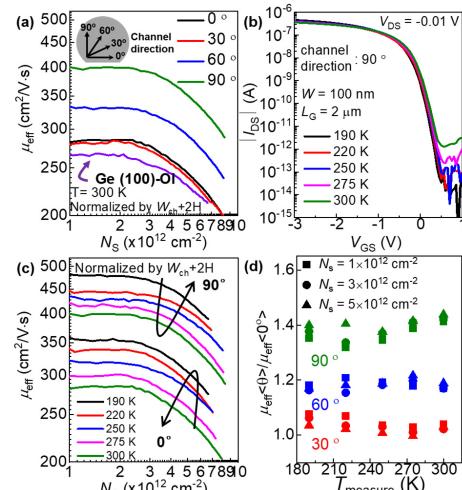
Additionally, to experimentally verify the anisotropic shape of the valence band in the Ge (110) channel, the channel orientation of  $0^\circ$ ,  $30^\circ$ ,  $60^\circ$ , and  $90^\circ$  were defined, where  $0^\circ$  corresponds to  $\langle 100 \rangle$  channel orientation and  $90^\circ$  corresponds to  $\langle 110 \rangle$  channel orientation. The TEM images showed well-defined  $\langle 100 \rangle$  and  $\langle 110 \rangle$  channel orientation of the Ge



**Fig. 7.** (a) Transfer curves and (b) output curves of Ge (110)-OI p-FETs with (110) channel orientation. (c) C–V characteristics of Ge (110)-OI p-FETs with various gate lengths. (d) Extraction of  $C_{ov}$  using measured C–V curves to obtain pure  $C_{ox}$  for mobility calculation.

channel at the (110) surface orientation as depicted in the diffraction pattern.

Electrical characterization was performed on the fabricated Ge (110)-OI p-FETs. Fig. 7(a) and (b) depicted the transfer and output characteristics of Ge (110)/(110)-OI p-FETs with a gate length ( $L_g$ ) of 2  $\mu\text{m}$ . The obtained  $I$ – $V$  curves clearly showed a current increase with width shown in the inset, a sub-threshold swing of 130 mV/dec, high  $I_{on}/I_{off}$  ratio ( $\sim 10^6$ ), and clear current saturation in output curves. Fig. 7(c) showed the capacitance–voltage (C–V) characteristics of Ge (110)-OI p-FETs with several gate lengths at 1 MHz. We extracted the overlap capacitance ( $C_{ov}$ ), which was performed using measured C–V curves in order to obtain the pure gate oxide capacitance ( $C_{ox}$ ) for mobility calculation. The elimination of gate-to-source/drain  $C_{ov}$  was achieved through linear extrapolation for the gate length according to several gate lengths. Finally, we obtained  $C_{ox}$  of  $4.6 \times 10^{-7} \text{ F/cm}^2$  except for  $C_{ov}$ , which is apparently low capacitance considering the thickness of  $\text{Al}_2\text{O}_3$  of 10 nm. This is attributed to the formation of  $\text{GeO}_x$  through preplasma oxidation for improving interface quality. Additionally, to investigate the effective field-effect mobility ( $\mu_{eff}$ ) according to the channel direction,  $\mu_{eff}$  of the devices was evaluated by tilting 30°, 60°, and 90° from the flat zone, as shown in Fig. 8(a). The highest  $\mu_{eff}$  of 400  $\text{cm}^2/\text{V}\cdot\text{s}$  at sheet charge density ( $N_s$ ) =  $1 \times 10^{12} \text{ cm}^{-2}$  was achieved along the (110) channel orientation, which was 1.4 times higher than that of Ge (110)/(100)-OI p-FETs and 1.5 times higher than that of Ge (100)/(110)-OI p-FETs at room temperature. The electrical characteristics for Ge channel with (110) surface orientation experimentally showed that the hole mobility has higher mobility characteristics in the (110)/(110) channel due to the strong anisotropic shape of the valence band, as depicted in Fig. 2, which indicates mobility enhancement would be possible through surface orientation engineering without any process modification by transferring the channel with small  $m^*$ s considering the operating direction. Moreover, surface and channel orientation engineering are highly effective in NS structure, whereas hole mobility decreases rapidly in the high



**Fig. 8.** (a) Mobility curves for channel orientation dependence with 0°, 30°, 60°, 90°, and Ge (100)/(110) channel orientation at 300 K. (b) Transfer curves with temperature dependence with channel orientation of Ge (110)/(110) with several temperatures of 190, 220, 250, 275, and 300 K. (c) Mobility curves with temperature dependence and channel orientation of Ge (110)/(100) and Ge (110)/(110). (d) Mobility enhancement factor of channel orientations.

$N_s$  region. This reduction occurs at the high density of the interface trap ( $D_{it}$ ) inside the valence band [27]. As a result, it is important to reduce  $D_{it}$  inside valence band to prevent from degrading mobility at the high  $N_s$  region. To reduce  $D_{it}$  inside the valence band, researchers have pursued approaches, such as ozone oxidation [28], oxidizing post deposition annealing (PDA) [29] for optimizing quality and thickness of  $\text{GeO}_x$ , and so on. We expect to implement these strategies to achieve devices with improved interface characteristics.

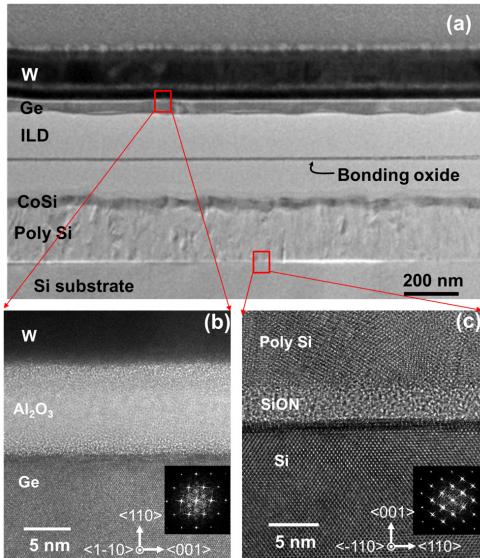
Furthermore, we investigated the temperature dependence of the  $\mu_{eff}$  enhancement for channel direction to access the mechanism. Fig. 8(b) showed the transfer curves with various temperatures. As the temperature decreases, the off current decreases and threshold voltage ( $V_T$ ) tends to shift negatively.  $\mu_{eff}$  characteristics of the temperature dependence in the (110)/(100) and (110)/(110) directions are shown in Fig. 8(c). As the temperature decreases, reduced phonon scattering leads to an  $\mu_{eff}$  enhancement. We extracted  $\mu_{eff}$  using the following equation:

$$I_{DS} = \mu_{eff} C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS} \quad (1)$$

where  $\mu_{eff}$ ,  $W$ ,  $L$ ,  $V_{GS}$ ,  $V_T$ , and  $V_{DS}$  are the effective mobility, width and length of devices, applied gate voltage, threshold voltage, and applied drain voltage, respectively. Our devices did not have substrate contact by ON-insulator structure. Hole carrier density ( $Q_h$ ) was defined by (2) [30]. We extracted  $C_{ox}$  by fabricating Ge metal-insulator-semiconductor (MIS) capacitor with the same process of the Ge p-FETs to exclude the parasitic capacitances, as shown in the inset of Fig. 8(b)

$$Q_h = C_{ox} (V_{GS} - V_T). \quad (2)$$

We extracted  $\mu_{eff}$  enhancement factor for channel direction and temperature dependence at  $N_s = 1 \times 10^{12}$ ,  $3 \times 10^{12}$ , and  $5 \times 10^{12} \text{ cm}^{-2}$  in Fig. 8(d). The  $\mu_{eff}$  enhancement factor was almost constant depending on the channel direction at

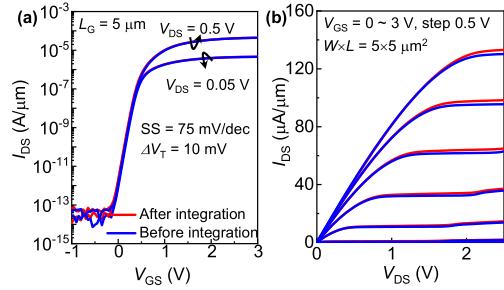


**Fig. 9.** (a) TEM images of heterogeneous 3-D sequential CFETs with top-tier Ge (110) p-FETs on bottom-tier Si (100) n-FETs. The gate-stack of (b) top- and (c) bottom-tier devices was clearly confirmed. In addition, the carrier transport direction Ge (110) and Si (100) was aligned in the (110) direction.

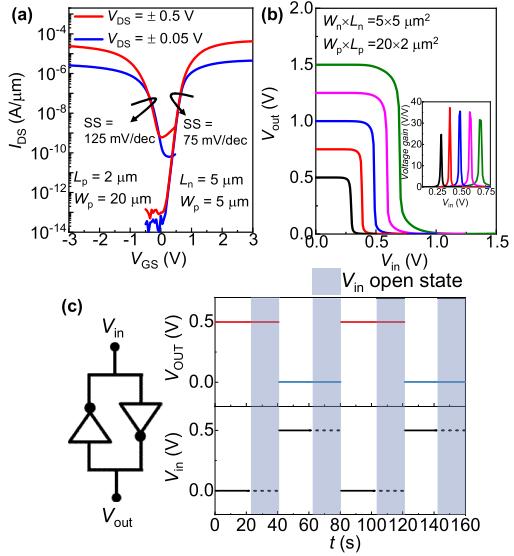
each temperature and  $N_s$ , indicating a correlation between  $m^*$  modulation and  $\mu_{\text{eff}}$  anisotropy according to the channel direction. It also suggests that  $\mu_{\text{eff}}$  enhancement is attributed to the effective mass modulation, which shows the constant  $\mu_{\text{eff}}$  enhancement regardless of the dominant carrier scattering mechanism. We obtained the enhancement factor that  $\mu_{\text{eff}}$  of <110> direction is approximately 1.4 times higher than that of <100> direction in (110) surface orientation at measured temperature dependence. Dissanayake et al. [18] reported channel direction, effective field, and temperature dependencies of hole mobility in Ge (110)-OI p-channel MOSFETs in large width (100  $\mu\text{m}$ ) devices by Ge condensation technique, which showed a mobility enhancement factor that  $\mu_{\text{eff}}$  of <110> direction is approximately 1.9 times higher than that of <100> direction in (110) surface orientation at 4 K. We believe that our device width is much smaller than that of the reported device, indicating that the mobility of the side wall is expected to decrease due to the plane direction of (100)/(110) at the sidewall, which is different from that of (110)/(110) at the top surface.

## V. THREE-DIMENSIONAL SEQUENTIAL CFETs COMPOSED OF GE (110) p-FETs ON TOP OF SI (100) n-FETs

Based on the findings above, we fabricated Ge (110) p-FETs as the top-tier device on Si (100) bulk n-FETs. Fig. 9(a) showed the cross-sectional TEM images of the fabricated 3-D sequential CFET, showing W/Al<sub>2</sub>O<sub>3</sub>/Ge/ILD/CoSi/Poly-Si/SiON/Si substrate structure. It is evident that the top- and bottom-tier devices are well positioned without any void at bonding interface. Fig. 9(b) and (c) showed the gate stacks of the top- and bottom-tier devices, respectively. The Ge (110) channel of the top-tier devices and Si (100) channel of bottom-tier devices were aligned in <110> channel orientation, respectively, which indicates that a high mobility channel



**Fig. 10.** (a) Transfer curve and (b) output curves of bottom-tier devices before and after 3-D sequential integration.



**Fig. 11.** (a) Transfer curves of bottom- and top-tier devices after 3-D sequential integration. (b) Voltage transfer curves of 3-D sequential CFETs. Inset shows quite a good voltage gain. (c) Transient curves of cross-coupled inverter for applicable SRAM operation.

with a specific surface and channel orientation is relatively easily stackable by using DWB technology. To investigate the electrical properties of the bottom Si n-FET, we measured the transfer and output curves before and after integration of the Ge (110)-OI p-FETs shown in Fig. 10. There was no significant difference in the  $I-V$  curves before and after the integration process, which means the maximum temperature of 400 °C during the process of the top-tier devices did not affect the bottom-tier devices. Fig. 11(a) showed the transfer characteristics of the 3-D sequential CFETs with Ge (110) p-FETs on Si (100) n-FETs. There is a big difference in SS performance between the top- and bottom-tier devices. To reduce the difference in SS, high- $k$  dielectric should be used for Ge p-FETs. However, using high- $k$  dielectric materials to reduce the SS poses a challenge for Ge channel compatibility. To address this issue, various studies have focused on improving the electrical performance by passivating the Ge channel with Si prior to high- $k$  dielectric deposition.

In particular, Laboratory in Belgium (IMEC) has actively studied Si growth on the Ge channel [31], [32]. Taking inspiration from these studies, Foundry Company in Taiwan (TSMC), research groups at Tokyo university, and others have demonstrated the potential for improved electrical performance through Si passivation of the Ge channel, as evidenced by the research papers [33], [34]. We expected that incorporating

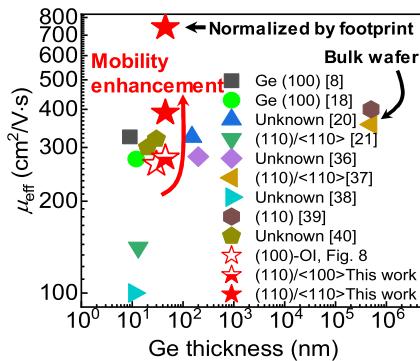


Fig. 12. Benchmark for  $\mu_{\text{eff}}$  as function of Ge channel thickness in case of pure Ge and no strain Ge channel.

this technology into our devices will have better electrical properties.

In addition, the Ge (110) p-FETs showed insufficient electrical properties, such as subthreshold swing and ON and OFF current compared to that of Si n-FETs; however, this is expected to be overcome by changing the gate oxide materials with high- $k$  characteristics for subthreshold swing. Also, we think that the electrical performance of Ge p-FETs is limited by unoptimized S/D resistance. By overcoming this drawback such as NiGe alloy with  $\sim 10^{-9} \Omega \cdot \text{cm}^2$  of  $\rho_c$ , we expect that it is possible to integrate the devices of top-tier Ge p-FETs and bottom-tier Si n-FETs with similar dimension. Additionally, we believe that the limitations can be overcome by introducing a large effective bandgap through the much more confinement by width and thickness scaling, which can be controlled within the OFF current limits specified by the IRDS requirement for both high-performance ( $100 \text{ nA}/\mu\text{m}$ ) and high-density application ( $100 \text{ pA}/\mu\text{m}$ ) at a supply voltage of  $0.65 \text{ V}$  [1], [33], [35]. Fig. 11(b) showed the voltage transfer curves of the corresponding 3-D sequential CFETs, demonstrating a well-behaved response to low  $V_{\text{in}} = 0.5 \text{ V}$ , which means that low power consumption is possible through 3-D sequential CFETs by  $V_{\text{in}}$  scaling through using optimized high mobility channels with Ge (110)/(110) p-channel and Si (100)/(110) n-channel. In addition, a decent level of voltage gain was depicted in the inset of Fig. 11(b). Additionally, we measured cross-coupled inverter for an applicable static random access memory (SRAM) in Fig. 11(c), which illustrated the transient characteristics for functionality. The bistable output logic can be maintained at the open input terminal, realizing the basic SRAM function.

Finally, Fig. 12 showed the benchmark for  $\mu_{\text{eff}}$  as a function of Ge channel thickness among pure Ge channel p-FETs without strain effects, indicating that channel orientation engineering in this work provides a record high value at a similar thickness range, which means that the potential of wafer bonding technique for M3D integration can be realized by transferring high mobility channel. Table I highlighted the benefits of Ge (110) on top of Si (100) channel heterogeneous 3-D sequential CFETs based on the DWB-based layer transfer process with high mobility channel transfer without any process modification and degradation of performance for bottom devices via low thermal budget ( $400 \text{ }^\circ\text{C}$ ).

TABLE I  
BENCHMARK OF 3-D STACKED DEVICES WITH PREVIOUS STUDIES FOR CFETS

Ref.	[6]	[7]	[8]	[41]	[42]	This work
Top device	Ge (111) n-FET	Si n-FET	Ge p-FET	Si p-FET	Ge p-FET	Ge (110) pFET
Bottom device	Ge (100) p-FET	Si p-FET	Si n-FET	GaN n-FET	Si n-FET	Si nFET
Technique for top channel bonding	Wafer bonding	Epitaxial growth	Smart cut	Wafer bonding	Wafer bonding	Wafer bonding
Thermal budget	$250 \text{ }^\circ\text{C}$	$670 \text{ }^\circ\text{C}$	$600 \text{ }^\circ\text{C}$	-	$400 \text{ }^\circ\text{C}$	$400 \text{ }^\circ\text{C}$
3D CFETs scheme	Monolithic	Monolithic	Sequential	Sequential	Monolithic	Sequential
Back interface engineering	Possible	Impossible	Possible	Possible	Possible	Possible
Orientation engineering	(111) nFET possible	Impossible	possible	possible	possible	(110) pFET possible

## VI. CONCLUSION

We demonstrated a 3-D sequential CFET using Ge (110) channel with high hole  $\mu_{\text{eff}}$  for high-performance logic application employing the DWB-based low-temperature layer transfer process and Ge (110)/(110) channel. We systematically investigated the behavior of  $\mu_{\text{eff}}$  according to channel orientation and temperature dependence. We obtained high  $\mu_{\text{eff}}$  of  $400 \text{ cm}^2/\text{V}\cdot\text{s}$  ( $760 \text{ cm}^2/\text{V}\cdot\text{s}$  normalized by foot print) at room temperature in the  $\langle 110 \rangle$  channel orientation due to the strong anisotropic shape of the valence band in Ge (110)/(110) channel, which was much higher mobility than that of Ge (110)/(100) and Ge (100). Finally, based on the above findings, we demonstrated high-performance 3-D sequential CFETs using optimized direction of the Ge (110)/(110) and Si (100)/(110) channel and DWB technology without any process modification to maintain channel direction and without degradation of bottom-tier devices by low process temperature during the fabrication of top-tier devices. These results are expected to have a great impact on the electronic industry from the perspective of low power consumption and a small form factor in the future.

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