

# MARMARA UNIVERSITY – FACULTY OF ENGINEERING

## LABORATORY ASSIGNMENT #2 REPORT



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## CPU DESIGN

We have designed 8-bit CPU with 4-bit opcode. It is designed for only L-type instructions. It has 7 components as shown below. This processor receives instruction from us as input. Gives us output in 4 ways. The first is with 7-segment driver. After each operation the value in accumulator is seen on this driver. In addition, Flag register values, PC value and current clock cycle are indicated by the LEDs on the FPGA on which we will install our processor. For this, we assign the appropriate output values to the correct LED pins.

```
1 module cpu_2(  
2  
3     input [3:0] opcode,  
4     input [7:0] data,  
5     input clk,  
6  
7     output c,  
8     output z,  
9     output n,  
10    output ov,  
11    output f,  
12    output d,  
13    output e,  
14    output [7:0] pc_address,  
15    output [6:0] seg0,  
16    output [6:0] seg1,  
17    output [6:0] seg2,  
18    output [6:0] seg3  
19 );  
20  
21 //CU  
22 control_unit(clk,f,d,e);  
23 //PC  
24 eight_bit_counter(clk,f,1'b1,pc_address);  
25  
26 //INSTRUCTION REGISTER  
27 wire [11:0] opcode_data;  
28 twelve_bit_instruction_register({opcode,data},d,1'b1,clk,opcode_data);  
29  
30 //ALU  
31 wire [7:0] result;  
32 wire [7:0] acc_result;  
33 wire cw,zw,nw,ovw;  
34 eight_bit_alu(opcode_data[11:8],opcode_data[7:0],acc_result,result,cw,zw,nw,ovw);  
35  
36 //FLAG REGISTER  
37 flag_register({cw,zw,nw,ovw},e,1'b1,clk,{c,z,n,ov});  
38  
39 //ACCUMULATOR  
40 eight_bit_accumulator(result,e,1'b1,clk,acc_result);  
41  
42 //SEVEN SEGMENT  
43 seven_segment(clk,acc_result,seg0,seg1,seg2,seg3);  
44  
45  
46 endmodule  
47
```

Figure-1: Verilog Code for the 8-bit CPU

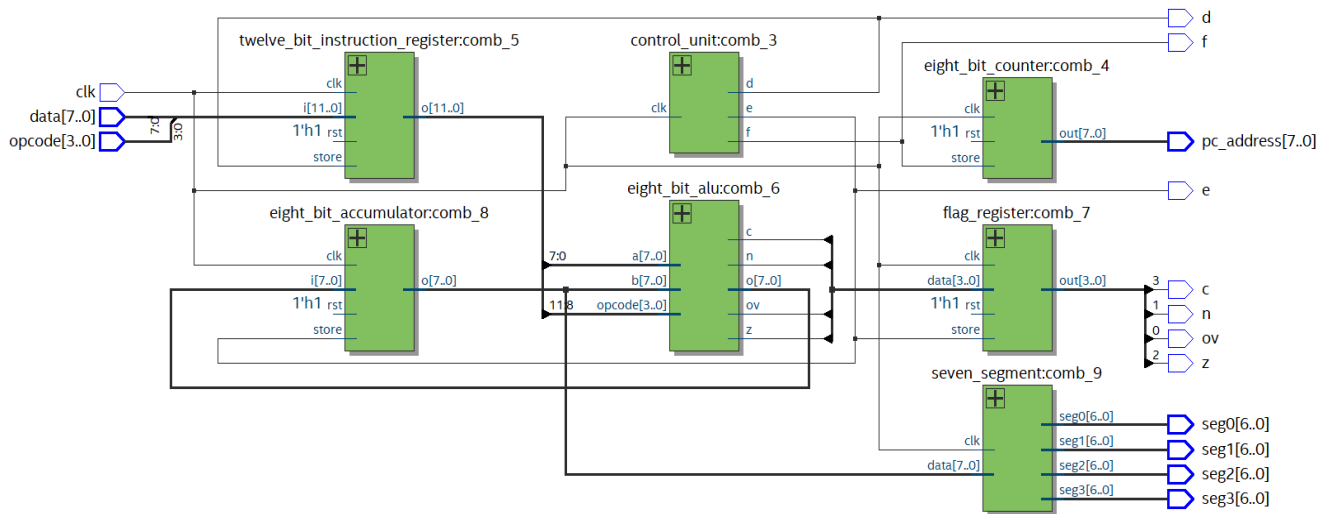


Figure-2: RTL View for the 8-bit CPU

## COMPONENTS FOR CPU

### 8-BIT ALU

We had designed the 8-bit ALU for the previous lab project so the details about the ALU available there.

### CONTROL UNIT

We control 3 clock cycles with the Control Unit. These three cycles are Fetch, Decode and Execute respectively. Each cycle signal is connected to an LED pin on the FPGA. The appropriate LED lights up according to which cycle is running. Control Unit is not in any clock cycle by default. It moves to the next cycle at every clock that comes to itself. In this way, it controls that the instruction is running correctly.

```

1  module control_unit(
2      input clk,
3      output reg f,
4      output reg d,
5      output reg e
6  );
7
8      reg [2:0] controlUnit;
9      always @(posedge clk)
10         begin
11             case (controlUnit)
12                 3'b000: controlUnit <= 3'b001;
13                 3'b001: controlUnit <= 3'b010;
14                 3'b010: controlUnit <= 3'b100;
15                 3'b100: controlUnit <= 3'b001;
16                 default: controlUnit <= 3'b000;
17             endcase
18         end
19
20         always @(*)
21         begin
22             case (controlUnit)
23                 3'b001: begin
24                     f <= 1'b1;
25                     d <= 1'b0;
26                     e <= 1'b0;
27                 end
28                 3'b010: begin
29                     f <= 1'b0;
30                     d <= 1'b1;
31                     e <= 1'b0;
32                 end
33                 3'b100: begin
34                     f <= 1'b0;
35                     d <= 1'b0;
36                     e <= 1'b1;
37                 end
38             default: begin
39                 f <= 1'b0;
40                 d <= 1'b0;
41                 e <= 1'b0;
42             end
43         endcase
44     end
45 endmodule

```

Figure-1: Verilog Code for Control Unit (1)

```

36         end
37     default: begin
38         f <= 1'b0;
39         d <= 1'b0;
40         e <= 1'b0;
41     end
42 endcase
43 end
44 endmodule
45

```

Figure-2: Verilog Code for Control Unit (2)

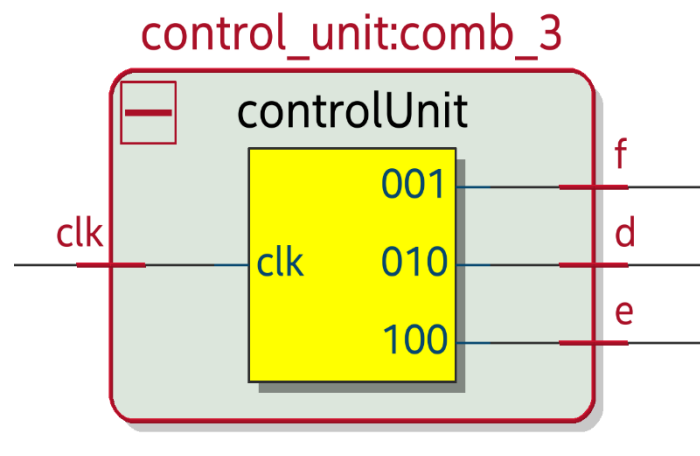


Figure-3: RTL View of Control Unit

## 8-BIT ACCUMULATOR

Accumulator is a register. We use an 8-bit accumulator for this processor. It consists of 8 1-bit registers. We keep the ALU results in this register. For the next operation, an input of the ALU comes from the accumulator.

```
1 module eight_bit_accumulator(  
2  
3     input [7:0] i,  
4     input store,  
5     input rst,  
6     input clk,  
7     output [7:0] o  
8 );  
9  
10    eight_bit_register(i,store,rst,clk,o);  
11  
12 endmodule
```

Figure-1: Verilog Code of 8-bit accumulator

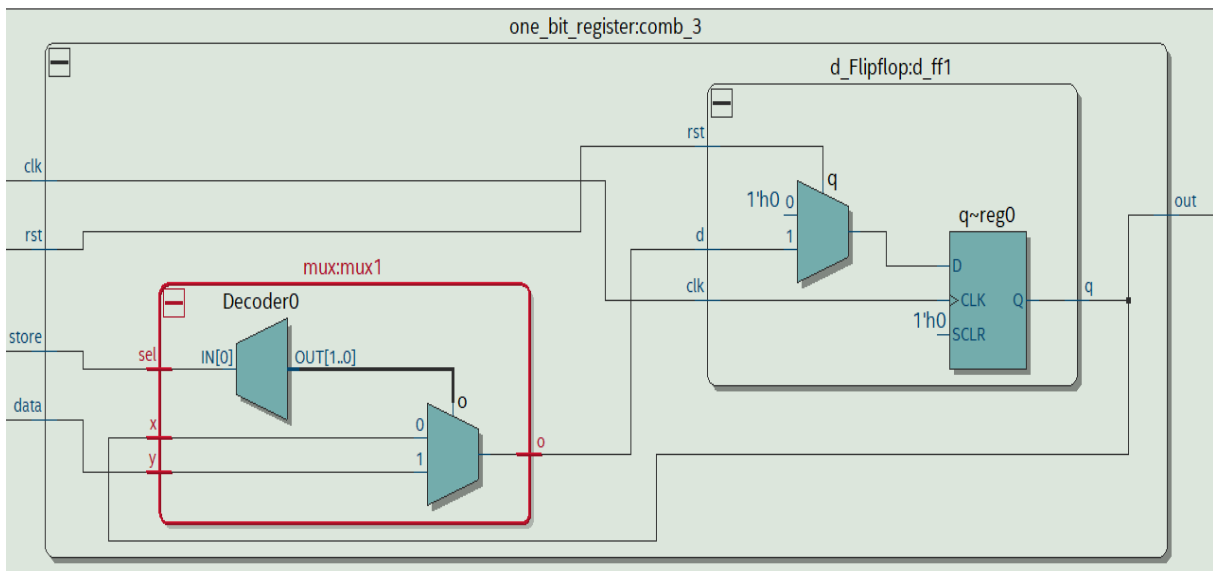


Figure-2: RTL View of 1-bit register



```

1  module twelve_bit_instruction_register(
2
3      input [11:0] i,
4      input store,
5      input rst,
6      input clk,
7      output [11:0] o
8  );
9      one_bit_register(i[11],store,rst,clk,o[11]);
10     one_bit_register(i[10],store,rst,clk,o[10]);
11     one_bit_register(i[9],store,rst,clk,o[9]);
12     one_bit_register(i[8],store,rst,clk,o[8]);
13     one_bit_register(i[7],store,rst,clk,o[7]);
14     one_bit_register(i[6],store,rst,clk,o[6]);
15     one_bit_register(i[5],store,rst,clk,o[5]);
16     one_bit_register(i[4],store,rst,clk,o[4]);
17     one_bit_register(i[3],store,rst,clk,o[3]);
18     one_bit_register(i[2],store,rst,clk,o[2]);
19     one_bit_register(i[1],store,rst,clk,o[1]);
20     one_bit_register(i[0],store,rst,clk,o[0]);
21
22
23  endmodule
24

```

Figure-1: Verilog Code of 12-bit Instruction Register



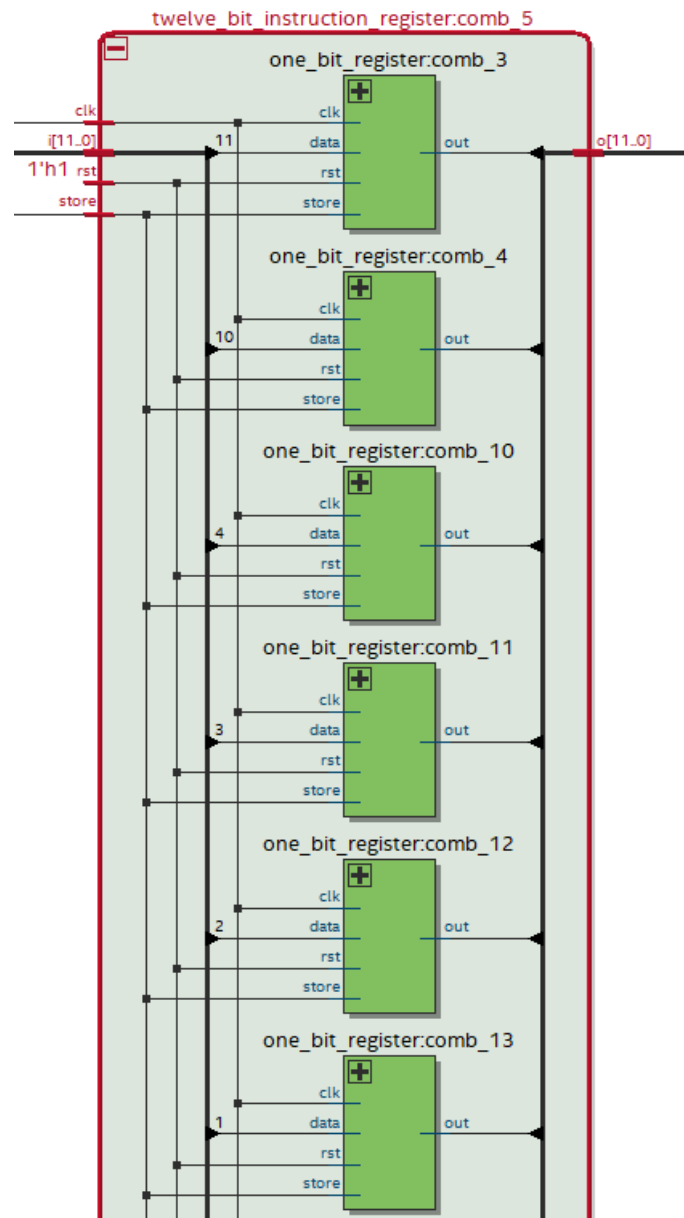


Figure-2: RTL View of 12-bit Instruction Register (1)

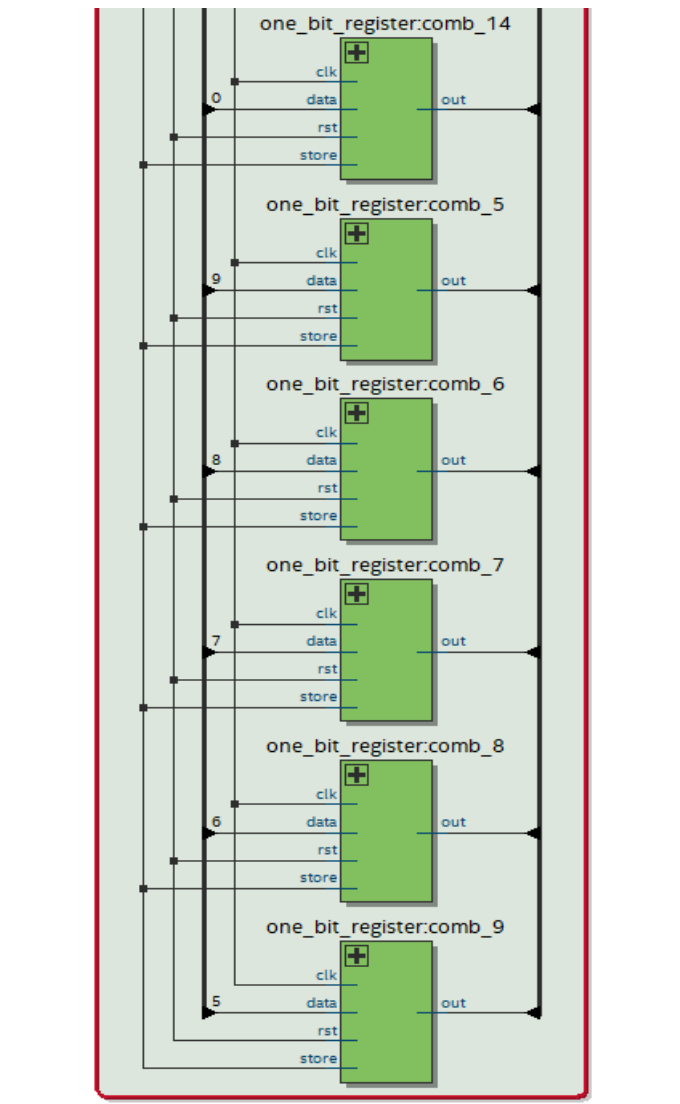


Figure-3: RTL View of 12-bit Instruction Register (2)

## 8-BIT PROGRAM COUNTER

A PC is a component that normally gives an instruction address. However, we do not use ROM in this processor, and the output from the PC is connected to the LED pins. It has an incrementer and its value increases by one after each fetch signal from the control unit.

```

1 module eight_bit_counter(
2     input clk,
3     input store,
4     input rst,
5     output reg [7:0] out
6 );
7     always @(posedge clk)
8     begin
9         if (store == 1'b1)
10        begin
11            if (!rst || out == 8'b11111111) out <= 8'b00000000;
12            else out <= out + 1'b1;
13        end
14    end
15 endmodule
16

```

Figure-1: Verilog Code of 8-bit Program Counter

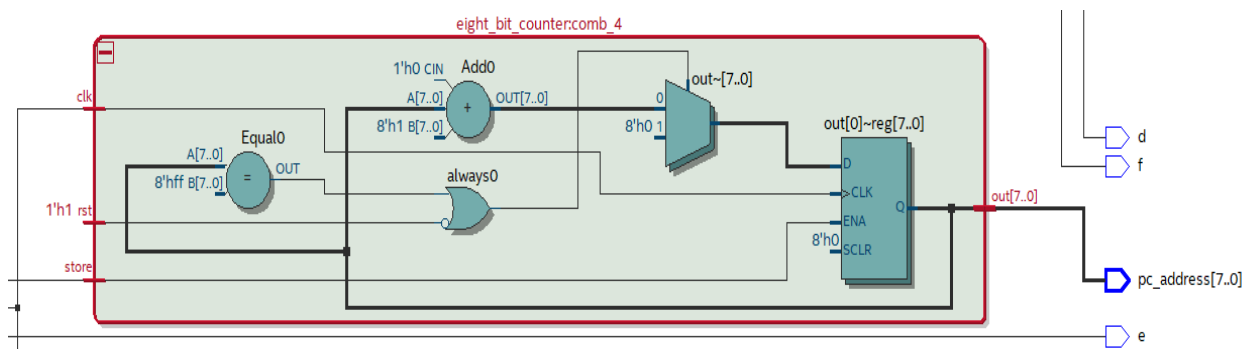


Figure-2: RTL View of 8-bit Program Counter

## 7-SEGMENT DRIVER

7-Segment Driver is connecting to the accumulator. In our processor, it is responsible for displaying the data in the accumulator. It analyzes the binary data it coming from acc, converts it to decimal and displays that decimal value.

```

1  module seven_segment(
2      input clk,
3      input [7:0] data,
4      output reg [6:0] seg0,
5      output reg [6:0] seg1,
6      output reg [6:0] seg2,
7      output reg [6:0] seg3
8  );
9
10     reg [7:0] temp;
11     reg sign;
12     reg [3:0] hundreds;
13     reg [3:0] tens;
14     reg [3:0] ones;
15
16     always @(posedge clk)
17     begin
18         temp = data;
19
20         //HUNDREDS
21         if (data[7] == 1) begin
22             sign = 1'b1;
23             temp = ~(data - 1'b1);
24         end
25         else begin
26             sign = 1'b0;
27         end
28
29         if (temp >= 100) begin
30             hundreds = 1;
31         end
32         else begin
33             hundreds = 0;
34         end
35     end
36

```

Figure-1: Verilog Code of 7-bit Segment Driver (1)

```

37
38
39 //TENS
40 temp = data - hundreds*100;
41
42 if (data[7] == 1) begin
43     temp = ~(data - 1'b1) - hundreds*100;
44 end
45
46
47 if (temp >= 90) begin
48     tens = 9;
49 end
50 else if (temp >= 80) begin
51     tens = 8;
52 end
53 else if (temp >= 70) begin
54     tens = 7;
55 end
56 else if (temp >= 60) begin
57     tens = 6;
58 end
59 else if (temp >= 50) begin
60     tens = 5;
61 end
62 else if (temp >= 40) begin
63     tens = 4;
64 end
65 else if (temp >= 30) begin
66     tens = 3;
67 end
68 else if (temp >= 20) begin
69     tens = 2;
70 end
71 else if (temp >= 10) begin
72     tens = 1;
73 end

```

Figure-2: Verilog Code of 7-bit Segment Driver (2)

```

73     else begin
74         tens = 0;
75     end
76
77     //ONES
78     ones = temp - tens*10;
79 end
80
81 always @(*)
82 begin
83
84     case (sign)
85         1'b0: seg0 = 7'b1000000;
86         1'b1: seg0 = 7'b0111111;
87         default: seg0 = 7'b1000000;
88     endcase
89
90     case (hundreds)
91         4'b0000: seg1 = 7'b1000000;
92         4'b0001: seg1 = 7'b1001111;
93         4'b0010: seg1 = 7'b0100100;
94         default: seg1 = 7'b1000000;
95     endcase
96
97     case (tens)
98         4'b0000: seg2 = 7'b1000000;
99         4'b0001: seg2 = 7'b1001111;
100        4'b0010: seg2 = 7'b0100100;
101        4'b0011: seg2 = 7'b0000110;
102        4'b0100: seg2 = 7'b0001011;
103        4'b0101: seg2 = 7'b0010010;
104        4'b0110: seg2 = 7'b0010000;
105        4'b0111: seg2 = 7'b1000111;
106        4'b1000: seg2 = 7'b0000000;
107        4'b1001: seg2 = 7'b0000010;
108        default: seg2 = 7'b1000000;
109    endcase
110
111    case (ones)
112        4'b0000: seg3 = 7'b1000000;
113        4'b0001: seg3 = 7'b1001111;
114        4'b0010: seg3 = 7'b0100100;
115        4'b0011: seg3 = 7'b0000110;
116        4'b0100: seg3 = 7'b0001011;
117        4'b0101: seg3 = 7'b0010010;
118        4'b0110: seg3 = 7'b0010000;
119        4'b0111: seg3 = 7'b1000111;
120        4'b1000: seg3 = 7'b0000000;
121        4'b1001: seg3 = 7'b0000010;
122        default: seg3 = 7'b1000000;
123    endcase
124 end
125 endmodule
126

```

Figure-3: Verilog Code of 7-bit Segment Driver (3)

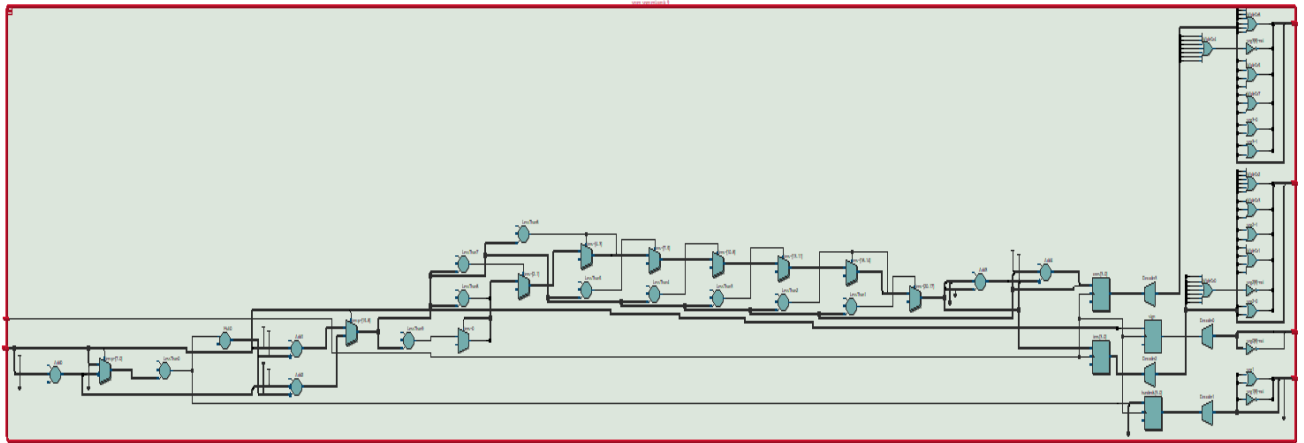


Figure-4: RTL View of 7-bit Segment Driver

## FLAG REGISTER

The Flag Register consists of 4 1-bit registers. Each holds the value of a flag. Flag values come from the ALU. Each register is also connected to some LEDs on the FPGA and when their value is 1, the LED they are connected to lights up.

```

1  module flag_register(
2      input [3:0] data,
3      input store,
4      input rst,
5      input clk,
6      output [3:0] out
7  );
8
9      one_bit_register(data[3],store,rst,clk,out[3]);
10     one_bit_register(data[2],store,rst,clk,out[2]);
11     one_bit_register(data[1],store,rst,clk,out[1]);
12     one_bit_register(data[0],store,rst,clk,out[0]);
13
14 endmodule
15

```

Figure-1: Verilog Code of Flag Register

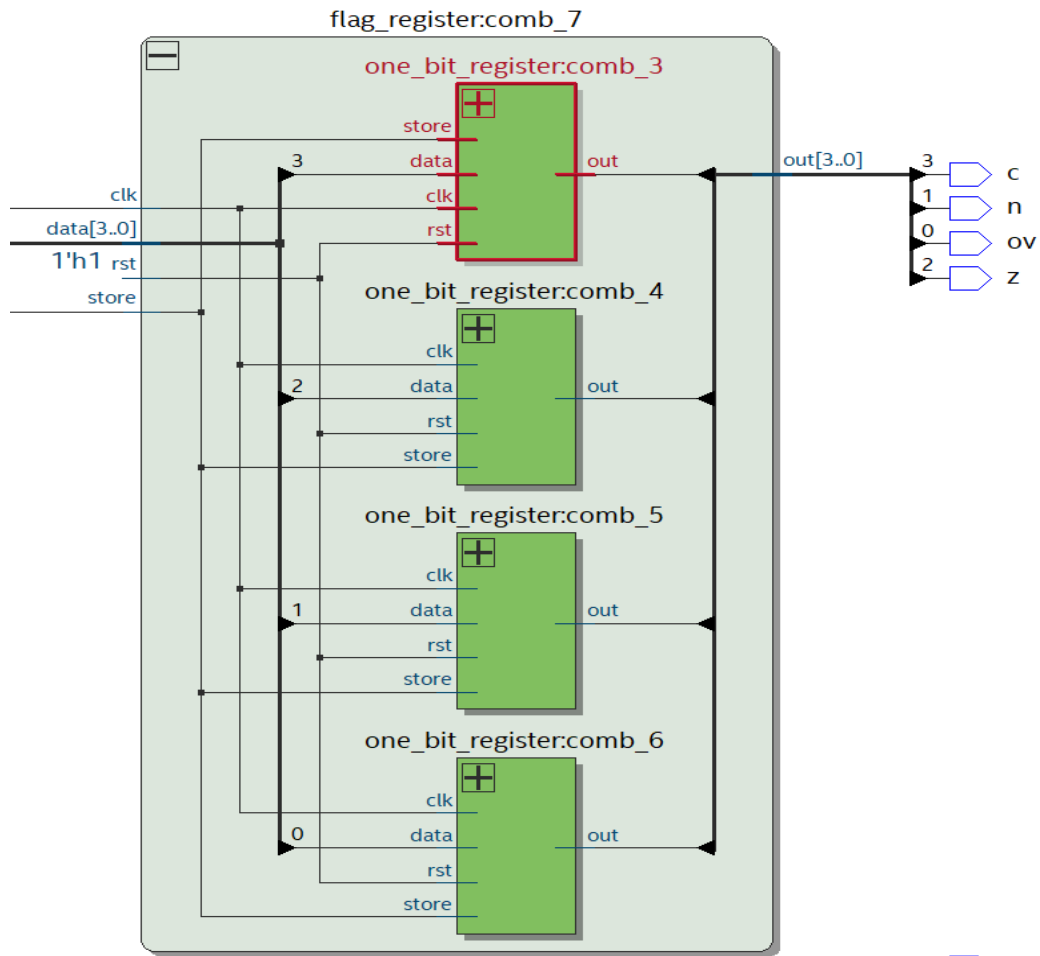


Figure-2: RTL View of Flag Register

## 8 SAMPLE OPERATION EXECUTING ON THE FPGA

First of all, we have compiled our CPU code by connecting to the lab computer. We made the necessary pin assignments. We have connected the right inputs to the appropriate switch pins for the instructions to be given as input and the suitable outputs to the correct LED pins. Then we uploaded our code to FPGA with programmer. Below, there are 8 operations and its details executed in the FPGA with our CPU.



Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserv
c	Output	PIN_F15	7	B7_N2	PIN_F15	2.5 V (default)	
ck	Input	PIN_AE24	4	B4_N0	PIN_AE24	2.5 V (default)	
d	Output	PIN_H16	7	B7_N2	PIN_H16	2.5 V (default)	
data[7]	Input	PIN_AC22	4	B4_N0	PIN_AC22	2.5 V (default)	
data[6]	Input	PIN_AE21	4	B4_N1	PIN_AE21	2.5 V (default)	
data[5]	Input	PIN_AF15	4	B4_N2	PIN_AF15	2.5 V (default)	
data[4]	Input	PIN_AF16	4	B4_N2	PIN_AF16	2.5 V (default)	
data[3]	Input	PIN_AE15	4	B4_N2	PIN_AE15	2.5 V (default)	
data[2]	Input	PIN_Y16	4	B4_N0	PIN_Y16	2.5 V (default)	
data[1]	Input	PIN_Y17	4	B4_N0	PIN_Y17	2.5 V (default)	
data[0]	Input	PIN_AC15	4	B4_N2	PIN_AC15	2.5 V (default)	
e	Output	PIN_J16	7	B7_N2	PIN_J16	2.5 V (default)	
f	Output	PIN_J15	7	B7_N2	PIN_J15	2.5 V (default)	
n	Output	PIN_G16	7	B7_N2	PIN_G16	2.5 V (default)	
opcode[3]	Input	PIN_AE25	4	B4_N1	PIN_AE25	2.5 V (default)	
opcode[2]	Input	PIN_AD25	4	B4_N0	PIN_AD25	2.5 V (default)	
opcode[1]	Input	PIN_AD22	4	B4_N0	PIN_AD22	2.5 V (default)	
opcode[0]	Input	PIN_AF21	4	B4_N1	PIN_AF21	2.5 V (default)	
ov	Output	PIN_H15	7	B7_N2	PIN_H15	2.5 V (default)	
pc_address[7]	Output	PIN_H19	7	B7_N2	PIN_H19	2.5 V (default)	
pc_address[6]	Output	PIN_J19	7	B7_N2	PIN_J19	2.5 V (default)	
pc_address[5]	Output	PIN_E18	7	B7_N1	PIN_E18	2.5 V (default)	
pc_address[4]	Output	PIN_F18	7	B7_N1	PIN_F18	2.5 V (default)	
pc_address[3]	Output	PIN_F21	7	B7_N0	PIN_F21	2.5 V (default)	
pc_address[2]	Output	PIN_F19	7	B7_N0	PIN_F19	2.5 V (default)	
pc_address[1]	Output	PIN_F19	7	B7_N0	PIN_F19	2.5 V (default)	
pc_address[0]	Output	PIN_G19	7	B7_N2	PIN_G19	2.5 V (default)	
seg0[6]	Output	PIN_H22	6	B6_N0	PIN_H22	2.5 V (default)	
seg0[5]	Output	PIN_J22	6	B6_N0	PIN_J22	2.5 V (default)	
seg0[4]	Output	PIN_I25	6	B6_N1	PIN_I25	2.5 V (default)	

Figure-1: Some pin assignments on the FPGA

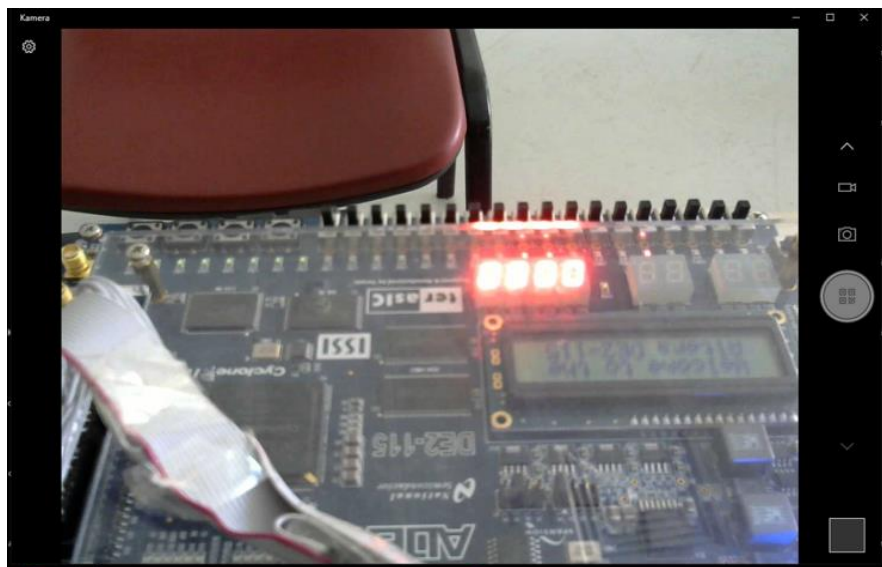


Figure-2: First condition of the FPGA

In the first condition of the FPGA, all LEDs are off and 7-segment is set to 0000. There are totally 18 LEDs in our FPGA. The first 8 left LEDs [0,7] are for the PC. [10, 12] LEDs are for the states; fetch, decode and execute respectively. [14,17] are for the flags; carry, zero, negative and overflow respectively. LED's 8, 9 and 13 are not used for our project.

After each clock signal to be given to the control unit, the next state will be active. PC increments by one after each fetch state is completed. After each execute state is completed the flags are set and the accumulator keeps the ALU result. In order to write this result to 7-segment, one more state is needed. When the fetch state of the instruction is complete, the accumulator value from the previous instruction is written to the 7-segment.

#### OPERATION 1:

MOVE 12      010000001100(Opcode + value 12)      After the operation ACC should be: 12

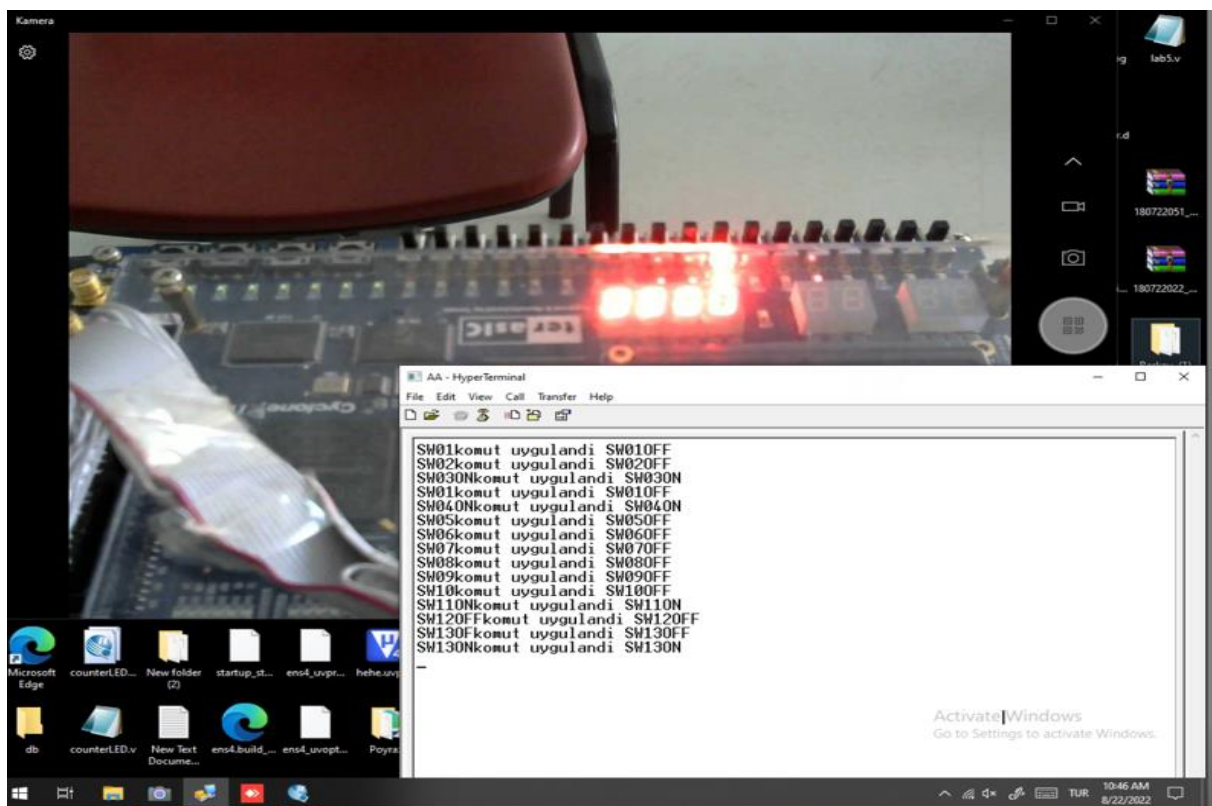


Figure-3: First Clock of the Operation 1

Current State: Fetch      -      PC:0      -      Flags: 0000      -      ACC:0      -      7-Segment: 0

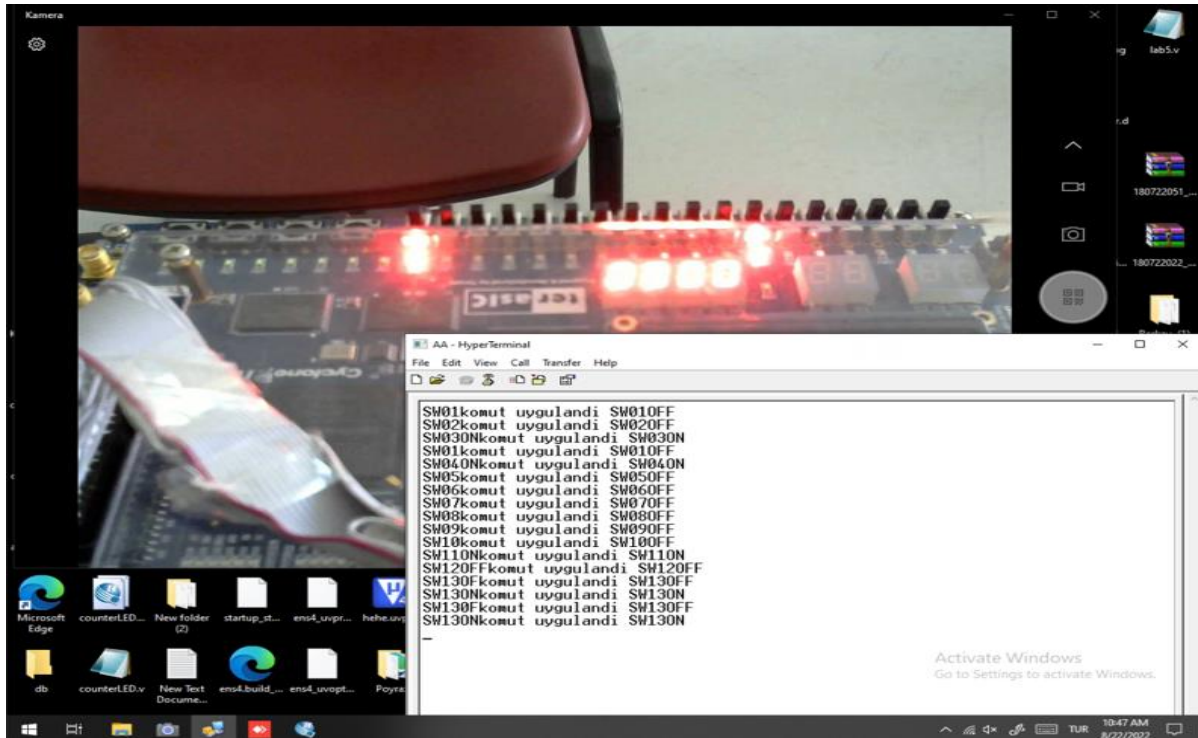


Figure-4: Second Clock of the Operation 1

Current State: Decode - Completed State: Fetch - PC:1 - Flags: 0000 - ACC: 0

7-Segment: 0

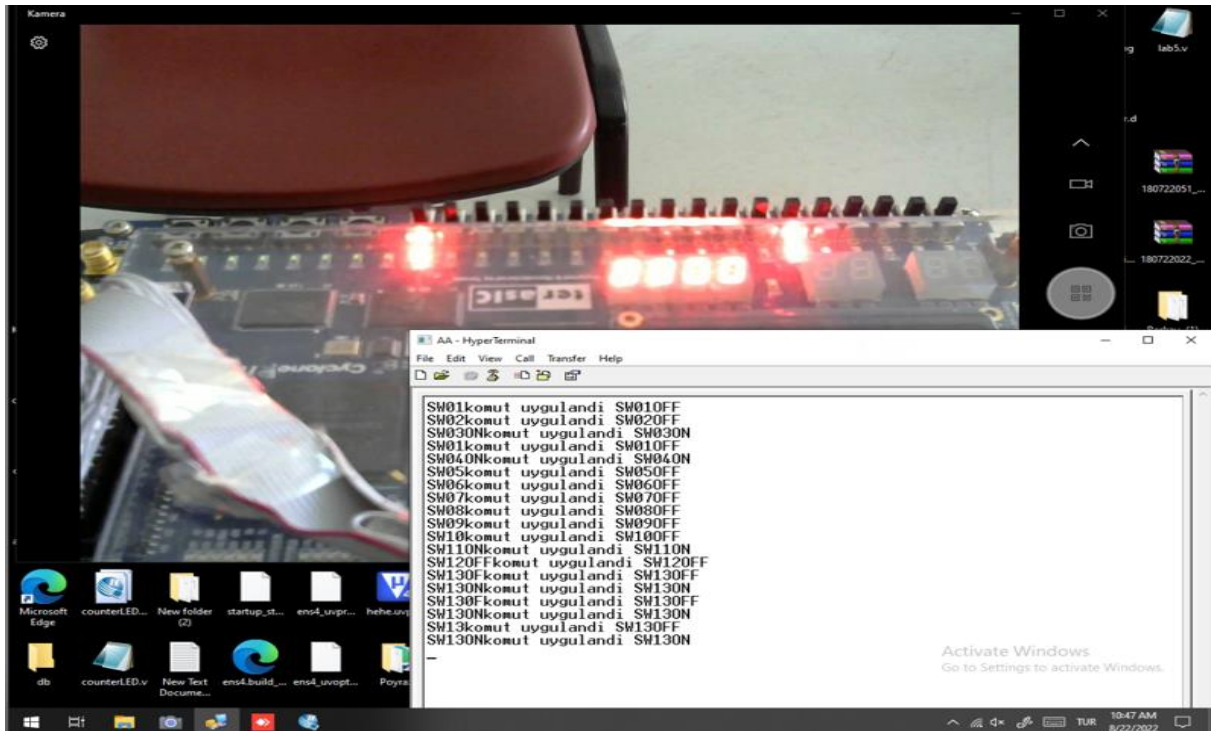


Figure-5:

Current State: Execute - Completed State: Decode - PC:1 - Flags: 0000 - ACC: 0  
7-Segment: 0

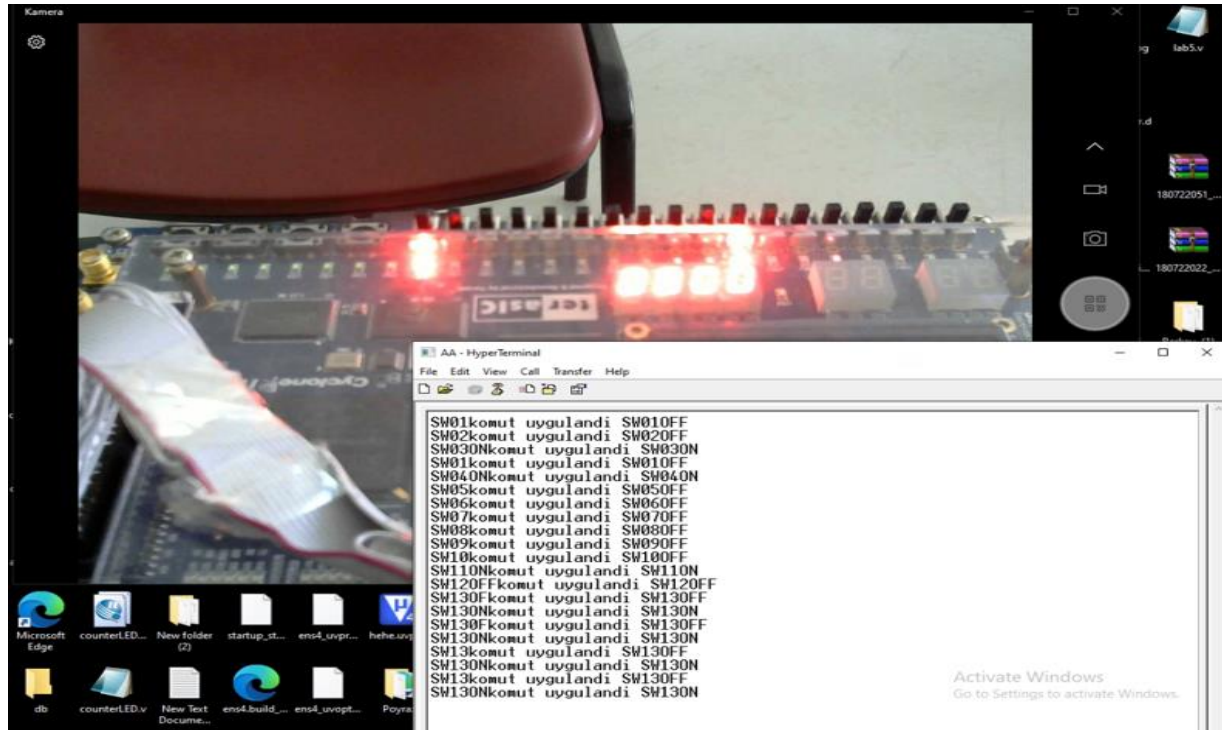


Figure-6:

Current State: Fetch - Completed State: Execute - PC:1 - Flags: 0000 (Flags are set in this state but all are still zero) - ACC: 12 - 7-Segment: 0



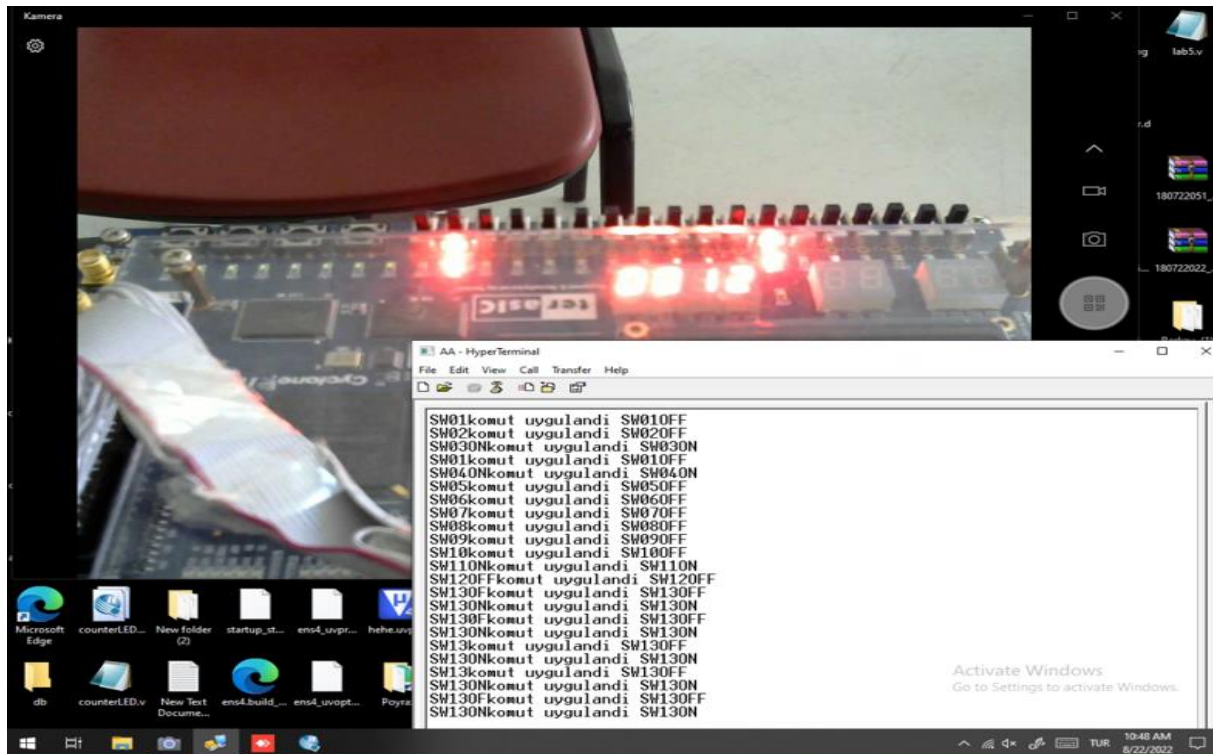


Figure-7:

Current State: Decode - Completed State: Fetch - PC:2 - Flags: 0000 - ACC: 12

7-Segment: 12

## OPERATION 2:

ADD 15      000000001111(Opcod + value 15)      After the operation ACC should be: 27

For this operation, it is enough to open the 1st and 2nd switches and close the 11th switch. Then, we give the Control Unit a new clock, so that the decode state is completed and thus the new input is taken to IR.

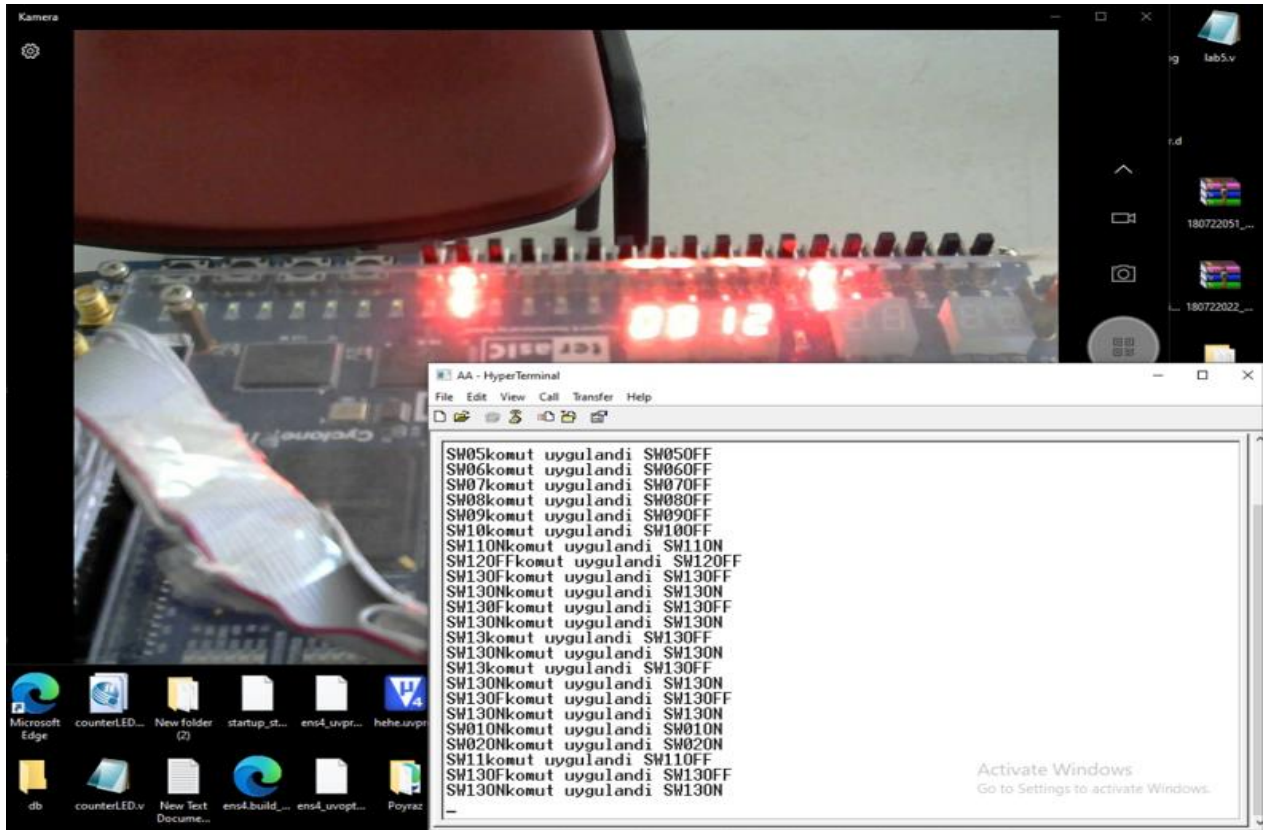


Figure-8:

Current State: Execute - Completed State: Decode - PC:2 - Flags: 0000 - ACC: 12

7-Segment: 12

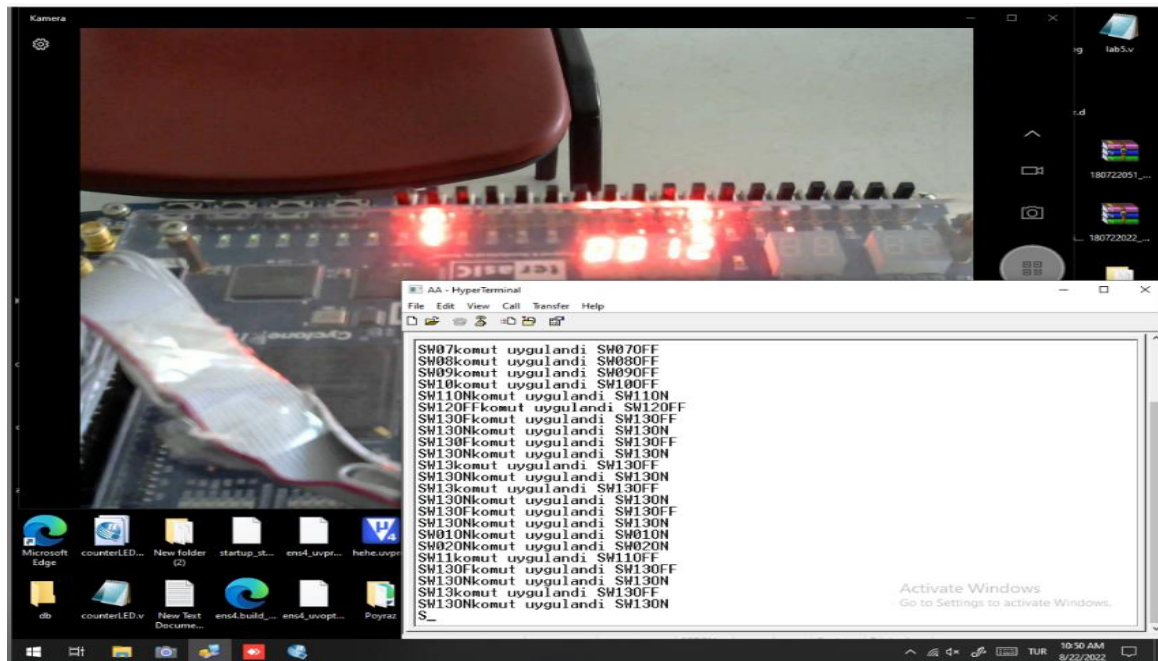


Figure-9:

Current State: Fetch - Completed State: Execute - PC:2 - Flags: 0000(Still all zero)  
ACC: 27 - 7-Segment: 12

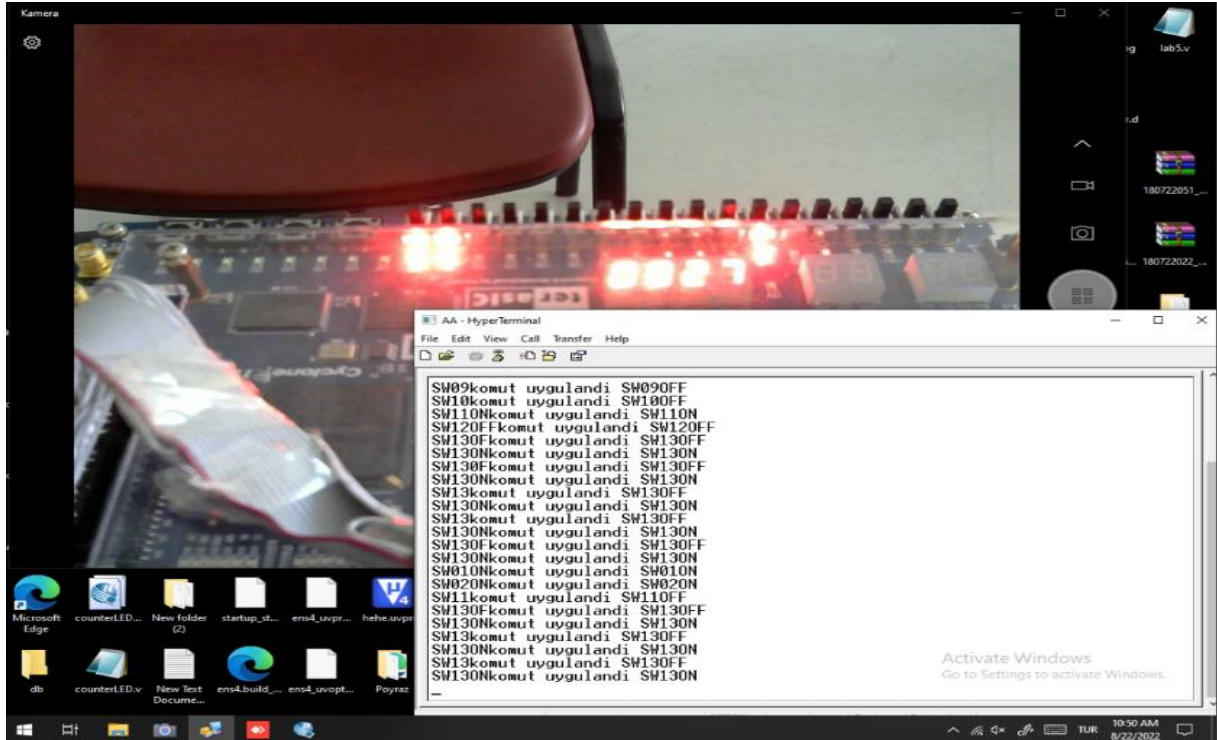


Figure-10:

Current State: Decode - Completed State: Fetch - PC:3 - Flags: 0000 - ACC: 27  
7-Segment: 27

### OPERATION 3:

SUB 36      000100100100(Opcode + value 36)      After the operation ACC should be: 9

For this operation, we opened the 6<sup>th</sup> and 9<sup>th</sup> switches and closed the 1<sup>st</sup>, 2<sup>nd</sup> and 4<sup>th</sup> switches. Then, we give the Control Unit a new clock, so that the decode state is completed and thus the new input is taken to IR.

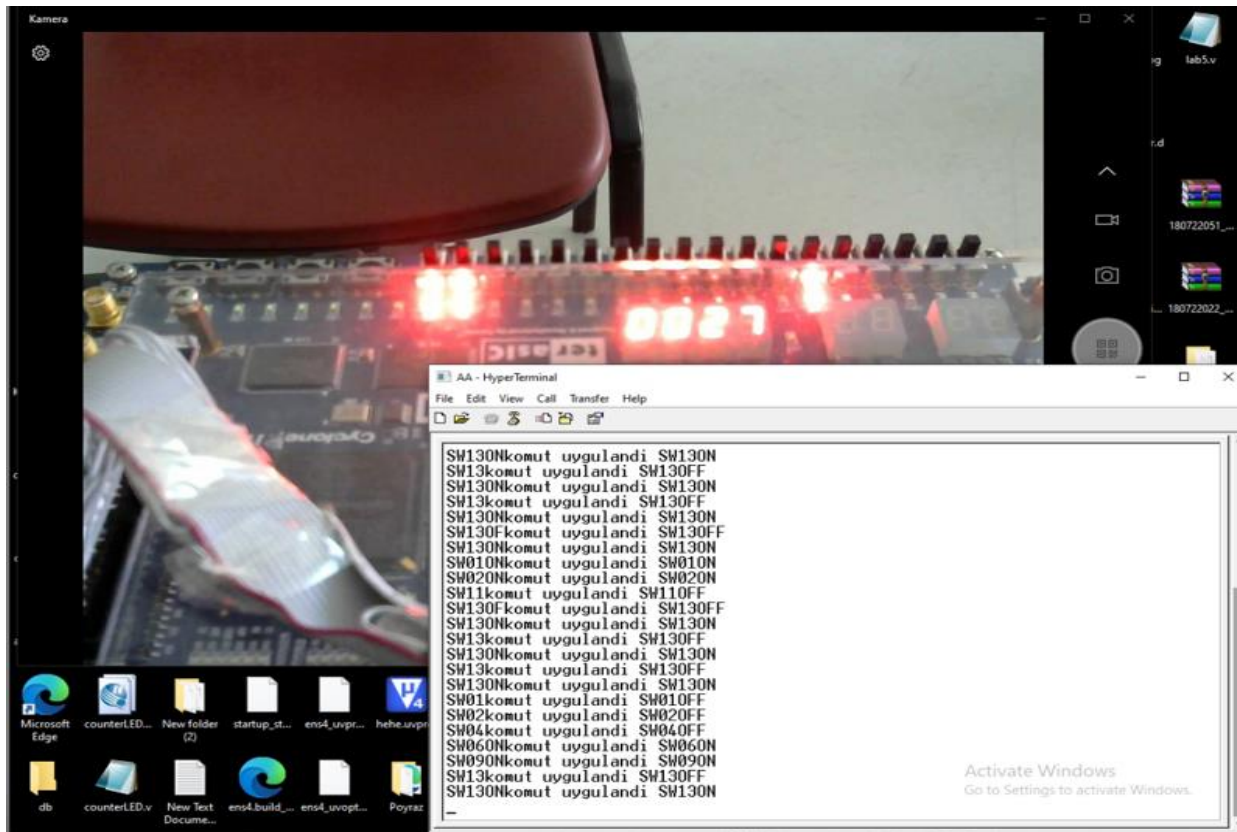


Figure-11:

Current State: Execute - Completed State: Decode - PC:3 - Flags: 0000 - ACC: 27

7-Segment: 27



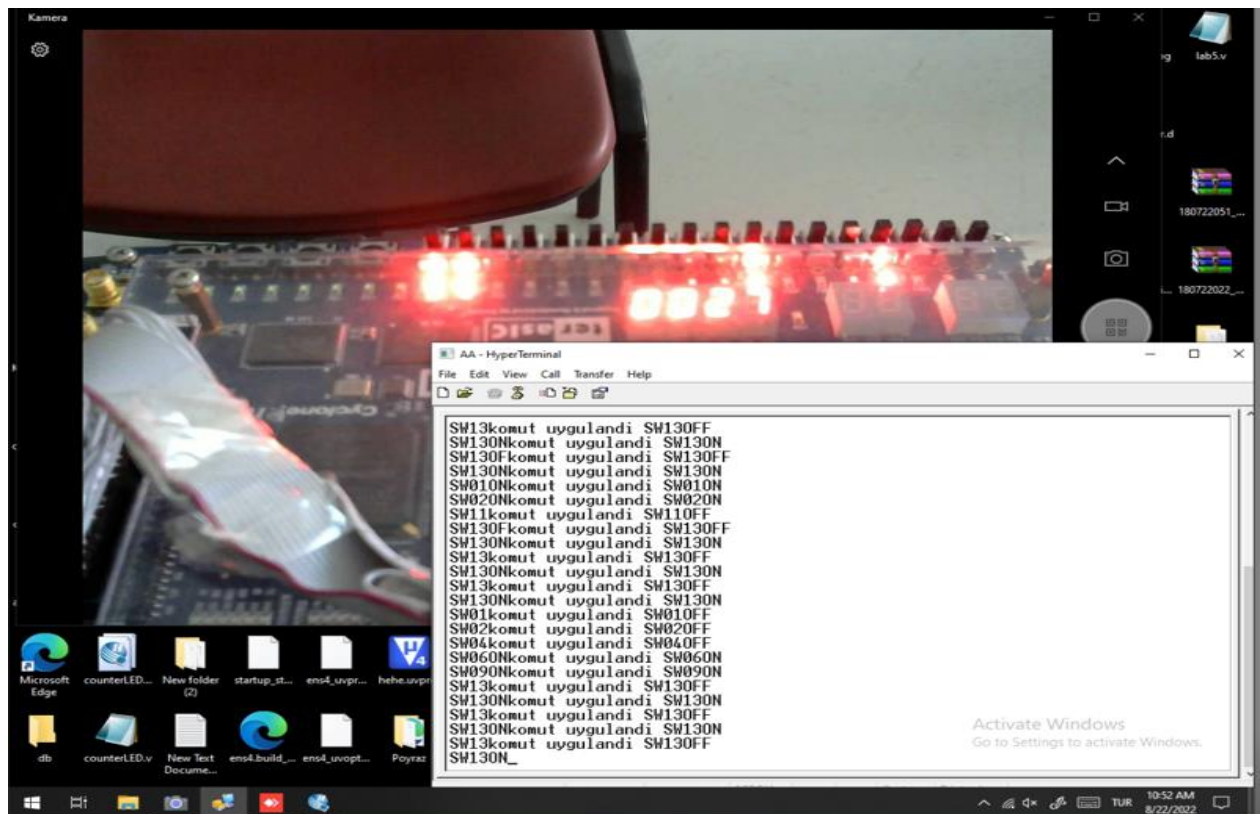
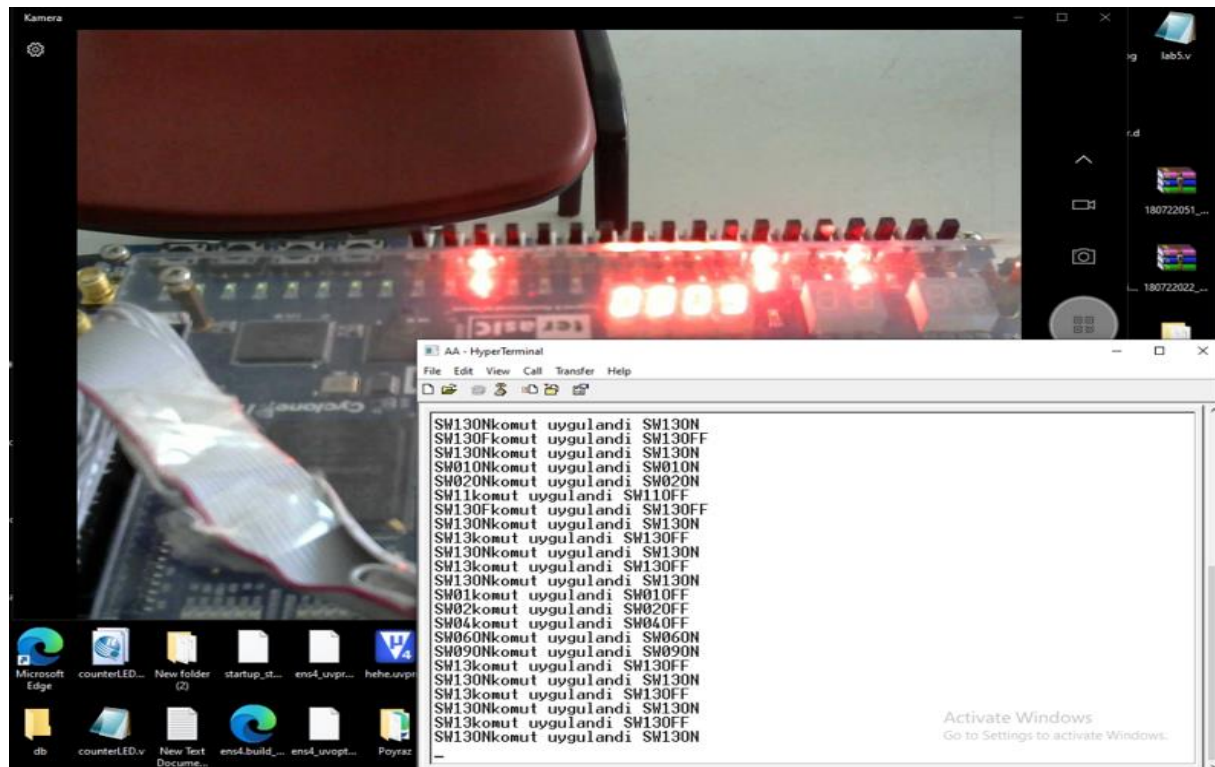


Figure-12:

Current State: Fetch - Completed State: Execute - PC:3 - Flags: 1000 - ACC: 9  
7-Segment: 27



Current State: Decode - Completed State: Fetch - PC:4 - Flags: 1000 - ACC:9  
7-Segment: 9

#### OPERATION 4:

INC 0      011100000000(Opcode + value 0)      After the operation ACC should be: 10

For this operation, we opened the 10<sup>th</sup> and 11<sup>th</sup> switches and closed the 3<sup>rd</sup> and 6<sup>th</sup> switches. Then, we give the Control Unit a new clock, so that the decode state is completed and thus the new input is taken to IR.

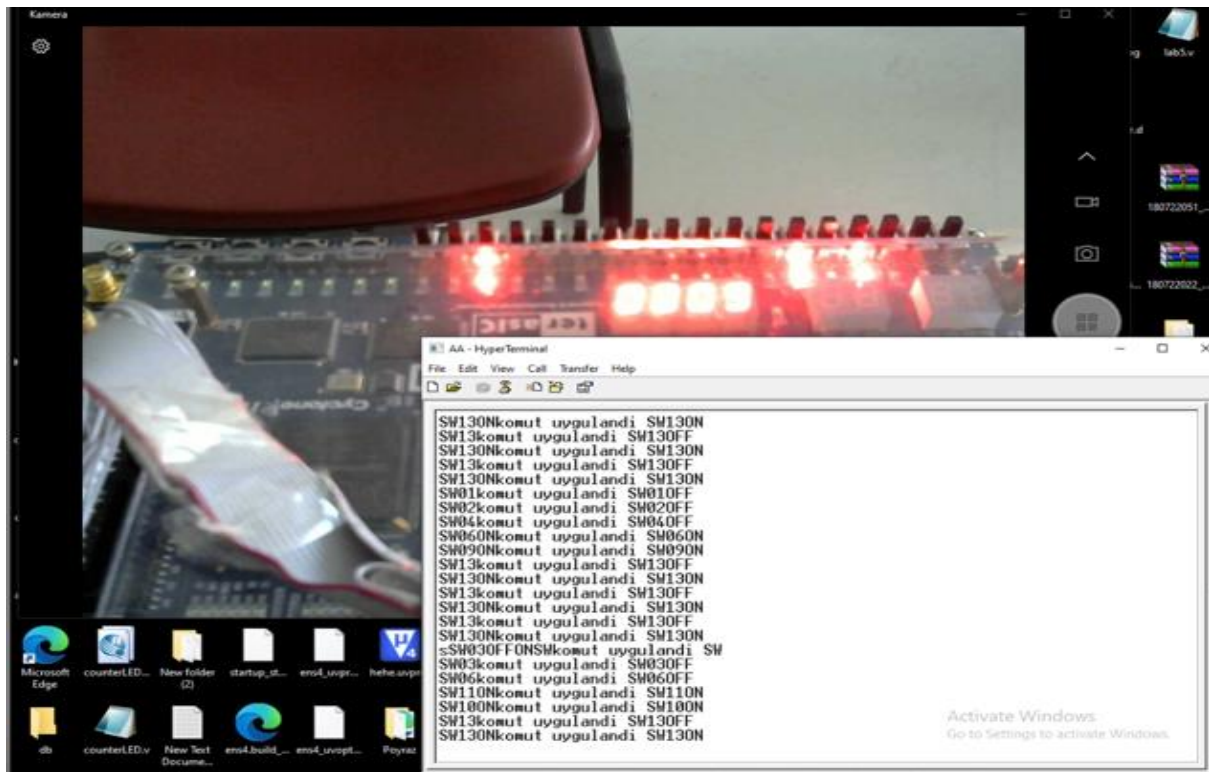


Figure-14:

Current State: Execute - Completed State: Decode - PC:4 - Flags: 1000 - ACC:9  
7-Segment: 9

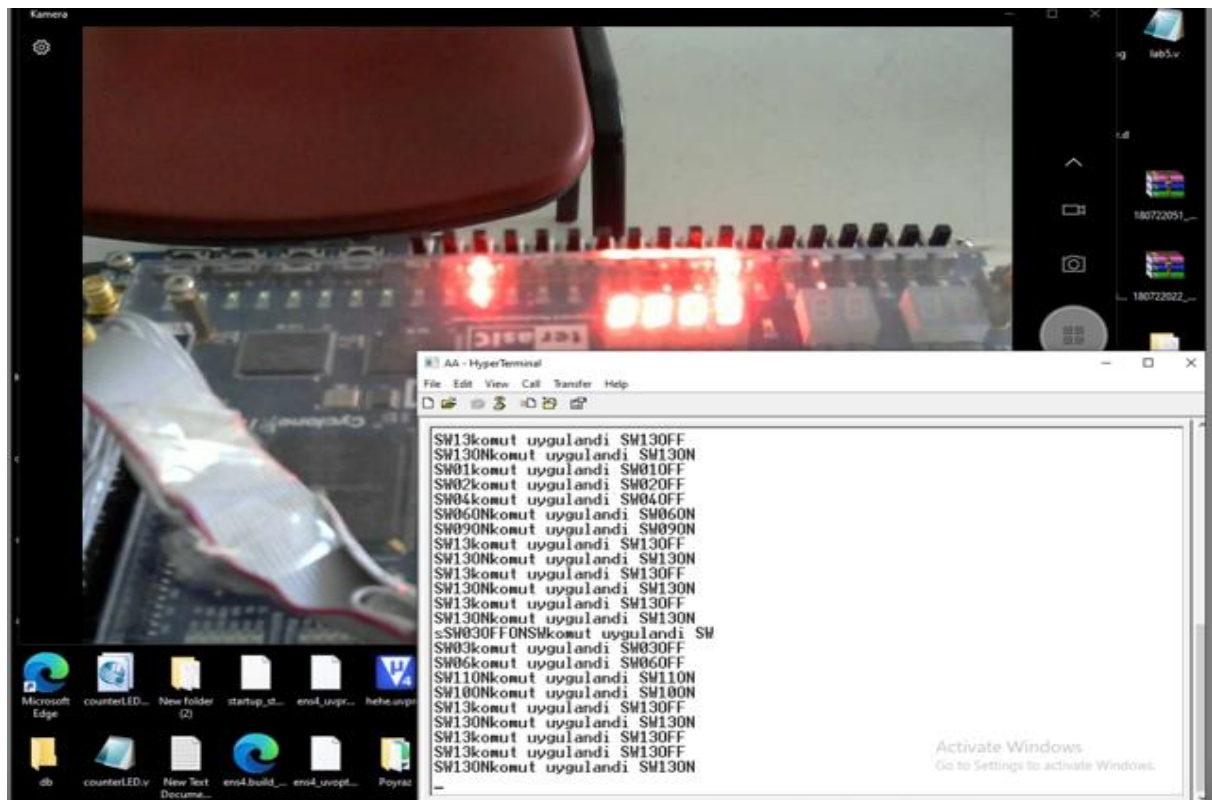


Figure-15:

Current State: Fetch - Completed State: Execute - PC:4 - Flags: 0000 - ACC:10  
7-Segment: 9

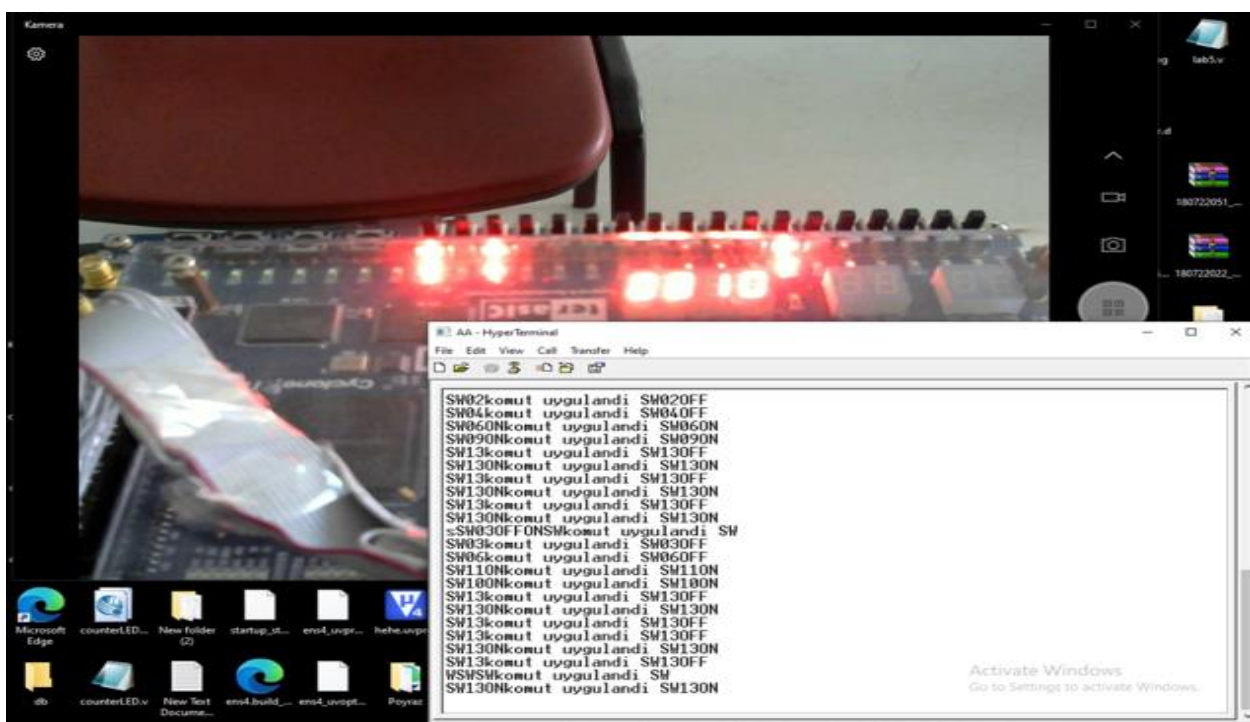


Figure-16:



Current State: Decode - Completed State: Fetch - PC:5 - Flags: 0000 - ACC:10

7-Segment: 10

#### OPERATION 5:

SHFL 8      010100001000 (Opcode + value 8)      After the operation ACC should be: 16

For this operation, we opened the 4<sup>th</sup> switch and closed the 10<sup>th</sup> switch. Then, we give the Control Unit a new clock, so that the decode state is completed and thus the new input is taken to IR.

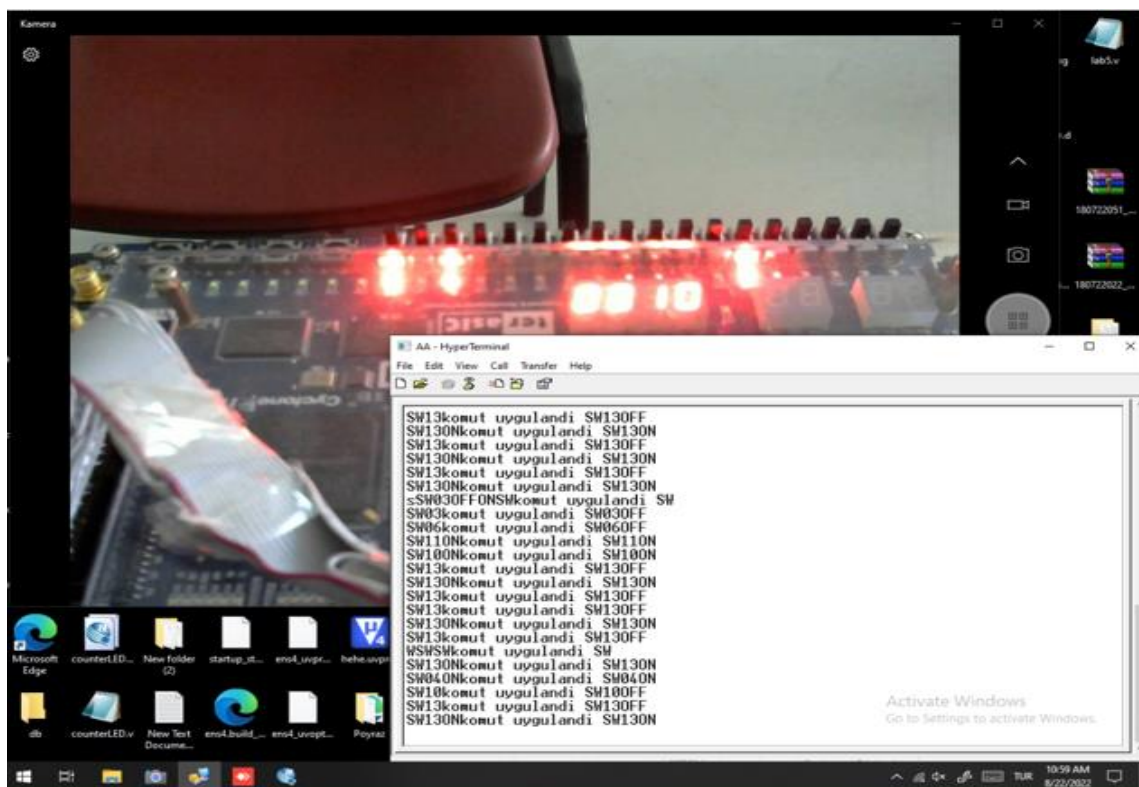


Figure-17:

Current State: Execute - Completed State: Decode - PC:5 - Flags: 0000 - ACC:10

7-Segment: 10

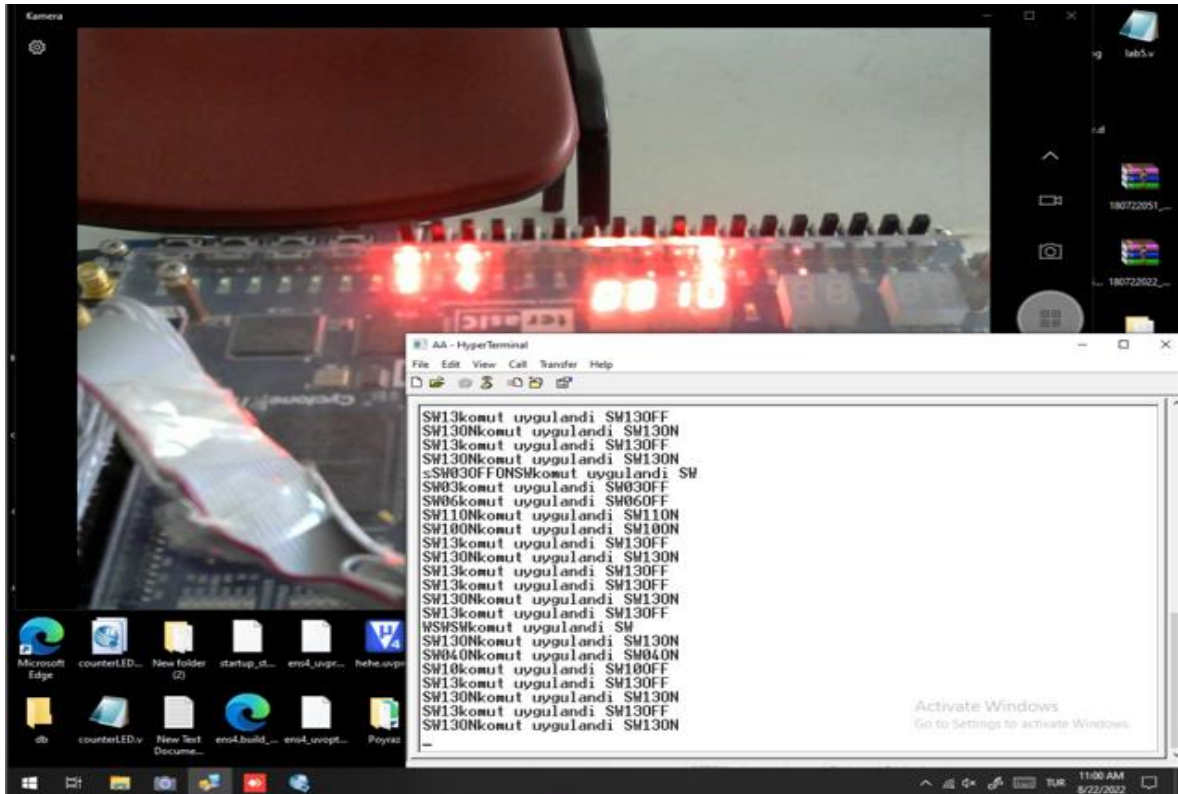


Figure-18:

Current State: Fetch - Completed State: Execute - PC:5 - Flags: 0000 - ACC:16  
7-Segment: 10

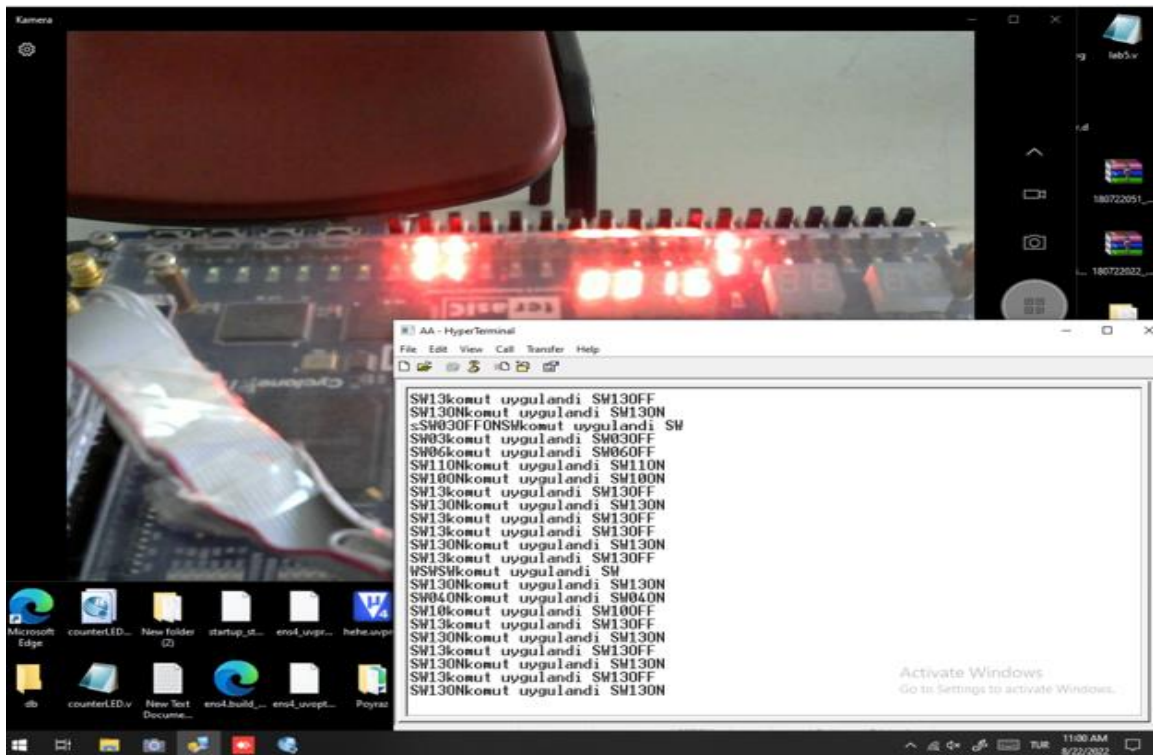


Figure-19:

Current State: Decode - Completed State: Fetch - PC:6 - Flags: 0000 - ACC:16

7-Segment: 16

#### OPERATION 6:

SHFR 16      011000010000 (Opcode + value 16)      After the operation ACC should be: 8

For this operation, we opened the 5<sup>th</sup> and 10<sup>th</sup> switches and closed the 4<sup>th</sup> and 9<sup>th</sup> switches. Then, we give the Control Unit a new clock, so that the decode state is completed and thus the new input is taken to IR.

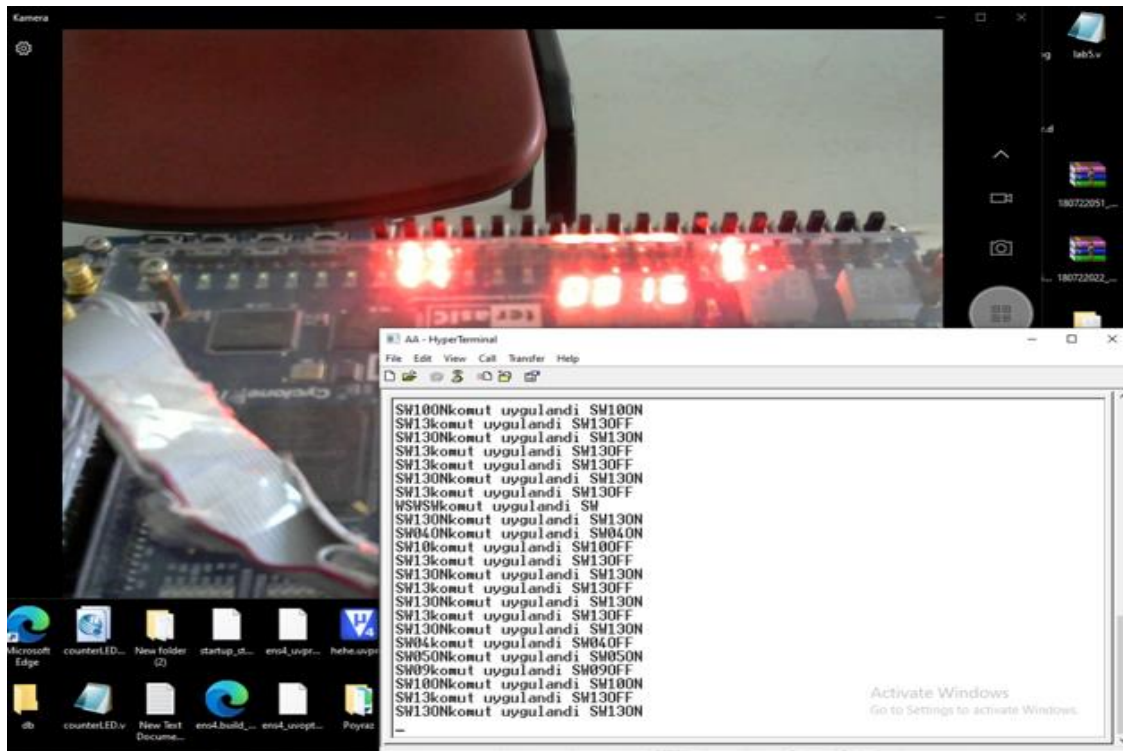


Figure-20:

Current State: Execute - Completed State: Decode - PC:6 - Flags: 0000 - ACC:16

7-Segment: 16

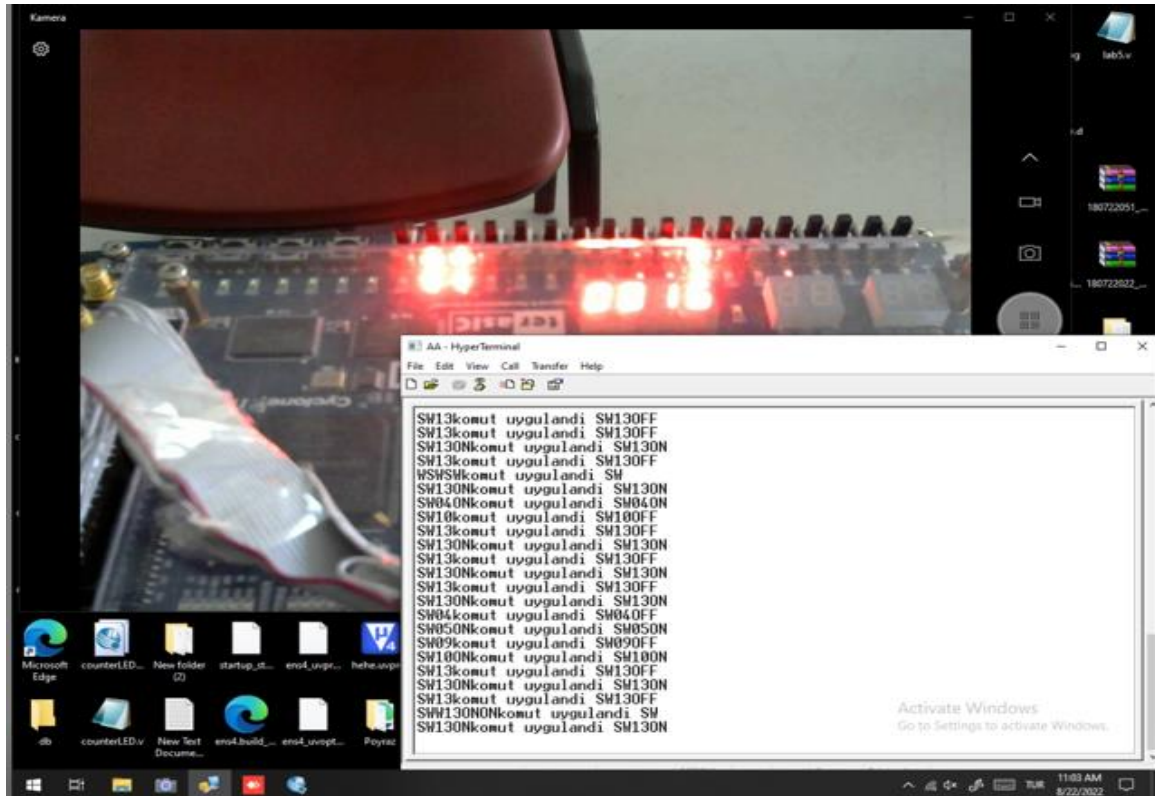


Figure-21:

Current State: Fetch - Completed State: Execute - PC:6 - Flags: 0000 (not changed)  
ACC: 8 - 7-Segment: 16

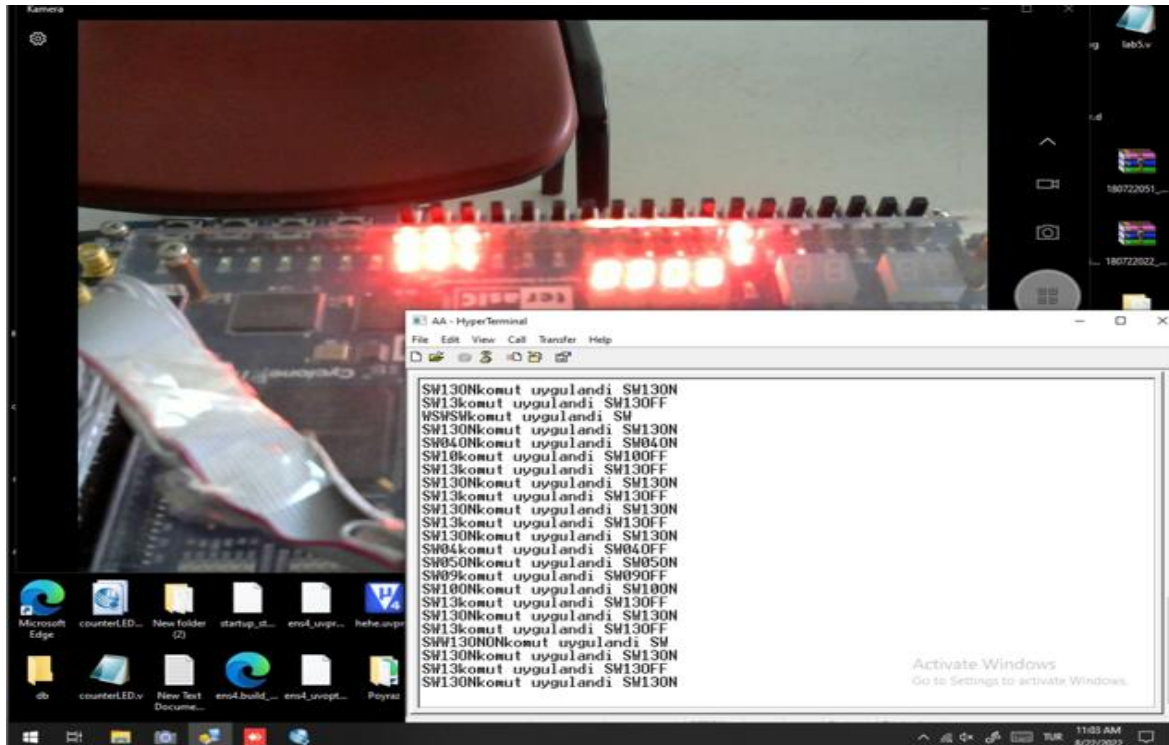


Figure-22:



Current State: Decode - Completed State: Fetch - PC:7 - Flags: 0000 ACC: 8  
7-Segment: 8

#### OPERATION 7:

OR 7      001100000111 (Opcode + value 7)      After the operation ACC should be: 15

For this operation, we opened the 1<sup>st</sup>, 2<sup>nd</sup>, 3<sup>rd</sup> and 9<sup>th</sup> switches and closed the 5<sup>th</sup> and 11<sup>th</sup> switches. Then, we give the Control Unit a new clock, so that the decode state is completed and thus the new input is taken to IR.

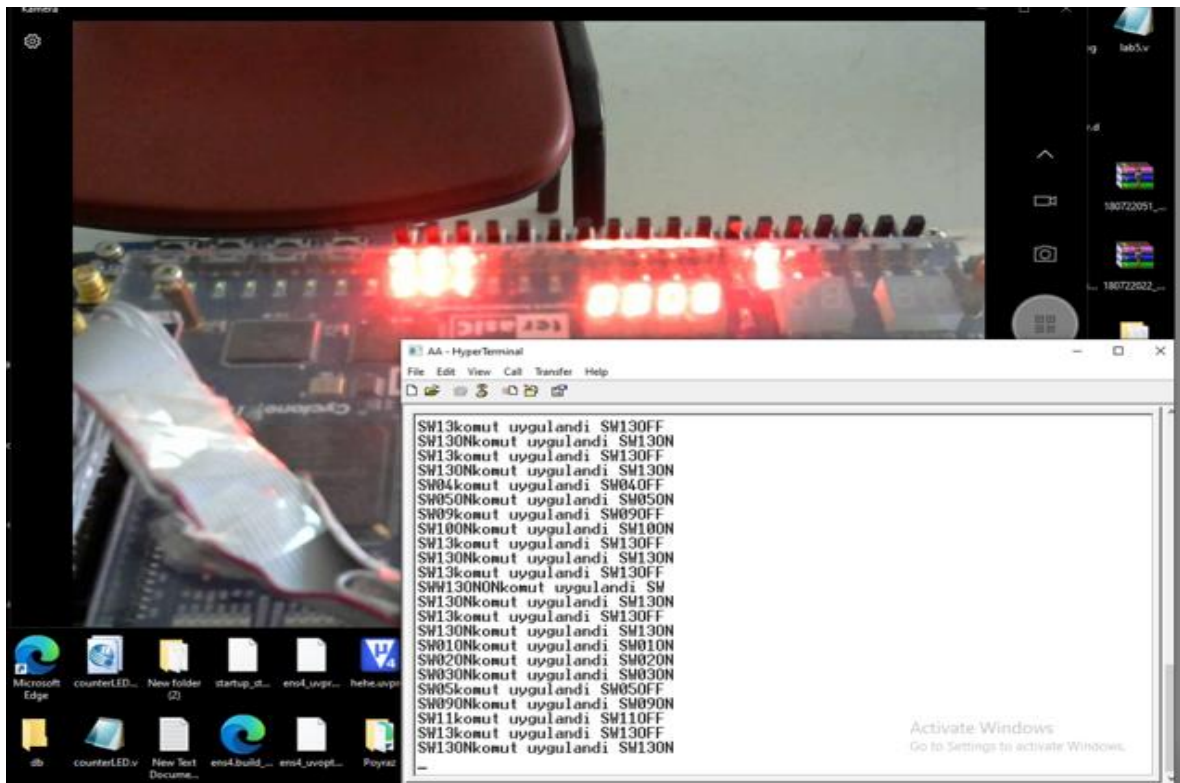


Figure-23:

Current State: Execute - Completed State: Decode - PC:7 - Flags: 0000 ACC:8  
7-Segment: 8



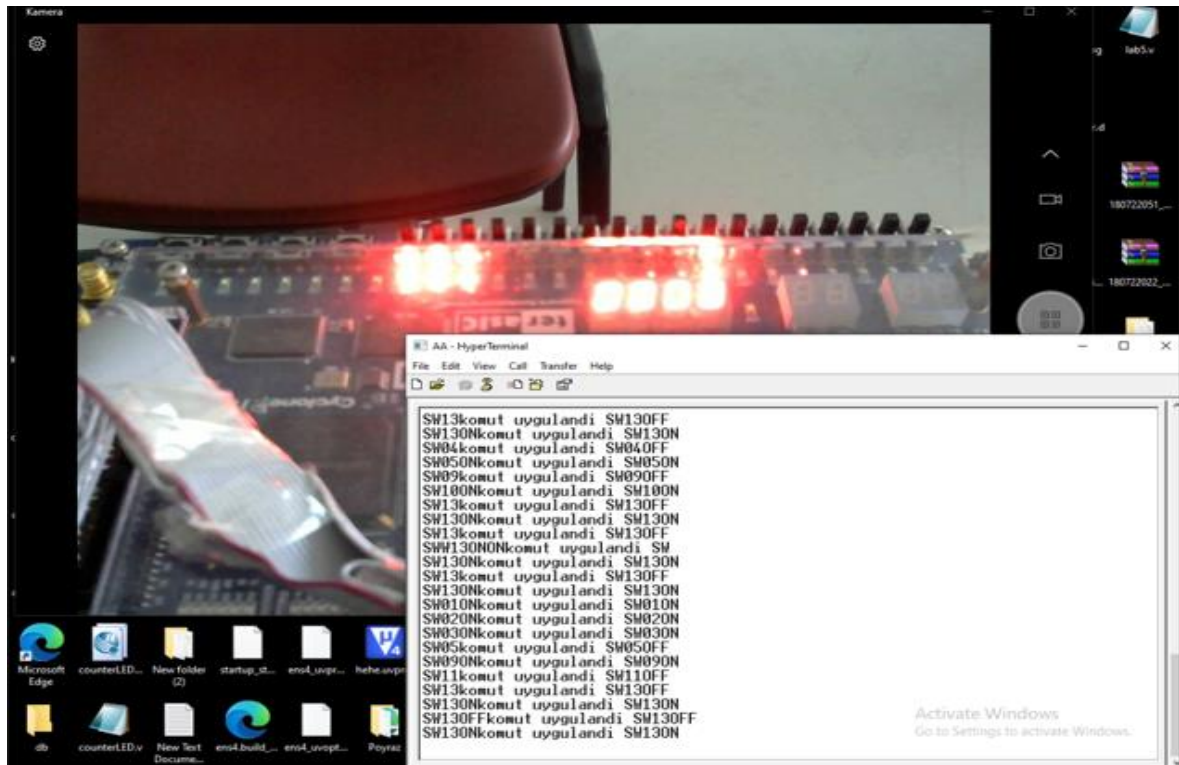


Figure-24:

Current State: Fetch - Completed State: Execute - PC:7 - Flags: 0000(not changed)  
ACC: 15 7-Segment: 8

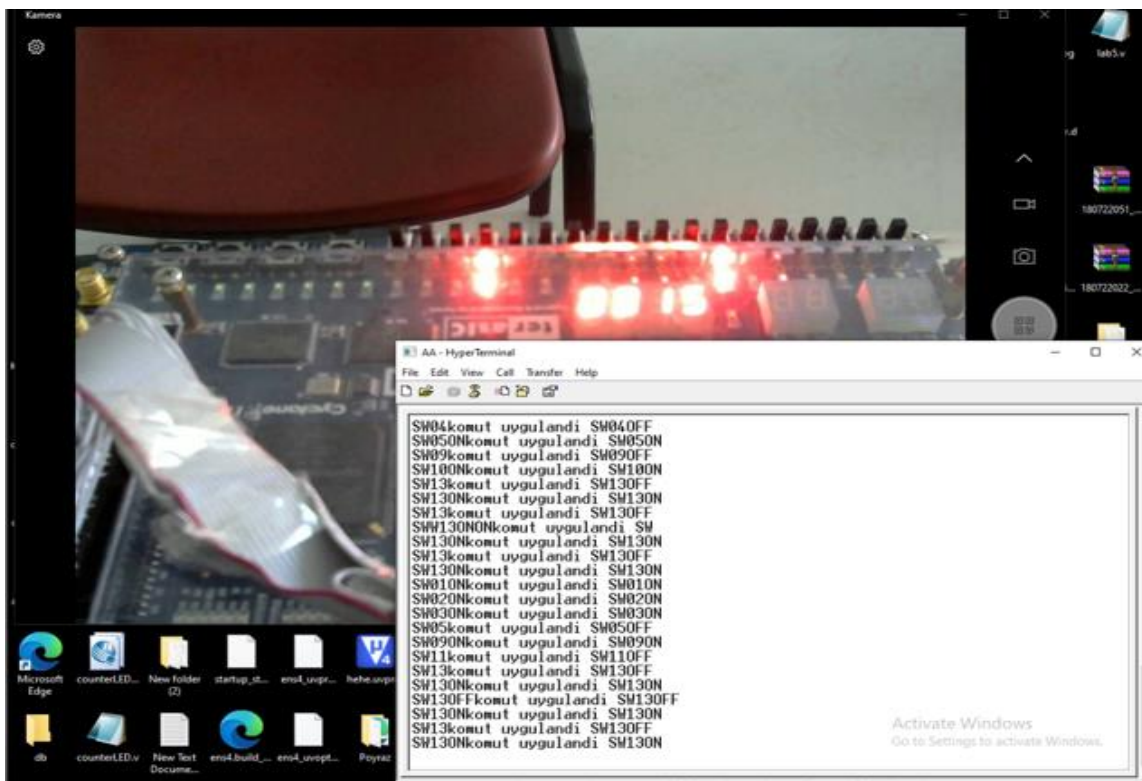


Figure-25:

Current State: Decode - Completed State: Fetch - PC:8 - Flags: 0000 - ACC: 15  
7-Segment: 15

#### OPERATION 8:

MOVE -128            010010000000 (Opcode + value -128)      After the operation ACC  
should be: -128

For this operation, we opened the 8<sup>th</sup> and 11<sup>th</sup> switches and closed the 1<sup>st</sup>, 2<sup>nd</sup>, 3<sup>rd</sup>, 9<sup>th</sup>  
and 10<sup>th</sup> switches. Then, we give the Control Unit a new clock, so that the decode state is  
completed and thus the new input is taken to IR.

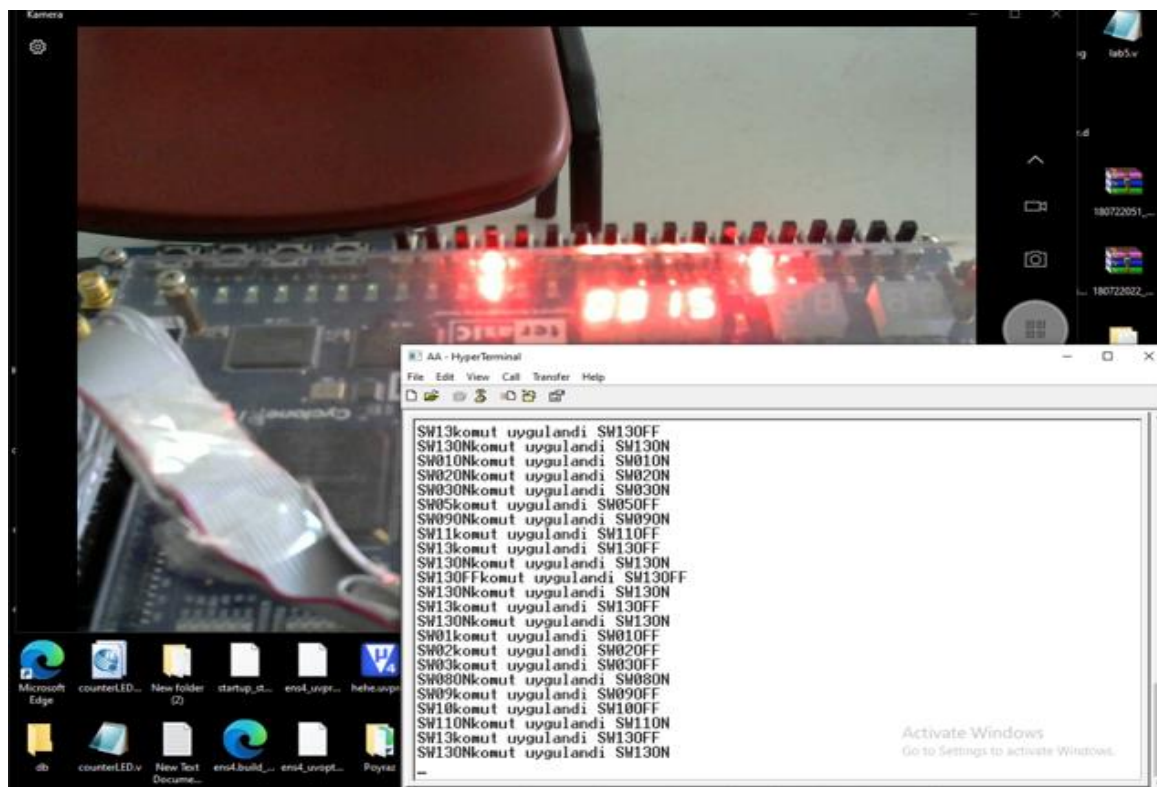


Figure-26:

Current State: Execute - Completed State: Decode - PC:8 - Flags: 0000 - ACC:15  
7-Segment: 15

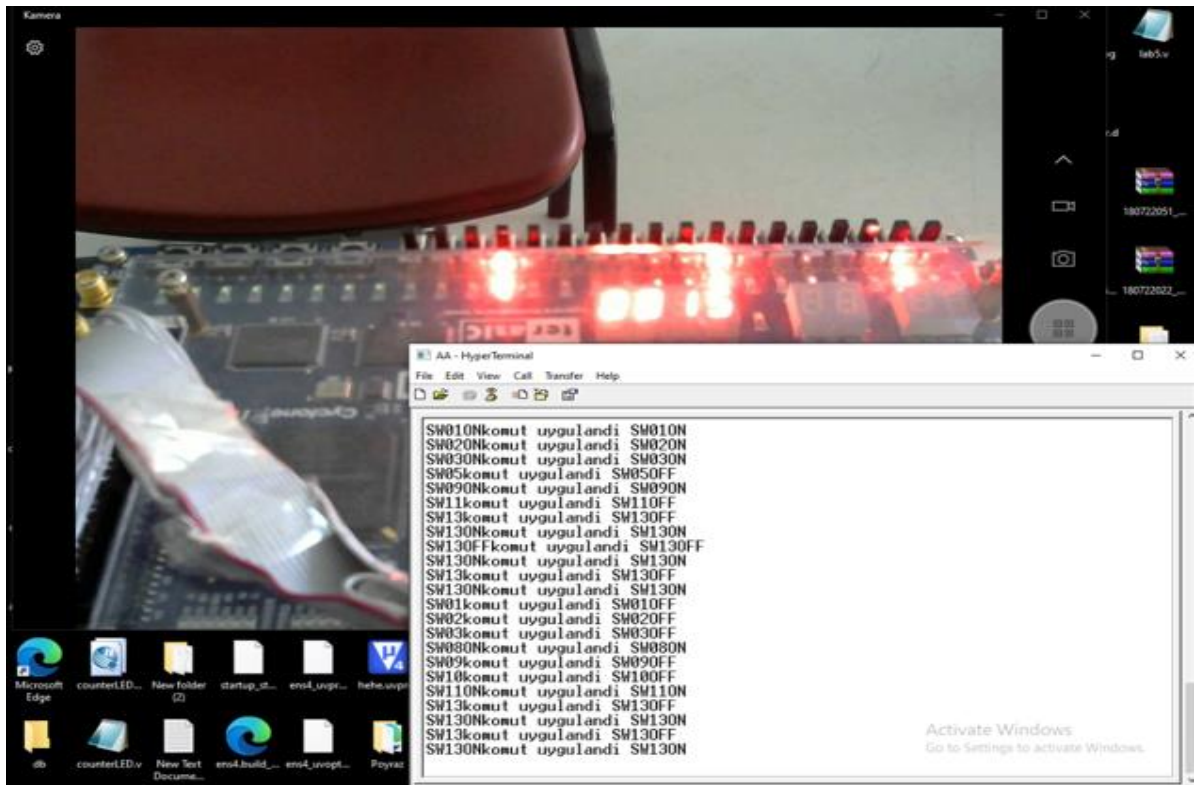


Figure-27:

Current State: Fetch - Completed State: Execute - PC:8 - Flags: 0010 - ACC:-128  
7-Segment: 15

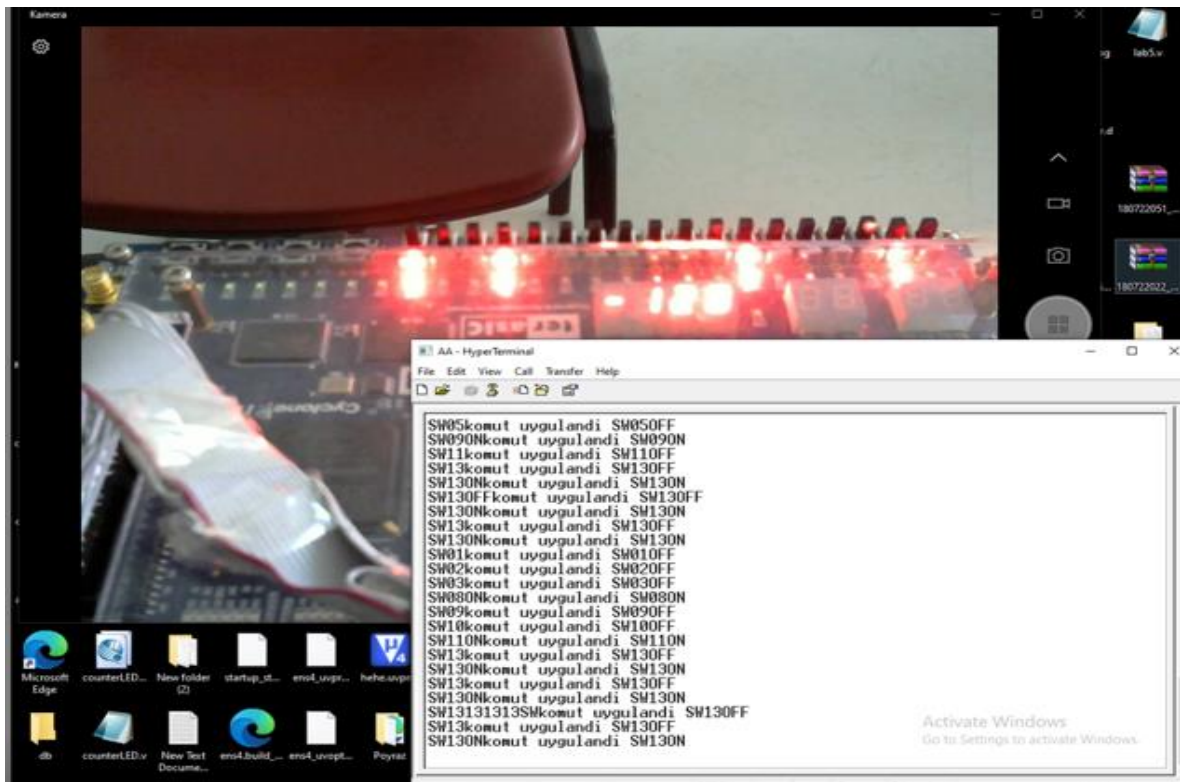


Figure-28:

Current State: Decode - Completed State: Fetch - PC:9 - Flags: 0010 - ACC: -128  
7-Segment: -128