Marmara University Electrical-Electronics Eng. Dept.

CSE4117 Microprocessors Laboratory Assignment #2

Each group must submit their own study. The group members have to work together and each member must know each step of the study. The studies will be submitted until 17.08.2022. A report (pdf file) should explain the digital circuits, operational blocks and all necessary technical information (You may use screenshots in your report). A short video file (<2 mins and <10 MByte)must be prepared to present the study. Each group must upload these files to a cloud-drive. The drive link must be sent to cse4117@yaani.com email address.

For this laboratory assignment, you will use Altera Quartus II software and Altera DE2-115 FPGA Kit to design and demonstrate some simple CPU blocks working together. Please follow the items below to complete your study:

1. 7-segment driver: Write a module that writes an 8-bit value (betw. 0-255) on to the 7-segments. Module should have 8 bit input and its output will be the 7-segments on theFPGA kit). (It may have a clock input)
2. Register: Design 8-bit register modüle with 8-bit input value, 8 bit output value, a store input and the clock. (Accumulator and Instuction register)
3. Counter: Design an 8-bit binary counter using am 8-bit register and an incrementer block. (program counter)
4. Control Unit: Design a FSM that has 3 outputs: Fetch, decode & execute. It will be a one-hot couter. (EDF- 001-010-100-001-...)
5. Connect these modules as they are given in the figüre above.
6. Use the LEDs to understand the current program counter value. PC will start from 0 end with 255.
7. Use the switches to enter your machine code in to the CPU.

You will write your own example code to run it by using the structure above. Your code must include at least 3 aritmetic, 3 logic and 2 move operations.