Marmara University Electrical-Electronics Eng. Dept.

CSE4117 Microprocessors Laboratory Assignment #3

Each group must submit their own study. The group members have to work together and each member must know each step of the study. The studies will be submitted until 02.09.2022. A report (pdf file) should explain the digital circuits, operational blocks and all necessary technical information (You may use screenshots in your report). A short video file (<2 mins and <10 MByte)must be prepared to present the study. Each group must upload these files to a cloud-drive. The drive link must be sent to cse4117@yaani.com email address.

For this laboratory assignment, you will use Altera Quartus II software and Altera DE2-115 FPGA Kit to design and demonstrate some simple CPU blocks working together. Please follow the items below to complete your study:

1. Design a binary cell (B.C.) with the following inputs/outputs: R/W input (it chooses the operation type), S Input (it selects the B.C., read or write operation cannot be performed without activated S signal), R Input (Synchronous reset: this input will write zero into the
   B.C. in the next clock), I Input (1-bit Data in), O output (1-bit data out. The output will remain logic zero if the current operation is not read. If it is read then update O output with the value inside B.C.). Design and test the module. Use switches for inputs and LEDs for outputs.
2. RAM block: Design a 8-bit RAM block with 8 addresses. The inputs/outputs: CS (chip select), Data In, Data Out, R/W, address. Use B.C. modules, decoder and or gates. Test its functionality. Use switches for inputs and LEDs for outputs.
3. ROM block: Design a ROM block to store your instructions. Choose the data length according to your instruction size. The ROM should store 8 instructions. Test its functionality. Use switches for inputs and LEDs for outputs.
4. Clock source: Design a clock divider that has a clock input and an output. Use the 50MHz clock source in the FPGA kit as an input to your clock divider. Divide the input clock frequency to 250 million to decrease output clock frequency in this way you can achieve one clock cycle per 10 seconds. Test the output frequency using an LED on the FPGA kit.
5. Connect the ROM to your CPU design completed in previous assignment. Connect the clock dividers' output to the clock input of your CPU design. Upload your code to ROM and follow the LEDs and 7-segments if it s working properly.
6. Connect RAM module to your CPU using the connection diagram given below.
7. Change the control unit structure to implement R-type instructions.
8. Test at least 3 R-type instruction to see that your design 1. can write into the RAM, 2. Can read from the ram and 3 can read fro the ram than adds it to the value inside acc (1. STORE,
   2. MOVR and 3. ADDR).

Marmara University Electrical-Electronics Eng. Dept.

CSE4117 Microprocessors Laboratory Assignment #3

Each group must submit their own study. The group members have to work together and each member must know each step of the study. The studies will be submitted until 02.09.2022. A report (pdf file) should explain the digital circuits, operational blocks and all necessary technical information (You may use screenshots in your report). A short video file (<2 mins and <10 MByte)must be prepared to present the study. Each group must upload these files to a cloud-drive. The drive link must be sent to cse4117@yaani.com email address.