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Designing of a Battery-Powered Wearable ECG Signal Acquisition System

by:

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1 Introduction

The advancement of wearable biomedical devices has become increasingly vital due to the rising demand for continuous, real-time health monitoring. Among these innovative solutions, wearable Electrocardiogram (ECG) acquisition systems play a crucial role in detecting cardiovascular abnormalities, effectively monitoring patient health, and supporting remote diagnostics. This assignment focuses on the design of a battery-powered wearable ECG signal acquisition device, thoroughly detailing the entire process of capturing, conditioning, digitizing, and wirelessly transmitting bio potential signals from the human body.

The system architecture integrates several key subsystems, including an instrumentation amplifier for signal enhancement, a Driven Right Leg (DRL) circuit for noise attenuation, a high-resolution Analog to Digital Converter (ADC) for accurate digitization, a reference voltage source for stability, and a microprocessor featuring Bluetooth Low Energy (BLE) capabilities for wireless communication. Together, these components ensure precise acquisition of ECG signals, effective noise suppression, reliable digitization, and low-power wireless transmission. To facilitate portability and operational efficiency, the device is powered by a lithium-ion battery, supplemented by a buck-boost converter and dedicated low-dropout (LDO) voltage regulators for both analog and digital circuits, ensuring clean and stable power rails that are essential for the performance of sensitive electronic components.

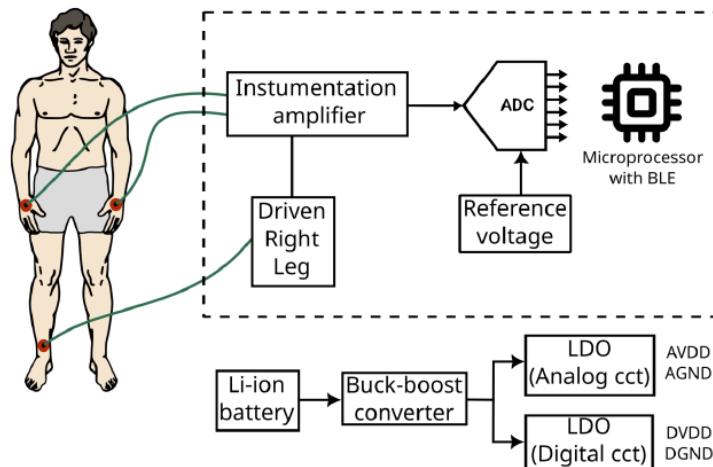


Figure 1: System Architecture-Block Diagram

This design features a comprehensive Printed Circuit Board (PCB) that integrates all functional blocks, adhering to best practices for signal integrity, grounding, power distribution, and analog-digital isolation. The final deliverables include the PCB schematic, layout, supporting documentation, and a brief report that explains the key design decisions and implementation considerations.

2 Subsystem Breakdown

Instrumentation Amplifier

The instrumentation amplifier is responsible for amplifying the low-amplitude ECG signals acquired from the body electrodes with high precision. Its high common mode rejection ratio (CMRR) enables accurate extraction of the differential ECG signal while minimizing common mode noise such as power line interference and motion-induced artifacts. This stage forms the core of the analog front end.

Driven Right Leg (DRL) Circuit

The Driven Right Leg (DRL) circuit actively stabilizes the patient's common mode voltage by feeding back an inverted common mode signal to the right leg electrode. This significantly reduces electromagnetic interference, enhances common mode rejection, and improves the overall quality of the ECG measurement.

Analog-to-Digital Converter (ADC)

The ADC converts the conditioned analog ECG signal into digital form for microcontroller-based processing. A high-resolution, low-noise delta-sigma ADC is employed to capture subtle ECG waveform features with high fidelity. The ADC is operated in differential mode to improve noise immunity and measurement accuracy.

Reference Voltage Generator

The reference voltage generator provides a stable, low-noise voltage reference to the ADC and analog front-end circuitry. Its low drift and minimal noise characteristics ensure consistent measurement accuracy, regardless of supply variations or temperature changes.

Microcontroller with BLE Connectivity

The microcontroller handles signal processing, filtering, system control, and data management. Integrated Bluetooth Low Energy (BLE) allows efficient wireless transmission of ECG data to smartphones or monitoring stations. Its low-power operation enhances battery life, making it suitable for wearable applications.

Li-ion Battery

A Li-ion battery serves as the primary power source for the device. Its high energy density, compact size, and stable operating voltage range (3.0–4.2 V) make it ideal for portable biomedical devices requiring long-term operation and user comfort.

Buck-Boost Converter

The buck-boost converter regulates the variable battery voltage to a stable intermediate supply rail, ensuring consistent device operation throughout the battery discharge cycle. It steps the voltage up or down as needed, isolating the system from battery fluctuations.

Analog Low Dropout Regulator (LDO)

The analog LDO produces a clean, low-noise supply voltage (AVDD) for sensitive components such as the instrumentation amplifier, ADC, and reference voltage circuit. By attenuating switching noise from the DC-DC converter, it preserves the accuracy of analog signal processing.

Digital Low Dropout Regulator (LDO)

The digital LDO provides a regulated supply (DVDD) to the microcontroller and other digital circuits. Separating digital and analog supplies minimizes noise coupling, improving both digital stability and analog signal integrity.

3 PCB Design Choices

The PCB design for the wearable ECG signal acquisition system prioritizes low noise, strong signal integrity, and effective separation between analog, digital and power domains. Careful attention was given to the stackup configuration, component placement, routing strategies, and grounding methods to ensure accurate bio potential measurement and reliable device operation.

PCB Stack Up and Layer Selection

A **0.8 mm, 4-layer PCB stack up** was selected to minimize the physical distance between layers. The reduced thickness results in shorter return paths, lower loop inductance, and improved electromagnetic performance. This is particularly important for millivolt-level ECG signals, where signal integrity must be maintained across the entire analog front end.

The PCB follows a **Signal-Ground-Power-Signal** layer configuration, which provides:

- A continuous and uninterrupted ground plane to shield sensitive traces
- Improved impedance control and reduced crosstalk
- Stable return paths directly beneath signal traces
- Effective isolation between analog and digital signal routing.

This stack up supports a robust mixed signal environment and enhances the accuracy of the ECG acquisition.

Noise Minimization and Component Placement

To minimize noise coupling into the low-amplitude ECG signal path, the analog front end is placed on the opposite side of the PCB and in a diagonally opposite corner relative to the power circuitry and antenna. This three-dimensional separation maximizes physical isolation between noisy switching domains and sensitive analog blocks, significantly improving immunity to high-frequency ripple generated by the buck-boost converter.

A continuous internal ground plane further isolates the analog routing from power traces. The ground system is partitioned into AGND, DGND, and the main GND according to the mixed signal architecture. This ensures that digital switching currents and power return paths do not interfere with the analog reference and maintains a clean, stable ground for the front end.

Critical analog components, including the instrumentation amplifier, ADC, reference circuit, and DRL network, are clustered together with short, direct routing to preserve signal fidelity. ECG input traces are routed as balanced differential pairs where possible, improving common-mode noise rejection and maintaining signal symmetry. All analog supply rails to the op-amps and ADC are locally decoupled with 100 nF C0G capacitors placed directly at the device pins. This provides effective suppression of power-borne noise and enhances the stability of the analog section.

Component Selection and Protection Strategy

The analog front end was designed following Texas Instruments' recommendations to minimize noise and maximize performance. The number of op-amps was kept to a minimum to reduce internal noise sources, and low quiescent current devices were selected to maintain energy efficiency without compromising signal fidelity.

Input stage protection is provided by **TVS diodes**, which safeguard against electrostatic discharge (ESD) and transient overvoltages. This protection ensures the reliability and robustness of the device under real-world operating conditions. Additionally, passive component selection, such as precision resistors and low noise capacitors, was optimized to maintain signal integrity and minimize offset or drift in the analog front end.

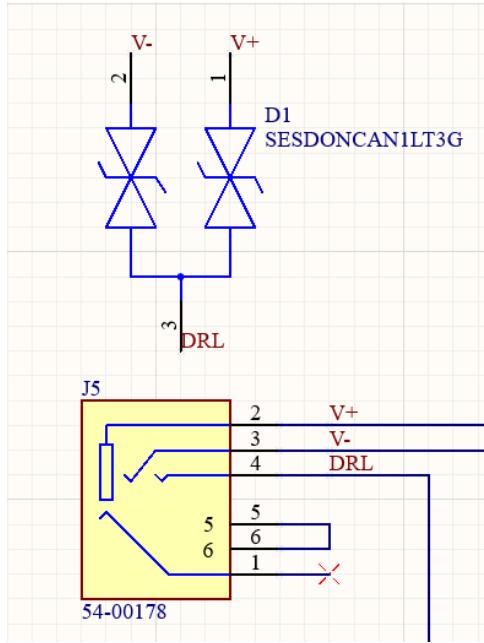


Figure 2: TVS Diode Connection in the ECG Input Stage

ADC Configuration

The ADC used in the system supports both common mode and differential mode acquisition. For improved noise immunity and rejection of external interference, the ECG front end is interfaced with the ADC using its **differential mode**, which provides superior performance for low-amplitude biopotential signals.

Ground Partitioning and Antenna Clearance

Given the mixed signal nature of the system, three separate ground sections are used:

- **AGND** for the analog front end,
- **DGND** for the ADC, microcontroller and BLE circuitry,
- **GND** for the power management, and delivery.

These sections are isolated to prevent digital switching noise and power ripple from contaminating the sensitive analog ground return paths. Furthermore, in accordance with the antenna manufacturer's specifications, the ground plane was removed beneath the antenna region to enable proper radiation performance and reduce electromagnetic interference with the BLE module.

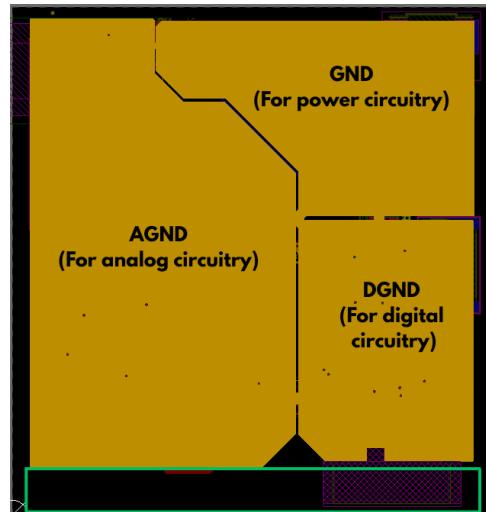


Figure 3: PCB layout of AGND, DGND, and GND regions, with the antenna clearance zone (in green)

4 Grounding Methods

Proper grounding is critical in ECG acquisition systems because bio potential signals are extremely low in amplitude and highly susceptible to interference. This design uses a combination of star point grounding and a four layer PCB stack up to ensure clean reference levels, minimize noise coupling and maintain stable operation.

According to the antenna specifications, the ground plane is intentionally removed beneath the antenna region to support correct radiation performance and reduce unwanted coupling.

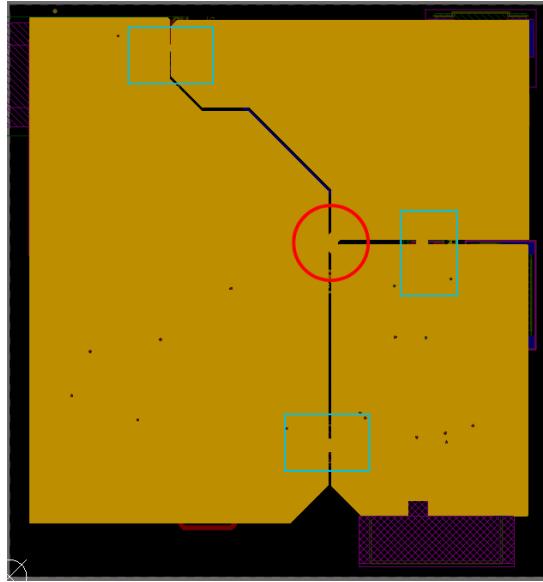


Figure 4: Ground layout showing the single star-point connection (in red) and the localized connection (in blue)

Star Point Grounding

Star point grounding is used to avoid ground loops and limit the transfer of digital switching noise into the analog front end. In this approach, all main ground return paths converge at a single common reference point rather than forming multiple looped ground paths.

The analog ground (AGND), which is associated with the instrumentation amplifier, ADC, reference voltage circuitry and DRL network is routed back to a dedicated star node. The digital ground (DGND) from the microcontroller and BLE subsystem also returns to the same star location but remains physically separated from the analog ground on the board. This prevents digital return currents from flowing through sensitive analog paths and improves the overall common mode noise rejection of the ECG system.

In addition to the star point structure, several controlled ground plane connections are introduced to prevent the creation of local potential differences that could lead to unintended loop currents. These localized ground connections are added only where they are electrically required:

- **AGND-DGND under the ADC:** Ensures the converter sees a consistent local ground reference.
- **GND-AGND under the analog LDO:** Prevents noise from appearing across the regulator's reference pins.
- **GND-DGND under the digital LDO:** Ensures DVCC stability.

These selective connections ensure that no unintended ground loops are formed while still giving each mixed signal component the consistent reference it requires.

Four Layer PCB Stack Up

A four-layer PCB structure is used to improve grounding reliability and overall signal integrity. The stack-up is arranged as follows:

#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.6mil	3.8	
1	Signal 1	CF-004	Signal	1oz	1.378mil		
	Dielectric 1	NP-155F	Prepreg		7.992mil	4.4	0.02
2	GND	CF-004	Signal	1oz	1.181mil		
	Dielectric 2	NP-155F	Core		9.843mil	4.23	0.02
3	POWER	CF-004	Signal	1oz	1.181mil		
	Dielectric 3	NP-155F	Prepreg		7.992mil	4.4	0.02
4	Signal 2	CF-004	Signal	1oz	1.378mil		
	Bottom Solder	Solder Resist	Solder Mask		0.6mil	3.8	
	Bottom Overlay		Overlay				

Figure 5: Layer Stack Manager

- **Layer 1 Top Layer:** Component placement and critical analog, digital signal routing.
- **Layer 2 Ground Plane:** A continuous ground reference supporting both analog and digital domains.
- **Layer 3 Power Plane:** Distribution of AVCC, DVCC.
- **Layer 4 Bottom Layer:** Some digital routing, BLE traces, and Power circuitry routing.

The continuous ground plane on Layer 2 provides a low impedance return path and a stable reference for low amplitude ECG signals. Analog and digital traces are routed on different layers to reduce crosstalk, and return currents naturally follow the shortest path beneath their corresponding traces. The separation of analog and digital routing zones, together with a unified ground reference plane, supports robust analog digital partitioning and helps maintain stable signal integrity across the system.

5 Schematic and PCB Design

Schematic Design

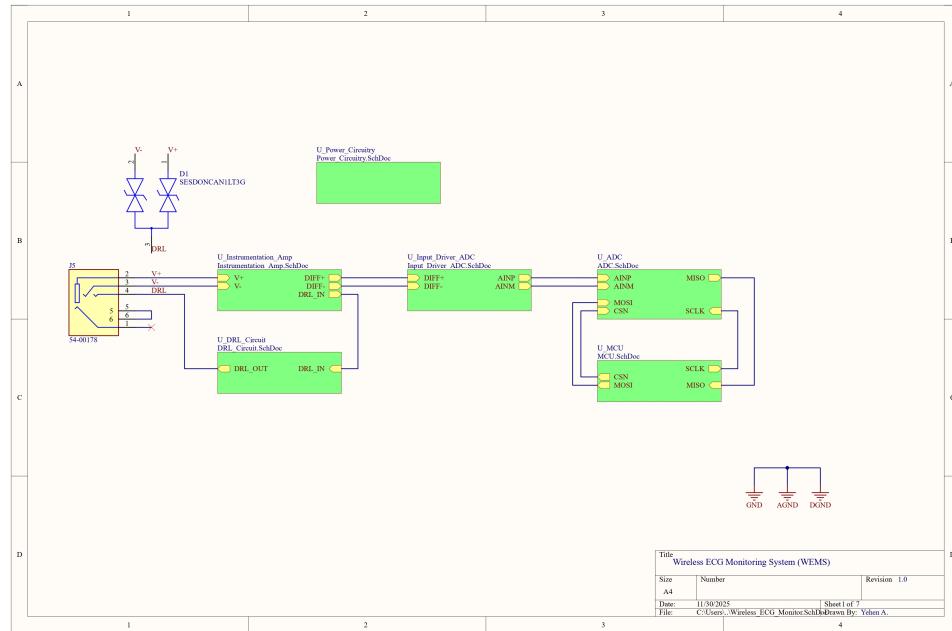


Figure 6: Hierarchical Overview

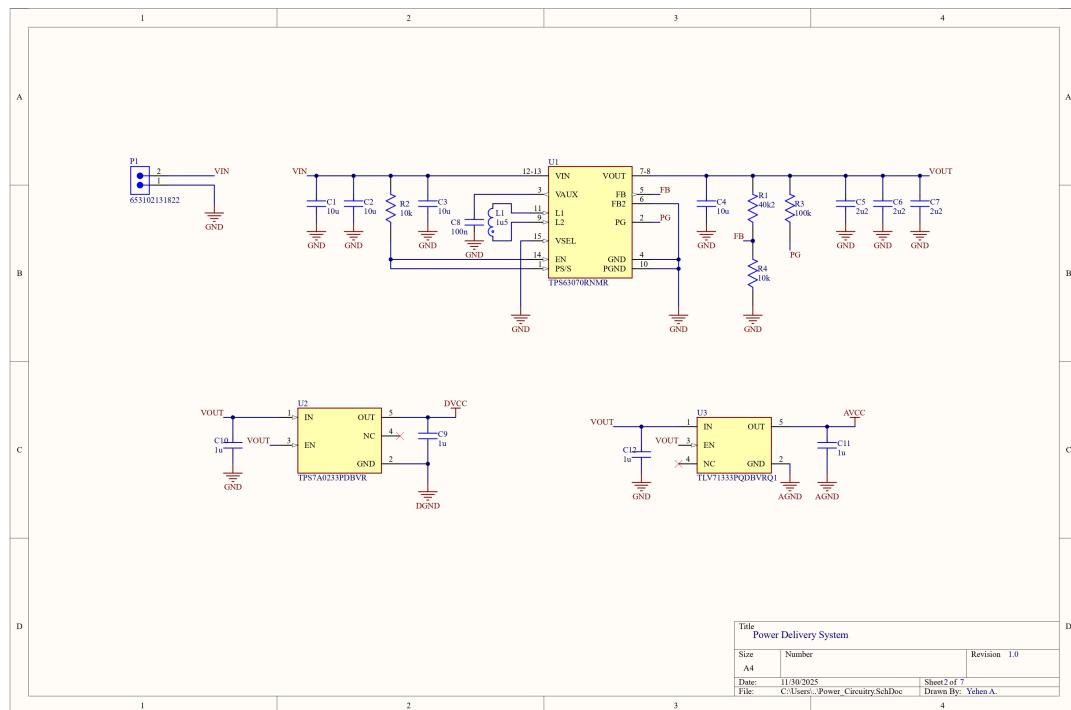


Figure 7: Power Delivery System

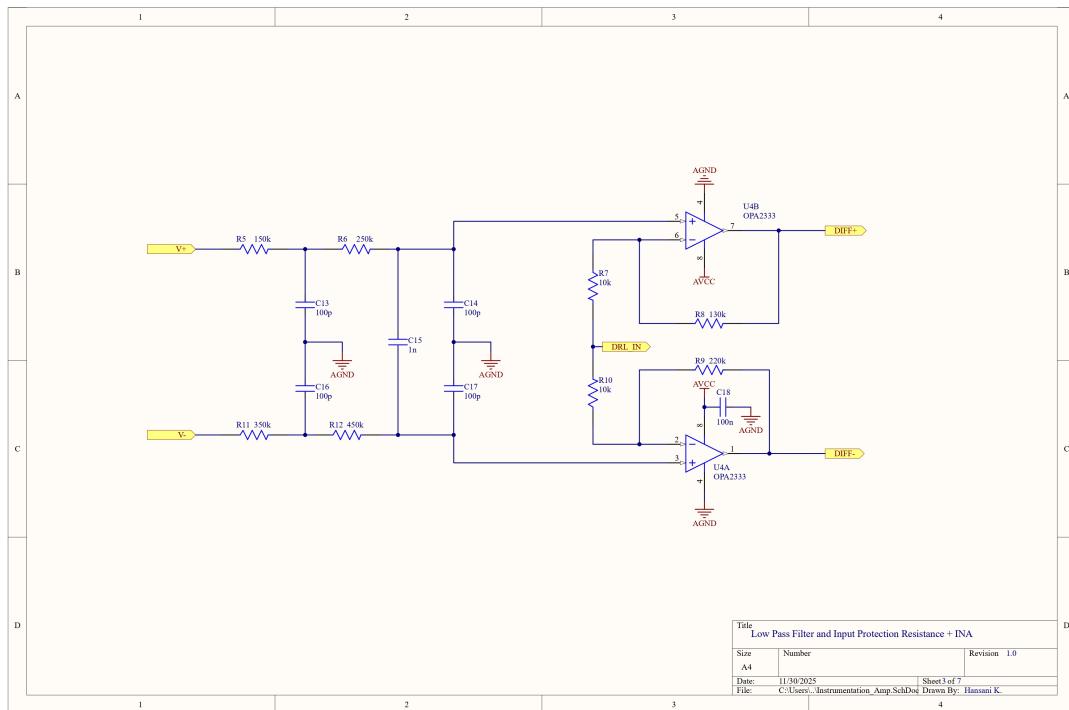


Figure 8: Low Pass Filter and Instrumentation Amplifier

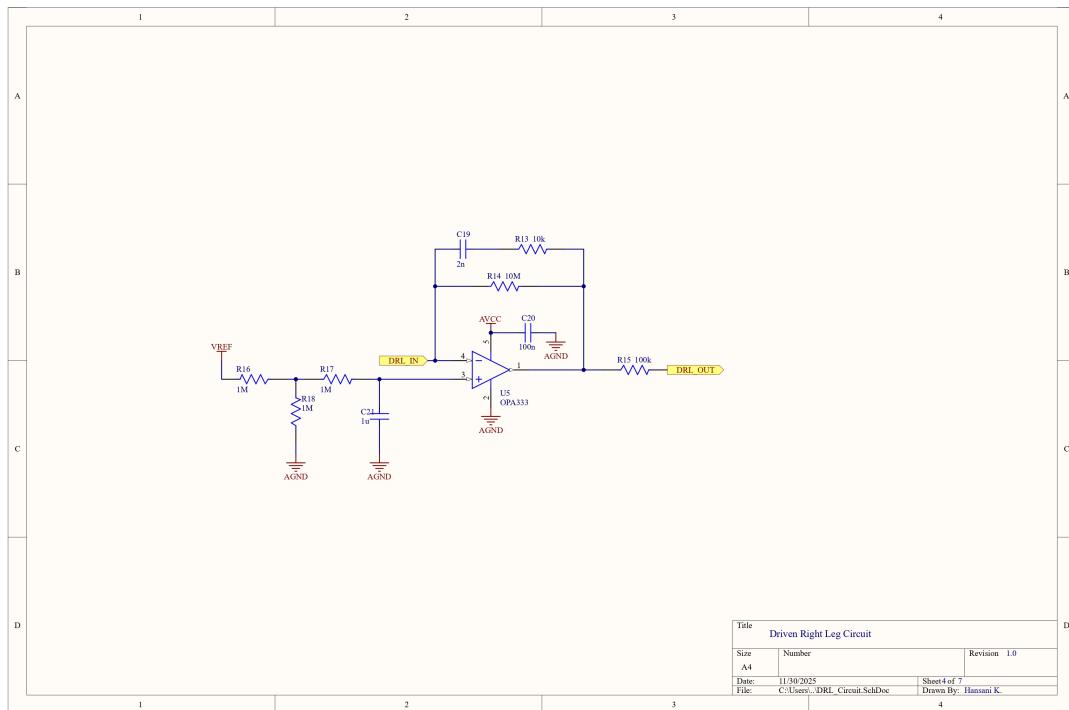


Figure 9: Driven Right Leg Circuit

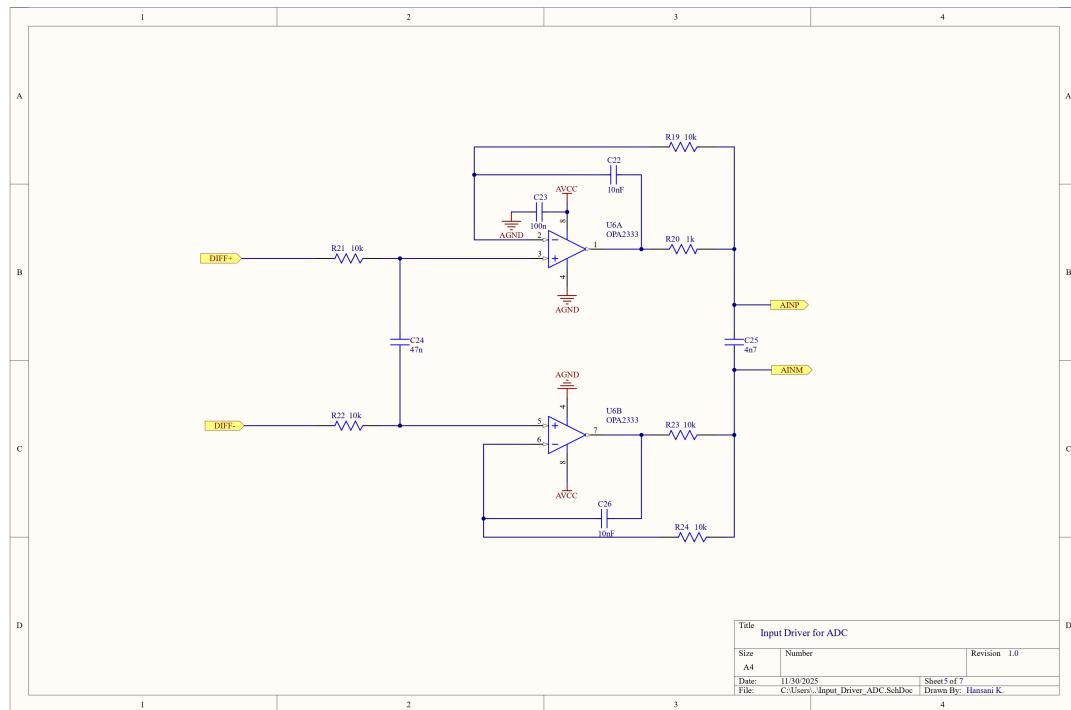


Figure 10: Input Driver for ADC

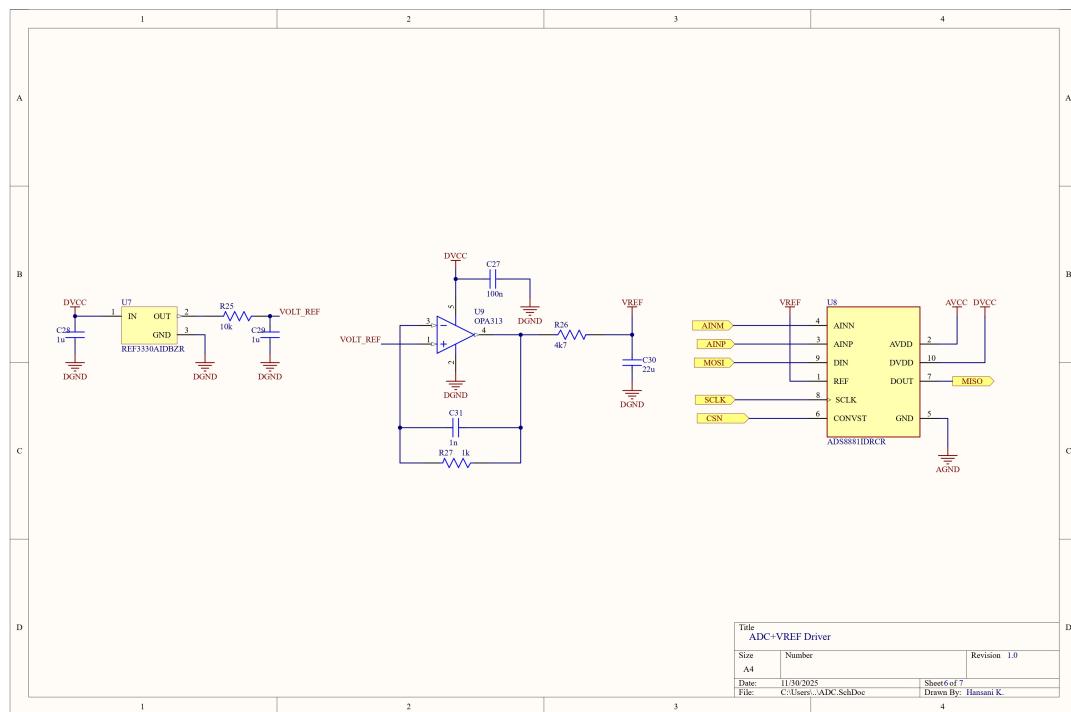


Figure 11: ADC and VREF Driver

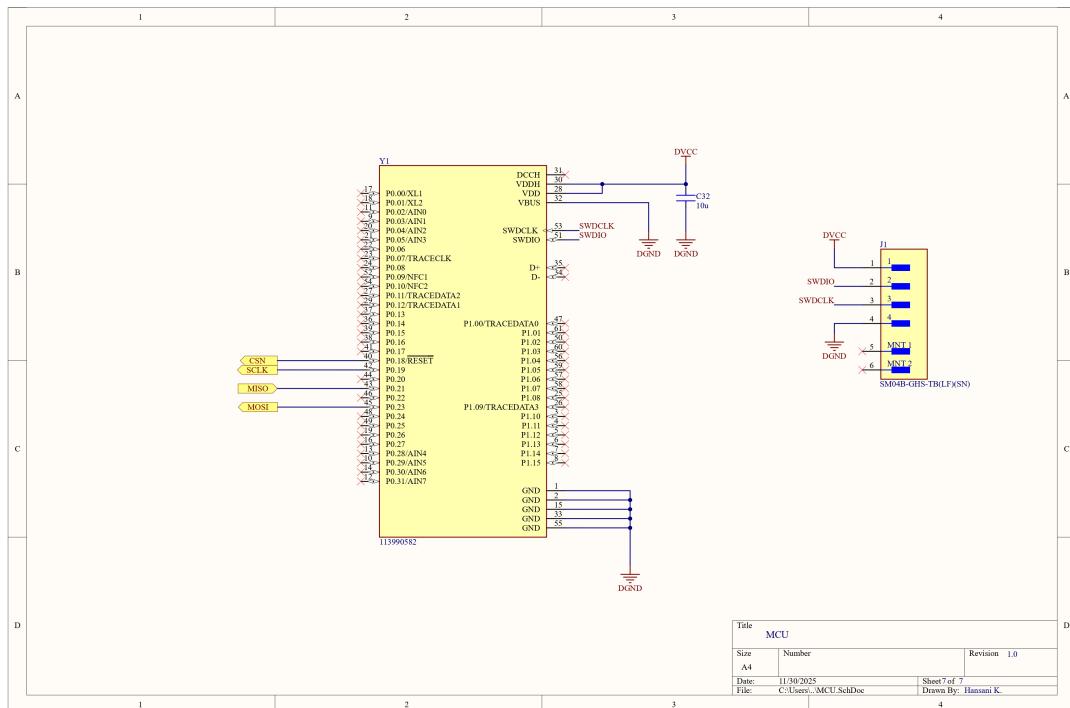


Figure 12: MCU

PCB Design

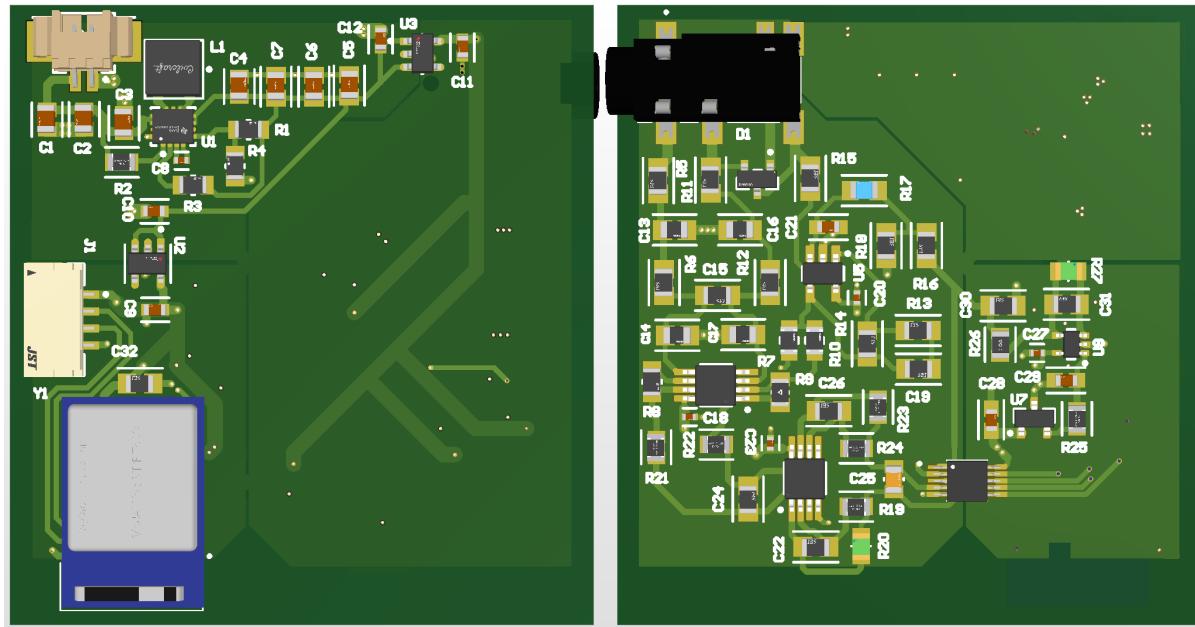


Figure 13: Top View

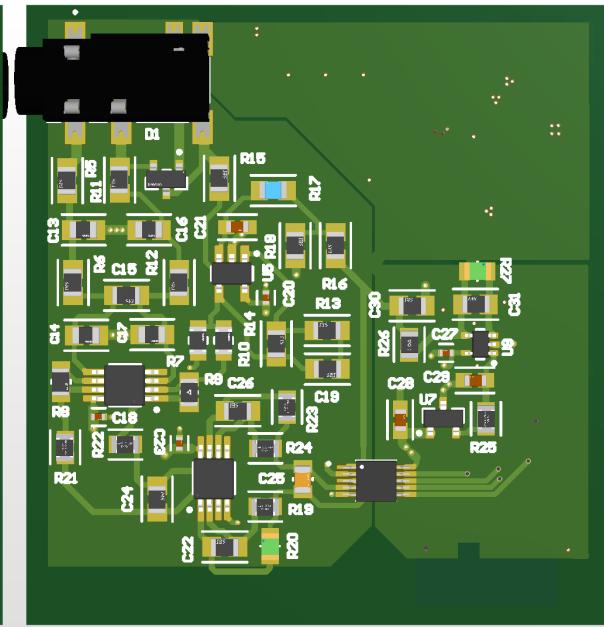


Figure 14: Bottom View



Figure 15: Signal Layer 1

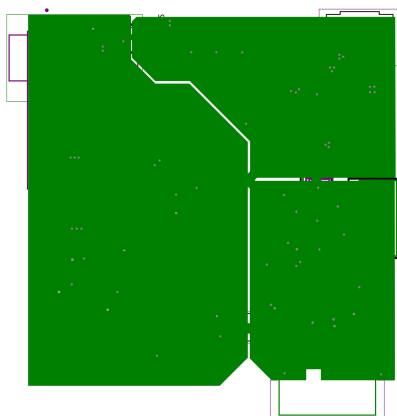


Figure 16: Ground Plane

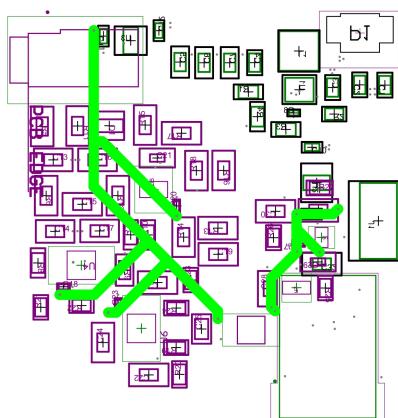


Figure 17: Power Plane

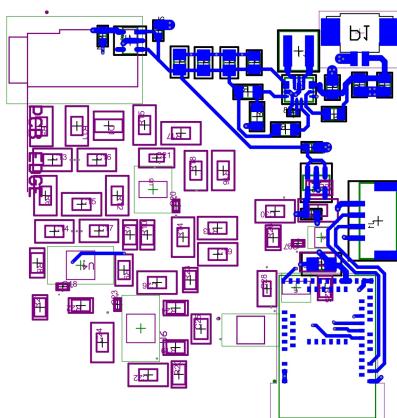


Figure 18: Signal Layer 2

Bill of Materials



Design Rule Verification Report

Date: 11/30/2025 **Time:** 10:27:59 AM **Elapsed Time:** 00:00:01 **Warnings:** 0 **Rule Violations:** 0
Filename: <D:\Yehen Folder\Altium Projects\Wireless ECG\Wireless ECG.PcbDoc>

Summary

Warnings	Count
	Total 0
Rule Violations	Count
Clearance Constraint (Gap=8mil)_(OnLayer('Bottom Layer') Or IsVia Or IsThruPin), (OnLayer('Bottom Layer') Or IsVia Or IsThruPin)	0
Clearance Constraint (Gap=4mil)_(OnLayer('Mid Layer 2') Or IsVia Or IsThruPin), (OnLayer('Mid Layer 2'))	0
Clearance Constraint (Gap=4mil)_(OnLayer('Mid Layer 1') Or IsVia Or IsThruPin), (OnLayer('Mid Layer 1'))	0
Clearance Constraint (Gap=8mil)_(OnLayer('Top Layer') Or IsVia Or IsThruPin), (OnLayer('Top Layer') Or IsVia Or IsThruPin)	0
Short-Circuit Constraint (Allowed=No)_(All),(All)	0
Un-Routed Net Constraint _(_All)_.	0
Modified Polygon (Allow modified: No),_(Allow shelved: No)	0
Width Constraint (Min=4mil)_(Max=71497.938mil)_(Preferred=8mil)_(All)	0
Routing Topology Rule(Topology=Shortest)_(All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=11.811mil)_(Conductor Width=4mil)_(Air Gap=4mil)_(Entries=4)_(OnLayer('Mid Layer 1'))	0
Power Plane Connect Rule(Relief Connect)(Expansion=11.811mil)_(Conductor Width=8mil)_(Air Gap=8mil)_(Entries=4)_(OnLayer('Bottom Layer'))	0
Power Plane Connect Rule(Direct Connect)(Expansion=20mil)_(Conductor Width=10mil)_(Air Gap=10mil)_(Entries=4)_(InPadClass('PowerPads'))	0

<u>Power Plane Connect Rule(Relief Connect)(Expansion=11.811mil).(Conductor Width=8mil).(Air Gap=8mil)(Entries=4)(OnLayer('Top Layer')).</u>	0
<u>Power Plane Connect Rule(Relief Connect)(Expansion=11.811mil).(Conductor Width=4mil).(Air Gap=4mil)(Entries=4)(OnLayer('Mid Layer 2')).</u>	0
<u>Hole Size Constraint (Min=7.874mil).(Max=248.031mil)(All).</u>	0
<u>Hole To Hole Clearance (Gap=5mil)(All),(All)</u>	0
<u>Minimum Solder Mask Sliver (Gap=0mil)(All),(All)</u>	0
<u>Silk To Solder Mask (Clearance=2mil)(IsPad),(All)</u>	0
<u>Silk to Silk (Clearance=0mil)(All),(All)</u>	0
<u>Net Antennae (Tolerance=0mil)(All)</u>	0
<u>Board Clearance Constraint (Gap=0mil)(All)</u>	0
<u>Height Constraint (Min=0mil).(Max=71497.938mil).(Prefered=500mil)(All)</u>	0
Total	0