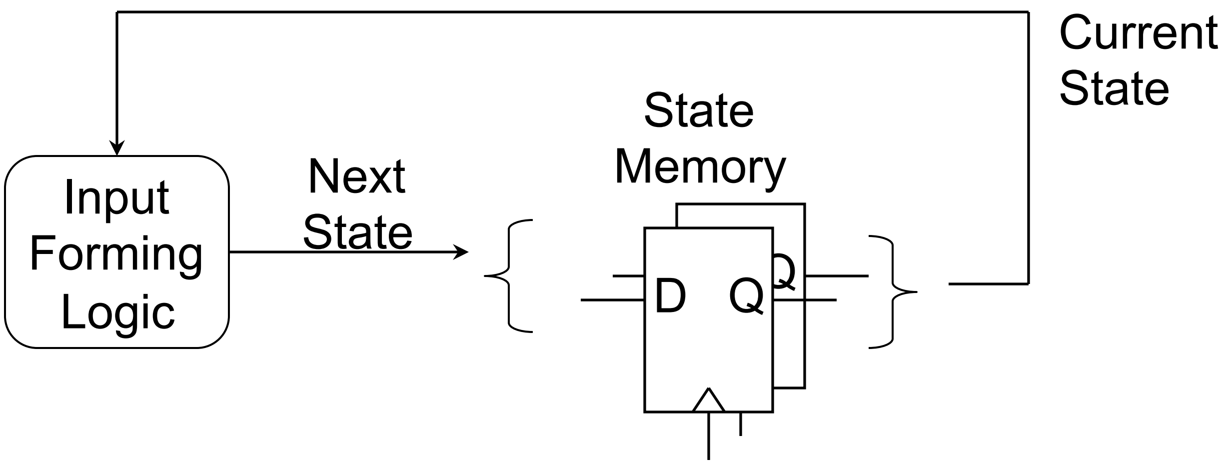
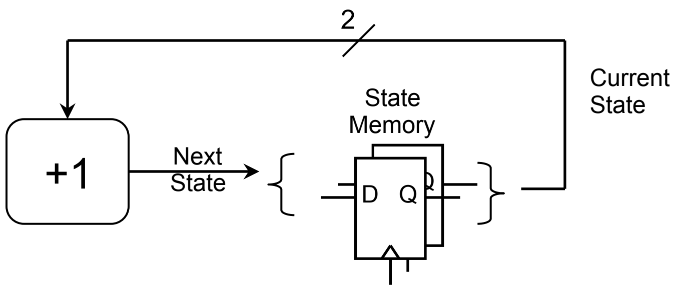
COUNTERS

Counters
Transition Tables
Moore Outputs
Counter Timing

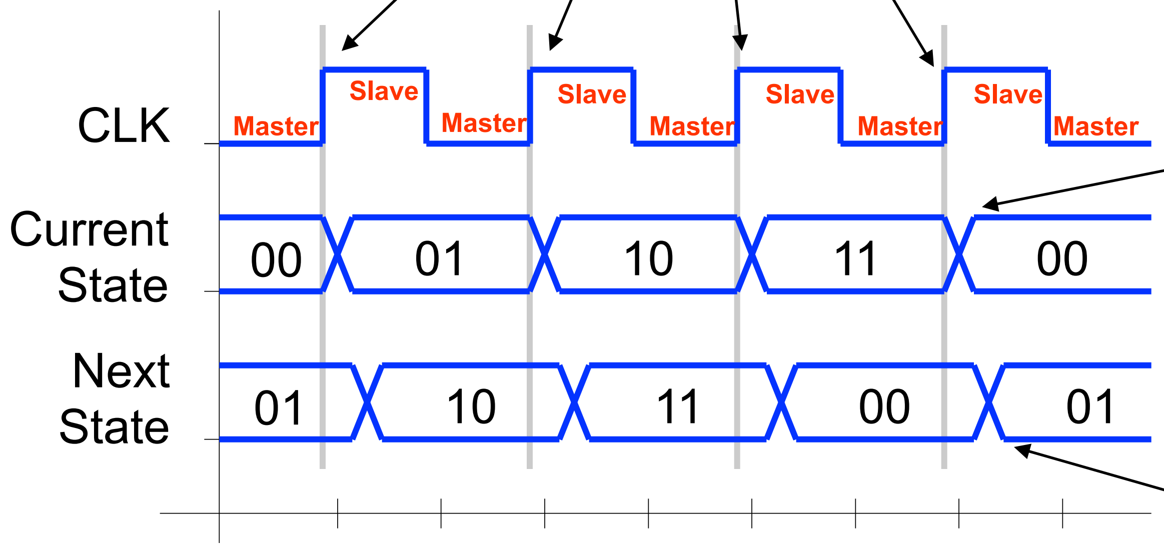
General Sequential Systems



A Sequential Counter



Clock edges…



The current state loads the next state values in response to the clock edge.

IFL reacts after some gate delays to produce a new next state.

Transition Table for 2-Bit Counter

Current State	Next State
00	01
01	10
10	11
11	00

Current State		Next State	
Q1	Q0	N1	N0
0	0	0	1
0	1	1	0
1	0	1	1
1	1	0	0

It is the truth table for the input forming logic…

It describes what the *next state* values are as a function of the *current state* (clock is assumed)

Implementation of 2-Bit Counter

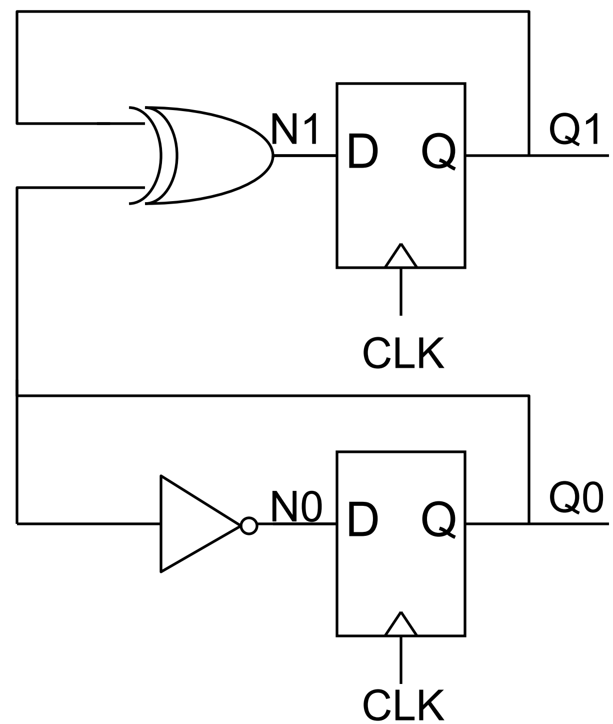
Current State		Next State	
Q1	Q0	N1	N0
0	0	0	1
0	1	1	0
1	0	1	1
1	1	0	0

Q0 \ Q1	0	1
0	1	1
1	0	0

N0 = Q0'

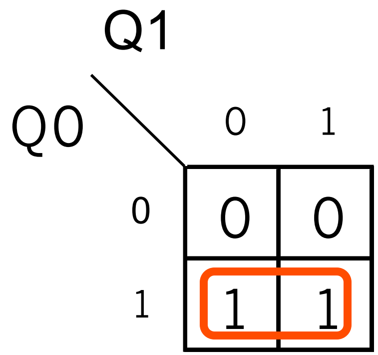
Q0 \ Q1	0	1
0	0	1
1	1	0

N1 = $Q1 \oplus Q0$

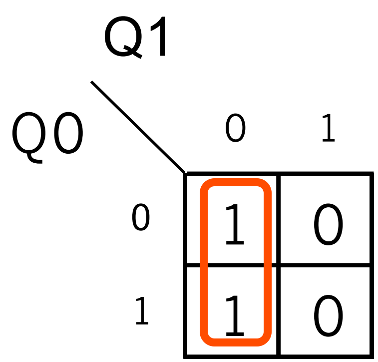


Example 2 – A Gray Code Counter

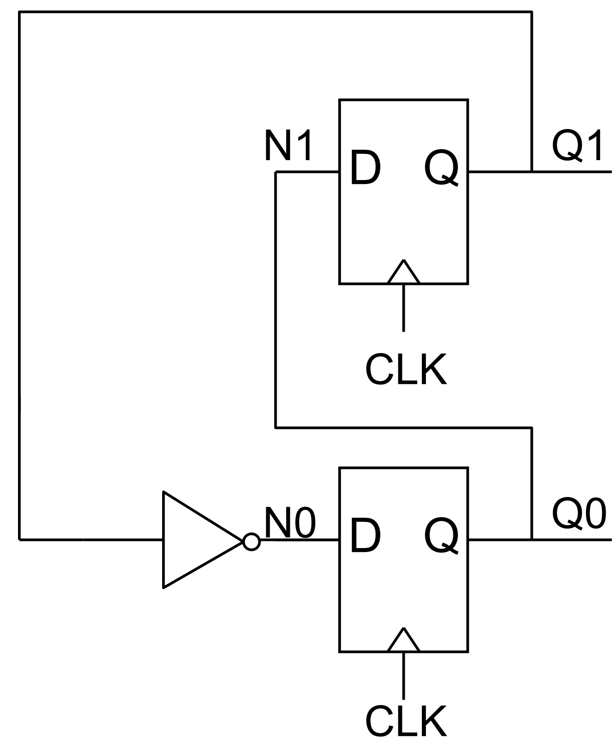
Q1	Q0	N1	N0
0	0	0	1
0	1	1	1
1	0	0	0
1	1	1	0



N1= Q0



N0 = Q1'



Example 3 – Not All Count Values Used

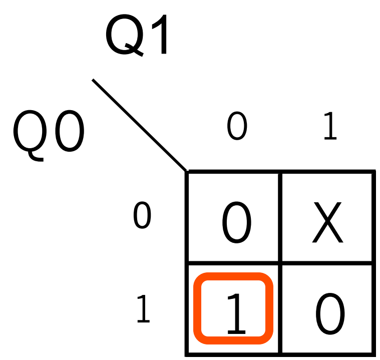
Desired count sequence = 00 – 01 – 11 - 00 …

Q1	Q0	N1	N0
0	0	0	1
0	1	1	1
1	0	?	?
1	1	0	0

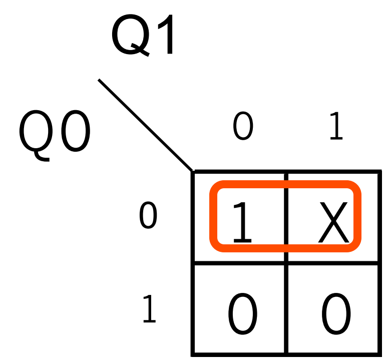
What should next state for 10 be?

Example 3 – Not All Count Values Used

Q1	Q0	N1	N0
0	0	0	1
0	1	1	0
1	0	X	X
1	1	0	0



N1 = Q0•Q1'



N0 = Q0'

Do the normal K-map minimization with don't cares

Example 4 – A Ring Counter

Desired count sequence = 001 – 010 – 100 - 001 …

Q2	Q1	Q0	N2	N1	N0
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

Example 4 – A Ring Counter

Desired count sequence = 001 - 010 - 100 - 001 …

Q2	Q1	Q0	N2	N1	N0
0	0	0	X	X	X
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	X	X	X
1	0	0	0	0	1
1	0	1	X	X	X
1	1	0	X	X	X
1	1	1	X	X	X

N2

Q_1Q_0 \ Q_2	0	1
00	X	
01		X
11	X	X
10	1	X

N1

Q_1Q_0 \ Q_2	0	1
00	X	
01	1	X
11	X	X
10		X

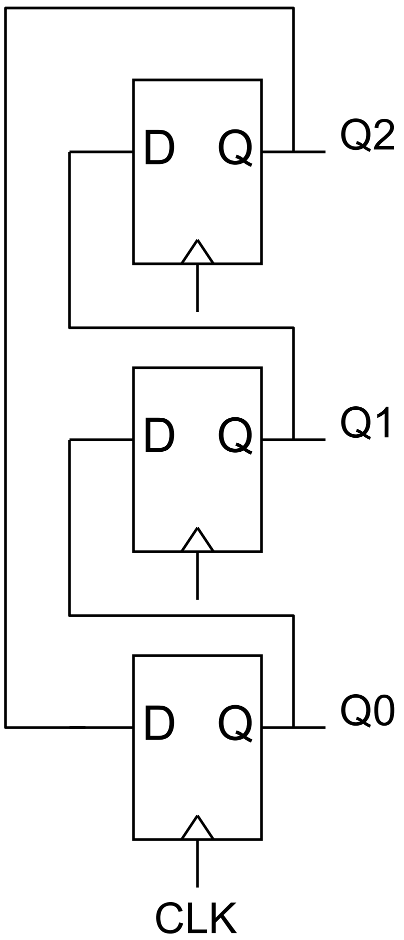
N0

Q_1Q_0 \ Q_2	0	1
00	X	1
01		X
11	X	X
10		X

Doing KMaps leads to:

N2 = Q1
N1 = Q0
N0 = Q2

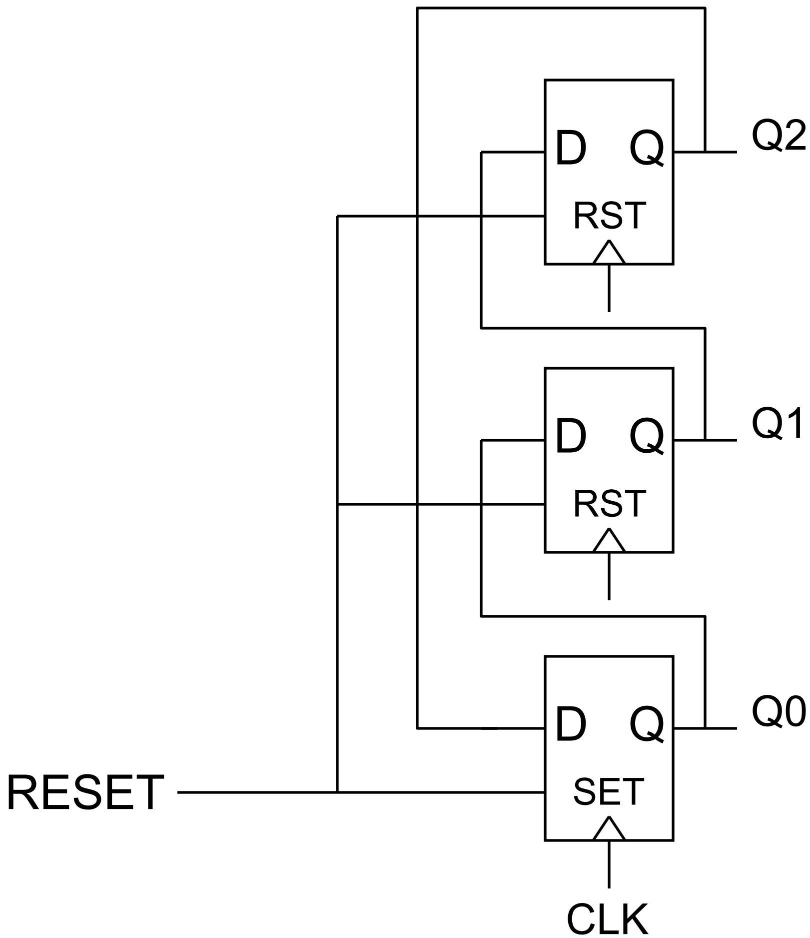
Example 4 – A Ring Counter



Initial State

- When a sequential circuit is powered on, we have no guarantee it will start in any particular state
- We must make sure our counters don't start in an invalid state
  - They could remain stuck in invalid states!
- Digital systems should have a reset signal that is asserted after power up
  - This reset could go into IFL or into the RESET inputs on flip flops.

A Ring Counter with Reset

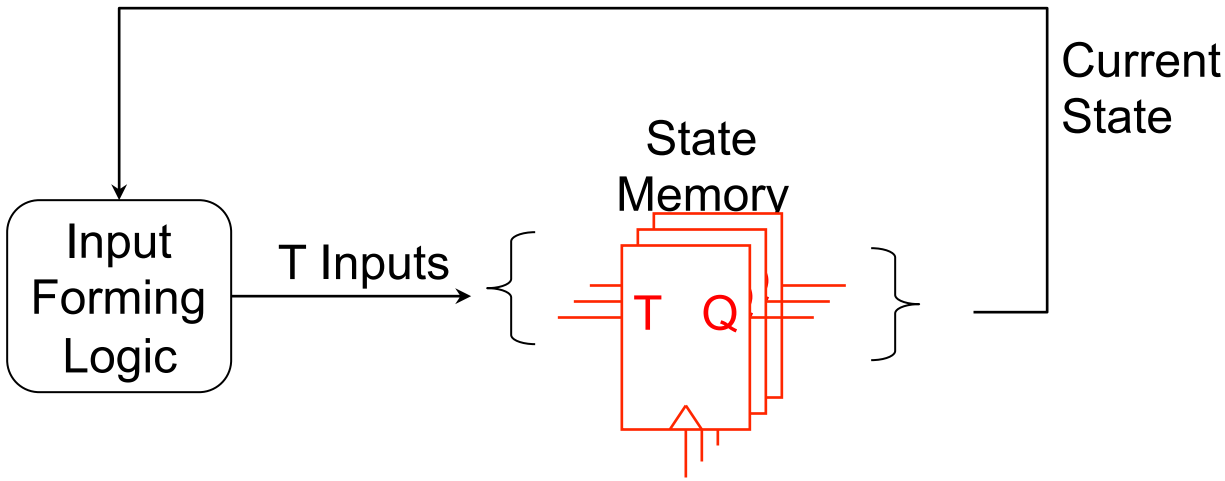


Reset causes circuit to start in state "001"

General Counter Design Procedure

- Write transition table for counter
  - Use X's as appropriate
- Reduce each NX variable to a minimized equation
- Implement input forming logic (IFL) using gates
- Draw schematic using FF's + IFL

Counters With Alternative FF's



Excitation Table for T Flip Flop

Transition Table

T	Q	Q+
0	0	0
0	1	1
1	0	1
1	1	0

Rearranging rows and/or columns…

Excitation Table

Q	Q+	T
0	0	0
0	1	1
1	0	1
1	1	0

Tells how inputs affect output

Tells what input is needed to achieve desired output transition

In the end, they are the same table, just rearranged…

TFF Counter Design Using Augmented Transition Table

Current State			Next State			TFF Inputs		
Q2	Q1	Q0	N2	N1	N0	T2	T1	T0
0	0	0	0	0	1			
0	0	1	0	1	0			
0	1	0	0	1	1			
0	1	1	1	0	0			
1	0	0	1	0	1			
1	0	1	1	1	0			
1	1	0	1	1	1			
1	1	1	0	0	0			

Next state values

Inputs to apply to achieve desired next state

TFF Counter Design Using Augmented Transition Table

Current State			Next State			TFF Inputs		
Q2	Q1	Q0	N2	N1	N0	T2	T1	T0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

Next state values

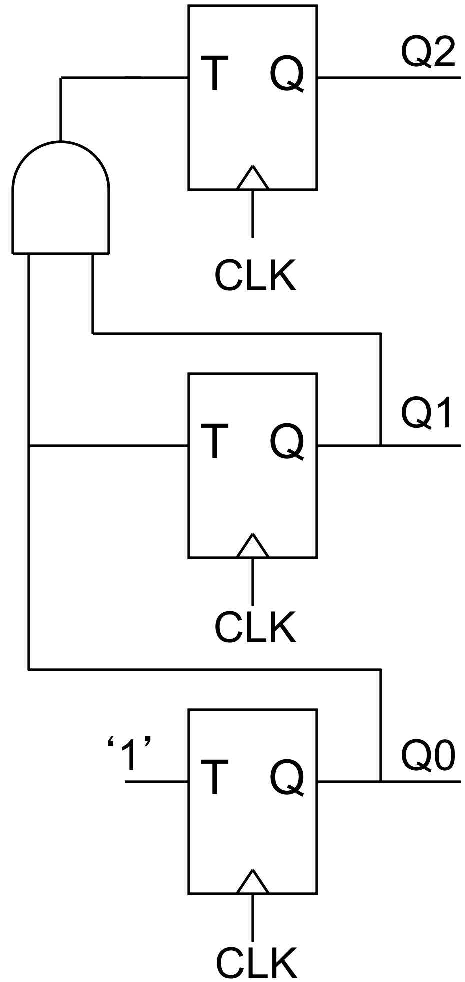
Inputs to apply to achieve desired next state

T2

Q_1Q_0 \ Q_2	0	1
00		
01		
11	1	1
10		

T2 = Q1•Q0
T1 = Q0
T0 = ‘1’

TFF Counter Design



Excitation Table for JK Flip Flop

J	K	Q	Q+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Tells how inputs affect output

Rearranging rows and/or columns…

Q	Q+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Tells what inputs to apply to achieve desired output transition

Do you see why the X's?

In the end, they are the same table, just rearranged…

JKFF Gray Code Counter Design

Q2	Q1	Q0	N2	N1	N0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1						
0	0	1	0	1	1						
0	1	0	1	1	0						
0	1	1	0	1	0						
1	0	0	0	0	0						
1	0	1	1	0	0						
1	1	0	1	1	1						
1	1	1	1	0	1						

Next state values

Inputs to apply to achieve desired next state

JKFF Gray Code Counter Design

Q2	Q1	Q0	N2	N1	N0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	1	0	X	1	X	X	0
0	1	0	1	1	0	1	X	X	0	0	X
0	1	1	0	1	0	0	X	X	0	X	1
1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	1	0	0	X	0	0	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	1	0	1	X	0	X	1	X	0

Next state values

Inputs to apply to achieve desired next state

J2 = Q1•Q0'
K2 = Q1'•Q0'

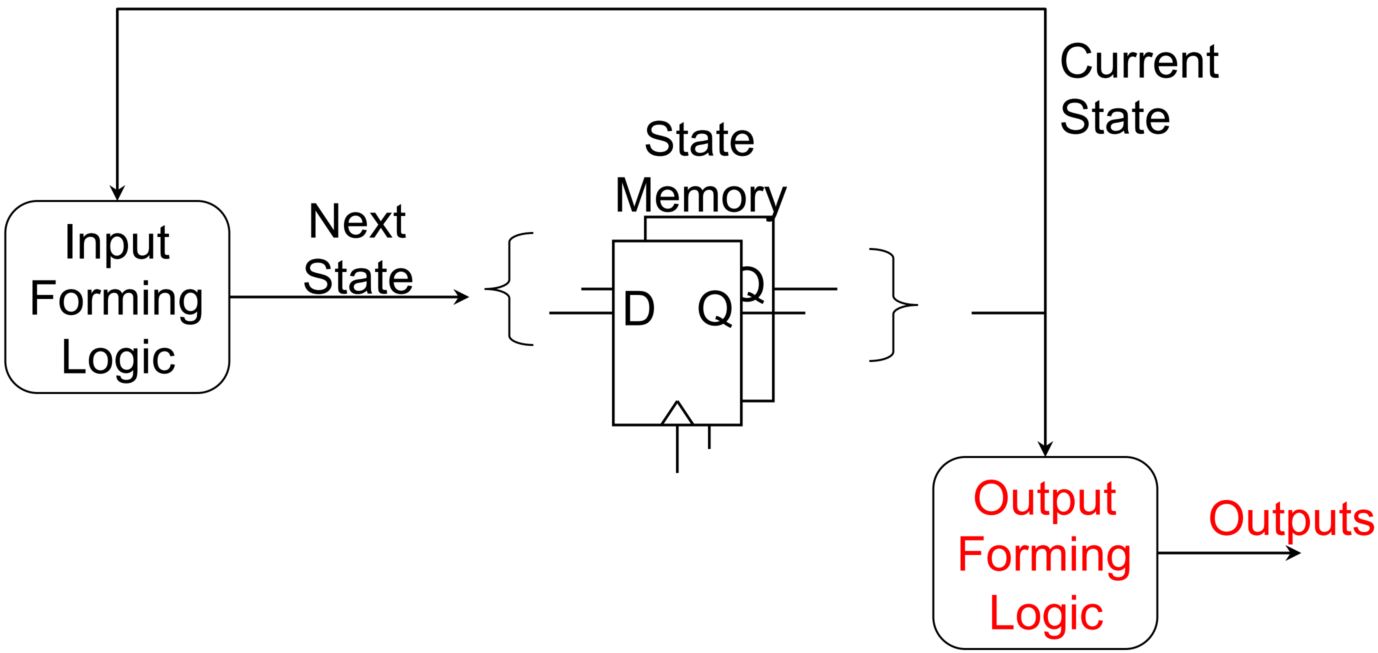
J1 = Q2'•Q0
K1 = Q2•Q0

J0 = Q2•Q1 + Q2'•Q1' = K0'
K0 = Q2'•Q1 + Q2•Q1' = Q2 ⊕ Q1

General Counter Design Procedure

- Write transition table for counter
  - Use X's as appropriate
  - <u>If not DFF's, augment table</u>
- Reduce each FF input variable to a minimized equation
- Implement IFL with gates
- Draw schematic using FF's + IFL

Counters With Outputs



$$\text{Outputs} = f\,(\text{CurrentState})$$

Counters With Outputs

Z=1 when count={0,3,6}

Q2	Q1	Q0	Z
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Z is called a *Moore* or *static* output.
It is a function only of the current state.

Combined Transition Table

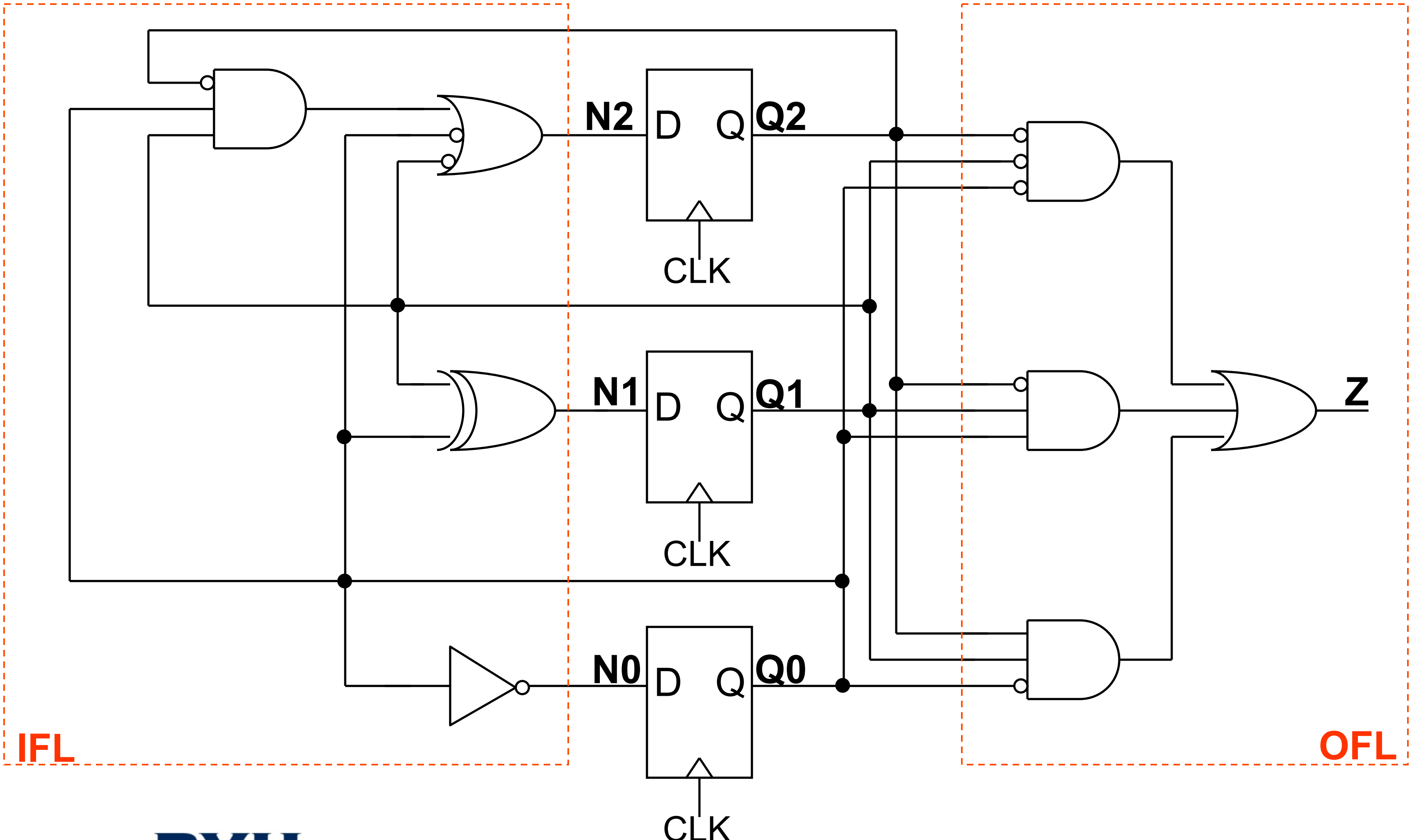
Q2	Q1	Q0	N2	N1	N0	Z
0	0	0	0	0	1	1
0	0	1	0	1	0	0
0	1	0	0	1	1	0
0	1	1	1	0	0	1
1	0	0	1	0	1	0
1	0	1	1	1	0	0
1	1	0	1	1	1	1
1	1	1	0	0	0	0

Current state   Next state   Output

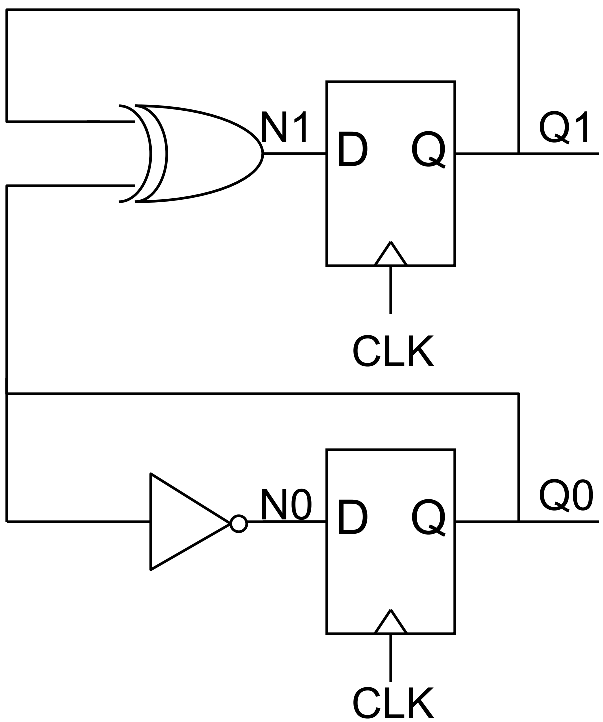
$$Z = Q2' \cdot Q1' \cdot Q0' + Q2' \cdot Q1 \cdot Q0 + Q2 \cdot Q1 \cdot Q0'$$

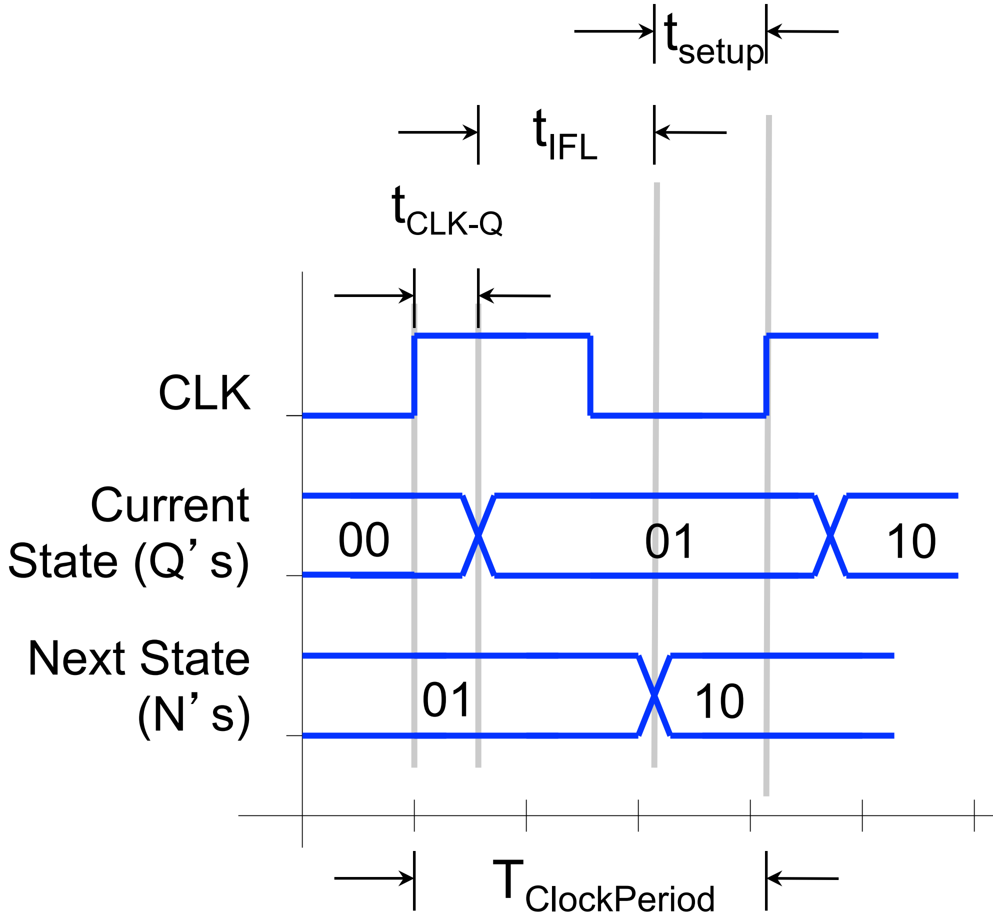
(implement OFL with gates)

Counter With A Moore Output



Counter Timing Characteristics





$$T_{ClockPeriod} >= t_{CLK\text{-}Q} + t_{IFL} + t_{setup}$$

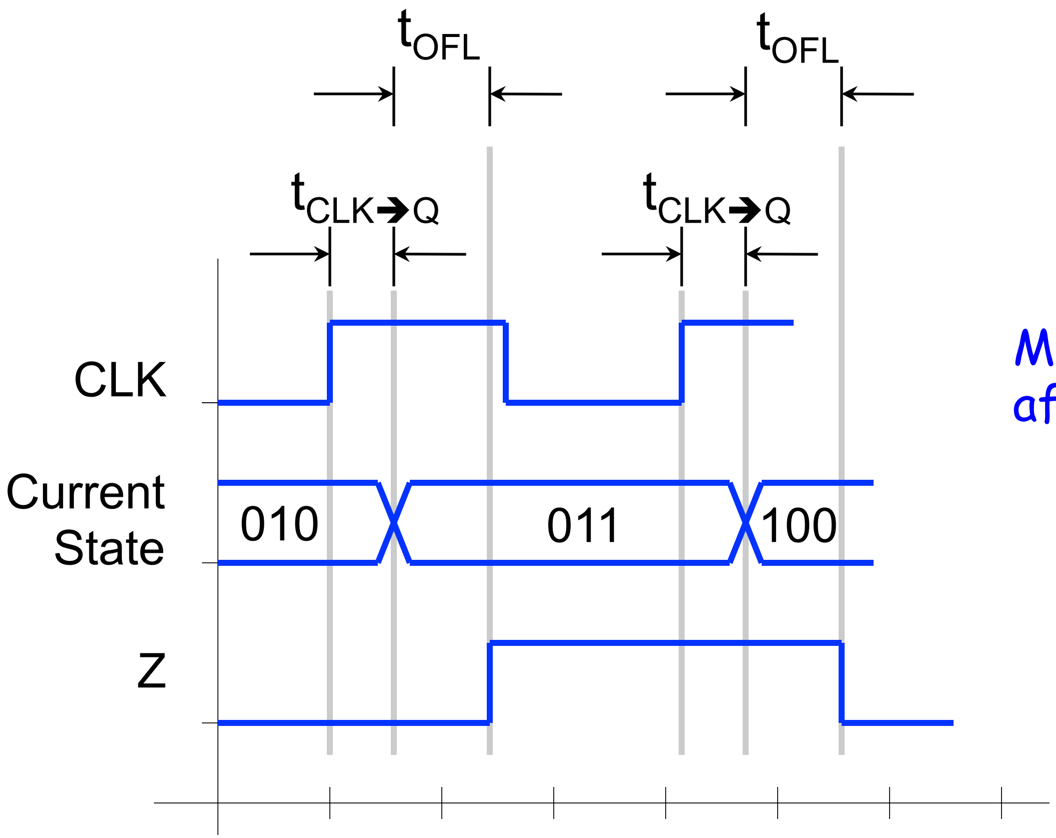
Counter Timing Example

- $t_{CLK \rightarrow Q}$ = 1ns
- t_{IFL} = 7ns
- t_{setup} = 2ns

- Recall the following:
  - T = Clock *period*
  - f = Clock *frequency* or *rate*
  - T = 1/f
  - f = 1/T

- T >= 1ns + 7ns + 2ns = 10 ns (10×10^{-9} s)
- f <= 1/T = 100 MHz (100×10^{6} Hz)

Output Timings



Moore outputs appear $t_{CLK \rightarrow Q} + t_{OFL}$ after the clock edge.

Counters and Timing

- The count sequence affects the size of IFL
- The size of the IFL affects t_{IFL}
- t_{IFL} affects $T_{ClockPeriod}$
- Choosing binary counts is not always fastest or smallest

Example Problem

- Design a 3-bit binary counter
- The Z output is TRUE iff count value is even
- The Y output is TRUE iff count value is multiple of 3