

Finite State Machines

Lecture 17

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Algorithmic State Machines (ASM) Charts

- The state diagrams and tables used in previous lectures are convenient for describing the behavior of FSMs that have only a few inputs and outputs.
- For larger machines the designers often use a different representation, called algorithmic state machine (ASM) chart.
- An ASM chart is a type of flowchart that can be used to represent transitions and generated outputs for an FSM. An ASM chart impliest timing information.

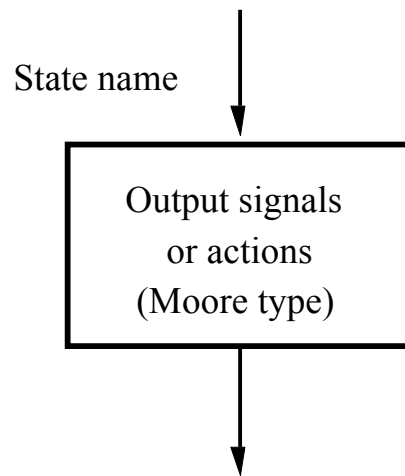
ASM Charts

- Three types of elements are used in ASM charts:
- **State box:** A rectangle represents the state of the FSM. The name of the state is indicated outside the box in the top-left corner. The Moore-type outputs are listed inside the box. These are the outputs that depend only on the values of the state variables that define the state (Moore outputs). It is customary to write only the name of the signal that has to be asserted. Thus is sufficient to write z , rather than $z=1$, to indicate that output z must have the value 1. Also, it may be useful to indicate an action that must be taken; for example $\text{Count} \leftarrow \text{Count} + 1$ specifies that the contents of a counter have to be incremented by 1. This is a simple way of saying that the control signal that causes the counter to be incremented must be asserted.

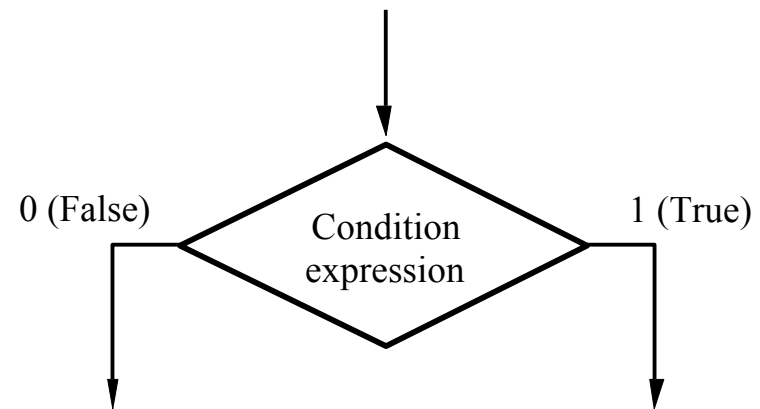
ASM Charts

- **Decision box:** A diamond indicates that the stated condition expression is to be tested and the exit path is to be chosen accordingly. The condition expression consists of one or more inputs to the FSM.
- **Conditional output box:** An oval denotes the output signals that are of the Mealy type. These outputs depend on the values of the state variables and the inputs of the FSM (Mealy outputs). The condition that determines whether such outputs are generated is specified in a decision box.

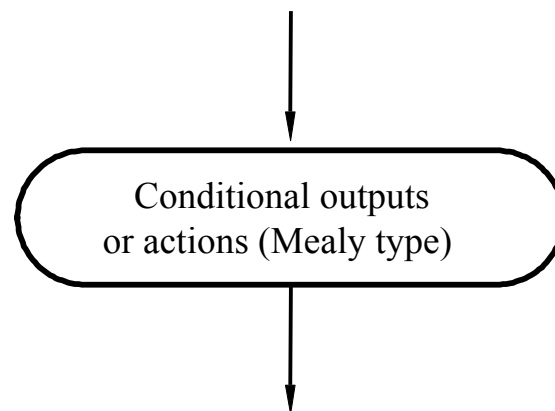
ASM Charts



(a) State box

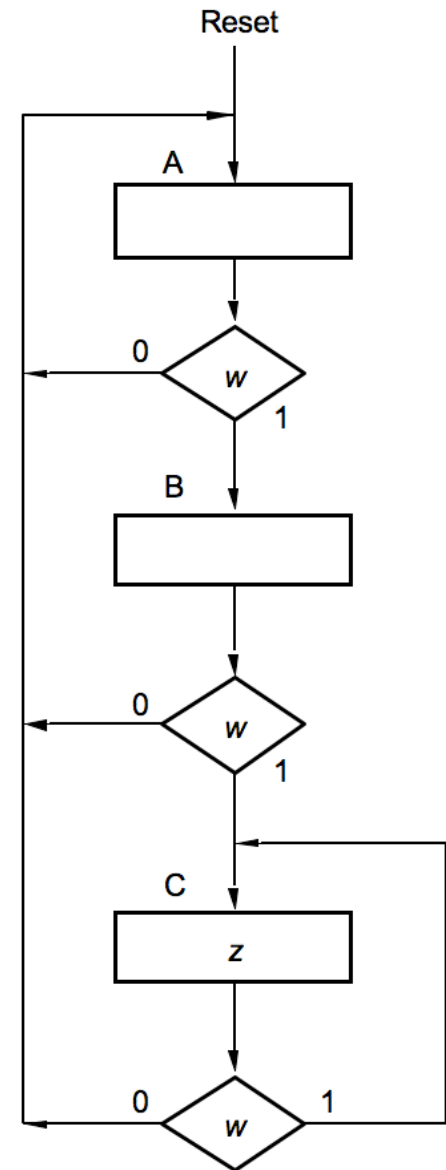
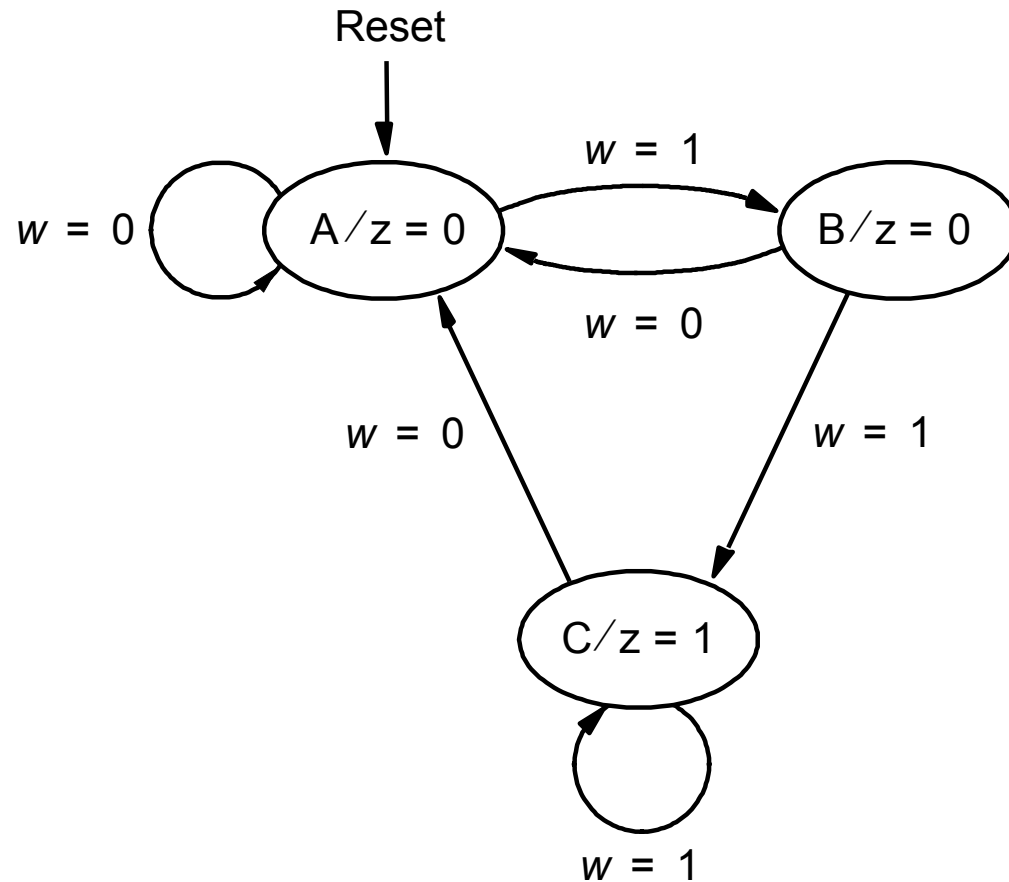


(b) Decision box

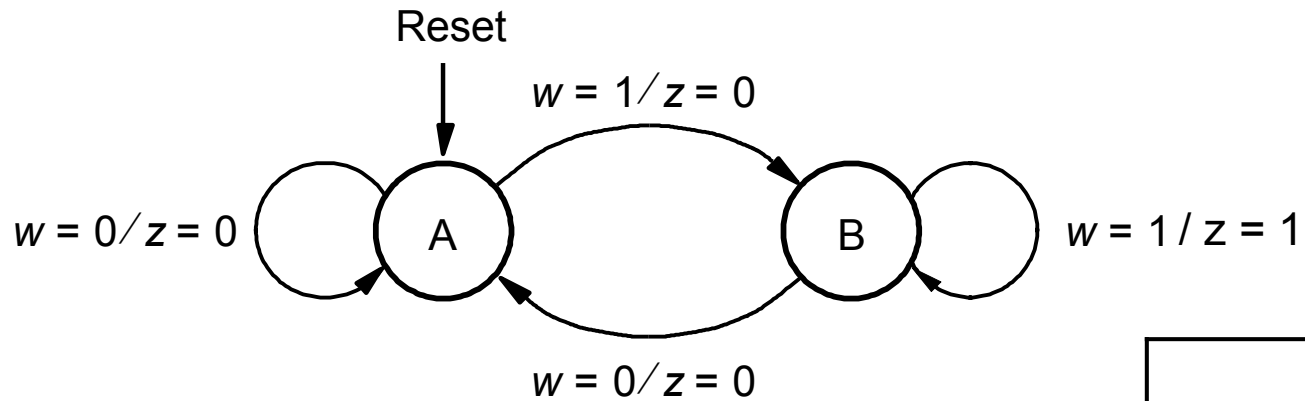


(c) Conditional output box

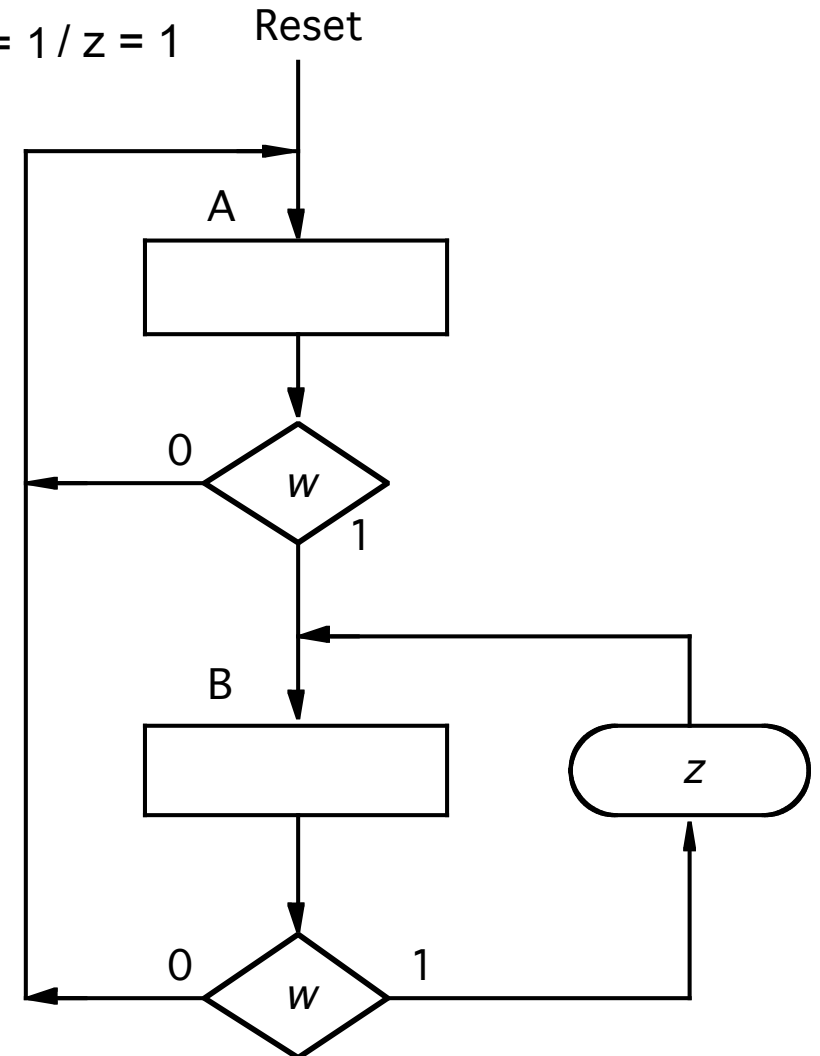
ASM Chart (Moore-Type)



ASM Chart (Mealy-Type)



State diagram



ASM chart

Digital Systems Design (DSD)

- A digital system consists of two main parts, called the datapath circuit and the control circuit.
- The *datapath* circuit is used to store and manipulate data and to transfer data from one part of the circuit to the other.
- The *control* circuit controls the operation of the datapath circuit.

DSD Example 1

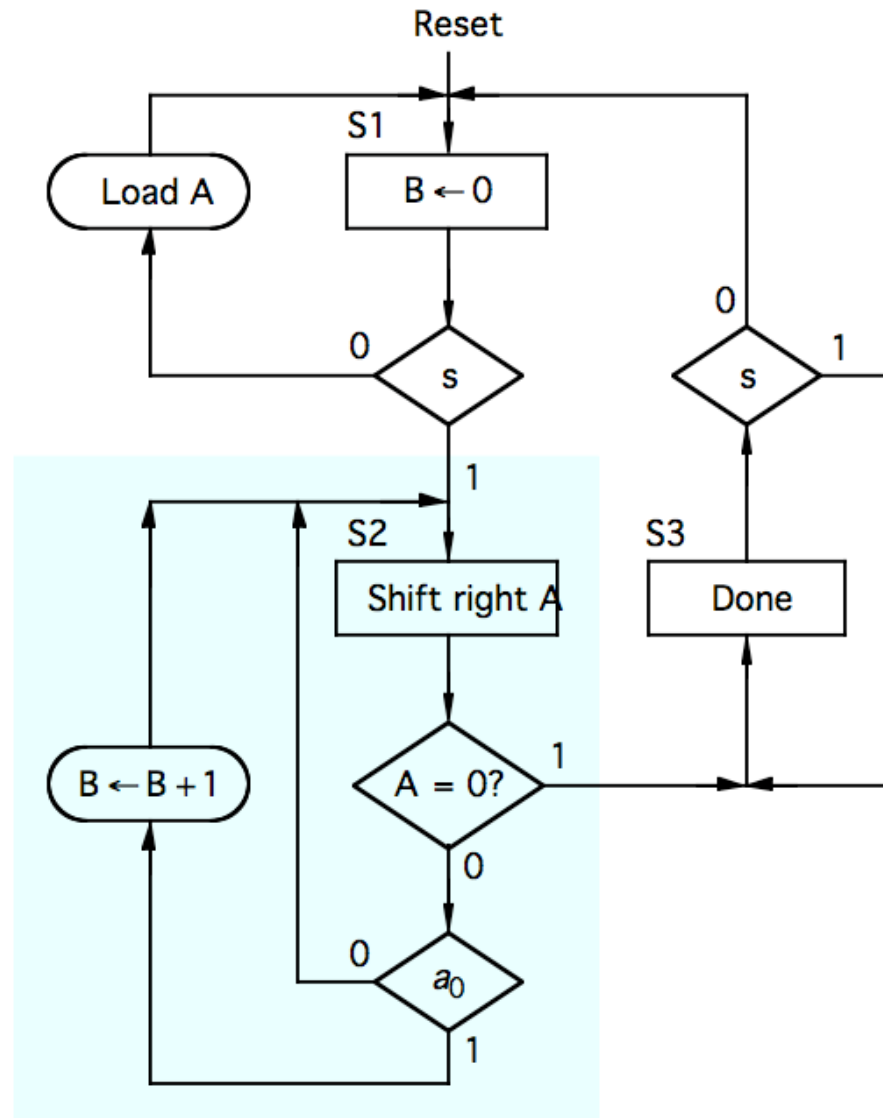
- Suppose the we wish to count the number of bits in a register A, that have the value 1. It assumes that A is stored in a register that can shift its contents in the left-to-right direction. The answer produced by the algorithm is stored in B.

Example 1 - Pseudo-code

```
 $B = 0 ;$   
while  $A \neq 0$  do  
    if  $a_0 = 1$  then  
         $B = B + 1 ;$   
    end if;  
    Right-shift  $A ;$   
end while;
```

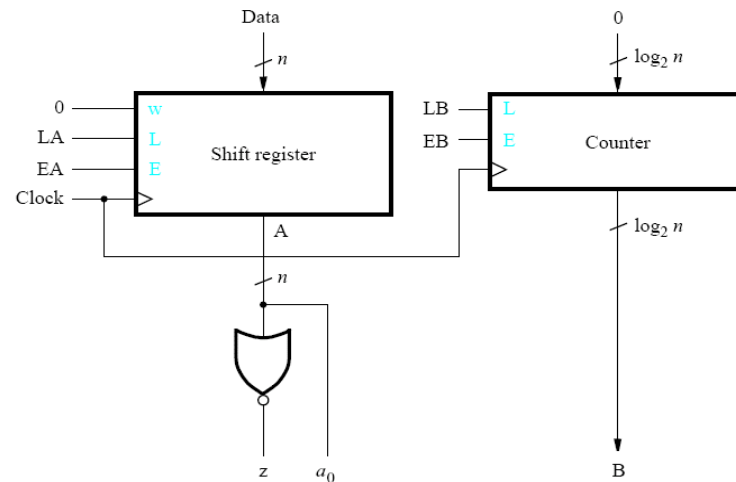
- Assume that in input signal s is used to indicate when the data to be processed has been loaded into A , so the machine can start processing data.

ASM Chart for Example 1



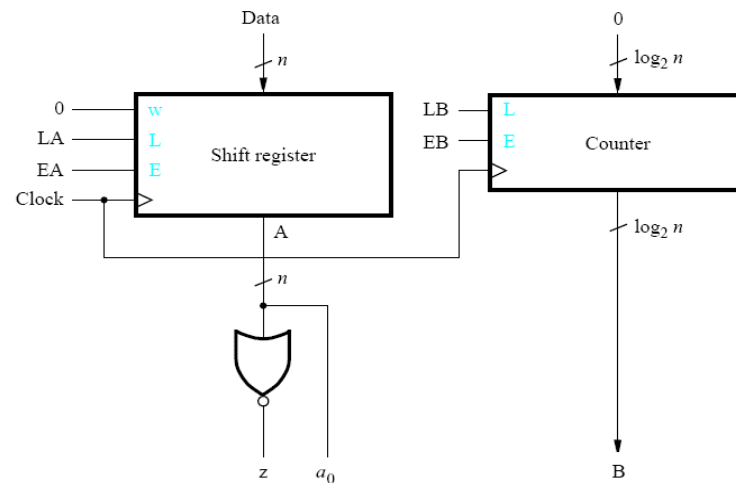
Datapath Circuit for Example 1

- Can use a shift register that shifts left-to-right to implement A.
- Requires parallel load capability to load data into A.
- Require enable capability because shifting should only occur in state S2.

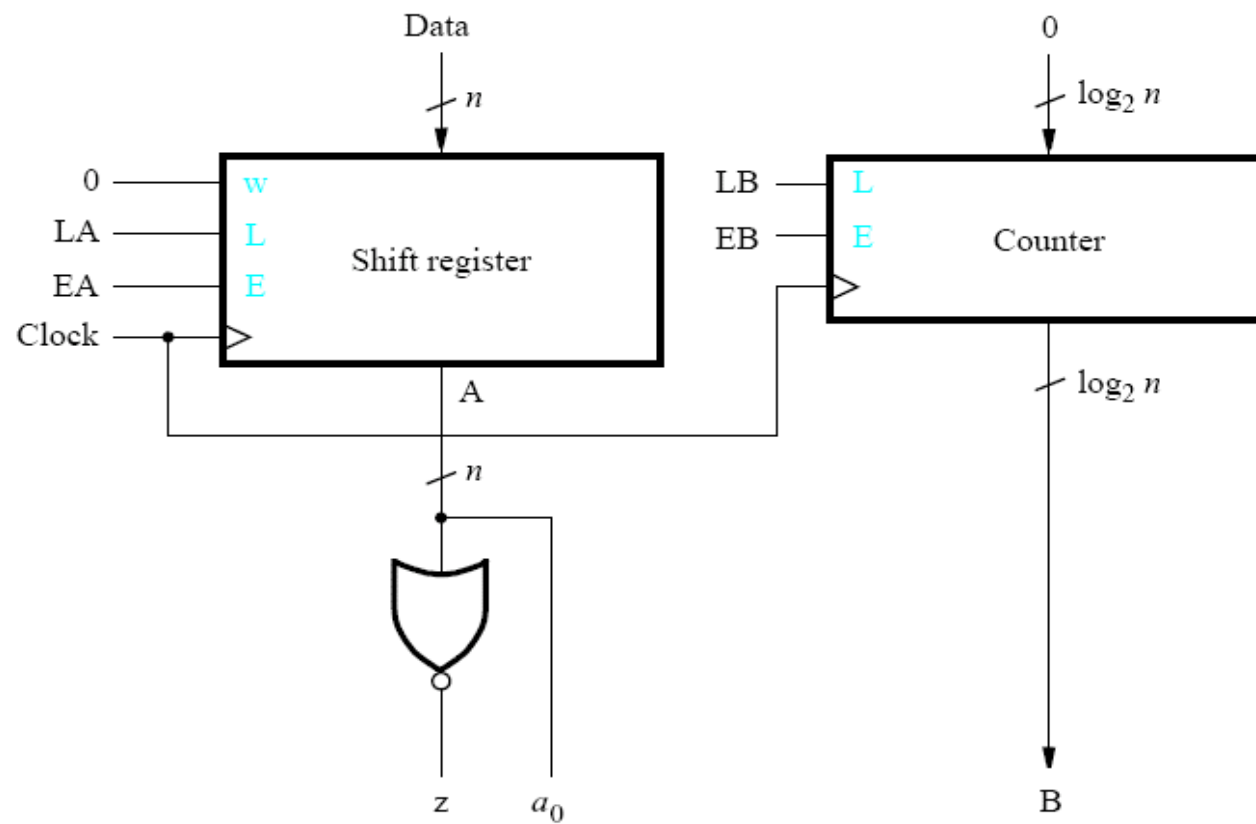


Datapath Circuit for Example 1

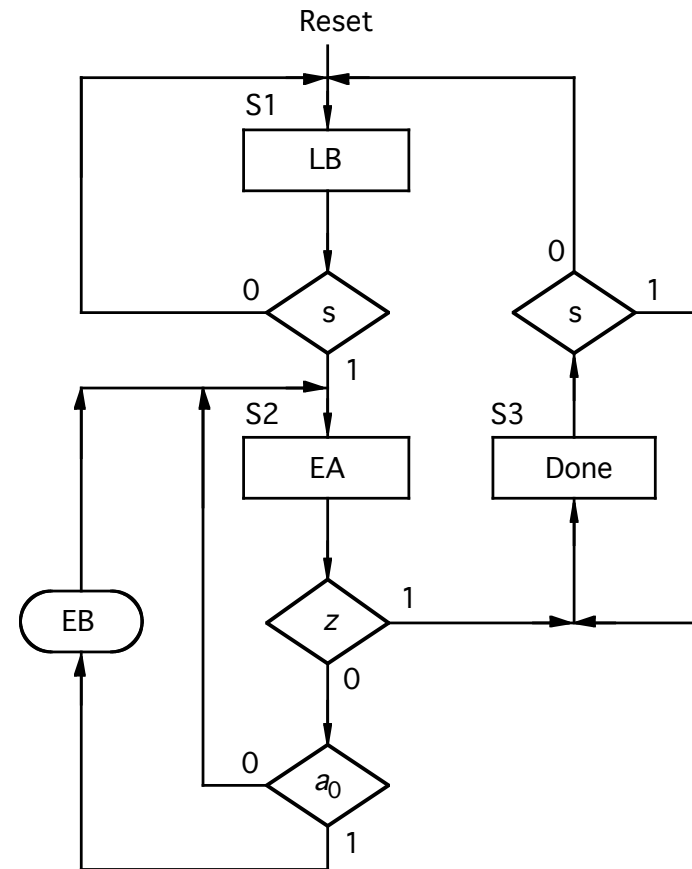
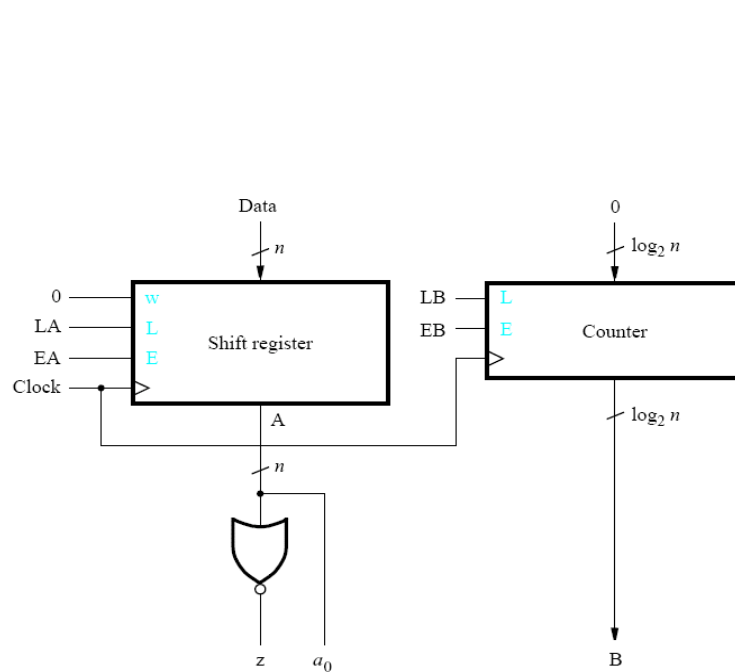
- Can also use a counter to implement B.
- Requires parallel load capability to load data into B.
- Note that a reset signal may not clear the contents of the counter. It's a better idea to load the counter with 0s.



Datapath Circuit for Example 1



ASM Chart for the Control Circuit of Example 1



- Here we assume that an external circuitry drives LA to 1 when valid data is present at the parallel inputs of the shift register.

DSD Example 2

Shift-and-Add Multiplier

Decimal	Binary	
13	1 1 0 1	Multiplicand
$\times 11$	$\times 1 0 1 1$	Multiplier
<hr/>	<hr/>	
13	1101	
13	1 1 0 1	
<hr/>	0 0 0 0	
143	1 1 0 1	
	<hr/>	
	1 0 001111	Product

(a) Manual method

- Assume unsigned numbers

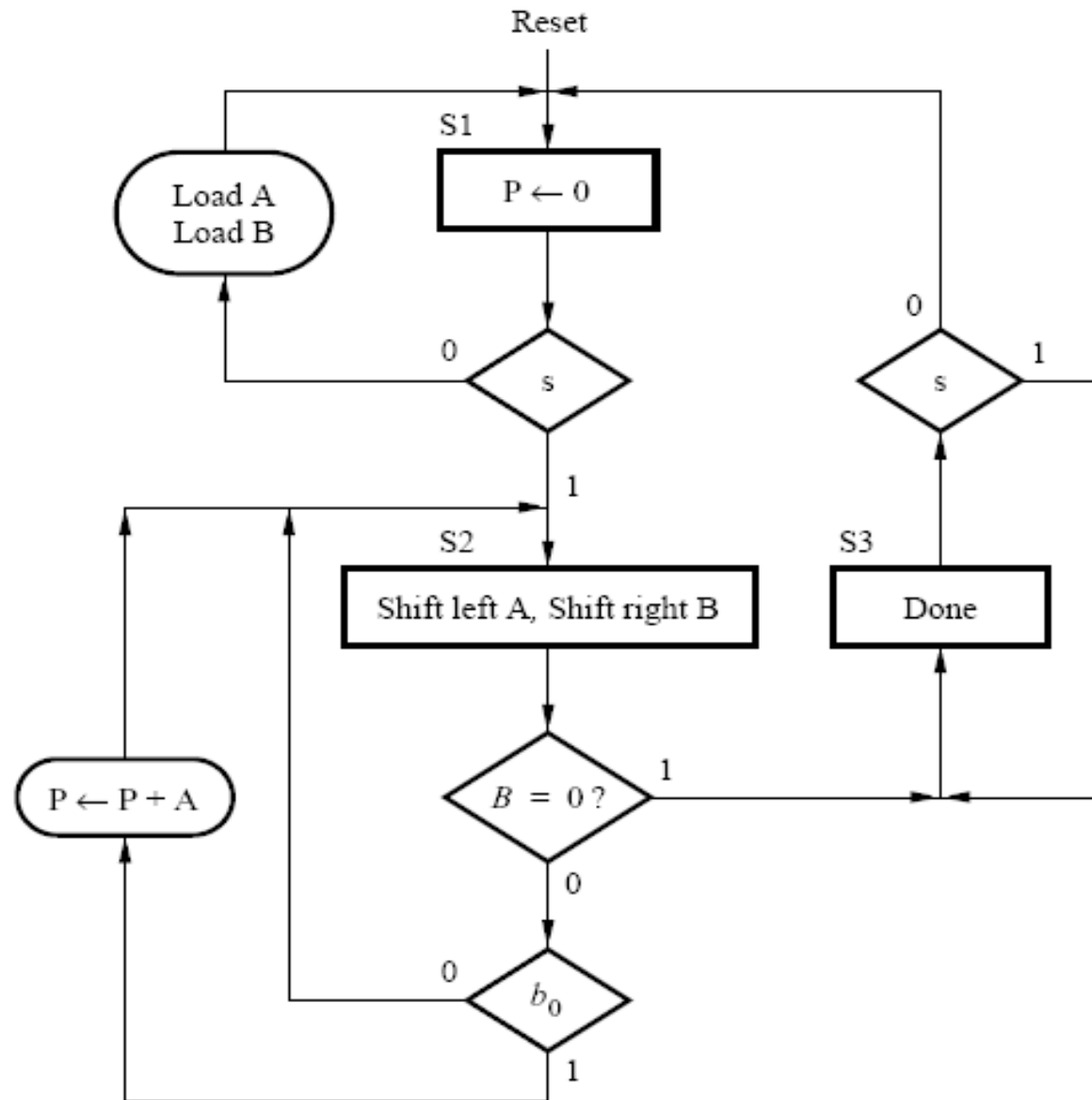
```

P = 0 ;
for i = 0 to n - 1 do
    if  $b_i = 1$  then
         $P = P + A$  ;
    end if;
    Left-shift A ;
end for;

```

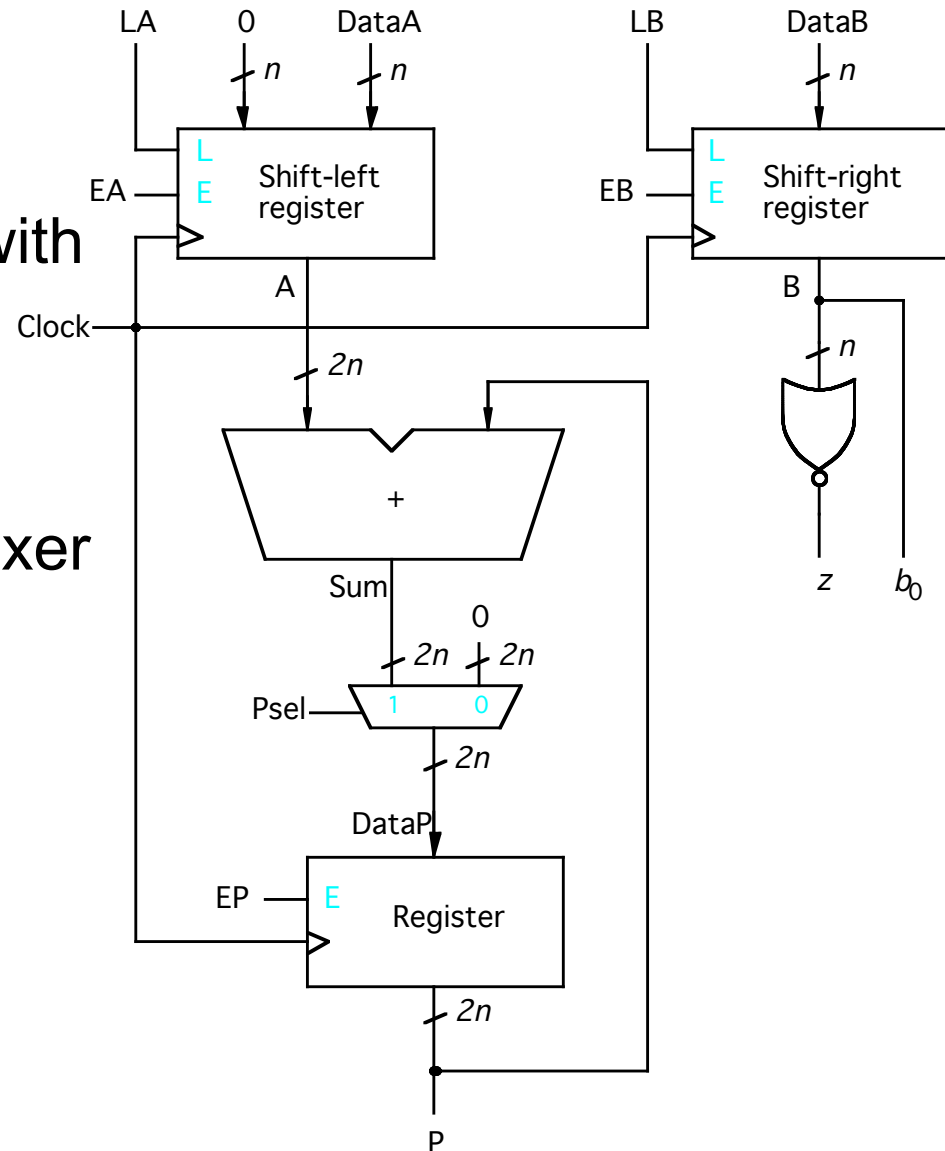
(b) Pseudo-code

ASM Chart for Example 2

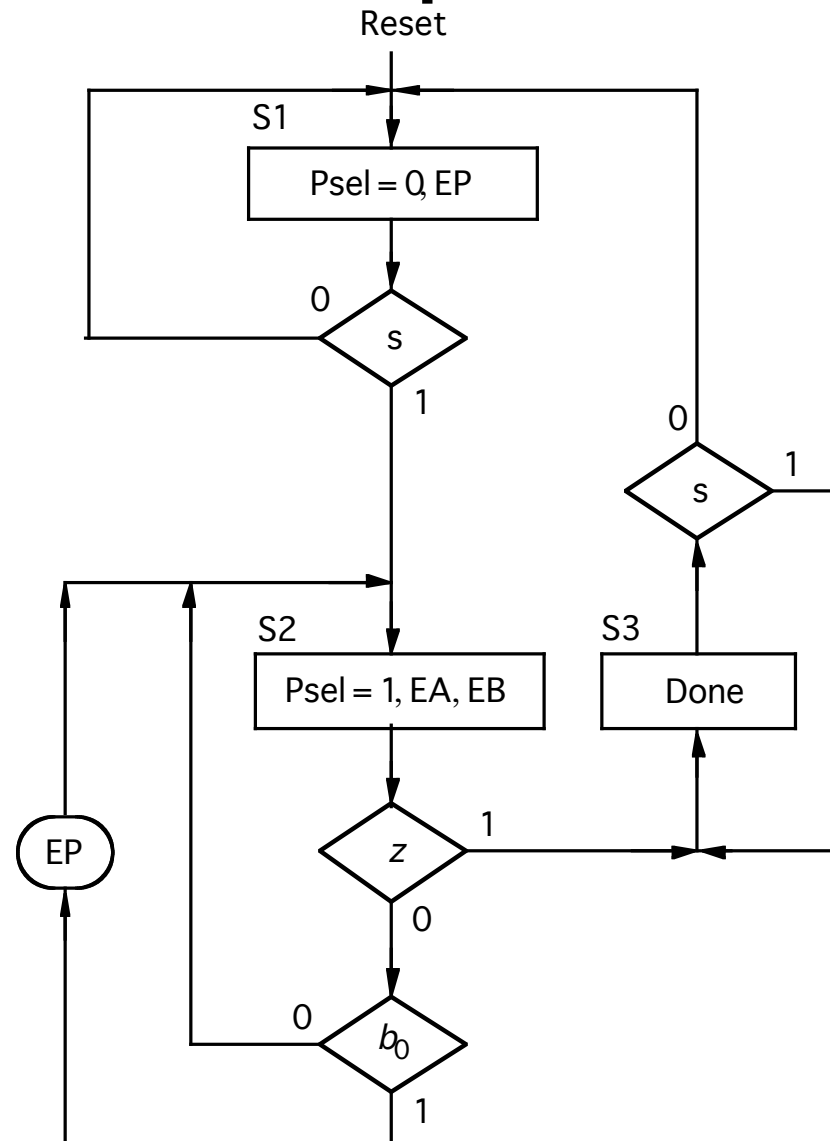


Datapath Circuit for Example 2

- Note that P is loaded with 0 in state S1, and P is loaded from the output of the adder in S2.
- Hence a 2-to-1 multiplexer is needed for each input to P.



ASM Chart for Control Circuit of Example 2

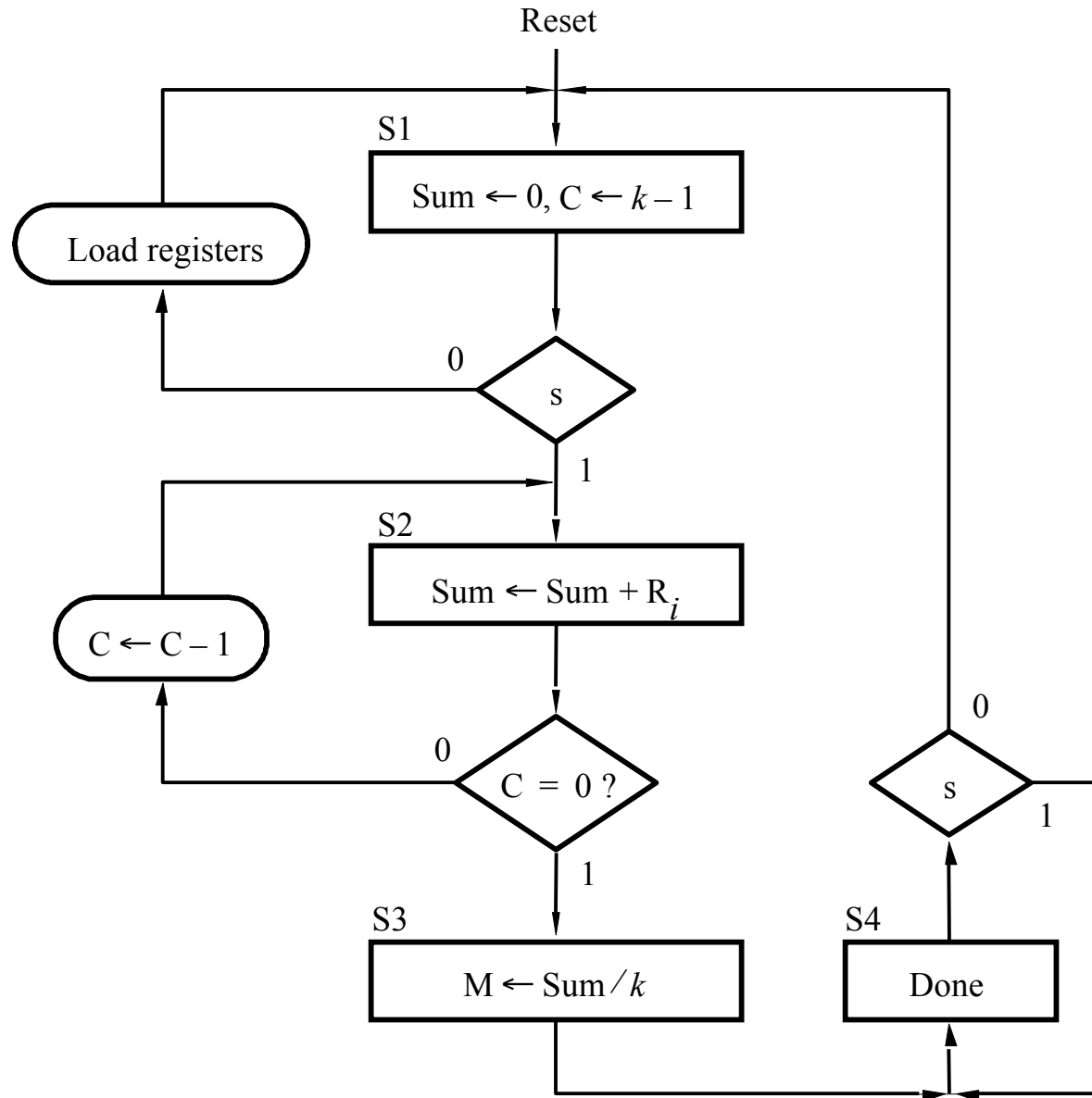


DSD Example 3 Arithmetic Mean

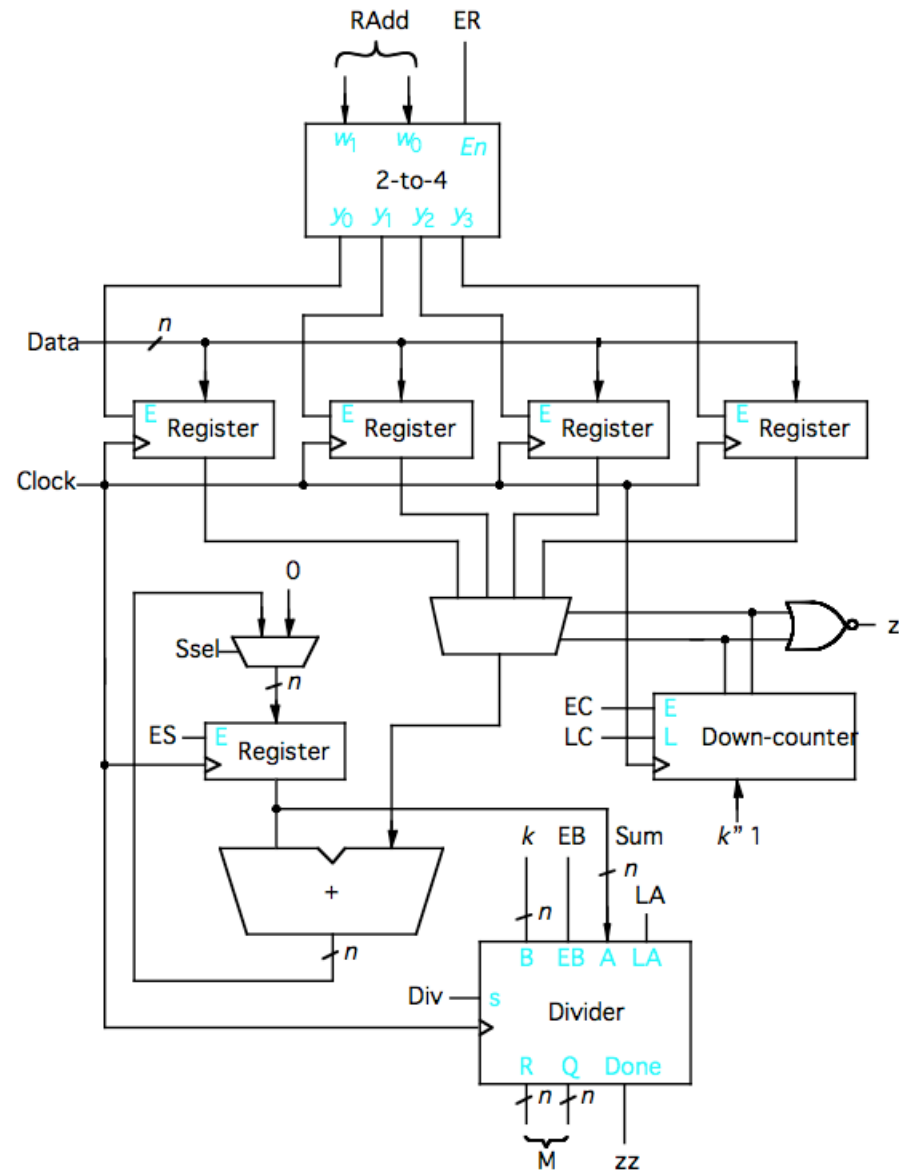
- Assume that k n -bit numbers are stored in register R_0, \dots, R_{k-1} . We wish to design a circuit that computes the mean M of the numbers in the registers

```
Sum = 0 ;  
for  $i = k - 1$  down to 0 do  
     $Sum = Sum + R_i$  ;  
end for;  
 $M = Sum \div k$  ;
```

ASM Chart for Example 3

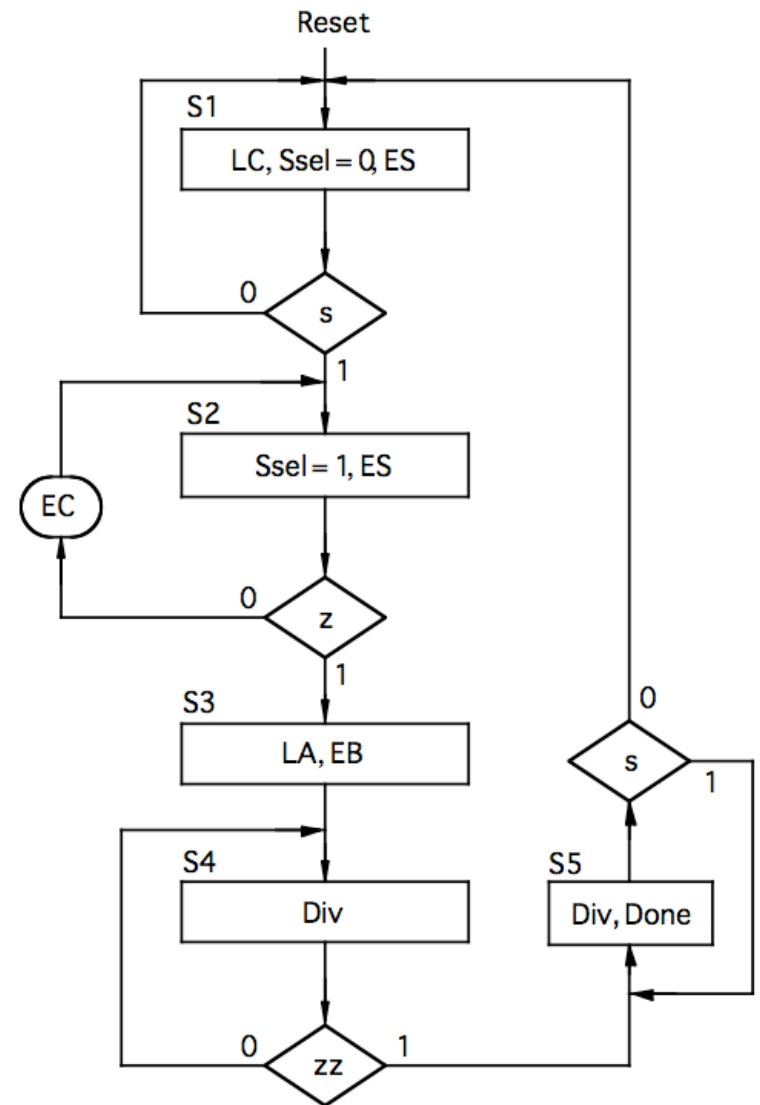
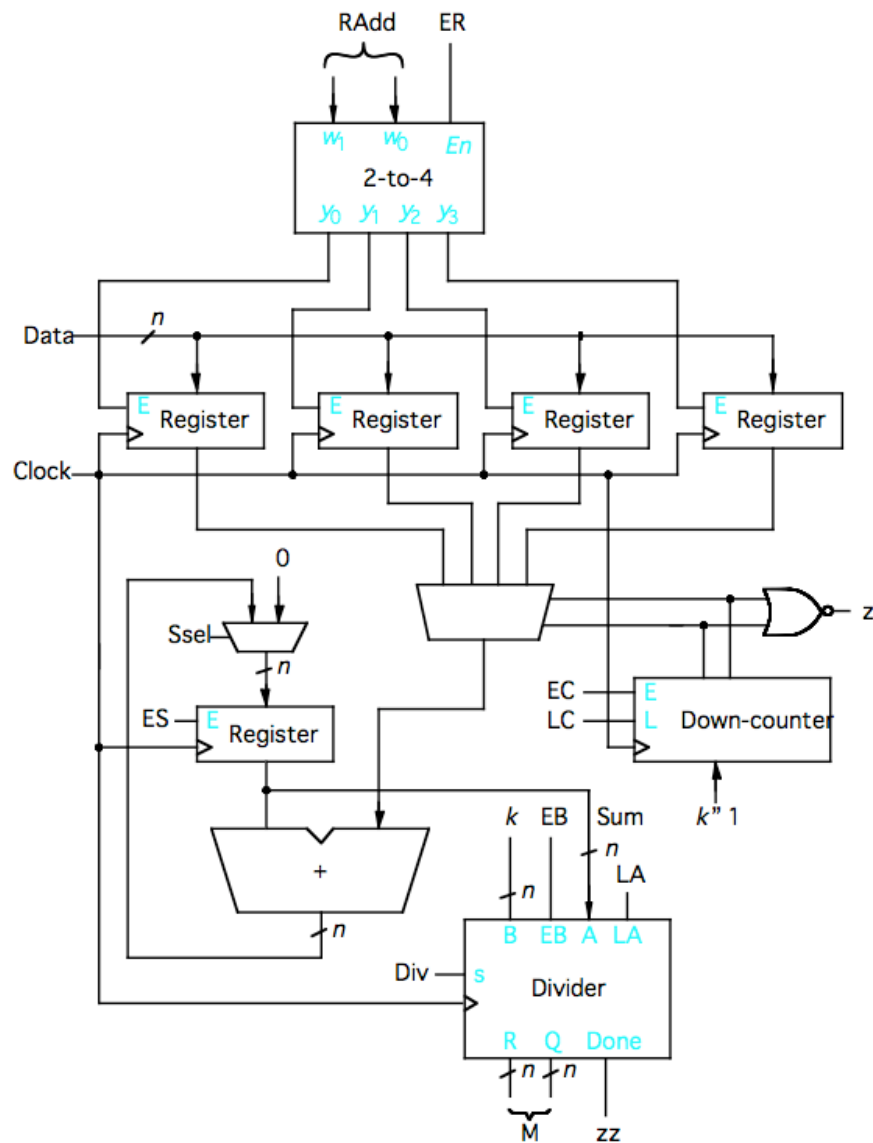


Datapath Circuit for Example 3



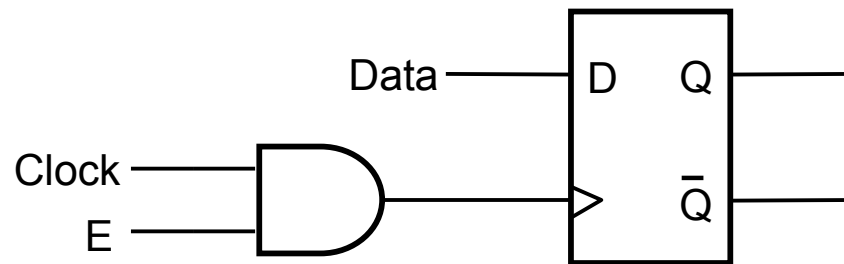
$$k = 4$$

ASM Chart for Control Circuit of Example 3



Clock Skew

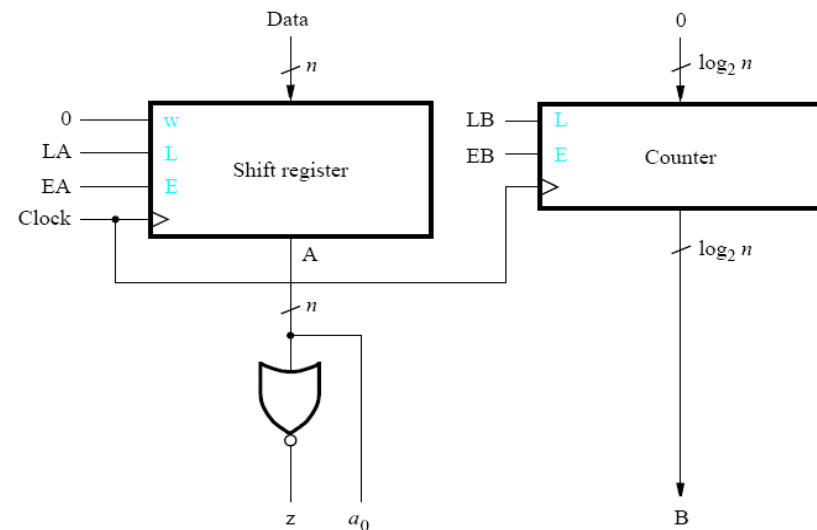
- The situation in which a clock signal arrives at different times at different flip-flops in a FSM, is known as clock skew



Clock enable circuit

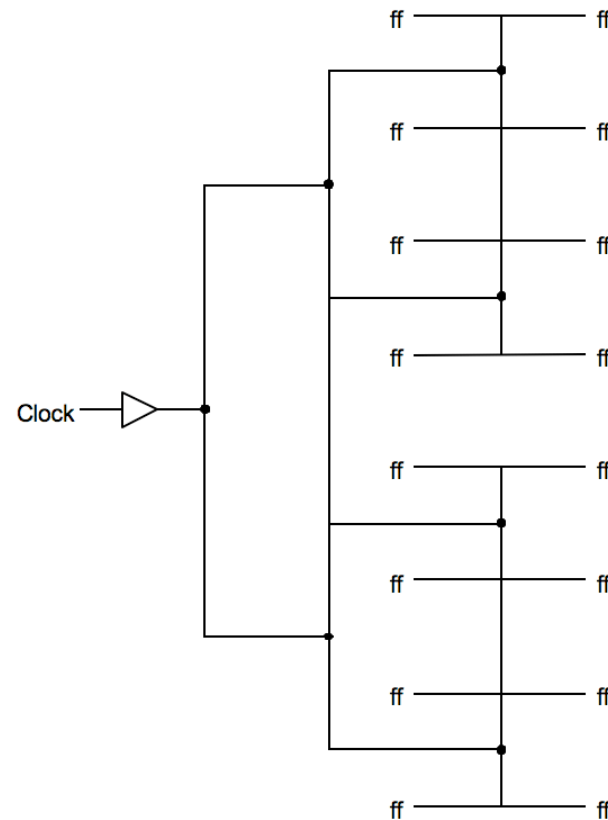
Clock skew

- The shift's register's LSB, a_0 , is used as a control signal that determines whether or not a counter is incremented. Assume that clock skew exists that causes the clock signal to arrive earlier at the shift-register flip-flops than at the counter. The clock skew may cause the shift register to be shifted before the value of a_0 is used to cause the counter to increment. Therefore, the signal EB may fail to cause the counter to be incremented on the proper edge even if the value of a_0 was 1.



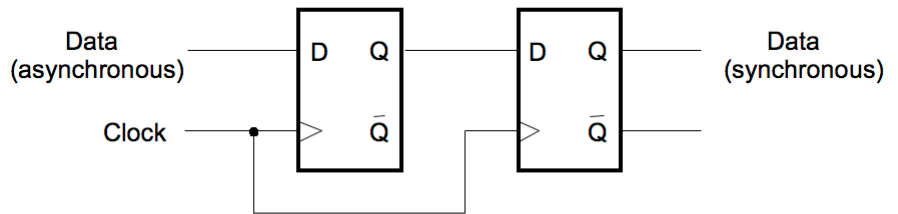
H-Tree Clock Distribution Network

- H-trees
- Asynchronous reset (clear) inputs of all flip-flops implemented in a low-skew reset signal are often provided in PLD circuits.



Asynchronous Inputs to Flip-flops

- If the set up or hold up times of a flip-flop are violated the output may assume a voltage level that does not correspond to the logic levels 0 or 1. The flip-flop is in a metastable state.



This introduces a delay
Of one clock signal before
Data can be used.

Example 4: Divider

$$\begin{array}{r} 15 \\ 9 \overline{) 140} \\ \underline{9} \\ 50 \\ \underline{45} \\ 5 \end{array}$$

(a) An example using decimal numbers

$$\begin{array}{r} 00001111 \leftarrow Q \\ B \rightarrow 1001 \overline{) 10001100} \leftarrow A \\ \underline{1001} \\ 10001 \\ \underline{1001} \\ 10000 \\ \underline{1001} \\ 1110 \\ \underline{1001} \\ 101 \leftarrow R \end{array}$$

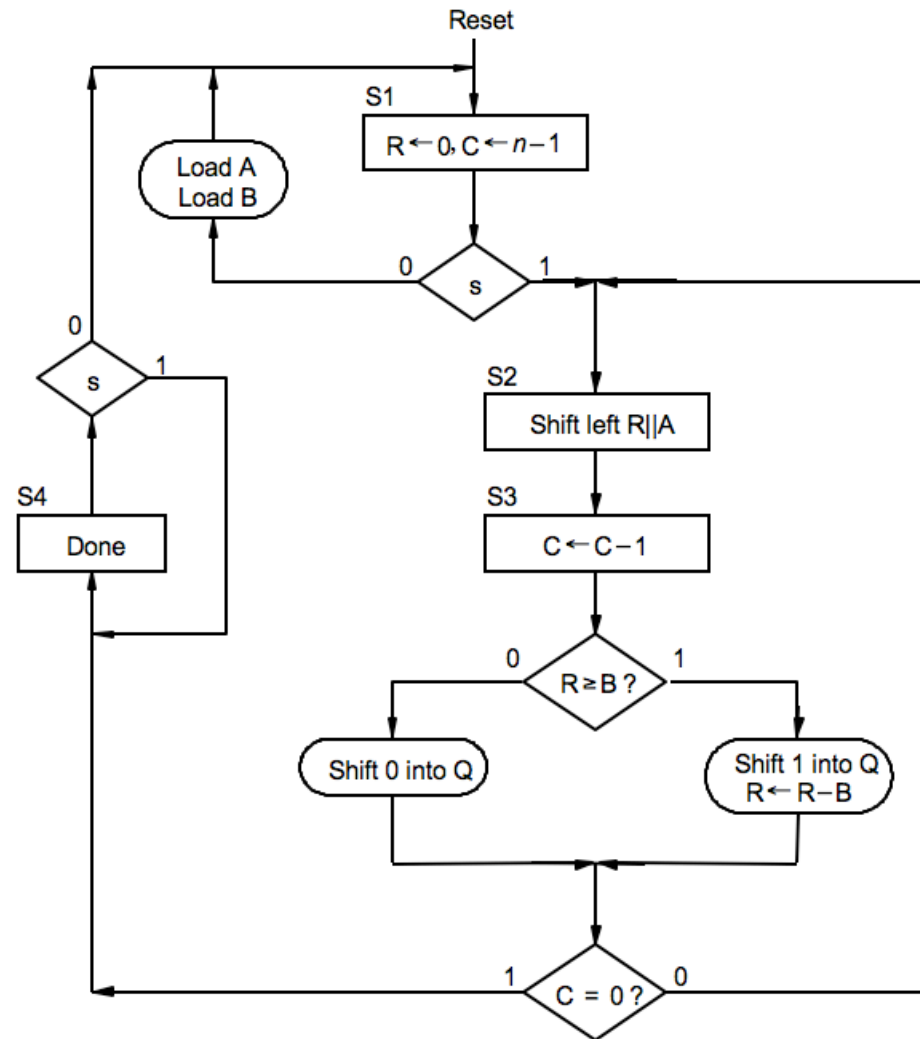
(b) Using binary numbers

```

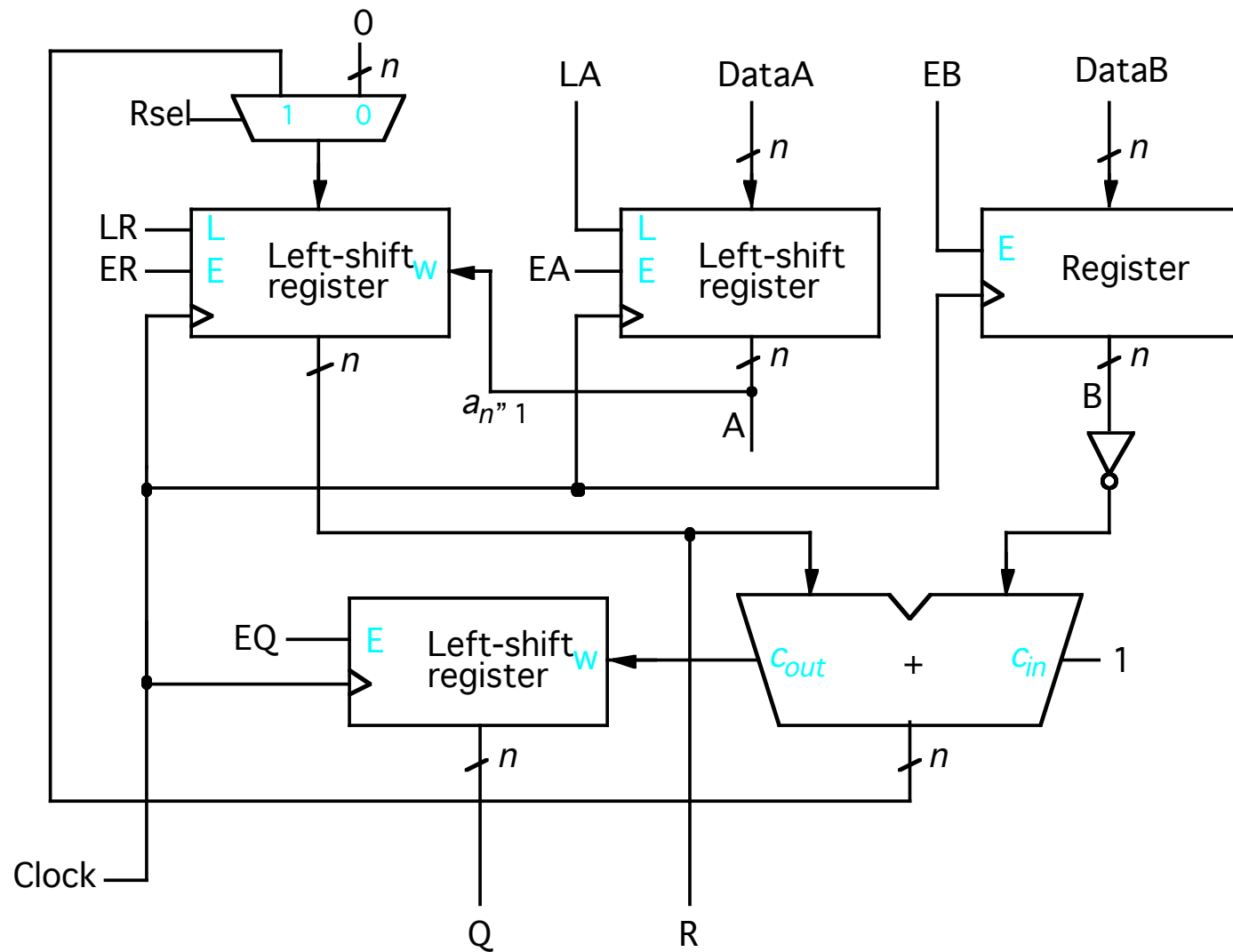
R = 0 ;
for i = 0 to n - 1 do
    Left-shift R || A ;
    if R ≥ B then
        qi = 1 ;
        R = R - B ;
    else
        qi = 0 ;
    end if;
end for;
    
```

(c) Pseudo-code

ASM Chart for Divider



Datapath Circuit for Divider



ASM Chart for Control Circuit

