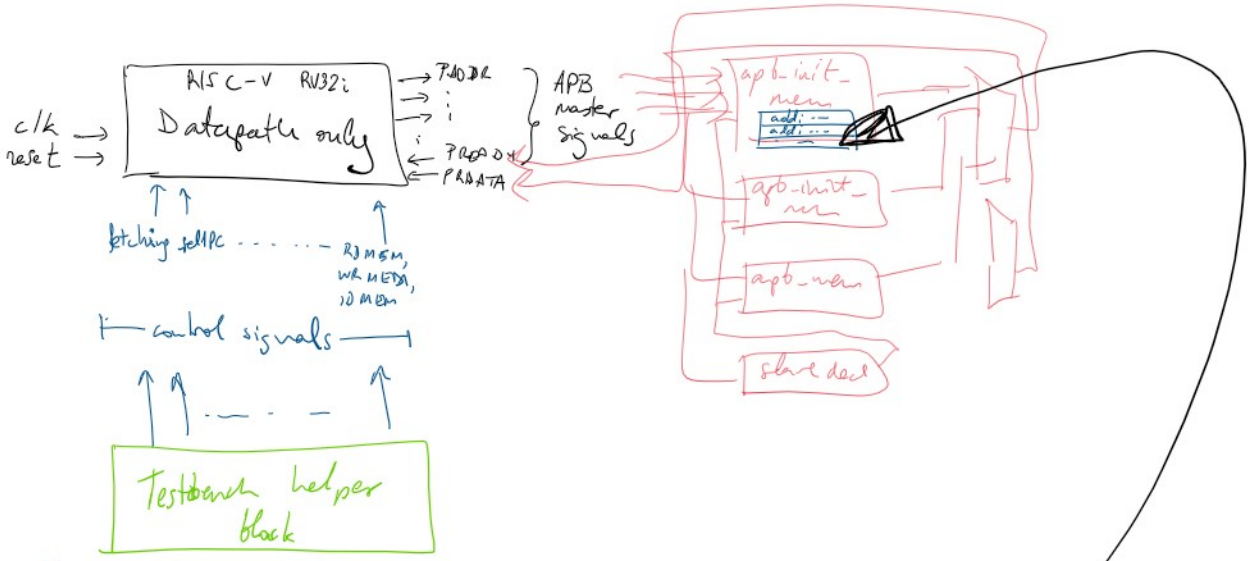
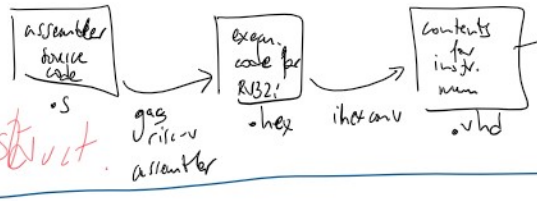
2023/07/17 Meeting

17 July 2023 12:41



Knowing what instructions must be executed, and in which order (addi ... addi ...)



fetch of ~~one~~ instruct.

PROCEDURE

clock 1: IDMEM=1, RDMEM=1, fetching=1, WRMEM=0, others — fetch_clock1

clock 2: wIR=1, others — fetch_clock2

repeat while MemBusy=1

we know the instruction is addi t0, zero, 1 ≡ addi (dst) (rs1) (I-imm) xx, xx, 1

we know the instruction is addi t0, zero, 1 ≡ addi x5, x0, 1 (dst) (rs1) (I-imm)

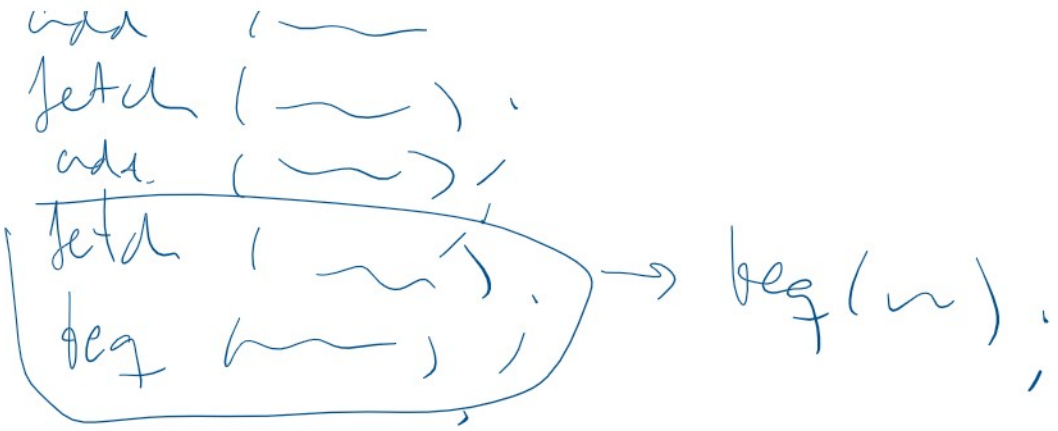
clock 1: sel1ALU = 0, sel2ALU = 01_2, selopALU = 0000_2, selRD = 0, wrRD = 1, (others = 0) ; PC = 1 → addi_clock1

{ VHDL code looks like...

```
fetch_clock1 ( ~~~ );
fetch_clock2 ( ~~~ );
addi_clock1 ( ~~~ );
fetch_clock1 ( ~~~ )
fetch_clock2 ( ~~~ );
addi_clock1 ( ~~~ );
```

→

```
fetch ( ~~~ )
addi ( ~~~ ) → addi ( ~ )
fetch ( ~~~ );
addi ( ~~~ );
fetch ( ~~~ );
add ( ~~~ ); → add ( ~ );
fetch ( ~~~ )
add ( ~~~
fetch ( ~ ) .
```



addi procedure:

control signals

```
fetch_clock1( ~ );
fetch_clock2( ~ );
imm_type1("0000", ~ );
```

andi procedure:

```
fetch_clock1( ~ );
fetch_clock2( ~ );
imm_type1("0101", ~ );
```