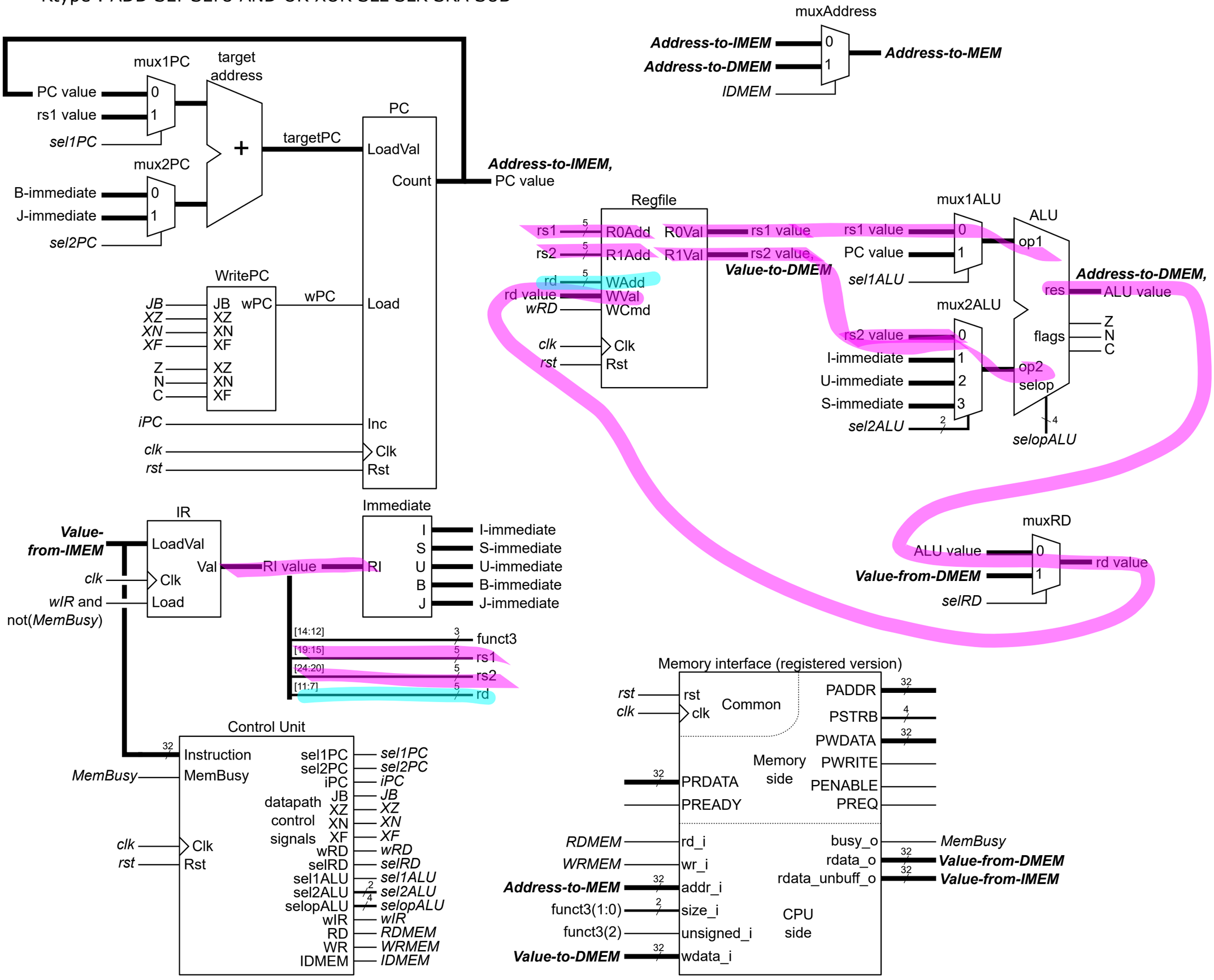
Rtype : ADD SLT SLTU AND OR XOR SLL SLR SRA SUB



instr.	ALU
ADD	op1+op2
SLT	op1<op2? 1:0
SLTU	op1<*op2? 1:0
AND	op1 and op2
OR	op1 or op2
XOR	op1 xor op2
SLL	op1<<op2[4:0]
SLR	op1>>op2[4:0]
SRA	op1>>**op2[4:0]
SUB	op1-op2

```
* considering op1 and op2 as unsigned
** shift-right arithmetic (matching sign, MSB of op1)
```