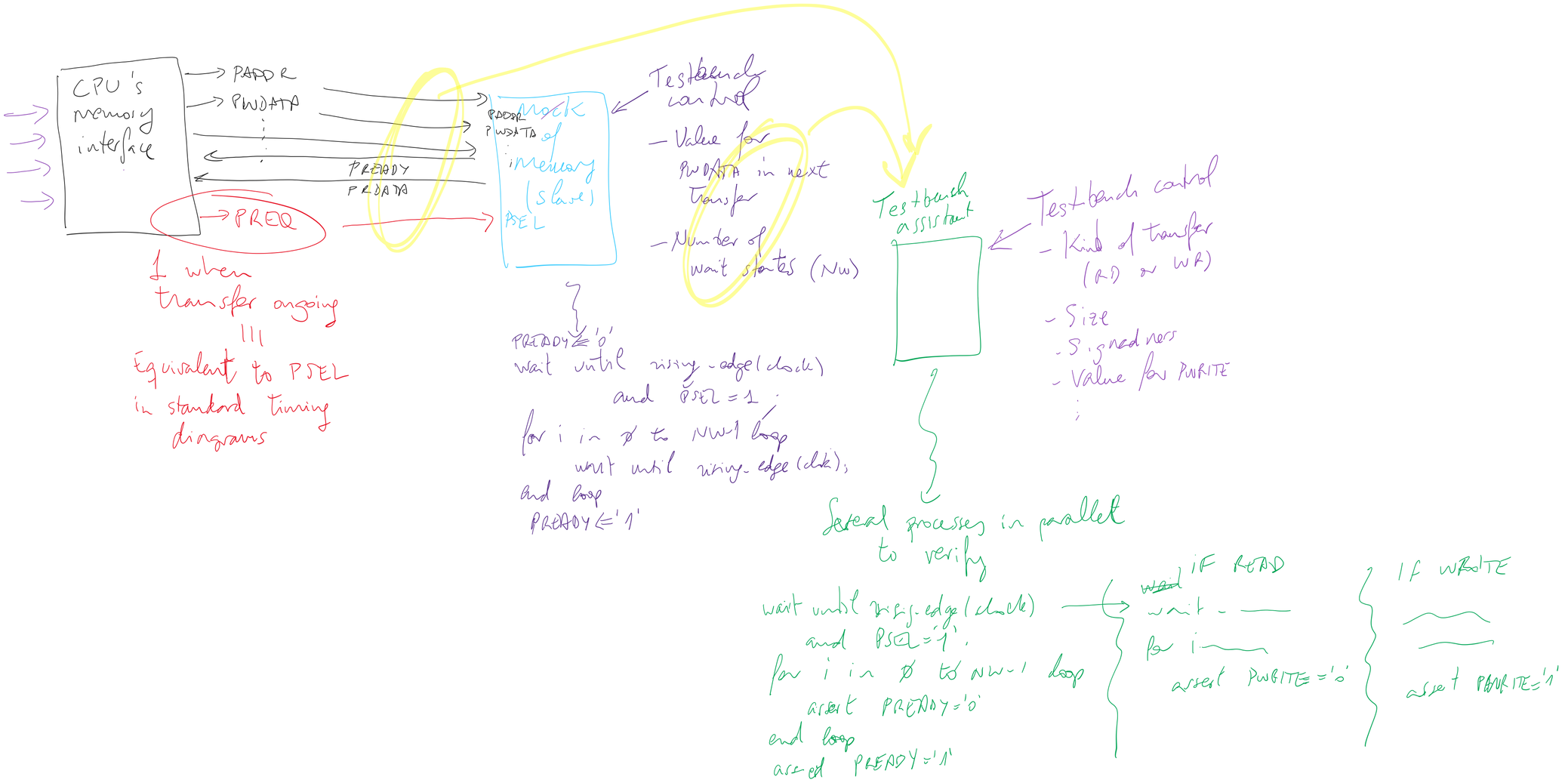
CPU's memory interface
PADDR
PWDATA
PREADY
PRDATA
PSEL
1 when transfer ongoing
III
Equivalent to PSEL in standard timing diagrams
Block of memory (slave)
Testbench control
- Value for PWDATA in next Transfer
- Number of wait states (Nw)
PREADY <= '0'
wait until rising_edge(clock) and PSEL = 1;
for i in 0 to NW-1 loop
wait until rising_edge(clk);
end loop
PREADY <= '1'
Testbench assistant
Testbench control
- Kind of transfer (RD or WR)
- Size
- Signedness
- Value for PWRITE
Several processes in parallel to verify
wait until rising_edge(clock) and PSEL = '1';
for i in 0 to NW-1 loop
assert PREADY = '0'
end loop
assert PREADY = '1'
IF READ
wait ...
for i ...
assert PWRITE = '0'
IF WRITE
assert PWRITE = '1'