JALR

muxAddress

Address-to-IMEM — 0
Address-to-DMEM — 1 — Address-to-MEM
IDMEM

mux1PC — target address

PC value — 0
rs1 value — 1
sel1PC

+ — targetPC

PC
LoadVal
Count — Address-to-IMEM, PC value

mux2PC

B-immediate — 0
J-immediate — 1
sel2PC

instr.	alu
JALR	rs1
JALR	rs1

Regfile

rs1 — /5 — R0Add R0Val — rs1 value
rs2 — /5 — R1Add R1Val — rs2 value, Value-to-DMEM
rd — /5 — WAdd
rd value — WVal
wRD — WCmd
clk — Clk
rst — Rst

mux1ALU

rs1 value — 0
PC value — 1
sel1ALU

ALU
op1
res — Address-to-DMEM, ALU value
flags — Z
N
C

mux2ALU

rs2 value — 0
I-immediate — 1
U-immediate — 2
S-immediate — 3
sel2ALU — /2

op2
selop — /4
selopALU

WritePC

JB — JB   wPC — wPC
XZ — XZ
XN — XN
XF — XF

Z — XZ
N — XN
C — XF

iPC — Inc

clk — Clk
rst — Rst

PC
Load

IR

Value-from-IMEM — LoadVal
clk — Clk
wIR and not(MemBusy) — Load

Val — RI value

Immediate

I — I-immediate
S — S-immediate
U — U-immediate
B — B-immediate
J — J-immediate
RI

[14:12] — /3 — funct3
[19:15] — /5 — rs1
[24:20] — /5 — rs2
[11:7] — /5 — rd

muxRD

ALU value — 0
Value-from-DMEM — 1 — rd value
selRD

Control Unit

Instruction — /32
MemBusy — MemBusy

datapath control signals

sel1PC — sel1PC
sel2PC — sel2PC
iPC — iPC
JB — JB
XZ — XZ
XN — XN
XF — XF
wRD — wRD
selRD — selRD
sel1ALU — sel1ALU
sel2ALU — sel2ALU — /2
selopALU — selopALU — /4
wIR — wIR
RD — RDMEM
WR — WRMEM
IDMEM — IDMEM

clk — Clk
rst — Rst

Memory interface (registered version)

rst — rst
clk — clk Common

PADDR — /32
PSTRB — /4
PWDATA — /32
PWRITE
PENABLE
PREQ

Memory side

PRDATA — /32
PREADY

RDMEM — rd_i
WRMEM — wr_i
Address-to-MEM — addr_i — /32
funct3(1:0) — size_i — /2
funct3(2) — unsigned_i
Value-to-DMEM — wdata_i — /32

CPU side

busy_o — MemBusy
rdata_o — /32 — Value-from-DMEM
rdata_unbuff_o — /32 — Value-from-IMEM