AD board DV14U25 REGISTERS reference Revision 1

Overview

DV14U25 High speed AD board specifications.
Data converted from analog signals with high-speed AD can be imported into PC.
The storage capacity of AD conversion data is 512 K samples.

Board structure contents

The AD board block is shown in Figure 1.
Analog signals are stored in memory after A / D conversion.
You can acquire the waveform memory data from the PC via USB.

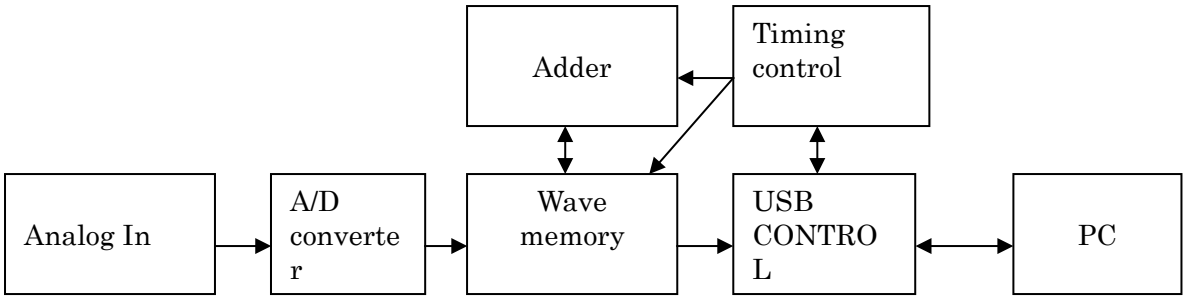


Figure1.AD BOARD BLOCK diagram

2. Register map

table 1. Register Map

address	contents	B7	B6	B5	B4	B3	B2	B1	B0
20	STATUS	x	PLL	SOVF	COVF	0	END	BUSY	SP
21	CONTROL	0	0	0	TEST	0	0	S.TRG	SP ON
22	MODE	0	INV	TC1	TC0	CS	C2	C1	C0
23	CLOCK	CK7	CK6	CK5	CK4	CK3	CK2	CK1	CK0
24	block size(LSB)	S7	S6	S5	S4	S3	S2	S1	S0
25	block size	S15	S14	S13	S12	S11	S10	S9	S8
26	block size(MSB)	0	0	0	0	0	S18	S17	S16
28	ITERATION COUNT(LSB)	D7	D6	D5	D4	D3	D2	D1	D0
29	ITERATION COUNT	D15	D14	D13	D12	D11	D10	D9	D8
2A	ITERATION COUNT(MSB)	0	0	0	0	0	0	D17	D16
2B	SPARE	–	–	–	–	–	–	–	–
2C	FRAME SIZE	F7	F6	F5	F4	F3	F2	F1	F0
30	COS RAM ADDR(LSB)	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
31	COS RAM ADDR	CA15	CA14	CA13	CA12	CA11	CA10	CA9	CA8
32	COS RAM ADDR(MSB)	0	0	0	0	0	CA18	CA17	CA16
34	SIN RAM ADDR(LSB)	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
35	SIN RAM ADDR	SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8
36	SIN RAM ADDR(MSB)	0	0	0	0	0	SA18	SA17	SA16
38	COS RAM DATA	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
39	SIN RAM DARA	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
3A	COS AD DATA(LSB)	CAD7	CAD6	CAD5	CAD4	CAD3	CAD2	CAD1	CAD0
3B	COS AD DATA(MSB)	0	0	CAD13	CAD12	CAD11	CAD10	CAD9	CAD8
3C	SIN AD DATA(LSB)	SAD7	SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0
3D	SIN AD DATA(MSB)	0	0	SAD13	SAD12	SAD11	SAD10	SAD9	SAD8
3E	BOARD REV	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0
3F	BOARD STRING	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

2-1. STATUS register

This is Read only.

ADDRESS	contents	B7	B6	B5	B4	B3	B2	B1	B0
20	STATUS	X	PLL	SOVF	COVF	0	END	BUSY	SP

SP : Sampling status

SP	0	AD sampling is stopped
	1	AD still sampling.

BUSY : State from receiving a sample start command until ending.

BUSY	0	AD sampling completed
	1	AD sampling now or wait for trigger

END : Sampling completed status

END	0	AD sampling not yet.
	1	AD sampling completed.

COVF : COS AD input level status

COVF	0	COS AD input level is normal.
	1	COS AD inputlevel is OVER VOLTAGE

SOVF : SIN AD input level status

SOVF	0	SIN AD input level is normal.
	1	SIN AD input is OVER VOLTAGE

PLL : PLL STATUS

PLL	0	PLL is locked(OK)
	1	PLL is Unlocked.(NG)

2-2. Control register

AD Board control register

address	contents	B7	B6	B5	B4	B3	B2	B1	B0
21	CONTROL	0	0	0	TEST	0	0	S.TRG	SP ON

SP : Set sampling start

SP ON	0	AD sampling stop.
	1	AD sampling start.

S.TRG : Set Softtrigger.

S.TRG	0	SOFT Trigger '0'
	1	SOFT Trigger '1'

TEST : Start transfer of test data

TEST	0	normal
	1	Start transfer of test data.

2-3. MODE register

address	contents	B7	B6	B5	B4	B3	B2	B1	B0
22	MODE	0	INV	TC1	TC0	CS	C2	C1	C0

The division ratio of the frequency divider 'C'
ADClock (MHz) ＝25 (MHz) / (divider'C' x divider'CK')

C2	C1	C0	division ratio 'C'
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

CS : select clock

S.TRG	0	internal clock
	1	external clock

TC0～TC1 : Trigger conditions

TC1	TC0	Trigger condition
0	0	software trigger
0	1	external trigger TTL rise edge
1	0	external trigger TTL fall edge
1	1	prohibited

INV : Setting to perform sign inversion during integration

INV	0	Normal addition mode
	1	Inversion addition mode

2-4. Division ratio 'CK'

address	contents	B7	B6	B5	B4	B3	B2	B1	B0
23	Divider'CK'	CK7	CK6	CK5	CK4	CK3	CK2	CK1	CK0

ADclock (MHz) ＝25 (MHz) / (division ratio(C)x division ratio (CK))

CK7	CK6	CK5	CK4	CK3	CK2	CK1	CK0	division ratio CK
0	0	0	0	0	0	0	0	~~1~~ --
0	0	0	0	0	0	0	1	~~2~~ 1
0	0	0	0	0	0	1	0	~~3~~ 2
0	0	0	0	0	0	1	1	~~4~~ 3
0	0	0	0	0	1	0	0	~~5~~ 4
0	0	0	0	0	1	0	1	~~6~~ 5
1	1	1	1	1	1	1	0	~~255~~ 254
1	1	1	1	1	1	1	1	~~256~~ 255

2-5. block size register

Number of samples per block. must be 1 or more

address	contents	B7	B6	B5	B4	B3	B2	B1	B0
24	block size	S7	S6	S5	S4	S3	S2	S1	S0
25		S15	S14	S13	S12	S11	S10	S9	S8
26		0	0	0	0	0	S18	S17	S16

2-6. Integration count setting register

notice:Write value is Number of iterations-1

address	contents	B7	B6	B5	B4	B3	B2	B1	B0
28	iteration count	D7	D6	D5	D4	D3	D2	D1	D0
29		D15	D14	D13	D12	D11	D10	D9	D8
2A		0	0	0	0	0	0	D17	D16

WriteValue	Number of iterations
0	1
1	2
2	3
3	4

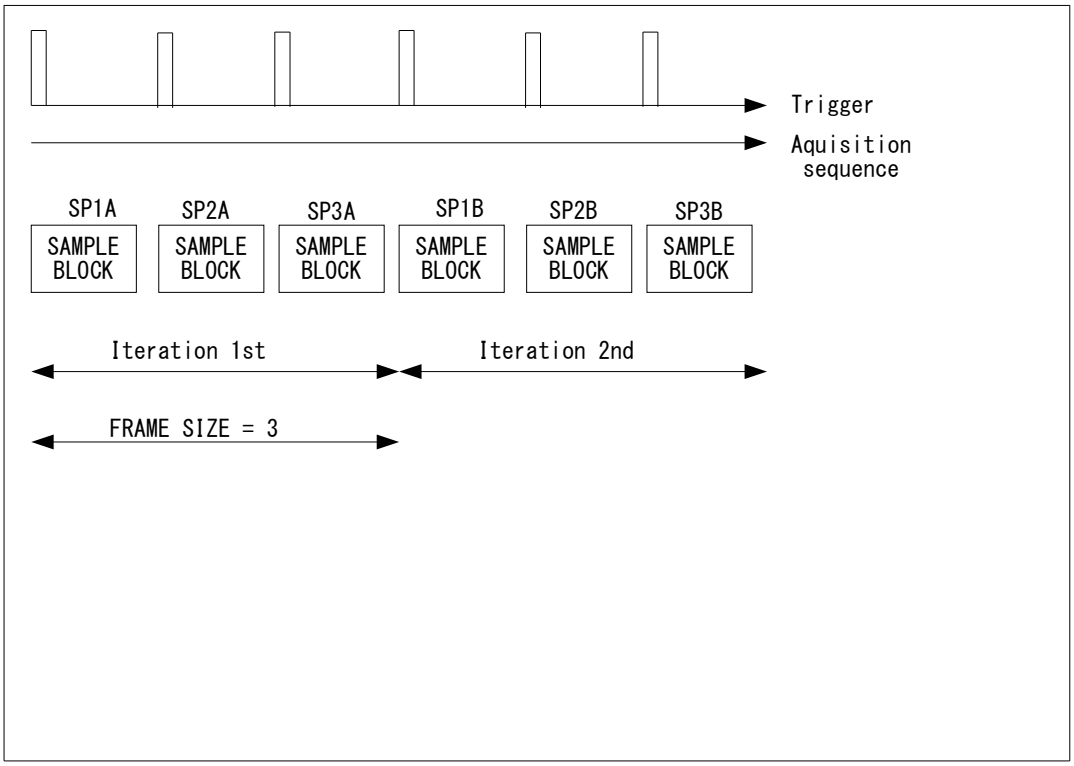
２－７．FRAME SIZE register

Number of blocks per FRAME
notice:write value is FRAMESIZE-1

address	contents	B7	B6	B5	B4	B3	B2	B1	B0
2C	FRAME SIZE	F7	F6	F5	F4	F3	F2	F1	F0

F7	F6	F5	F4	F3	F2	F1	F0	FRAME SIZE
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
1	1	1	1	1	1	1	1	256

example) setting for iteration count=2(value=1) and FRAME SIZE=3(value=2)
The integration calculates SP1A + SP1B, SP2A + SP2B, SP3A + SP3B.



2-8. COS RAM address

RAM address of COS channel
Set before start sampling.

address	contents	B7	B6	B5	B4	B3	B2	B1	B0
30	COS RAM ADDR	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
31		CA15	CA14	CA13	CA12	CA11	CA10	CA9	CA8
32		0	0	0	0	0	CA18	CA17	CA16

2-9. SIN RAM address

RAM address of SIN channle
set before start sampling.

address	contents	B7	B6	B5	B4	B3	B2	B1	B0
34	SIN RAM ADDR	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
35		SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8
36		0	0	0	0	0	SA18	SA17	SA16

2-10. COS RAM DATA

RAM data of COS channel

address	contents	B7	B6	B5	B4	B3	B2	B1	B0
38	COS RAM DATA	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0

・The order of the data at the time of reading

Each time it is read, it is read in order from the lower byte data. When reading of 4 bytes of data is completed, the RAM address is automatically incremented. Therefore, data can be read in order from the lowest byte of the next address.

read count	RAM address	data
1	address＋0	CD0 7-0
2		CD0 14-8
3		CD0 23-16
4		CD0 31-24
5	address＋1	CD1 7-0
6		CD1 14-8
7		CD1 23-16
8		CD1 31-24
9	address＋2	CD2 7-0

2-11. SIN RAM DATA

RAM data of SIN channel

address	contents	B7	B6	B5	B4	B3	B2	B1	B0
39	SIN RAM DATA	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0

・The order of the data at the time of reading

Each time it is read, it is read in order from the lower byte data.When reading of 4 bytes of data is completed, the RAM address is automatically incremented. Therefore, data can be read in order from the lowest byte of the next address.

read count	RAM address	data
1	address＋0	SD0 7-0
2		SD0 14-8
3		SD0 23-16
4		SD0 31-24
5	address＋1	SD1 7-0
6		SD1 14-8
7		SD1 23-16
8		SD1 31-24
9	address＋2	SD2 7-0

2-12. COS AD DATA

Before reading out, please write 0 to address 3A (H).Transfer the AD value of the COS channel to the read register at the timing of writing.

address	contents	B7	B6	B5	B4	B3	B2	B1	B0
3A	COS AD DATA	CAD7	CAD6	CAD5	CAD4	CAD3	CAD2	CAD1	CAD0
3B		0	0	CAD13	CAD12	CAD11	CAD10	CAD9	CAD8

2-13. SIN AD DATA

Before reading out, please write 0 to address 3C (H).Transfer the AD value of the SIN channel to the read register at the timing of writing.

address	contents	B7	B6	B5	B4	B3	B2	B1	B0
3C	SIN AD DATA	SAD7	SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0
3D		0	0	SAD13	SAD12	SAD11	SAD10	SAD9	SAD8

2-14. board revision data

Read the revision of the board.

address	contents	B7	B6	B5	B4	B3	B2	B1	B0
3E	REV	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0

2-15. board ID string data

Read the ID string of the board.
Every time it reads it, it gets the next character.
The code at the end is 0.
When reading further, the first character is read.

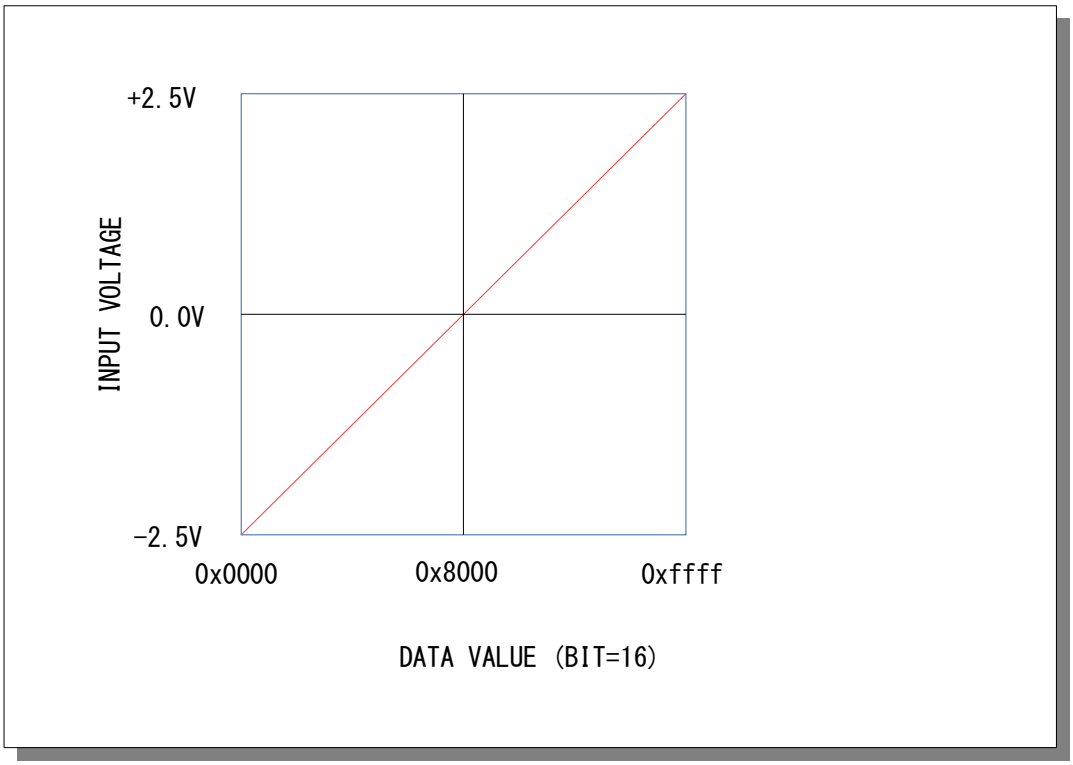
address	contents	B7	B6	B5	B4	B3	B2	B1	B0
3F	ID	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

read count	data	charactor
1	ID0 7-0	“D”
2	ID1 7-0	“V”
3	ID2 7-0	“1”
4	ID3 7-0	“4”
5	ID4 7-0	“U”
…	ID5 7-0	
45	ID44 7-0	0

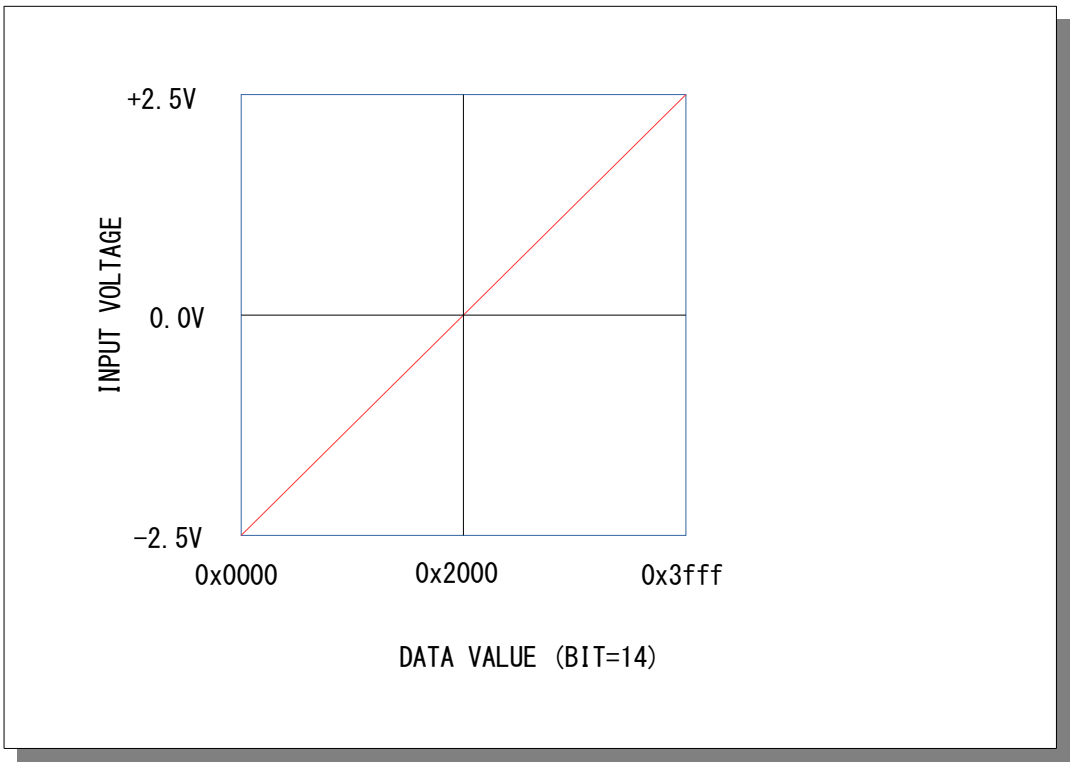
string example DV14U25 ,101025,CLK=25MHZ,BIT=14,RAM=524288,

A/D DATA vs Input voltage

case of BIT=16(In the case of AD board whose 'BIT=16' is included in the query result of *IDN?)



case of BIT=14(* In the case of AD board whose 'BIT=14' is included in the query result of *IDN?)



修正履歴
Revision History

Date	Revision	Changes
2018.12.25	0	Initial release
2018.12.26	1	Correction of register map divisio ratio(CK) (address:23)