ECE 380 Lab #04: K-Maps

In this lab you will use the Quartus II environment to download designs to programmable devices on the Altera DE1 board. You will create several simple designs, using VHDL and schematic entry, which will be downloaded to the Altera DE1 board.

Please select "Cyclone V" as the device family and "5CSEMA5F31C6" as the device in the Family & Device Setting when creating your projects.

During the lab session, you need to do the following:

1. Get your pre-lab signed by the Lab TA.

2. Use Quartus II to design the minimum SOP form of f(a,b,c,d) from **the pre-lab;** write VHDL. Compile and simulate the file. Print out the .vhd and .wav files. Download the design to the Altera Cyclone® V DE1 FPGA board. Use toggle switches **SW[3 … 0]** for the four inputs and **LEDR[7**] for the function output. Verify the design by testing all possible input valuations and observing the output f. Fill in the pre-lab data table column, **f (min SOP)**, with the values that you get from the DE1 board. Receive TA's initials after demonstrating this part of the lab.

3. Use Quartus II's graphics editor to design the gate diagram for the minimum SOP form of f(a,b,c,d) from **the pre-lab** using only NAND gates. Compile and simulate the file. Print out the .bdf and .wav files. Download the design to the Altera Cyclone® V DE1 board. Use toggle switches **SW[3 … 0]** for the four inputs and **LEDR[7**] for the function output. Verify the design by testing all possible input states from the truth table and observe the output, f. Fill in the pre-lab data table column output, **f (NAND)**, with the values that you observed from the DE1 board. Receive TA's initials after demonstrating this part of the lab.

4. Use Quartus II to design the minimum POS form of g(a,b,c,d) from **the pre-lab; write** VHDL. Compile and simulate the file. Print out the vhd and wav files. Download the design to the Altera Cyclone® V DE1 board. Use toggle switches **SW[3 … 0]** for the four inputs and **LEDR[7**] for the function output. Verify the design by testing all possible input valuations and observing the output g. Fill in the pre-lab data table column, **g (min POS)**, with the values that you get from the DE1 board. Receive TA's initials after demonstrating this part of the lab.

5. Use Quartus II's graphics editor to design a gate diagram for the minimum POS form of g(a,b,c,d) from **the pre-lab** using only NOR gates. Compile and simulate the file. Print out the bdf and wav files. Download the design to the Altera Cyclone® V DE1 board. Use toggle switches **SW[3 … 0]** for the four inputs and **LEDG[7**] for the function output. Verify the design by testing all possible input valuations and observing the output g. Fill in the data table column, **g (NOR)**, with the values that you get from the DE1 board. Receive TA's initials after demonstrating this part of the lab.

6. Make sure that you have printed out all of the files and received TA's initials.

7. Turn in the lab report one week from your lab session.

Homework #04 (100 points)

1) (60 pts) Prove the following statements using algebraic manipulation.

a) (30 pts) If $s = x \oplus y \oplus c$, please prove $c = x \oplus y \oplus s$.

b) (10 pts) $0 \oplus x = x$

c) (10 pts) $1 \oplus x = \bar{x}$

d) (10 pts) $x \oplus \bar{x} = 1$

2) (40 pts) Write the minimized SOP form for the following 6-variable K-Map:

$f = \sum m(0,1,2,3,8, 10,16,17, 18,19, 24, 26, 32,33,34,35,40, 42, 48, 50, 56, 58)$

AB=00

EF \ CD	00	01	11	10
00	m0	m4	m12	m8
01	m1	m5	m13	m9
11	m3	m7	m15	m11
10	m2	m6	m14	m10

AB=10

EF \ CD	00	01	11	10
00	m32	m36	m44	m40
01	m33	m37	m45	m41
11	m35	m39	m47	m43
10	m34	m38	m46	m42

AB=01

EF \ CD	00	01	11	10
00	m16	m20	m28	m24
01	m17	m21	m29	m25
11	m19	m23	m31	m27
10	m18	m22	m30	m26

AB=11

EF \ CD	00	01	11	10
00	m48	m52	m60	m56
01	m49	m53	m61	m57
11	m51	m55	m63	m59
10	m50	m54	m62	m58