

ECE 380 Lab #05: Adders/Subtractor

In this lab, you will use the Quartus II software package to design and simulate behavioral adder, ripple carry adder, and LPM_ADD_SUB implementation. You are required to print the Megafunction schematic or VHDL files for Designs A, B, and C.

In the three designs, view the compilation report file (*.rpt) when you compile each design for the DE1 device. In the **DEVICE SUMMARY** section, note the number of logic cells (LCs) required for each design. Write the number you noted in your report.

1. Implement Design A

Create the test vectors in the prelab to verify the correctness of the circuit in functional simulations.

Download your design to the Cyclone® V 5CSEMA5F31C6 device on the DE1 board. Use inputs SW[9..6] (SW[6] is the LSB) for the X input and SW[5..2] (SW[2] is the LSB) for the Y input. Use SW[0] for Cin. Use LEDs LEDG[3..0] (LEDG[0] is the LSB) for the circuit output S. Use LEDs LEDR[9] and LEDR[8] for Cout and Over, respectively.

By using the created test vectors, verify that Design A is operational on the DE1 board. Receive TA initials when you complete verifications.

2. Implement Design B

3. Create the test vectors in the prelab to verify the correctness of the circuit in functional simulations.

Download your design to the Cyclone® V 5CSEMA5F31C6 device on the DE1 board. Use inputs SW[9..6] (SW[6] is the LSB) for the X input and SW[5..2] (SW[2] is the LSB) for the Y input. Use SW[0] for Cin. Use LEDs LEDG[3..0] (LEDG[0] is the LSB) for the circuit output S. Use LEDs LEDR[9] and LEDR[8] for Cout and Over, respectively.

By using the created test vectors, verify that Design B is operational on the DE1 board. Receive TA initials when you complete verifications.

4. Implement Design C

Create the test vectors shown below to verify the correctness of the circuit in functional simulations.

Input	<i>Add Sub</i>	Add	add	add	add	add	add	sub	sub	Sub
Input	<i>Cin</i>	1	1	0	1	0	0	1	1	1
Input	X	0x3	0xB	0xB	0x6	0x6	0xA	0xB	0x5	0xC
Input	Y	0x2	0x3	0xA	0x2	0xE	0xE	0x2	0x2	0x5
Output	S									
Output	<i>Cout</i>									
Output	<i>Over</i>									

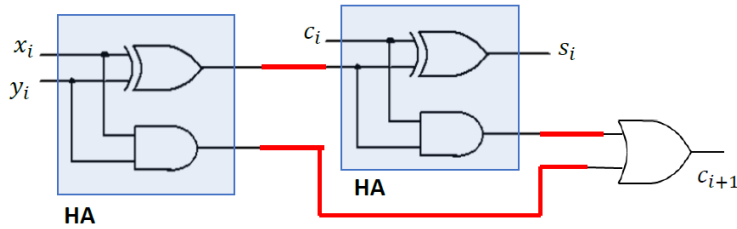
Download your design to the Cyclone® V 5CSEMA5F31C6 device on the DE1 board. Use inputs SW[9..6] (SW[6] is the LSB) for the X input and SW[5..2] (SW[2] is the LSB) for the Y input. Use SW[0] for Cin. Use LEDs LEDG[3..0] (LEDG[0] is the LSB) for the circuit output S. Use LEDs LEDR[9] and LEDR[8] for Cout and Over, respectively.

By using the created test vectors, verify that Design C is operational on the DE1 board. Receive TA initials when you complete verifications.

Homework #05 (100 points)

Q1 (50 pts): Show that the following circuit implements a full adder.

You need to show $c_{i+1} = x_i y_i + x_i c_i + y_i c_i$ and $s_i = c_i \oplus x_i \oplus y_i$ based on the following schematic of the full adder.



Q2 (50 pts): Use the truth table to prove the validity of the expression: $\text{Overflow} = c_n \oplus c_{n-1}$ for addition of n-bit signed numbers.

Hint: construct first the truth table for both Overflow and c_n , as a function of x_{n-1} , y_{n-1} , and c_{n-1} .

Q3 (Bonus 10 pts): Prove the validity of the expression for the overflow flag in the addition of n-bit signed numbers:

$$f = x_{n-1} \oplus y_{n-1} \oplus s_{n-1} \oplus c_n$$