ECE 380: Prelab #9: Flip-flops and Counters

Prelab tasks: Before your lab session, you need to perform the following designs in Quartus Prime:

Design A-1: Design an edge–triggered D flip-flop in a .bdf file. The D flip-flop symbol is under c:/altera… > primitive > storage > dff, after you launch the Symbol dialogue window.

Design A-2: Design an edge–triggered D flip-flop using a VHDL code. Plot the outputs, Q and Q'.

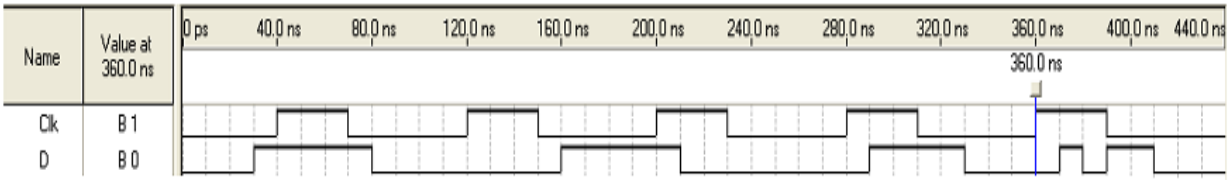

Fig. 1 Timing Waveforms for D-Flip Flop Inputs.

Design B-1: Design a JK flip-flop in a .bdf file. The JK flip-flop symbol is under c:/altera > primitive > storage > jkff, after you launch the Symbol dialogue window.

Design B-2: Design a JK flip-flop using a VHDL code. Plot outputs, Q and Q'.

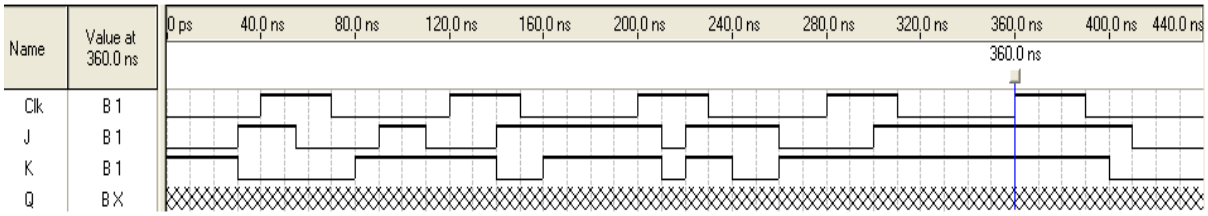

Fig. 2 Timing Waveforms for JK-Flip Flop Inputs.

Design C-1 (BCD counter): Use the VHDL code to create a BCD counter to count upward. This counter has the following control inputs: **En**,$\overline{reset}$**, CLK.** The counting outputs are Q0, Q1, Q2, and Q3.

$\overline{reset}$ clears the outputs of the counter to 0. **En** enables the counting when **En**=1. When **En**=0, the counter stops. The counter sequentially counts from 0000, 0001, …, to 1001, back to 0000, 0001, …, to 1001, etc.

Design C-2: BCD counter with a LED display. Main procedures:

- Generate 1 Hz clock signal. Please follow Lab 2 Part II.
- Use your four-bit down-counter in Design C-1.
- Create a seven-segment LED display that shows 0 to 9.

- Connect 1 Hz clock signal with the four-bit counter. And use the seven-segment LED to display the counting numbers, 0 to 9.

Pre-Lab (30%)	**Score**	**TA initial**
30% Designs		

Report (70%)	
10% Introduction	
10% Procedures	
20% Results	
30% Conclusions	

Lab Grade (100%)	
Bonus Points:	