ECE 380: Lab #06: Adder Design Tradeoffs

In this lab, you will use the Quartus prime software package to design and simulate one 4-bit subtractor and one 4-bit CLA adder. The requirements for this lab consist of completing Quartus Prime designs, downloading designs to the Atlera DE1 board, printing circuit diagrams, VHDL files, simulation results, and the laboratory report.

1. Implement Design A of the prelab. Use the test vectors given in the table below to verify the correctness of the circuit in functional simulation.
   Suggested pin assignment:
   Cout LEDR[9]
   Over LEDR[8]

   S[3] LEDR[3]
   S[2] LEDR[2]
   S[1] LEDR[1]
   S[0] LEDR[0]

   X[3] SW[9]
   X[2] SW[8]
   X[1] SW[7]
   X[0] SW[6]

   Y[3] SW[5]
   Y[2] SW[4]
   Y[1] SW[3]
   Y[0] SW[2]

2. Download and test Design B to the DE1 board, Cyclone® V 5CSEMA5F31C6 chip. Use the same test vectors as in 3 and compare the results you get from the board and the simulator.

   Suggested pin assignment:
   Cout LEDR[9]

   S[3] LEDR[3]
   S[2] LEDR[2]
   S[1] LEDR[1]
   S[0] LEDR[0]

   A[3] SW[9]
   A[2] SW[8]
   A[1] SW[7]
   A[0] SW[6]

B[3] SW[5]
B[2] SW[4]
B[1] SW[3]
B[0] SW[2]

3. (Bonus part) Download and test Design C to the DE1 board, Cyclone® V 5CSEMA5F31C6 chip. Use the same test vectors as in 3 and compare the results you get from the board and the simulator.

   (Bonus part): Use HEX0 [6..0] to display the sum, A.
   Use HEX1 [6..0] to display the sum, B.
   Use HEX2 [6..0] to display the sum, S.
   Use LEDR[8] for Cout.
   User LEDR[9] for overflow.

4. **Have the TA verify your results**

Design A										
Input	X	0x5	0xB	0xB	0x7	0x7	0x9	0xB	0x5	0xC
Input	Y	0x2	0x2	0xE	0x2	0xE	0xE	0x2	0x2	0x5
EXPECTED	S									
EXPECTED	*Cout*									
EXPECTED	*Over*									
SIMULATED	S									
SIMULATED	*Cout*									
SIMULATED	*Over*									

Design B								
		EXPECTED		**SIMULATED**			**DE1 Board**	
A(hex)	**B(hex)**	**S**	**Cout**	**S**	**Cout**		**S**	**Cout**
8	E							
E	5							
C	3							
3	2							
8	F							

Homework #06 (100 points):

Q1(30 pts). Use full adders to implement a multiplier from Z = X * Y, where X is 3-bit unsigned number and Y is a 3-bit unsigned number, and Z is a 6-bit unsigned number. Draw the block diagram of the circuit and explain your design.

You can use simple logic functions as the inputs to the full adders.

Q2 (30 pts). Carry Look-Ahead (CLA) adder to add two 5-bit binary numbers (X=$x_4x_3x_2x_1x_0$, Y= $y_4y_3y_2y_1y_0$).

Please derive the logic expression of the carryouts, c_1, c_2, c_3, c_4, c_5

Q3 (40 pts): Write down the truth table and the SOP logic function for a 2-out-of-4 detector.

Definition of 2-out-of-4 detector: for a 4-input logic, if and only if 2 of inputs are '1', the output will be true.