Lab 03
Multifunctional Logic Circuit

ECE 380-002
University of Alabama

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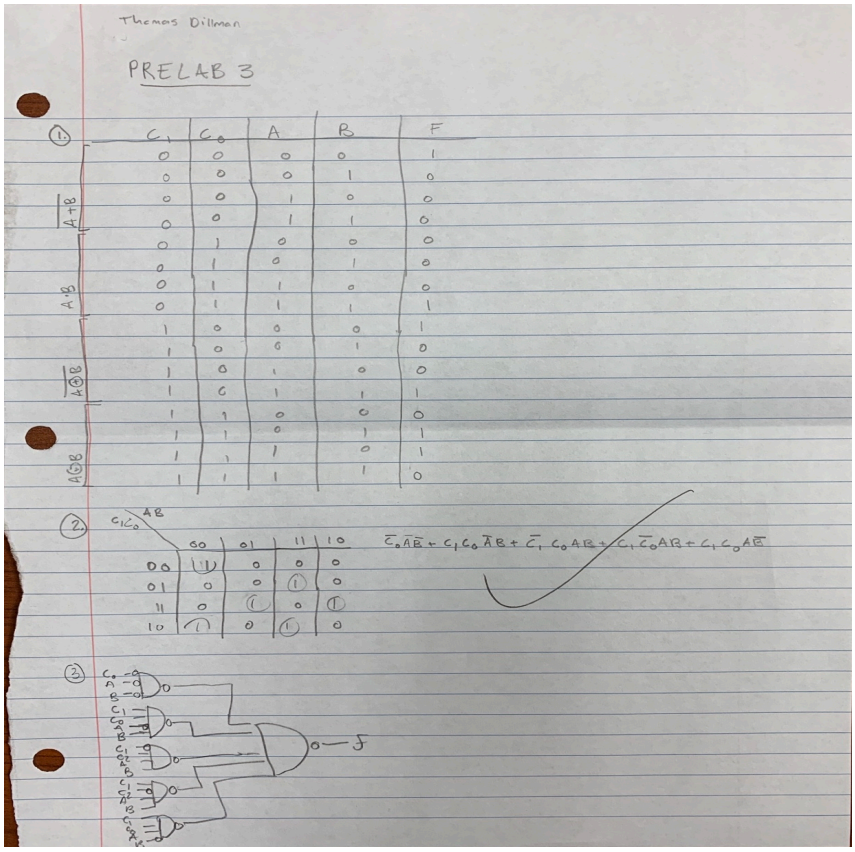
Introduction

In Lab#03, our team designed, built, and tested a multifunctional logic circuit that implements multiple logic functions. We use the Quartus II CAD tool to design the circuit and write VHDL code. After compiled the files, we test the designs on Altera's DE1 board and valid the outcome in the prelab truth table.

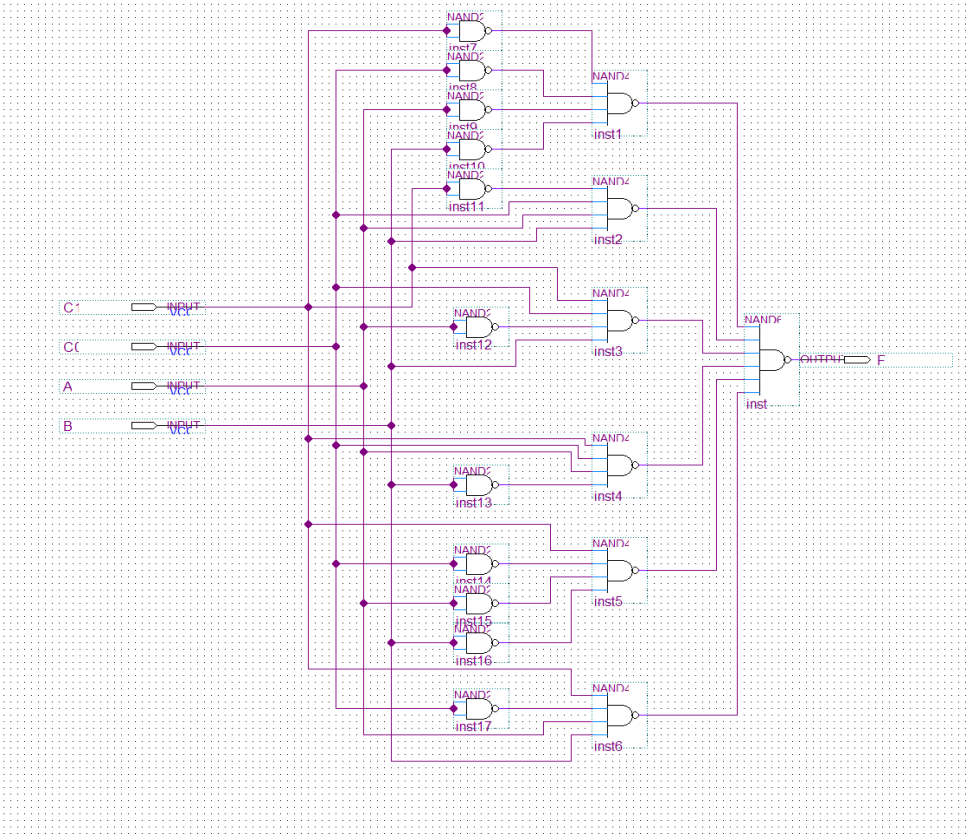
Procedure

a) Prelab

In the prelab, we firstly analyze the problem and finish the truth table of the function. We also make a K-Map of the function, calculate the function through minimum term method and build truth table. Finally, we draw the NAND-only schematic on the paper.



Then we created two projects for two different circuit implementations, the VHDL and schematic.



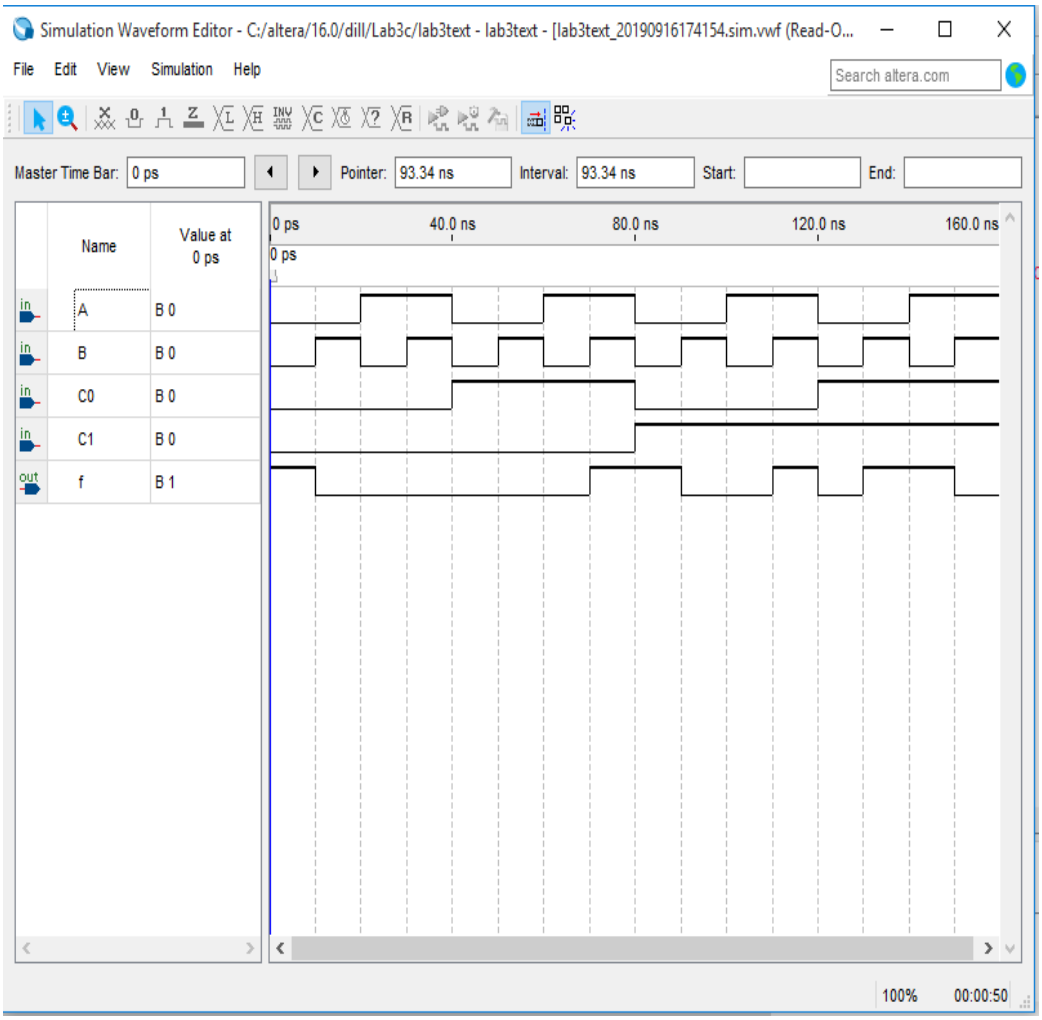
lab3text.vhd | Compilation Report - lab3text

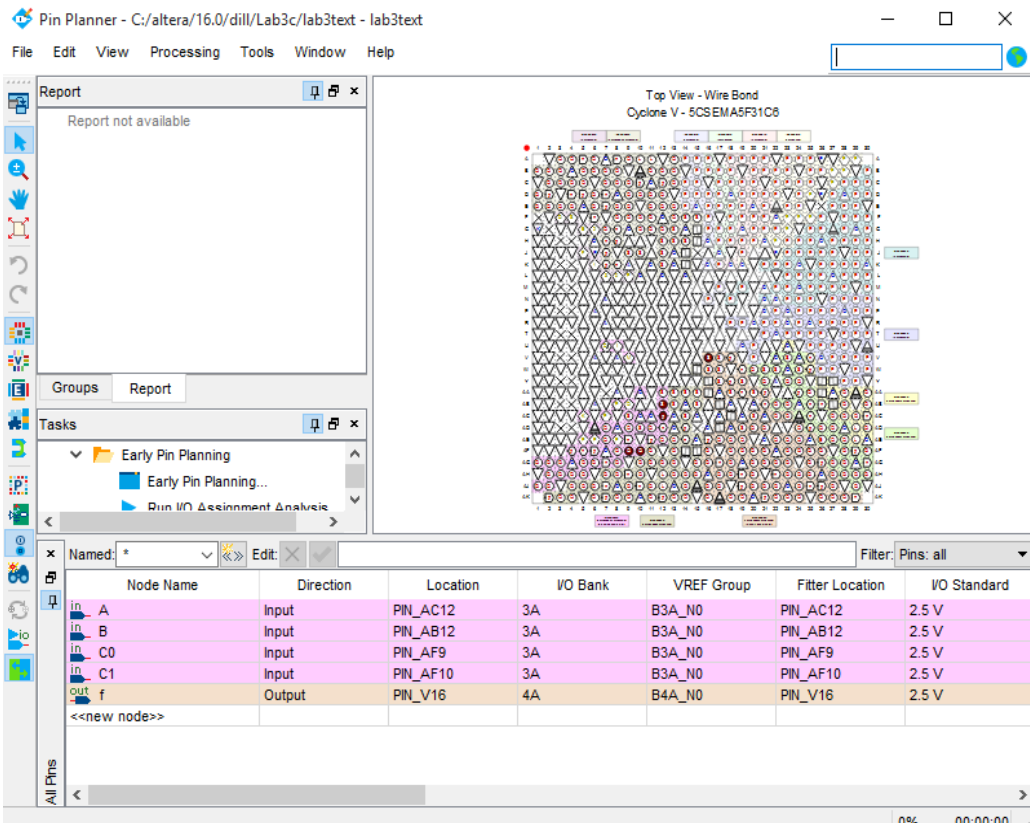
```
1  Entity lab3text IS
2  PORT (C1, C0, A, B : IN  BIT;
3  f : OUT BIT);
4  END lab3text;
5
6  ARCHITECTURE Behavior OF lab3text IS
7  BEGIN
8  f <= NOT(NOT(NOT C0 AND NOT A AND NOT B) AND NOT(C1 AND C0 AND NOT A AND B) AND NOT(N
9  END Behavior;
```

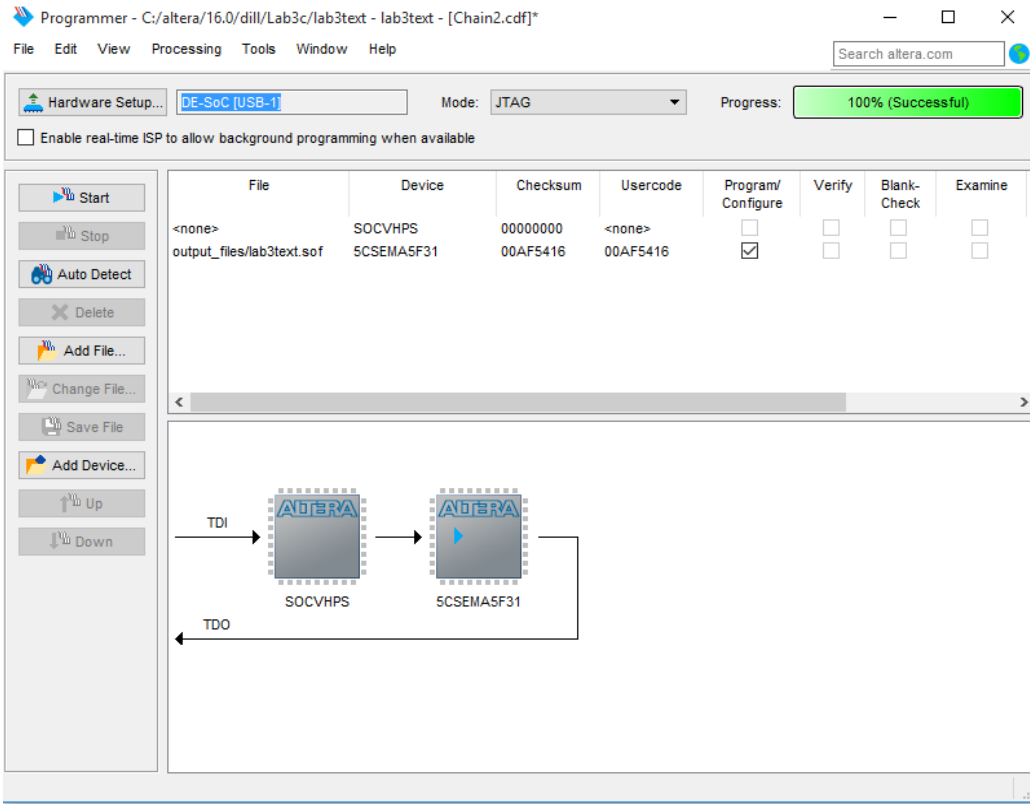
b) During the Lab

a. VHDL Part

We compile the file and run simulation for the file. The result is same as we predict in the prelab. Then we import the file to the Altera's DE1 board and set the switches by the instruction of the TA. We test the function on the board by different combination of switches to check if the function import to the board is same as we predict.

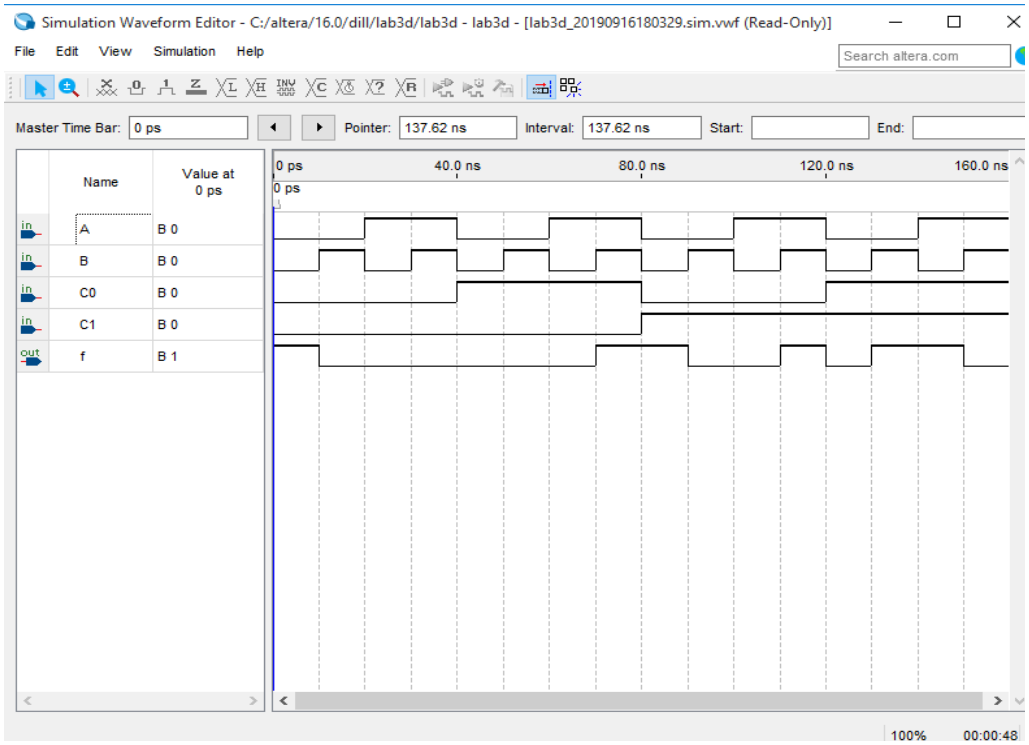


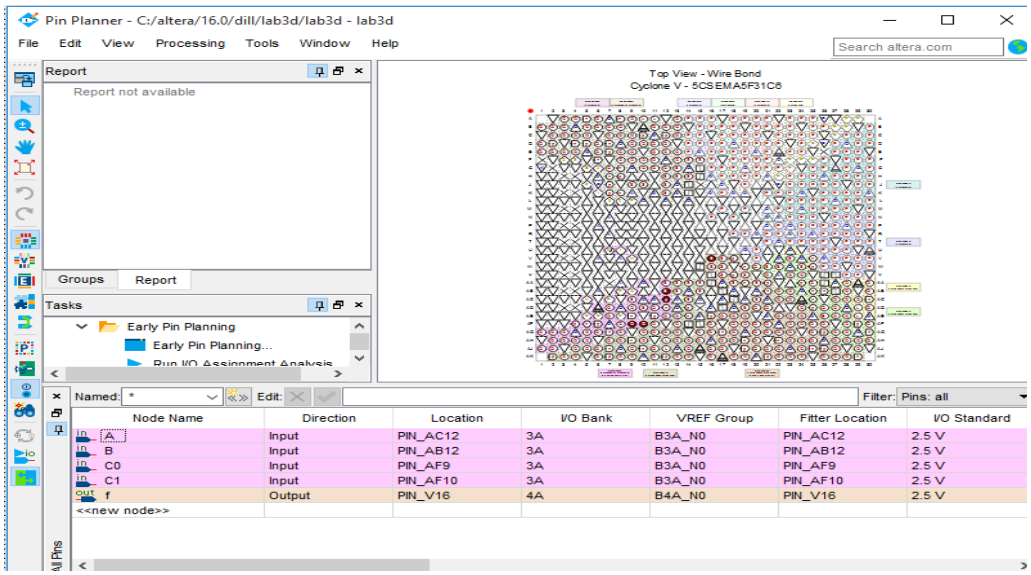

Pin Planner - C:/altera/16.0/dill/Lab3c/lab3text - lab3text
File Edit View Processing Tools Window Help
Report
Report not available
Groups Report
Tasks
Early Pin Planning
Early Pin Planning...
Top View - Wire Bond
Cyclone V - 5CSEMA5F31C6
Named: * Edit: Filter: Pins: all
Node Name Direction Location I/O Bank VREF Group Fitter Location I/O Standard
A Input PIN_AC12 3A B3A_N0 PIN_AC12 2.5 V
B Input PIN_AB12 3A B3A_N0 PIN_AB12 2.5 V
C0 Input PIN_AF9 3A B3A_N0 PIN_AF9 2.5 V
C1 Input PIN_AF10 3A B3A_N0 PIN_AF10 2.5 V
f Output PIN_V16 4A B4A_N0 PIN_V16 2.5 V
<<new node>>
All Pins

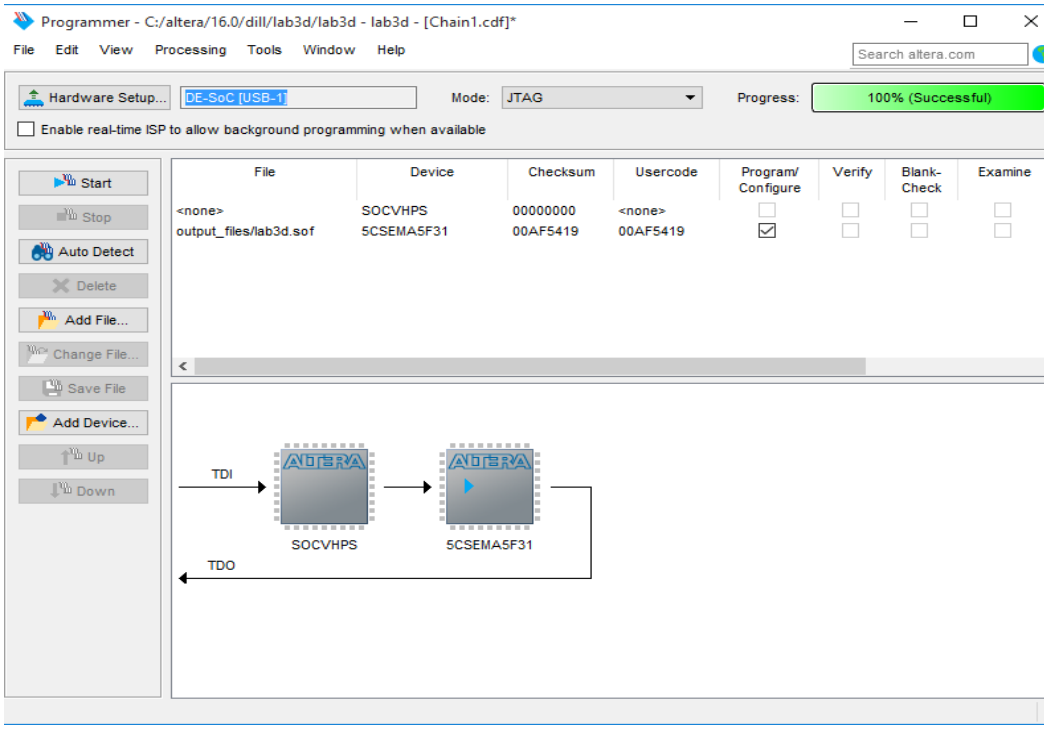

Programmer - C:/altera/16.0/dill/Lab3c/lab3text - lab3text - [Chain2.cdf]*
File Edit View Processing Tools Window Help
Search altera.com
Hardware Setup... DE-SoC [USB-1] Mode: JTAG Progress: 100% (Successful)
Enable real-time ISP to allow background programming when available
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File Device Checksum Usercode Program/ Configure Verify Blank-Check Examine
<none> SOCVHPS 00000000 <none>
output_files/lab3text.sof 5CSEMA5F31 00AF5416 00AF5416
TDI
SOCVHPS
5CSEMA5F31
TDO

b. Schematic Part

We compile the schematic file and test the file. Then import to the board, after setting the switches, we test the different combination on the board.

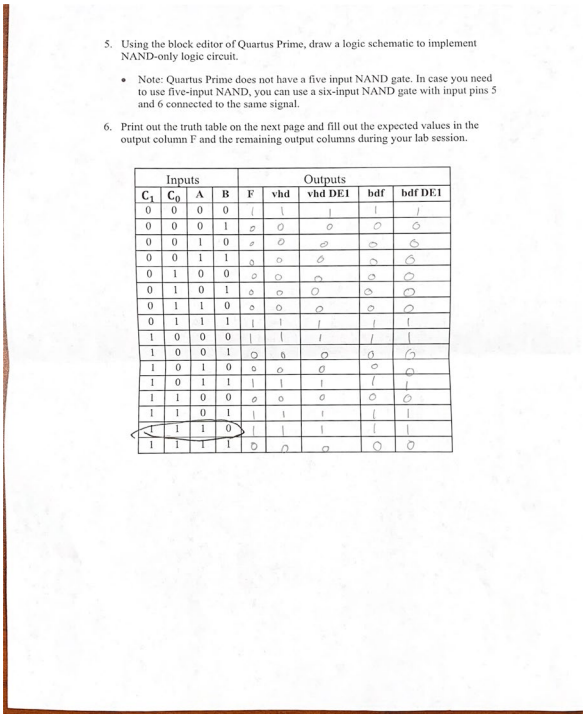






Result

The testing schematic file and VHDL file are same as we predict in the prelab.

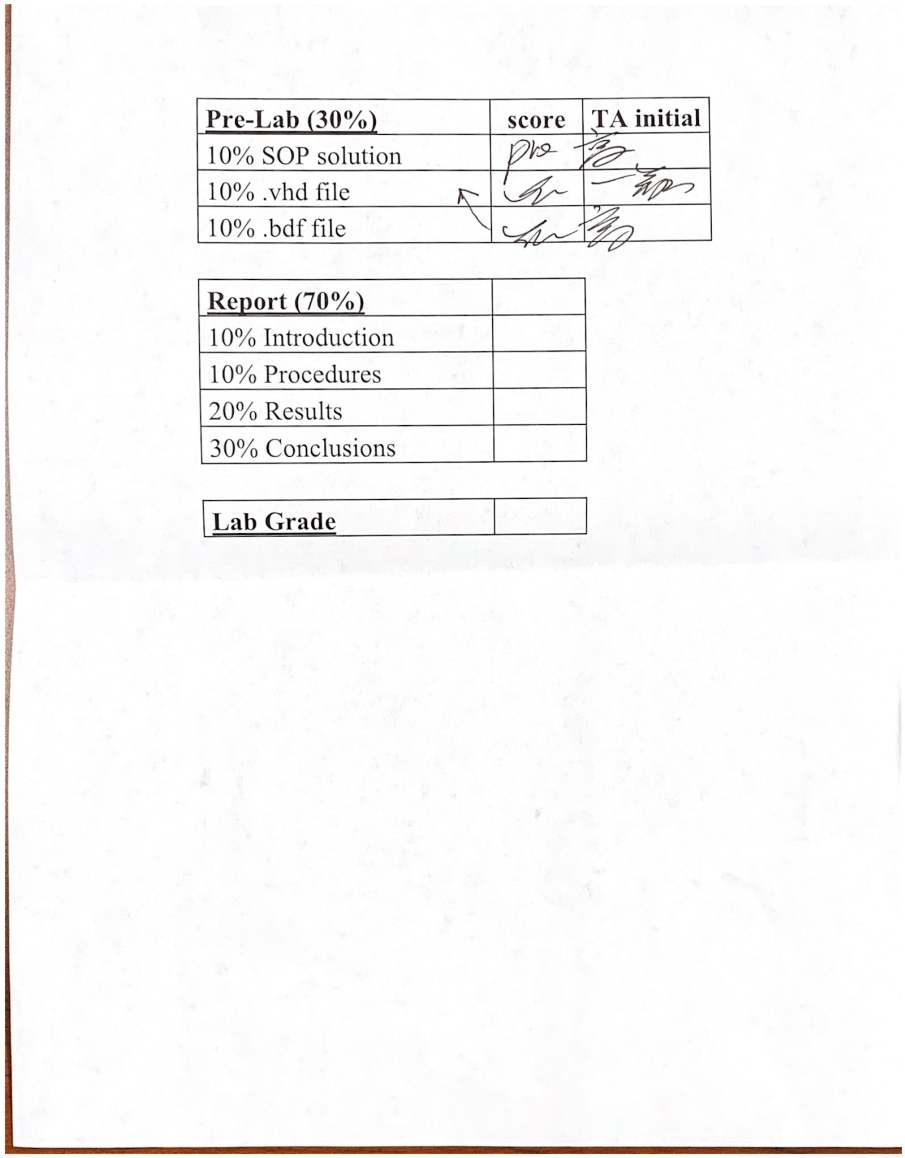


5. Using the block editor of Quartus Prime, draw a logic schematic to implement NAND-only logic circuit.
   - Note: Quartus Prime does not have a five input NAND gate. In case you need to use five-input NAND, you can use a six-input NAND gate with input pins 5 and 6 connected to the same signal.
6. Print out the truth table on the next page and fill out the expected values in the output column F and the remaining output columns during your lab session.

Inputs				Outputs				
C_1	C_0	A	B	F	vhd	vhd DE1	bdf	bdf DE1
0	0	0	0					
0	0	0	1					
0	0	1	0					
0	0	1	1					
0	1	0	0					
0	1	0	1					
0	1	1	0					
0	1	1	1					
1	0	0	0					
1	0	0	1					
1	0	1	0					
1	0	1	1					
1	1	0	0					
1	1	0	1					
1	1	1	0					
1	1	1	1					

Conclusion

During the lab, we understand how to configure the Altera's DE1 board and test the function through VHDL method and Schematic method to check the actual result from the board is same as we predict in the prelab.



Pre-Lab (30%)	score	TA initial
10% SOP solution		
10% .vhd file		
10% .bdf file		

Report (70%)	
10% Introduction	
10% Procedures	
20% Results	
30% Conclusions	

Lab Grade	