

Lab 02
ECE 380-002
University of Alabama

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Introduction

This laboratory has two parts. The first part aims at building a simple circuit by VHDL and Schematic file through a truth table. In the second part, we upload the file done by the part one to the Altera's DE1 board.

Procedure

a) Part I

a. Design A

Before the lab, our team have figured out the function by Max Term (POS). Then on the lab, we created the VHDL File called designA.vhl (Figure 1) After the successfully compiling, we run the stimulation test, in the waveform file called designA_test.wvf. (Figure 2) we created 8 possible scenarios. The result shows that the outcome is same as the truth table.

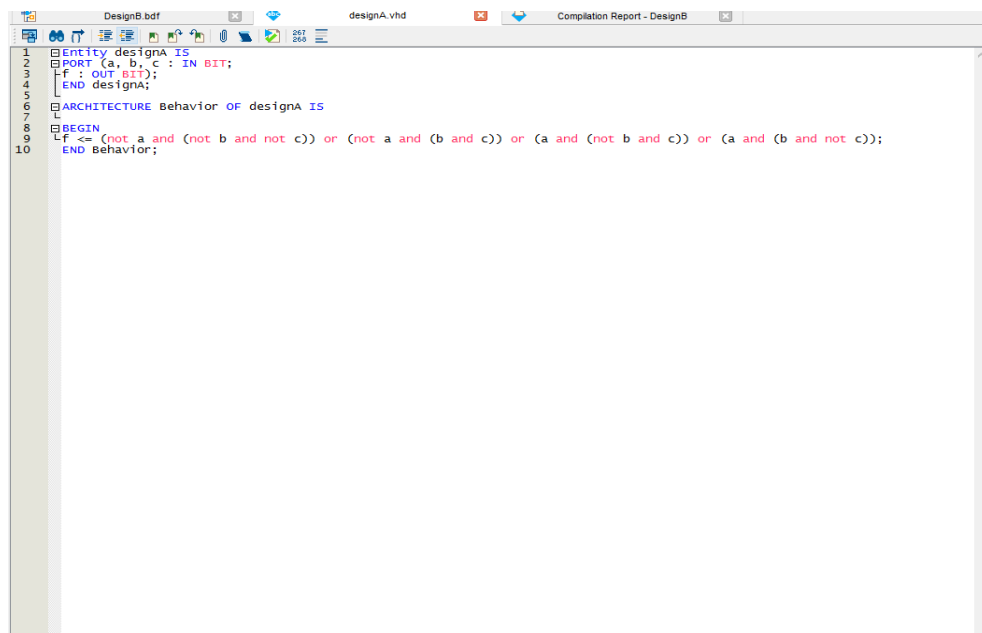


Figure 1 designA.vhl

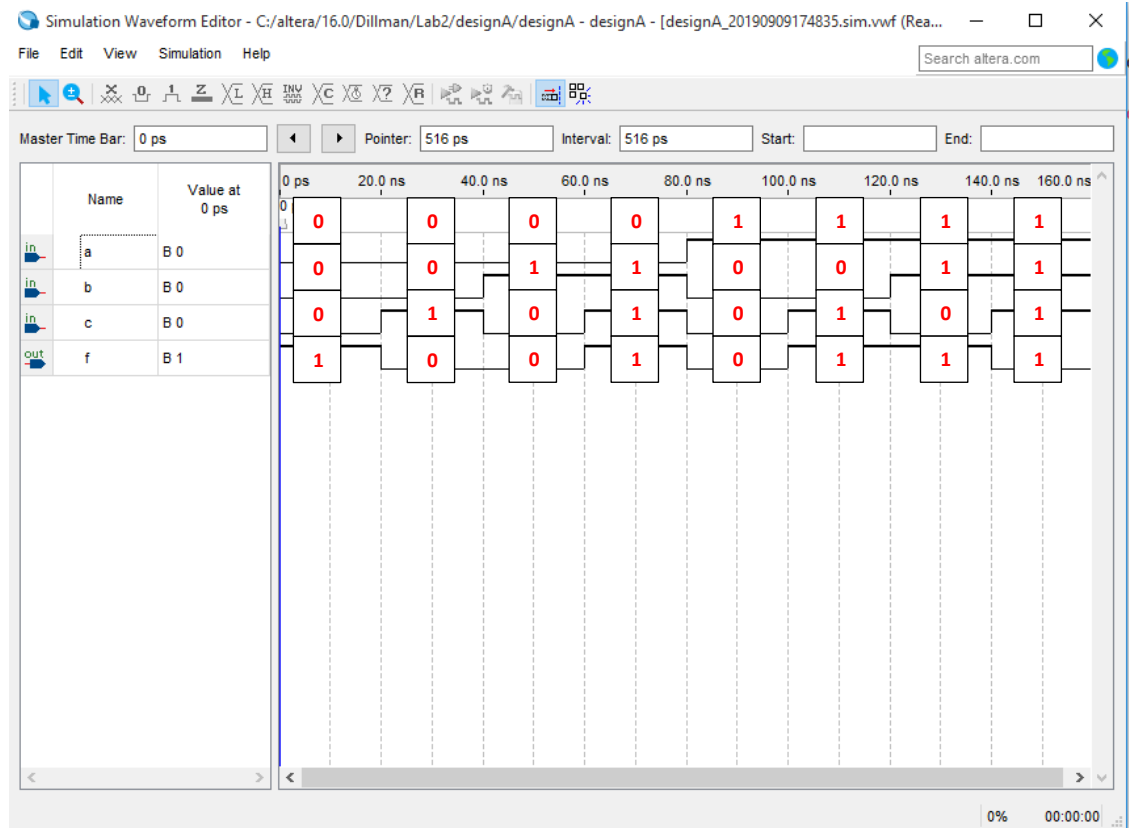


Figure 2 designA_test.wvf

b. Design B

In design B, we built the same circuit in design A through schematic form. We created a Body Diagram File named designB.bdf. (Figure 3) After compiling, we run the same test in the design A. The result is also same as the truth table outcome. (Figure 4)

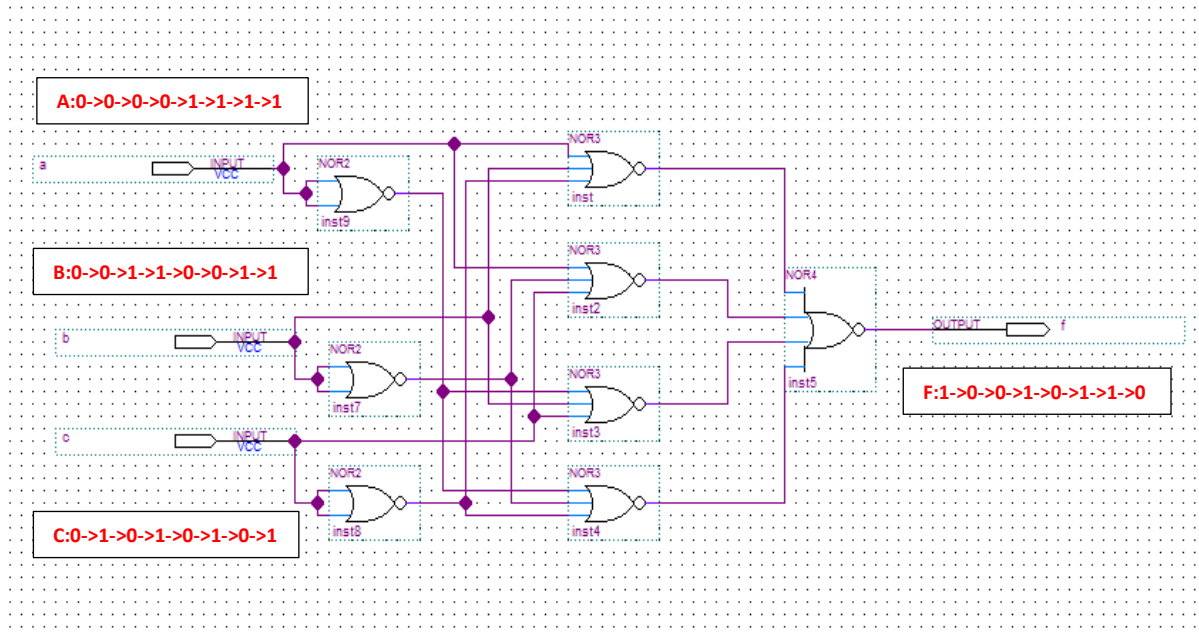


Figure 3 designB.bdf

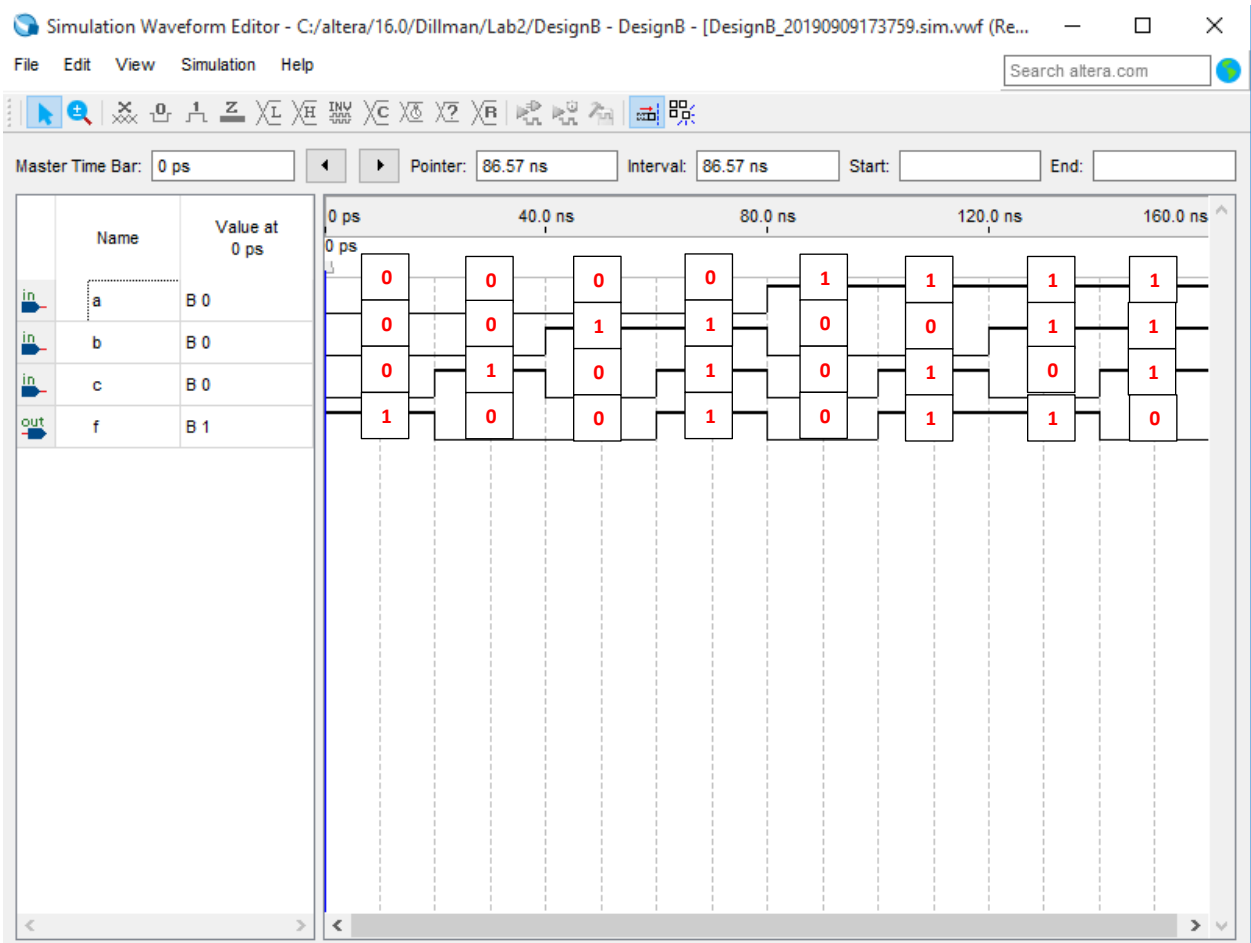


Figure 4 designB.wvf

b) Part II

We make a simple design by the guide in the lab2 assignment. We follow the instruction and configure the Altera's DE1 board. Then create a project named frequency. We created a new BDF File named frequency.bdf. (Figure 5) After compiling, we assigned the pins on the board. (Figure 6) Then compile again, the LED on the Board is flashing, and the progress shows successful.

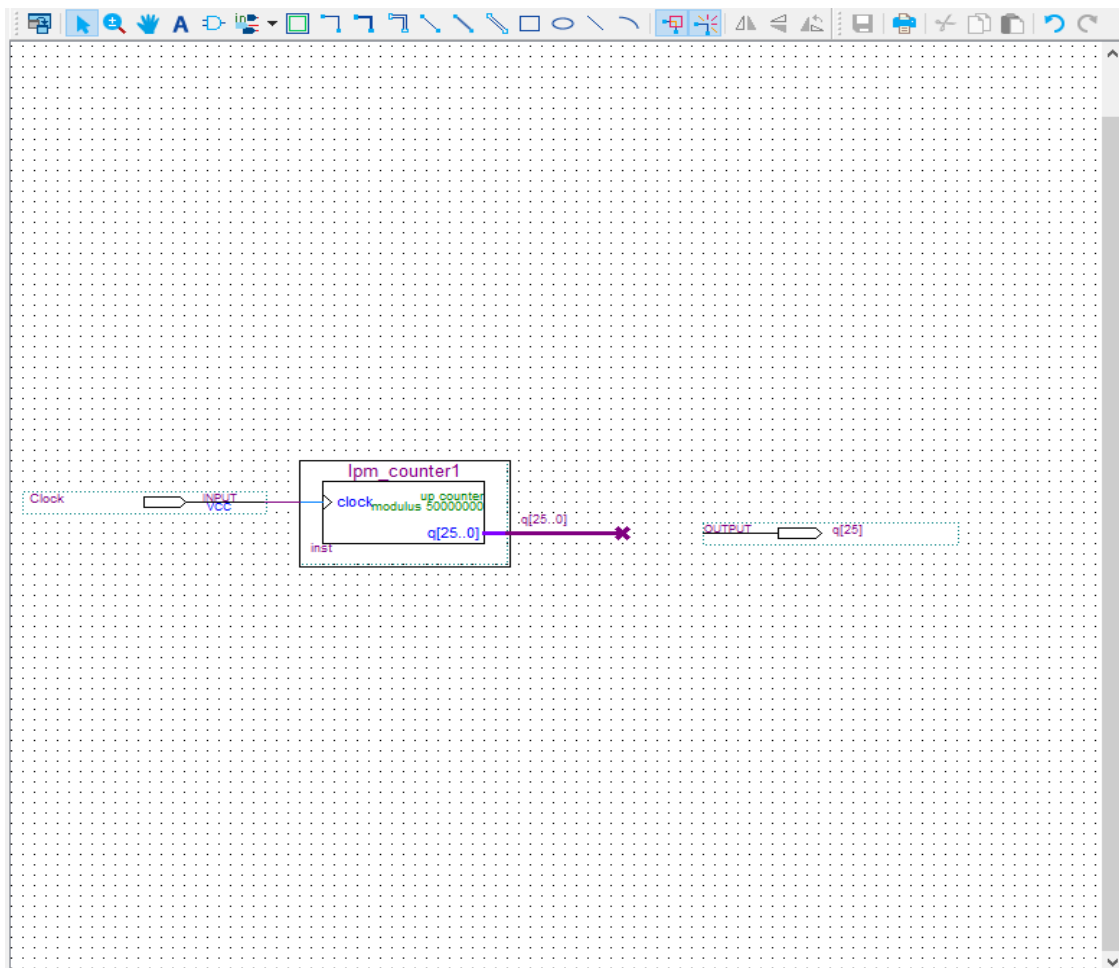


Figure 5 frequency.bdf

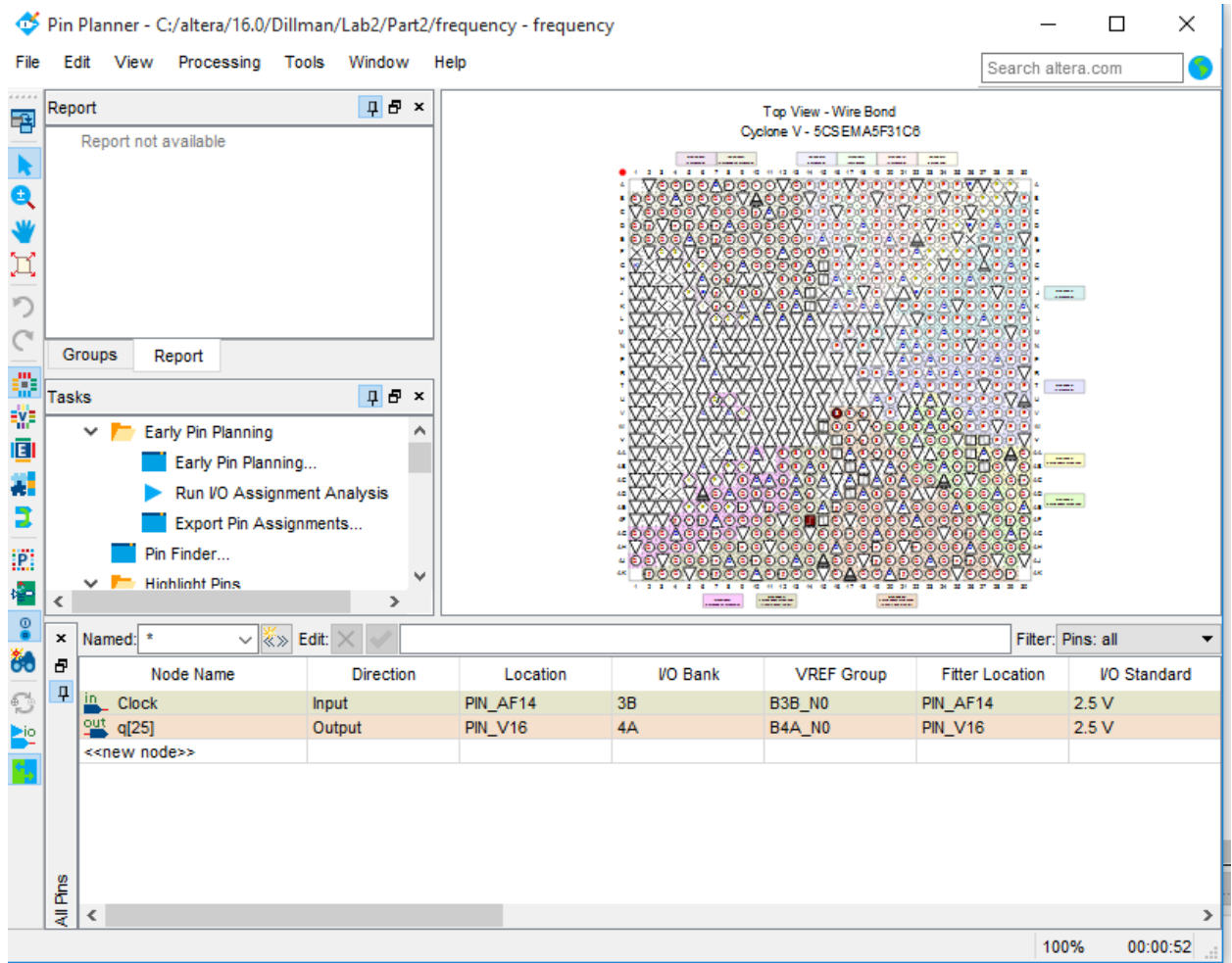


Figure 6 assign the pin

Conclusion

All two parts in the lab 2 are all finished successful.

Print this page, bring the hardcopy to your lab session, get it signed by the TA after the demo, and submit it along with your report

Lab demo (50 pts)	Score	TA initial
Part I (Designs A, B), 25 pts	A	SM
	B	SM
	C	SM
Report (50 pts)		
Lab 2 Total Grade (100 pts)		
Bonus: Quartus Prime Installation (25 pts) (Note: You only get one time 25 pts, not both times)	Thomas Dillman	

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