ECE 380: Lab #8: Code Converters

Design A

Implement Design A (for the Cyclone® V device) of the pre-lab. Verify the design correctness by simulating it in Quartus Prime.

Download and test Design A on the Cyclone® V device. **Have the TA verify your results.**

- Use inputs SW[3..0] (Note: SW[0] is the LSB) for the input h_3-h_0.
- Use seven-digit display HEX0 [6..0] (note: HEX1 [0] is the MSB(led_0) and HEX0[6] is the LSB(led_6)) for the LED's outputs (led_0 - led_6).

Design B

Implement Design B (for the Cyclone® V device) of the pre-lab. Verify the design correctness by simulating it in Quartus Prime. Download and test Design B on the Cyclone® V device. You can decide on the pin assignments yourself.

- Use inputs SW [3..0] (note: SW[0] is the LSB) for the inputs (h_3-h_0).
- Use two seven-digit displays HEX1 [6] and HEX0 [6..0] (Note: HEX1 [6] is the MSB and HEX0[6] is the LSB) for the LED's outputs (led_0 - $leds_7$).

Design C

Implement Design C (for the Cyclone® V device) of the pre-lab. Verify the design correctness by simulating it in Quartus Prime. Download and test Design C on the Cyclone® V device. You can decide on the pin assignments yourself. Fill out the form below.

- Use inputs SW [9..6] (note: SW[6] is the LSB) for the X input (X_3-X_0).
- Use inputs SW [5..2] (note: SW[2] is the LSB) for the Y input (Y_3-Y_0).
- Use inputs SW [0] for ADD_SUB.
- Use inputs LEDR [3..0] (note: LEDR[0] is the LSB) for the S output (S_3-S_0).
- Use inputs LEDR [9], LEDR[8] for overflow and Cout.
- Use two seven digit display HEX5 [6] and HEX4 [6..0] (note: HEX5 [6] is the MSB and HEX4[6] is the LSB) for the outputs ($hexx_0$ - $hexx_7$). Use two seven-digit displays HEX3 [6] and HEX2 [6..0] (again, HEX3 [6] is the MSB and HEX2[6] is the LSB) for the outputs ($hexy_0$ - $hexy_7$). Use two seven-digit displays HEX1 [6] and HEX0 [6..0] (again, HEX1 [6] is the MSB and HEX0[6] is the LSB) for the outputs ($hexs_0$ - $hexs_7$).

			EXPECTED			SIMULATED			DE1 Board		
	A	B	S	fo	co	S	Fo	co	S	fo	co
ADD	5	2									
ADD	8	F									
ADD	7	E									
ADD	9	E									
SUB	E	F									
SUB	7	3									
SUB	7	E									
SUB	E	4									

Homework #8 (100 points)

1) (20 pts) Draw two implementations of gated SR latches and their characteristic table.

2) (20 pts) Draw a D latch and its characteristic table.

3) (20 pts) Draw a negative-edge-triggered D flip-flop using the master-slave configuration. Draw its characteristic table.

4) (20 pts) Draw a positive-edge-triggered D flip-flop using the master-slave configuration. Draw its characteristic table.

5) (20 pts) Explain the difference between the following pair of concepts:

a) D latches versus D flip-flops
b) Basic latches versus gated latches
c) Asynchronous clear versus synchronous clear
d) Level sensitive devices versus edge-triggered devices