Lab 07
Adder Design Tradeoffs

ECE 380-002
University of Alabama

Yichen Huang
Thomas Dillman

2019/10/7

Introduction

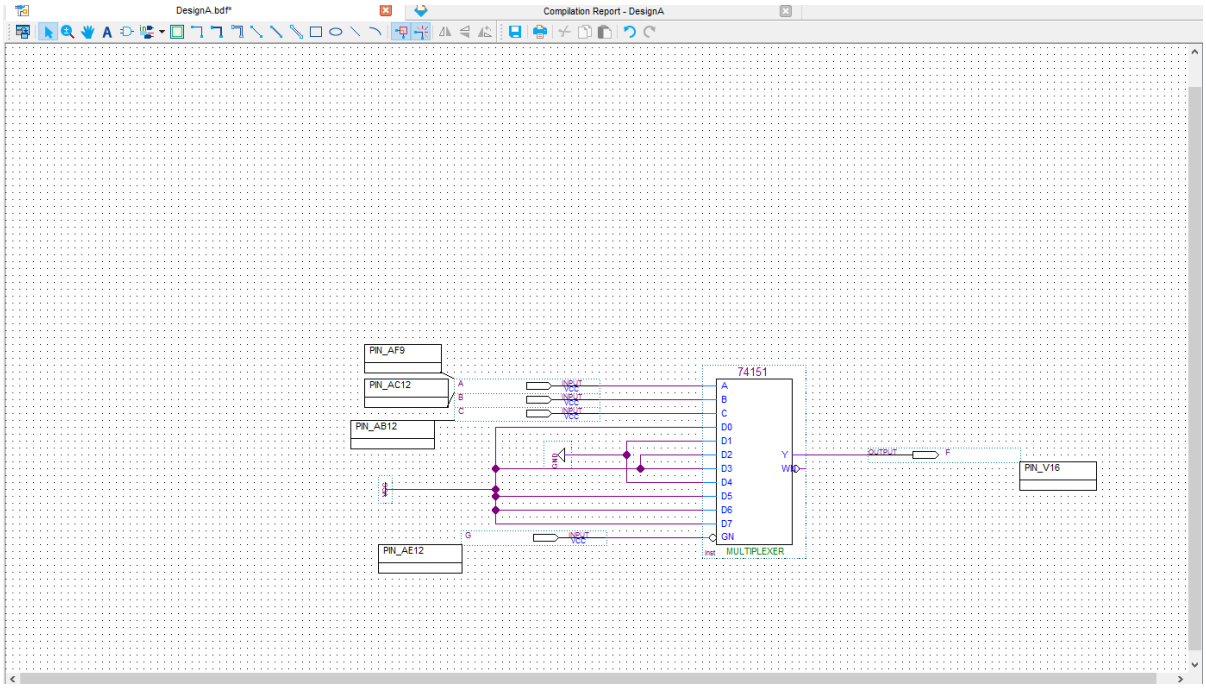
In this lab, we use the Quartus II software package to design and test combinational circuit designs with multiplexers and decoders. We understand standard IC chips 74151, an 8-to-1 multiplexer, and 74154, a 4-to-16 decoder and use them to implement logic functions.

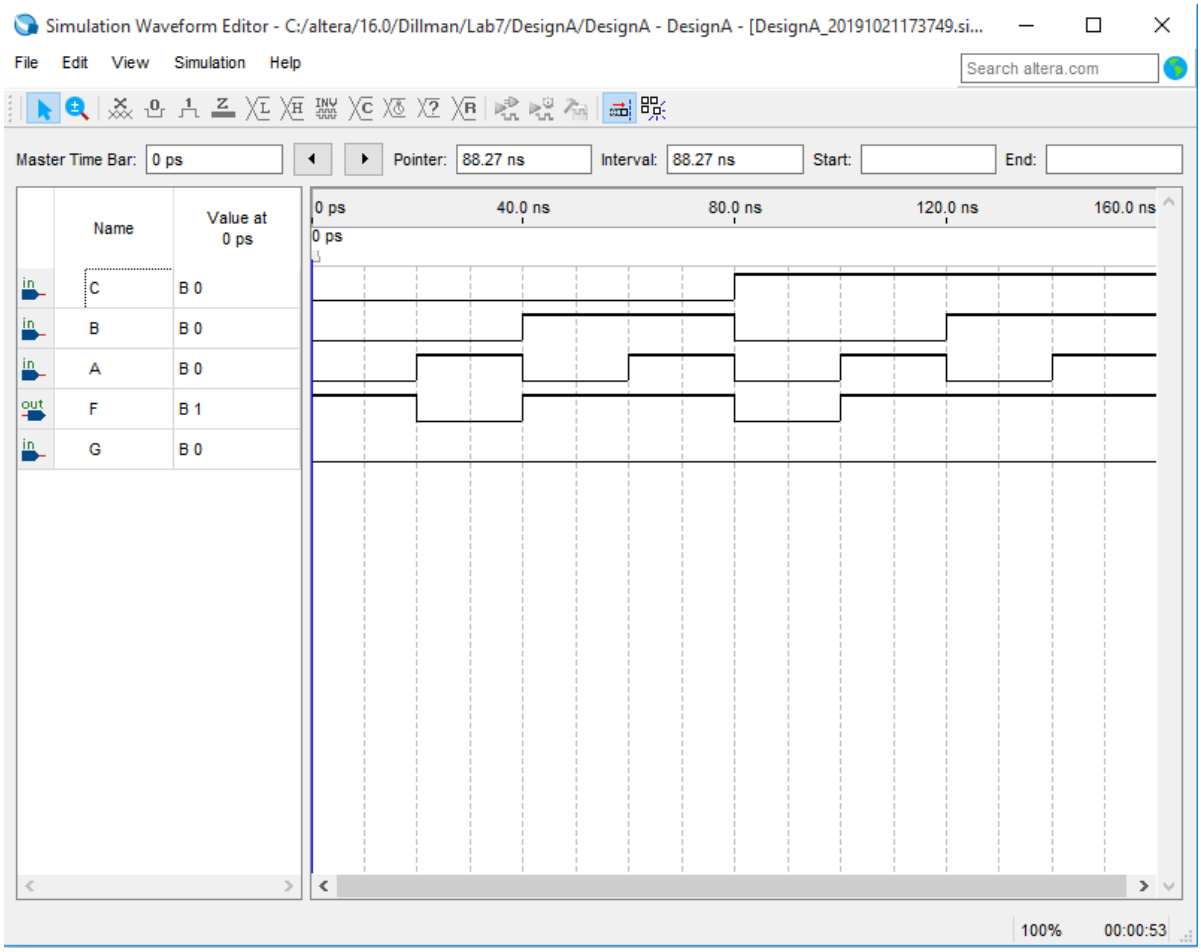
Procedure

A. Prelab

a. Design A

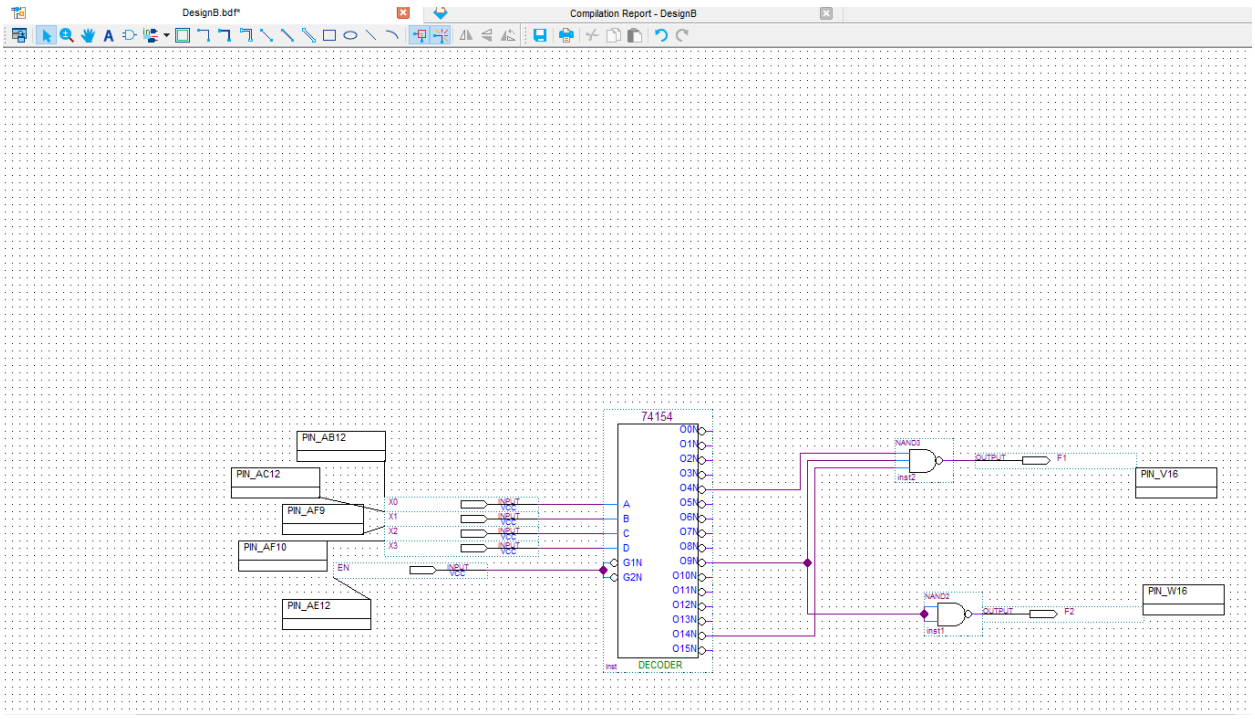
In the design A, we analyze the logic function by truth table. Then we implement the function to the multiplexer. Then stimulate the schematic file, which is same as we expect.

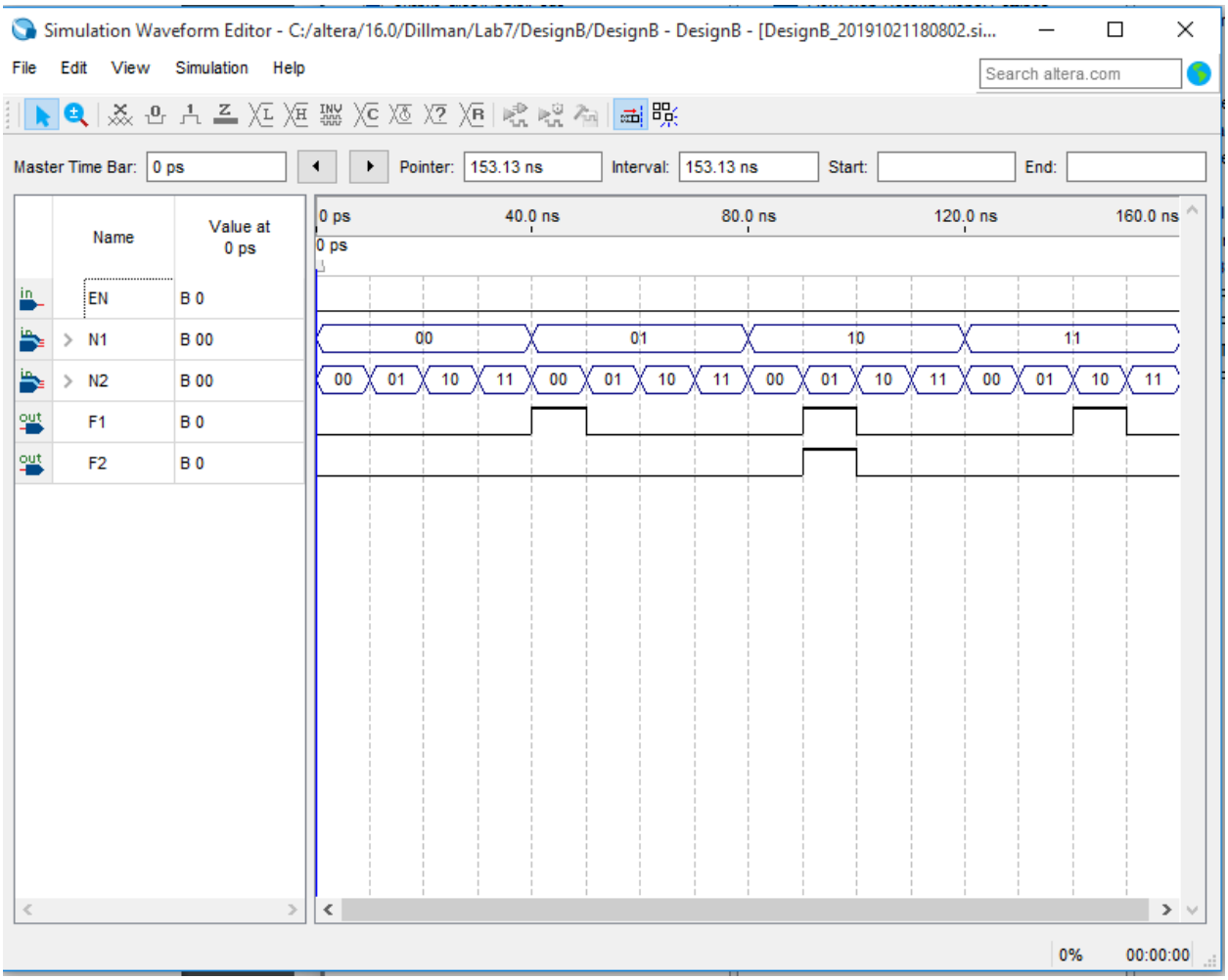




b. Design B

In the design B, we also analyze the problem by created a 4-varible truth table. Then, we implement to the 4-to-16 decoder. Then we compile and simulate the file. The result is also matching our expected in the analyzing part.


DesignB.bdf*
Compilation Report - DesignB
74154
PIN_AB12
PIN_AC12
PIN_AF9
PIN_AF10
PIN_AE12
EN
A
B
C
D
G1N
G2N
DECODER
PIN_V16
PIN_W16
F1
F2


Simulation Waveform Editor - C:/altera/16.0/Dillman/Lab7/DesignB/DesignB - DesignB - [DesignB_20191021180802.si...
File
Edit
View
Simulation
Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 153.13 ns
Interval: 153.13 ns
Start:
End:
Name
Value at 0 ps
EN
B 0
N1
B 00
N2
B 00
F1
B 0
F2
B 0
0 ps
40.0 ns
80.0 ns
120.0 ns
160.0 ns
00
01
10
11
0%
00:00:00

c. Chips description

1. Chip 74151

This chip is an 8-to-1 multiplexer with an enable input, three select signal inputs and 8 function input.

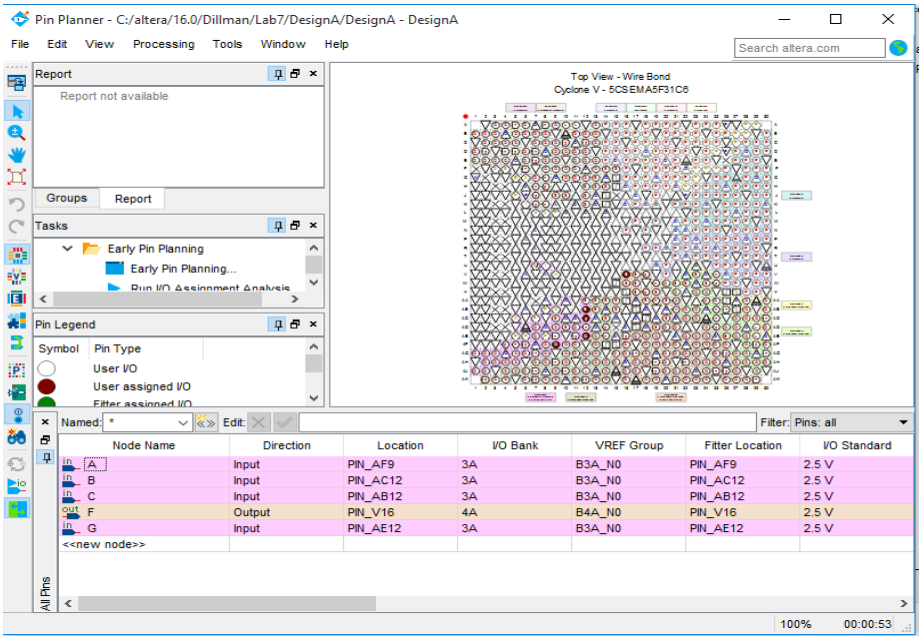
2. Chip 74154

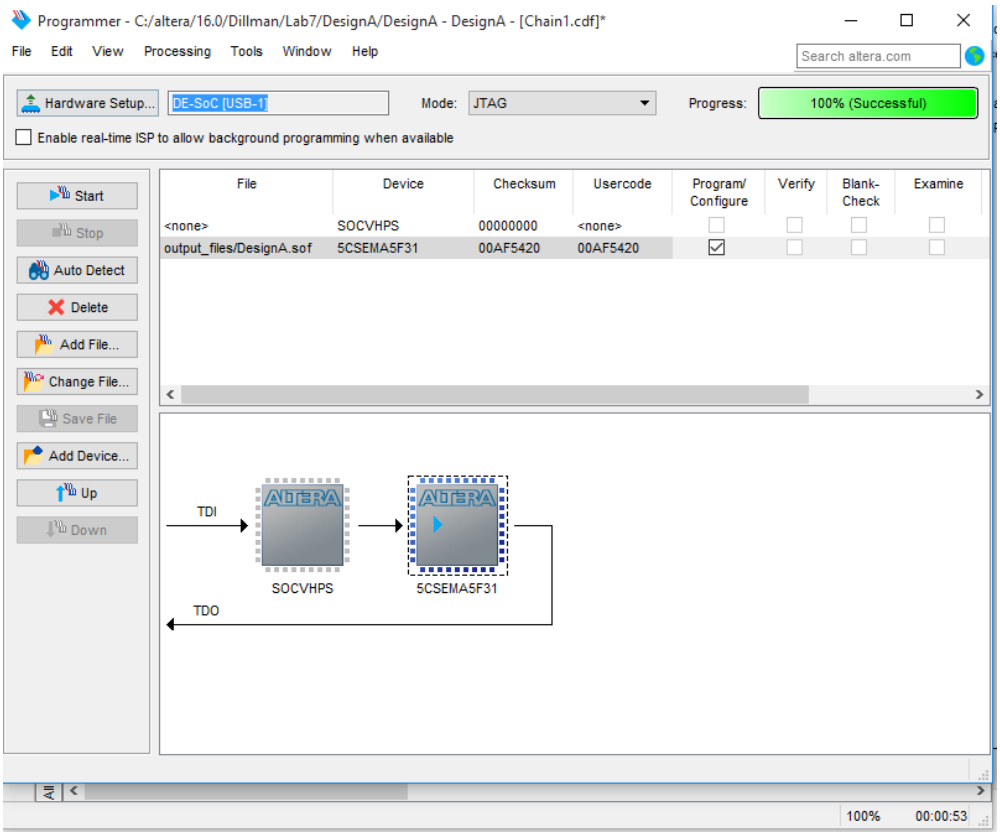
This chip is a 4-to-14 encoder. The chip will enable by both enable switch is off. The take 4-varibles for input.

B. During the lab

a. Design A

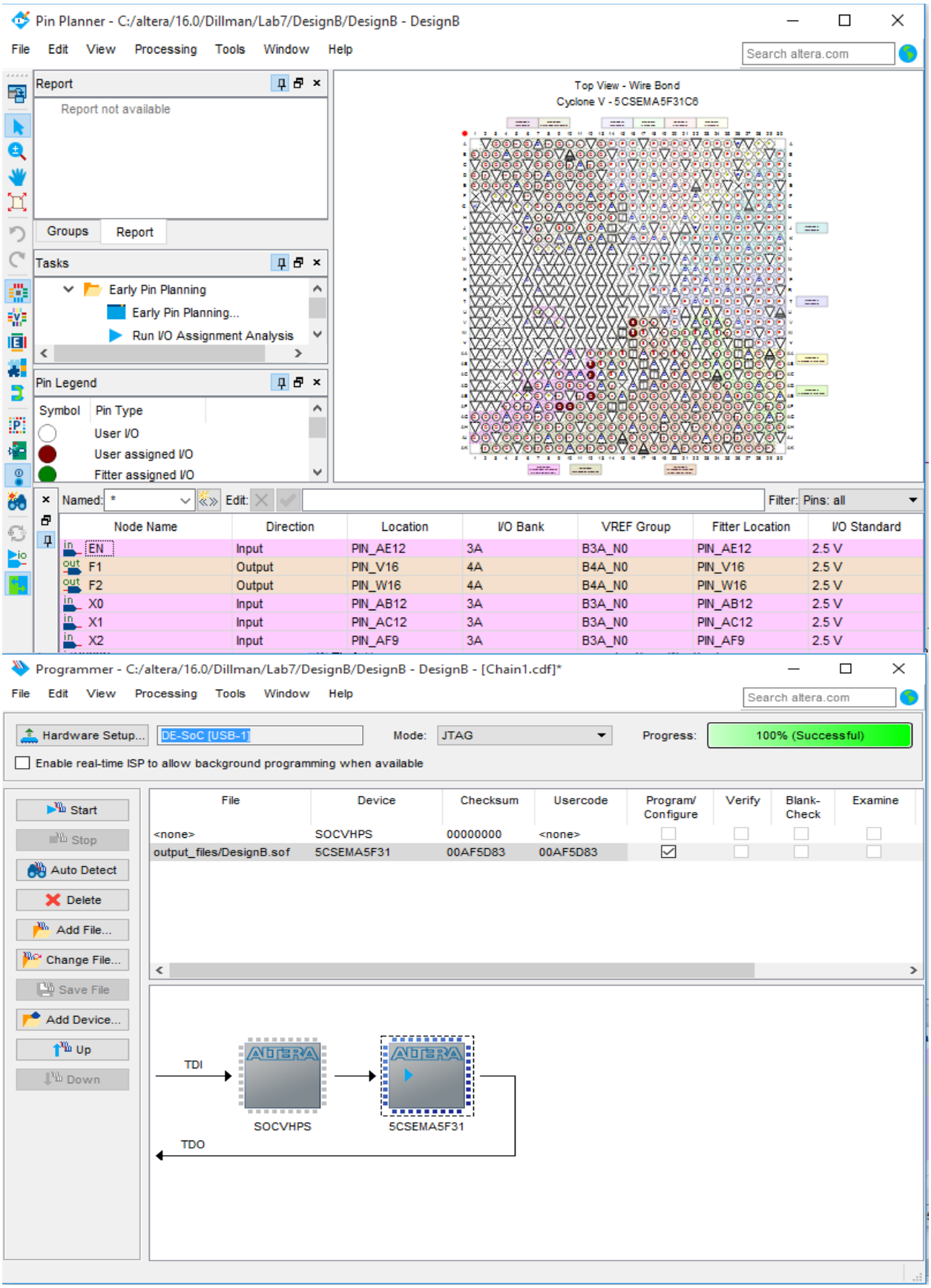
In the lab, we assign the input and the output to the pin. Then we compiled the file again and test on the DE1 board. The result is also correct our simulate result and expect result.





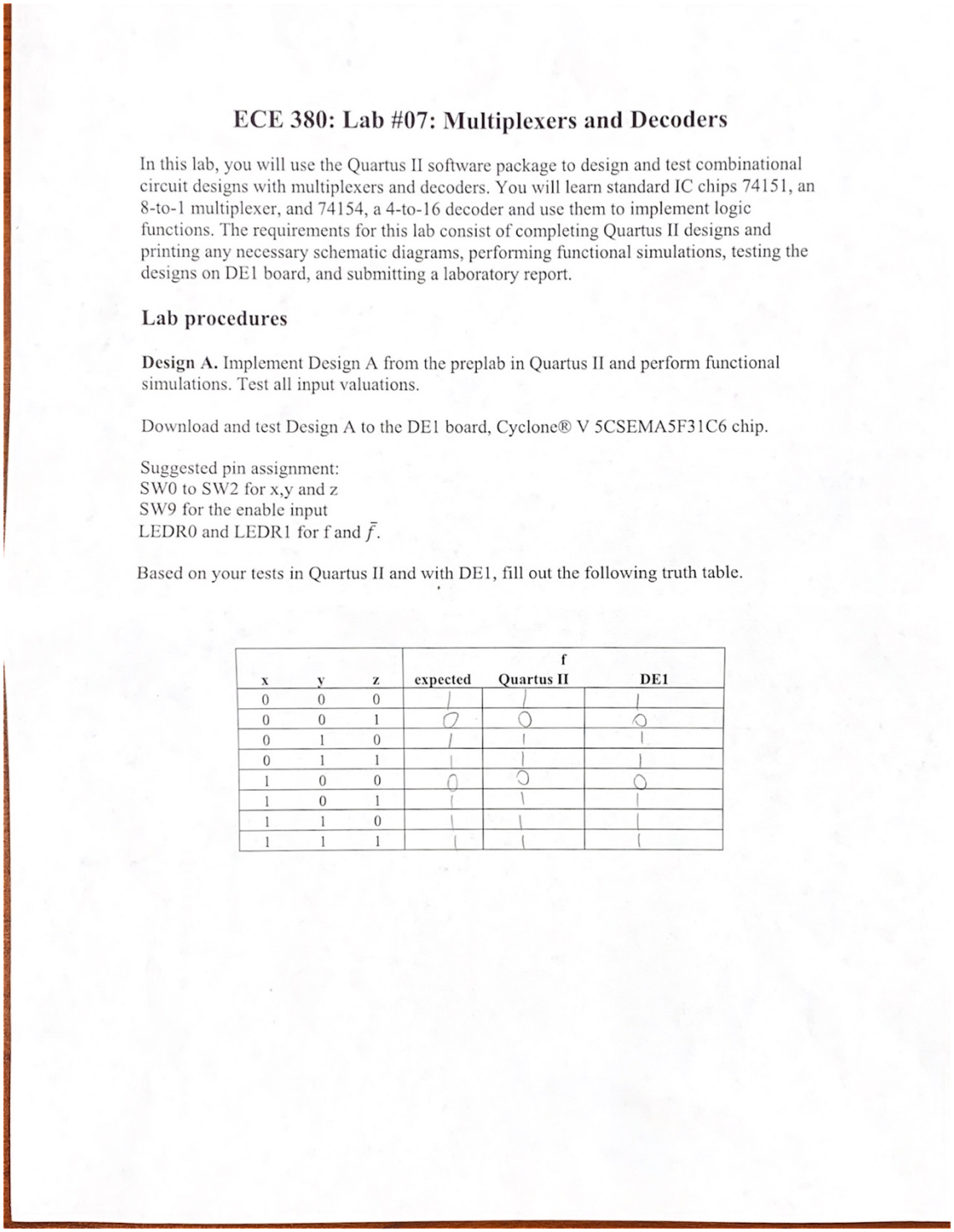
b. Design B

We repeat the same process in the design A, the result is also same as our simulate result and our respect result.


Pin Planner - C:/altera/16.0/Dillman/Lab7/DesignB/DesignB - DesignB
File Edit View Processing Tools Window Help
Search altera.com
Report
Report not available
Groups Report
Tasks
Early Pin Planning
Early Pin Planning...
Run I/O Assignment Analysis
Pin Legend
Symbol Pin Type
User I/O
User assigned I/O
Fitter assigned I/O
Top View - Wire Bond
Cyclone V - 5CSEMA5F31C6
Named: * Edit: Filter: Pins: all
Node Name Direction Location I/O Bank VREF Group Fitter Location I/O Standard
EN Input PIN_AE12 3A B3A_N0 PIN_AE12 2.5 V
F1 Output PIN_V16 4A B4A_N0 PIN_V16 2.5 V
F2 Output PIN_W16 4A B4A_N0 PIN_W16 2.5 V
X0 Input PIN_AB12 3A B3A_N0 PIN_AB12 2.5 V
X1 Input PIN_AC12 3A B3A_N0 PIN_AC12 2.5 V
X2 Input PIN_AF9 3A B3A_N0 PIN_AF9 2.5 V
Programmer - C:/altera/16.0/Dillman/Lab7/DesignB/DesignB - DesignB - [Chain1.cdf]*
File Edit View Processing Tools Window Help
Search altera.com
Hardware Setup... DE-SoC [USB-1] Mode: JTAG Progress: 100% (Successful)
Enable real-time ISP to allow background programming when available
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File Device Checksum Usercode Program/ Configure Verify Blank-Check Examine
<none> SOCVHPS 00000000 <none>
output_files/DesignB.sof 5CSEMA5F31 00AF5D83 00AF5D83
TDI
SOCVHPS
5CSEMA5F31
TDO

Result

The result is same as we expected and simulated result.



ECE 380: Lab #07: Multiplexers and Decoders

In this lab, you will use the Quartus II software package to design and test combinational circuit designs with multiplexers and decoders. You will learn standard IC chips 74151, an 8-to-1 multiplexer, and 74154, a 4-to-16 decoder and use them to implement logic functions. The requirements for this lab consist of completing Quartus II designs and printing any necessary schematic diagrams, performing functional simulations, testing the designs on DE1 board, and submitting a laboratory report.

Lab procedures

Design A. Implement Design A from the preplab in Quartus II and perform functional simulations. Test all input valuations.

Download and test Design A to the DE1 board, Cyclone® V 5CSEMA5F31C6 chip.

Suggested pin assignment:
SW0 to SW2 for x,y and z
SW9 for the enable input
LEDR0 and LEDR1 for f and $\bar{f}$.

Based on your tests in Quartus II and with DE1, fill out the following truth table.

x	y	z	f expected	f Quartus II	f DE1
0	0	0	1	1	1
0	0	1	0	0	0
0	1	0	1	1	1
0	1	1	1	1	1
1	0	0	0	0	0
1	0	1	1	1	1
1	1	0	1	1	1
1	1	1	1	1	1

Design B. Implement Design B from the preplab in Quartus II and perform functional simulations. Test all input valuations.

Download and test Design B to the DE1 board, Cyclone® V 5CSEMA5F31C6 chip.

Suggested pin assignment:
SW0 to SW3 for x0 to x3
SW8 and SW9 for two enable inputs
LEDR0 and LEDR1 for f1 and f2

Based on your tests in Quartus II and with DE1, fill out the following truth table.

N1		N2		expected		Quartus II		DE1	
x3	x2	x1	x0	f1	f0	f1	f0	f1	f0
0	0	0	0						
0	0	0	1						
0	0	1	0						
0	0	1	1						
0	1	0	0						
0	1	0	1						
0	1	1	0						
0	1	1	1						
1	0	0	0						
1	0	0	1						
1	0	1	0						
1	0	1	1						
1	1	0	0						
1	1	0	1						
1	1	1	0						
1	1	1	1						

Conclusion

In the lab, we understand how to use multiplexer and decoder to implement logic functions and test the result on the DE1 board.

After completing the design, you can compile the project and perform functional simulations. As the function only has four inputs, it is possible to test all the input valuations. You can specify these inputs as clock signals with different periods to realize all input valuations, in functional simulations. Please refer to Lab 02 for detailed procedures.

Prelab requirements:

At the beginning of your lab session, you need to present to the TA

- **Two short paragraphs to describe the standard chips, 74151 and 74154.**
- **Design A and Design B in the forms of Quartus II schematic entries.**

Pre-Lab (30%)	**Score**	**TA initial**
20% Designs	A	
10% Paragraphs	B	
Report (70%)		
10% Introduction		
10% Procedures		
20% Results		
30% Conclusions		
Lab Grade (100%)		