ECE 380 lab1 tutorial

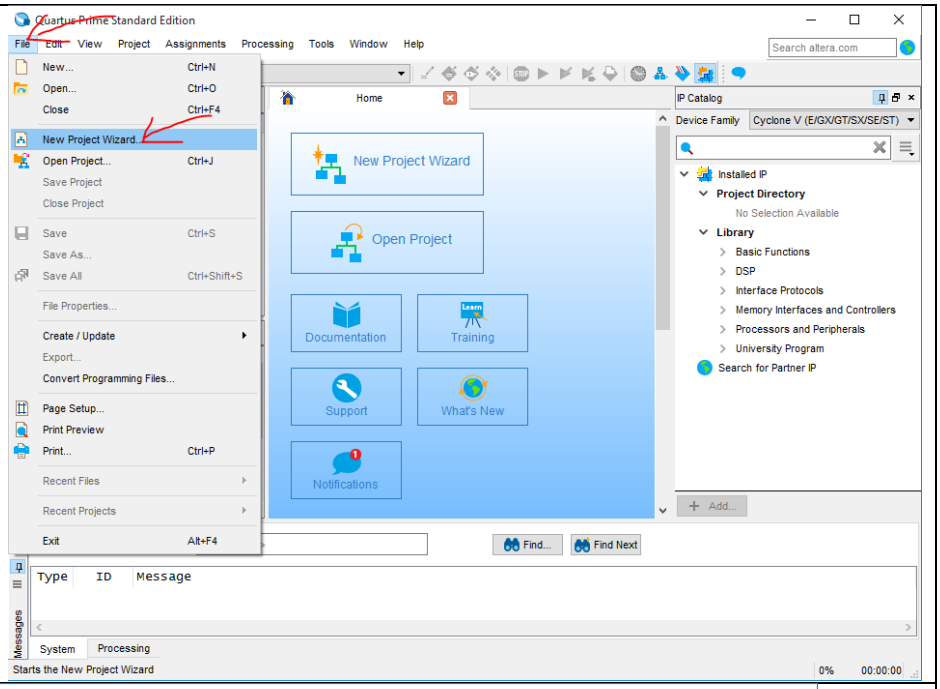
Quartus II version 16.0

Step1: Learn via Quartus II Tutorial

1. Build a new project:

File -> New Project Wizard

Press **Next** button in **Introduction** window

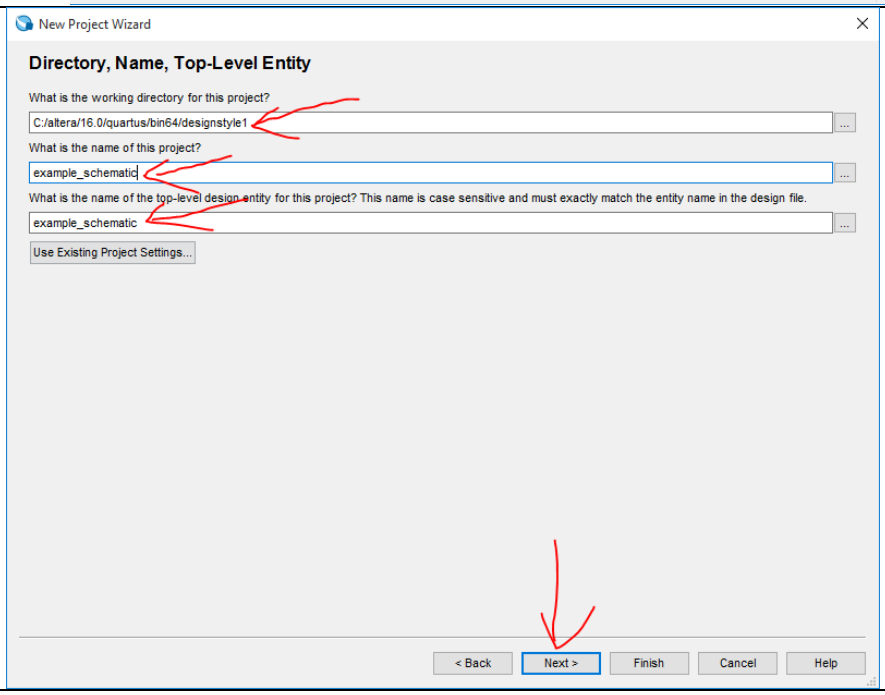


Create a particular directory for the project: **C:/altera/16.0/quartus/bin64/designstyle1** (If the directory has been created by previous group, just create a new folder with another name. Remember the directory of your project, because we will use it later)

Project name: **example_schematic**

The name of the top-level entity for the project: **example_schematic**

Click Next

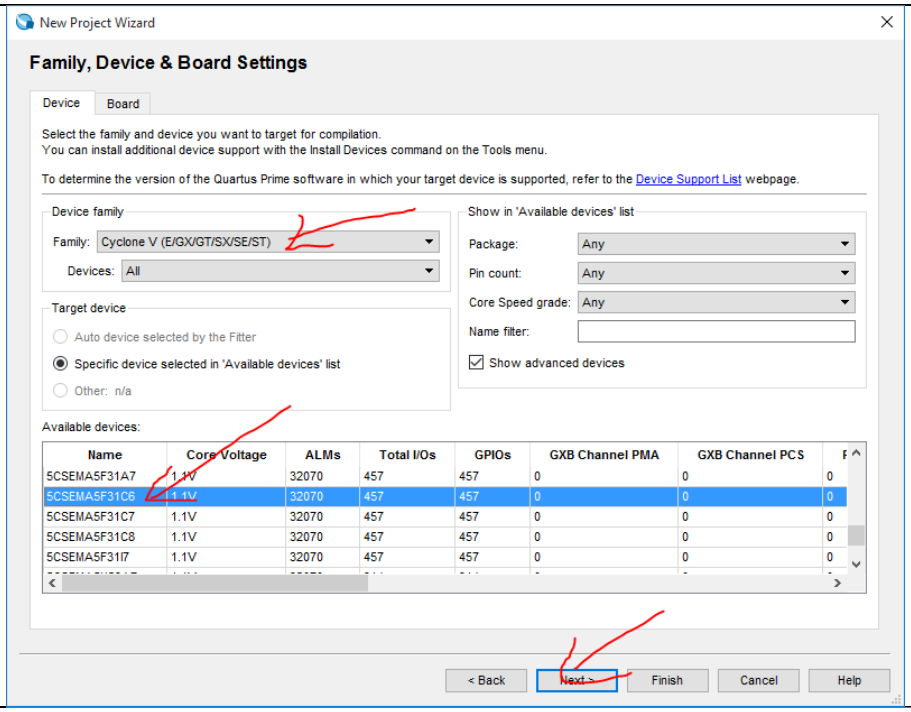


Directly press Next button in **Project Type** Window and **Add Files** window

In the **Family, Device & Board Settings** window,

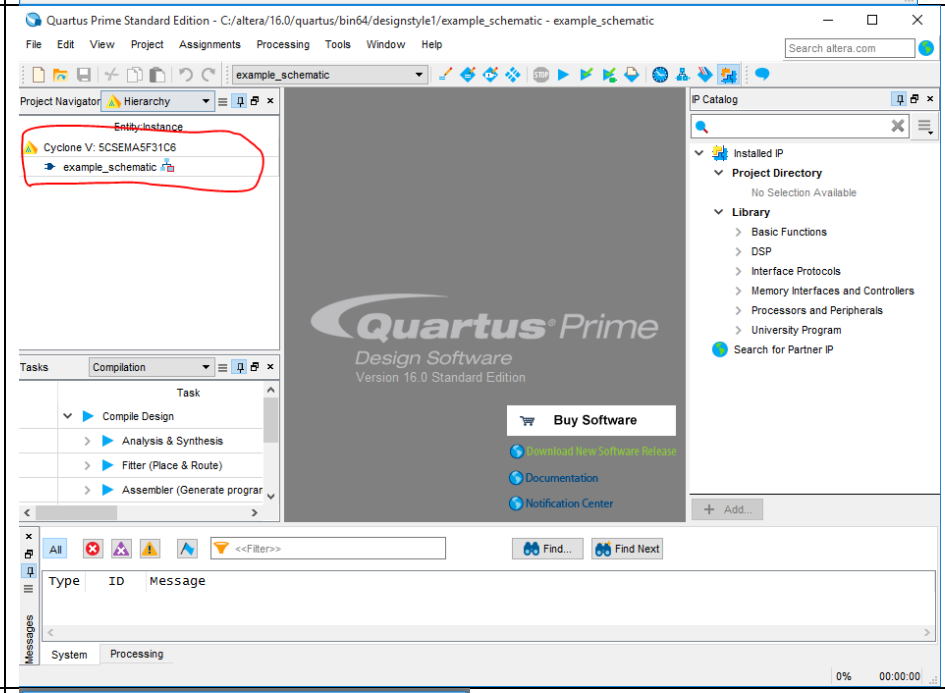
Device family:
Cyclone V (E/GX/GT/SX/SE/ST)

Available device:
5CSEMA5F31C6



Click: **finish** button

You will see your project in **Project Navigator** window

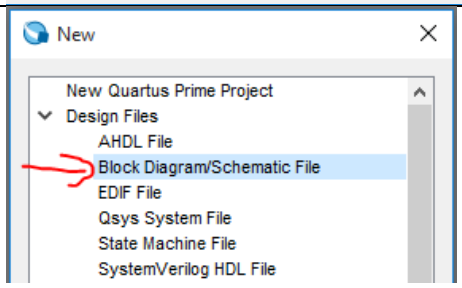


2. Using the Block Editor:

File -> New

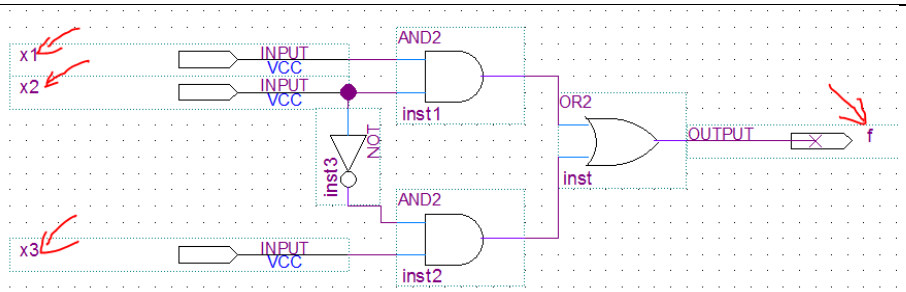
Select: **Block Diagram/Schematic File**

Press: OK



Now, you are about to build a schematic as shown in Figure.

1. Import two **AND2** gates, three **INPUT**, one **OR2** gate, one **OUTPUT**, and one **NOT** gate
2. Connect the elements
3. Rename the three **INPUT** and one **OUTPUT** as shown in figure.

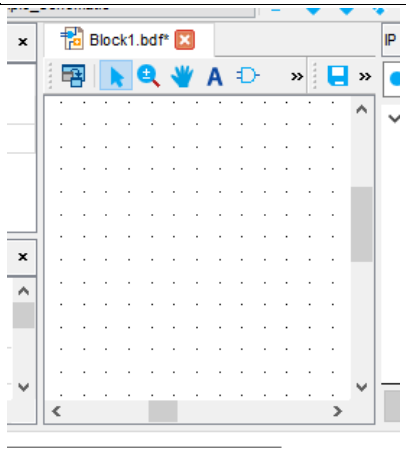


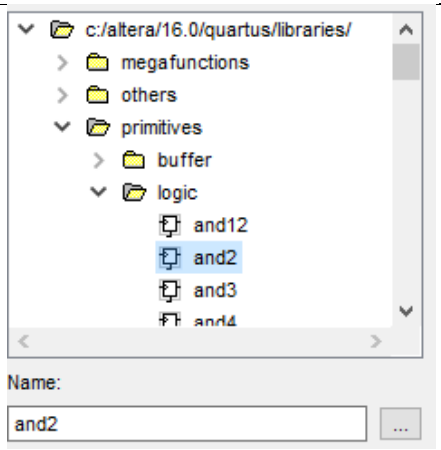
To import circuit elements, double-click on the blank space inside the Block Editor (left figure).

Find the **AND2**, **OR2**, **NOT** gates under directory: **primitives->logic** (right figure)

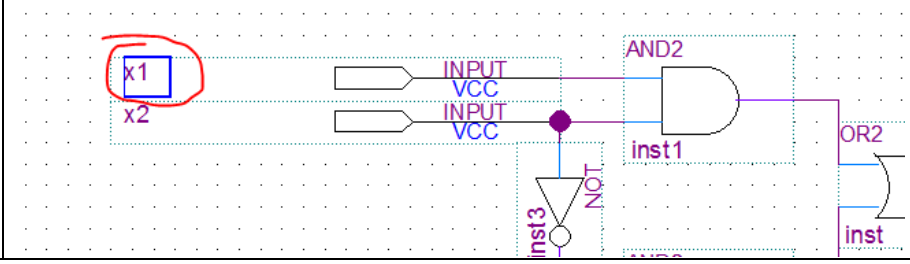
Find the **INPUT** and **OUTPUT** under directory: **primitives->pin**

Connect circuit elements: While the mouse is pointing at a pinstub, click and hold the mouse button. Then, drag the mouse to the next pinstub.



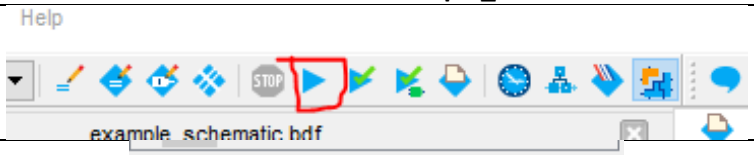


Double click the label to change the name of three INPUTs and one OUTPUT to x1, x2, x3 and f, respectively.

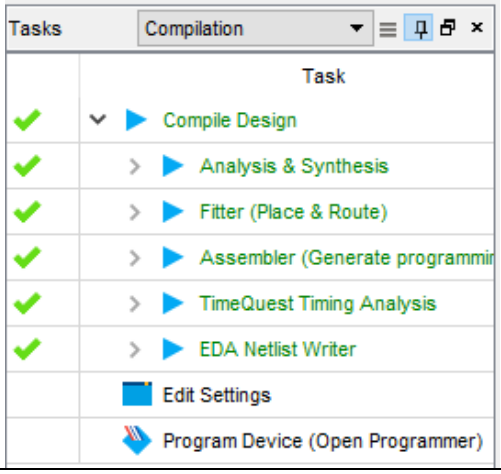


After you finish the schematic, save the file using: **File -> Save AS** and choose the name **example_schematic**

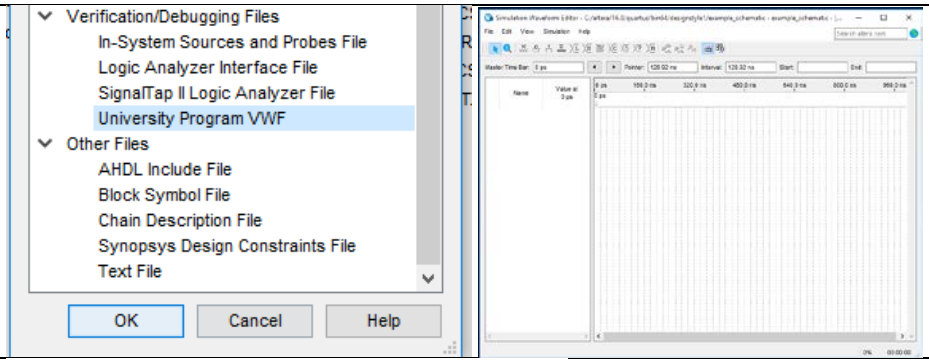
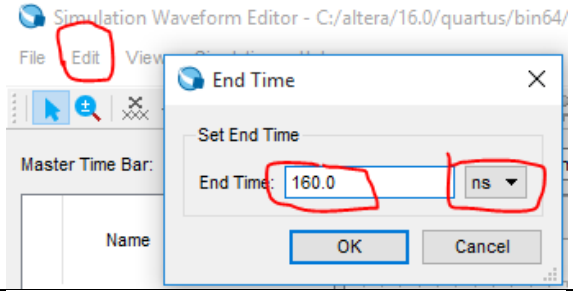
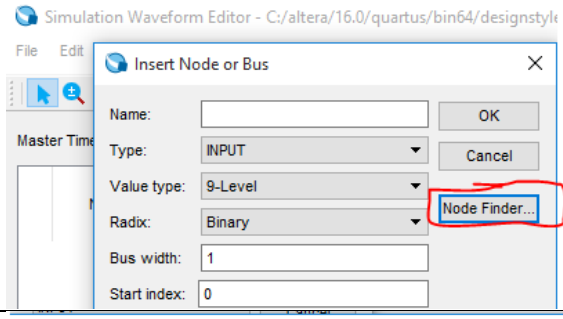
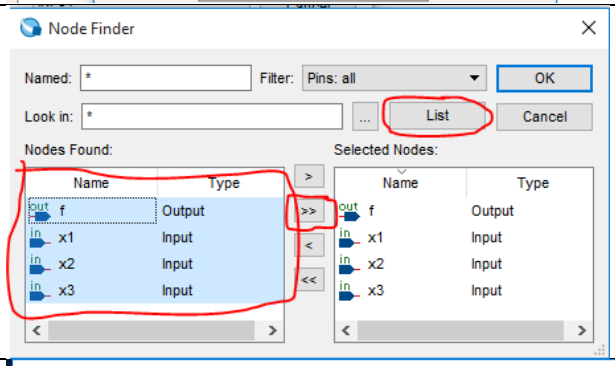
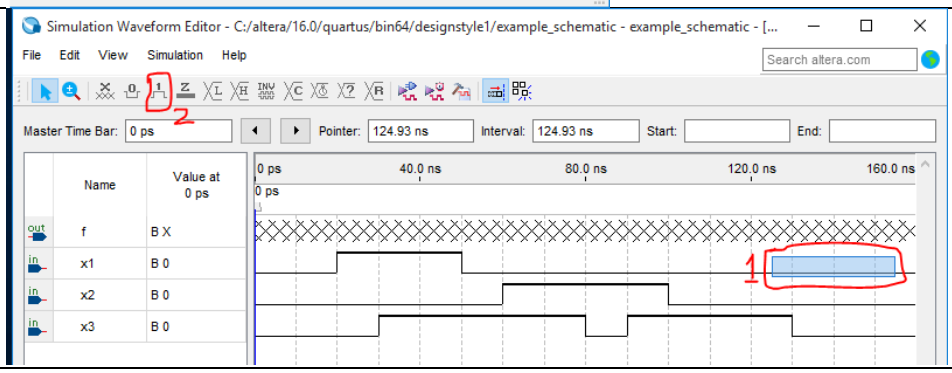
Compile your schematic by clicking the blue triangle button.



If your schematic is compiled successfully, you will see the figure shown at the left bottom window.

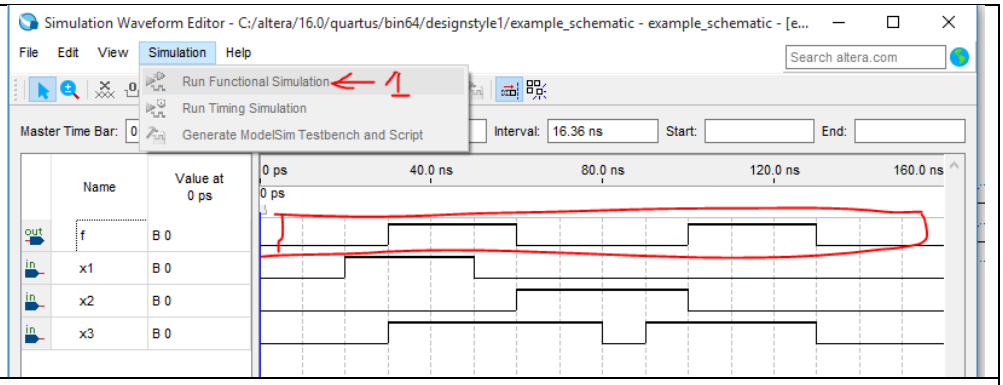


3. Once you compile your schematic successfully, you are going to simulate the circuit. To do so, you need to generate some waveforms as the inputs of your schematic.

File -> New Select: **University Program VWF** (Left figure) Press: **OK** You will get the **Simulation Waveform Editor** (Right figure)	
On the Simulation Waveform Editor: Set the simulation end time by: Edit -> Set End Time Set End Time to **160.0 ns** Press **OK**	
Edit -> Insert -> Insert Node or Bus Press **Node Finder**	
Press **List** button Select all the input and output Press **>>** button Press OK	
Please note the inputs of your schematic are x1, x2 and x3. Thus, select a time interval by hold and drag your mouse and click **Forcing High** button. Don't do anything on f, since it is an output. Randomly give some pulses on x1, x2 and x3 like shown in figure. Save your file: File -> Save	

To run the simulation:
Simulation -> Run Function Simulation

You will see the generated output f



You have got the step1 done. In step 1, you built a schematic (circuit) by the Block Editor.
The Block Editor is not the only way to build a schematic (circuit). In the step 2, you will use VHDL code to build a similar circuit.

Step2: Generate VHDL result:

Create a new project: File -> New Project Wizard

Directory, Name, Top-Level Entity Window:
Working directory: C:\altera\16.0\quartus\bin64\designstyle2
Name of this project: **example_vhdl**
Name of top-level design: **example_vhdl**

Family,Device & Board Setttings:
Available devices: 5CSEMA5F31C6

Finish

Create a new VHDL file:
File -> New -> VHDL File->Press OK

Input the VHDL code as shown in the left figure
Save the file with the name **example_vhdl**

Compile your code by clicking blue triangle button. (If there are some errors, check the message window at bottom and fix the typos)

```
1  Entity example_vhdl IS
2      PORT ( x1, x2, x3 : IN  BIT;
3             f          : OUT BIT);
4  END example_vhdl;
5
6  ARCHITECTURE Behavior OF example_vhdl IS
7  BEGIN
8      f <= (x1 AND x2) OR (NOT x2 and x3);
9  END Behavior;
```

Once you compile the code sucessfully, you have built an exactly same schematic (circuit) as step 1 via VHDL code.
Then, you should generate some waveforms to simulate your schematic. The procedure is identical with Step 1 -> Part 3.

After successfully simulate the circuit built by VHDL, you are required to build a schematic in a mixing way (Block Editor and VHDL).

Create a new project: File -> New Project Wizard

Directory, Name, Top-Level Entity Window:
Working directory: C:\altera\16.0\quartus\bin64\designstyle3
Name of this project: **example_mixed1**
Name of top-level design: **example_mixed1**

Family,Device & Board Setttings:
Available devices: 5CSEMA5F31C6
Press **Finish**

Create a new VHDL File
Input the VHDL code
Save the file with the name **vhdlfuntions**

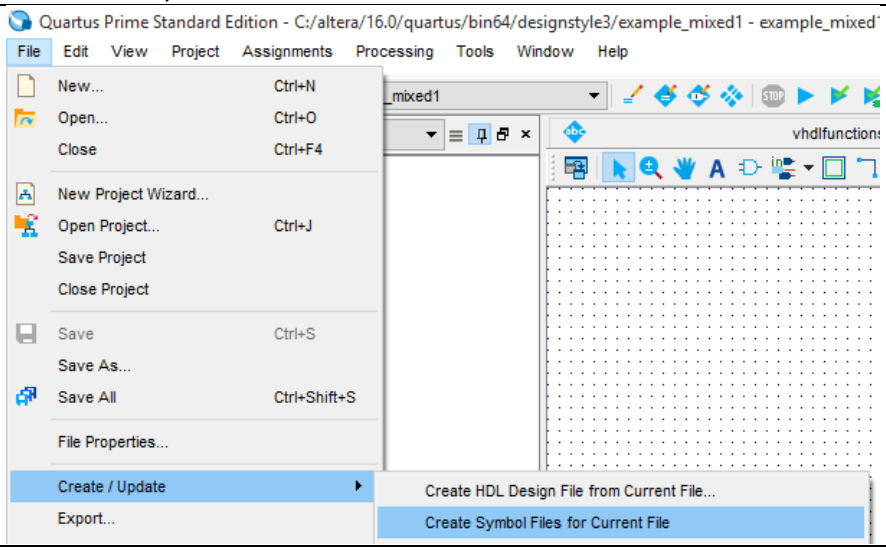
File -> Create/update -> Create Symbol Files for Current File

```
ENTITY vhdlfunctions IS
    PORT ( w1, w2, w3, w4   : IN    BIT ;
           g, h             : OUT   BIT ) ;
END vhdlfunctions ;

ARCHITECTURE LogicFunc OF vhdlfunctions IS
BEGIN
    g <= (w1 AND w2) OR (w3 AND w4);
    h <= (w1 AND w3) OR (w2 AND w4);
END LogicFunc ;
```

Open the saved **example_schematic.bdf** file in step 1: File -> Open; browse and open the **example_schematic.bdf** file.
The directory of this tutorial is: **C:/altera/16.0/quartus/bin64/designstyle1**
If you saved the file in other directory in step 1, just find and open it.

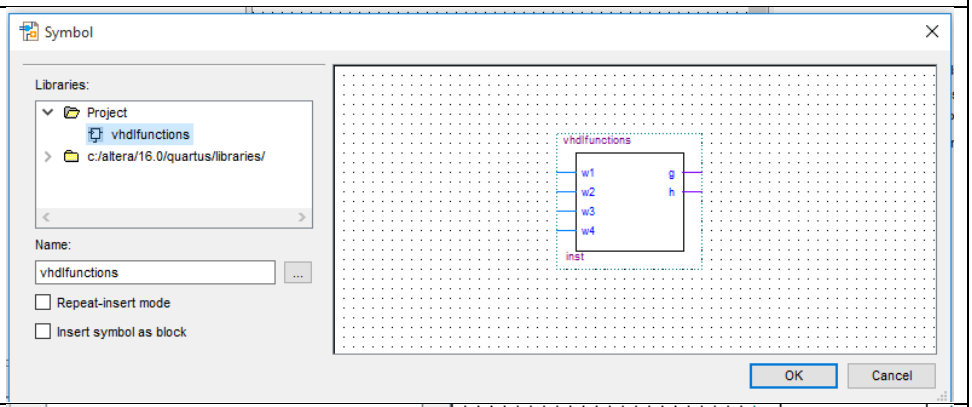
Leave the **example_schematic.bdf** file open.
File -> Create/Update -> Create Symbol File for Current File
Press save button, Quartus II will generate the file **example_schematic.bsf** in the "**C:/altera/16.0/quartus/bin64/designstyle1**" directory
Close the **example_schematic.bdf** file



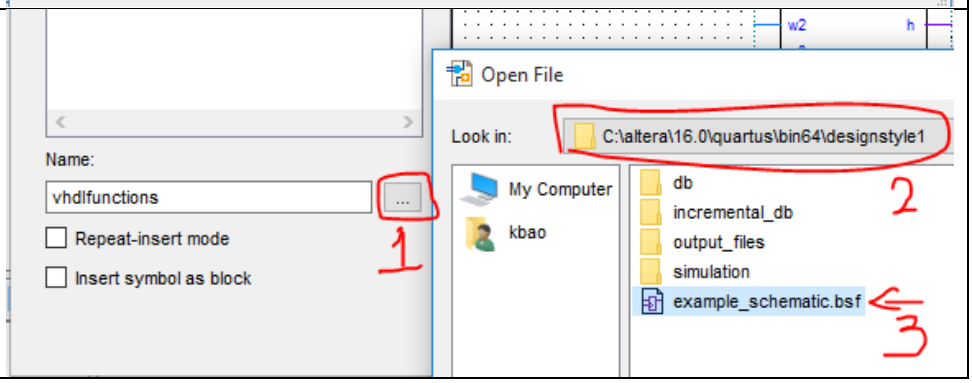
Create a top-level schematic: File -> New -> Block Diagram/Schematic File
Save the file in directory: (save as) C:\altera\16.0\quartus\bin64\designstyle3
Save the file with the name: **example_mixed1.bdf**

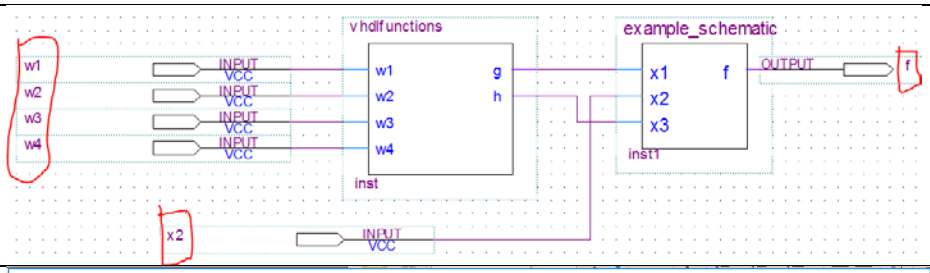
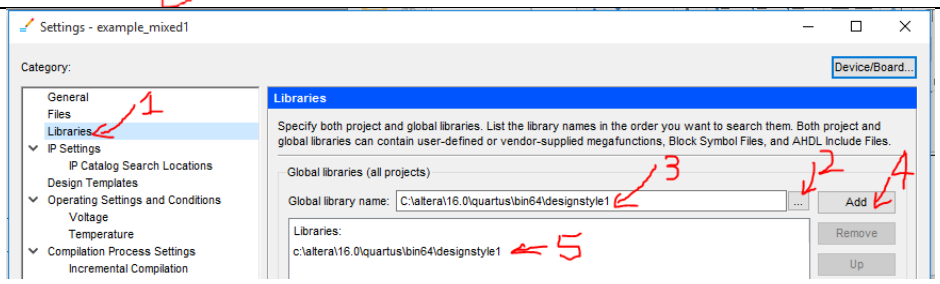
To import **vhdlfuntions,** double click the clock editor screen.

Select Project -> vhdlfunctions



To import **example_schematic,** double click the clock editor screen
Browse on the Name button
Find and open the **example_schematic.bsf** in the directory you saved before.



Import 5 INPUTs and 1 OUTPUTs. According to the left figure, rename them and connect all the elements together.	
Since the example_schematic.bdf file is not located in directory of the project, you need to tell Quartus II where to look for this file. Assignments -> Settings 1.Select Library 2. Browse Global Library name 3. Find the directory of **example_schematic.bdf** 4. Click **Add** 5. Press **Apply** and **OK** buttons	
Then, you should generate some waveforms to simulate your schematic. The procedure is identical with Step 1 -> Part 3.	