Lab 01: Quartus Prime Tutorial
ECE 380-002
University of Alabama

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Introduction

In this lab, I have got familiar with VHDL, a hardware description language, and Quartus Prime, CAD software. I have gone through three design methods in the CAD software, Quartus.

Procedure

a) Prelab

There was no prelab for this lab.

b) Setup and Data Collection

We followed the steps from the tutorial guide for the lab1.

Firstly, we create a new project named example_schematic. In the project, we create the Block Diagram File called example_schematic.bdf (Figure1). Then we

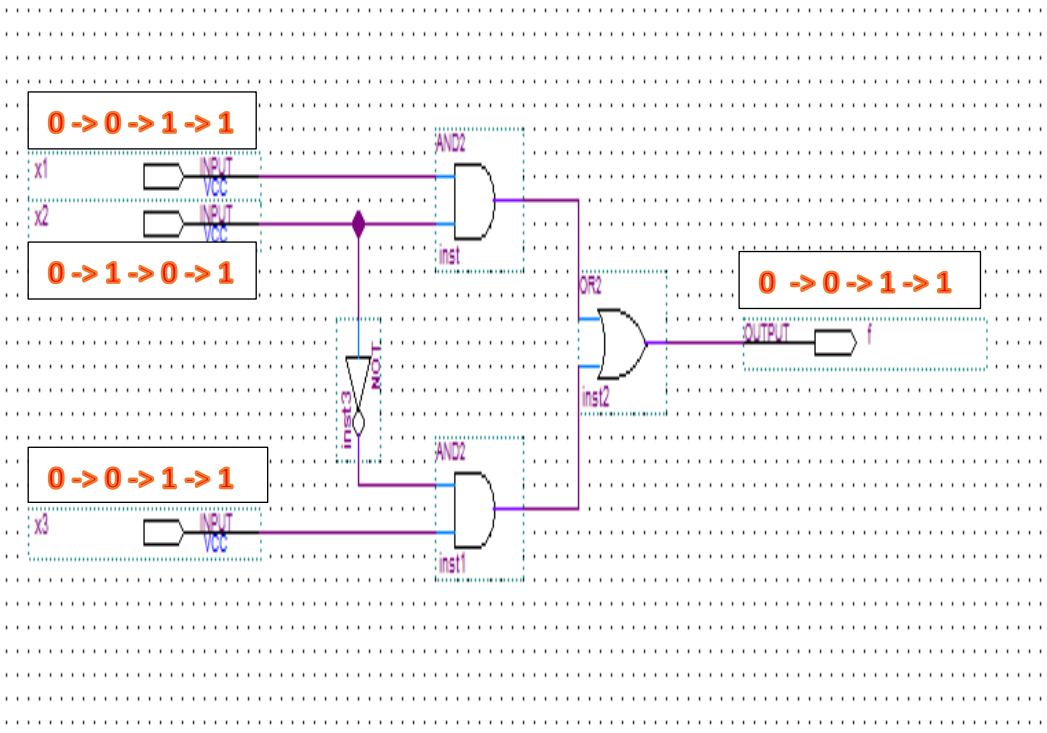


Figure 1 example_schematic.bdf

compile the project and run the stimulation by creating a VWF file called example_schematic.vwf. (Figure2)

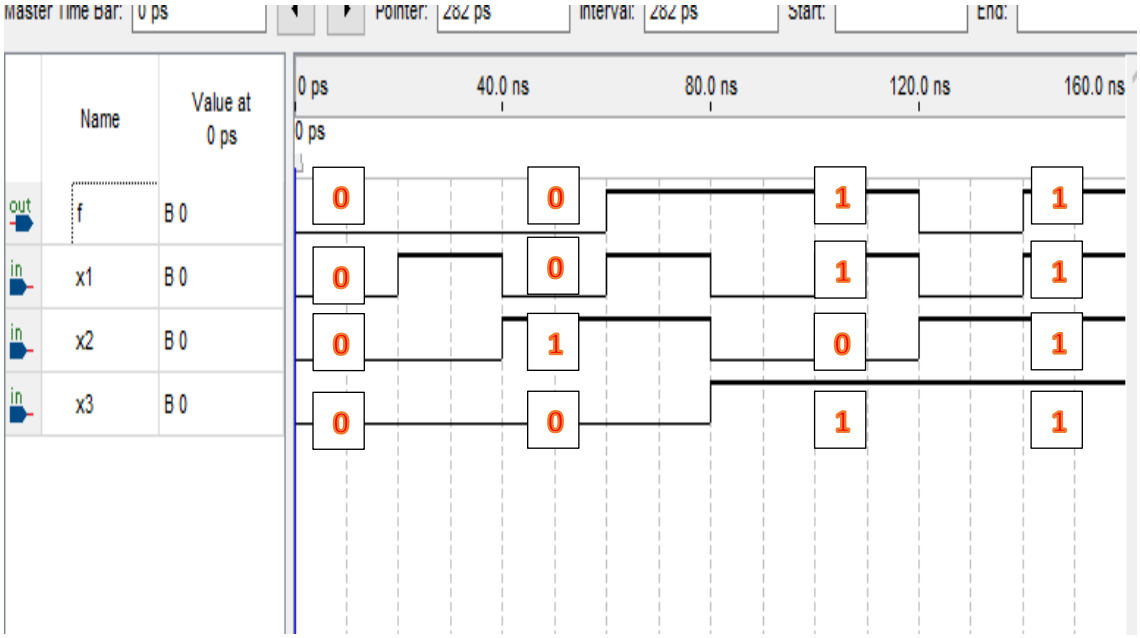


Figure 2 example_schematic.vwf

Secondly, we create the second project called example_vhdl. In this project, we create a VHDL file called example_vhdl.vhd. (Figure3) Then, we compile the file and run the stimulation step like the first project, the file name is example_vhdl.vwf. (Figure4)

```
1  Entity example_vdhl is
2     PORT ( x1, x2, x3 : IN  BIT;
3            f          : OUT BIT);
4  END example_vdhl;
5
6  ARCHITECTURE Behavior of example_vdhl is
7  BEGIN
8     f <= (x1 and x2) OR (not x2 and x3);
9  End Behavior;
```

Figure 3 example_vhdl.vhd

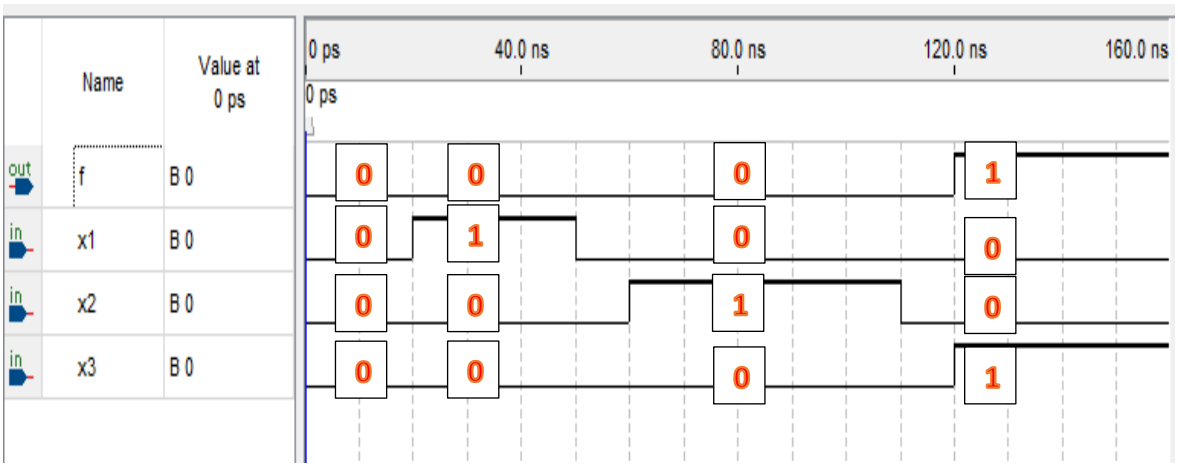


Figure 4 example_vhdl.vwf

Finally, we create the project named example_mixed1. In the project, we create a symbol called vhdlfunctions.bsf (Figure5) by coding a VHDL file called vhdlfunctions.vhd (Figure6). Then we create a block design file called

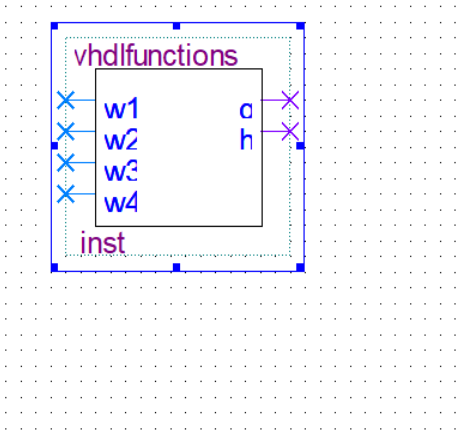


Figure 5 vhdlfunctions.bsf

```
ENTITY vhdlfunctions IS
    PORT (w1,w2,w3,w4 : IN BIT;
          g, h        : OUT BIT);
END vhdlfunctions;

ARCHITECTURE LogicFunc OF vhdlfunctions IS
BEGIN
    g<=(w1 AND w2)OR(w3 AND w4);
    h<=(w1 AND w3)OR(w2 AND w4);
END LogicFunc;
```

Figure 6 vhdlfunctions.vhd

example_mixed1.bdf (Figure7) and connect the circuits by the guide. After compiling, we create a file called example_mixed1.vwf (Figure8) to simulate the circuit.

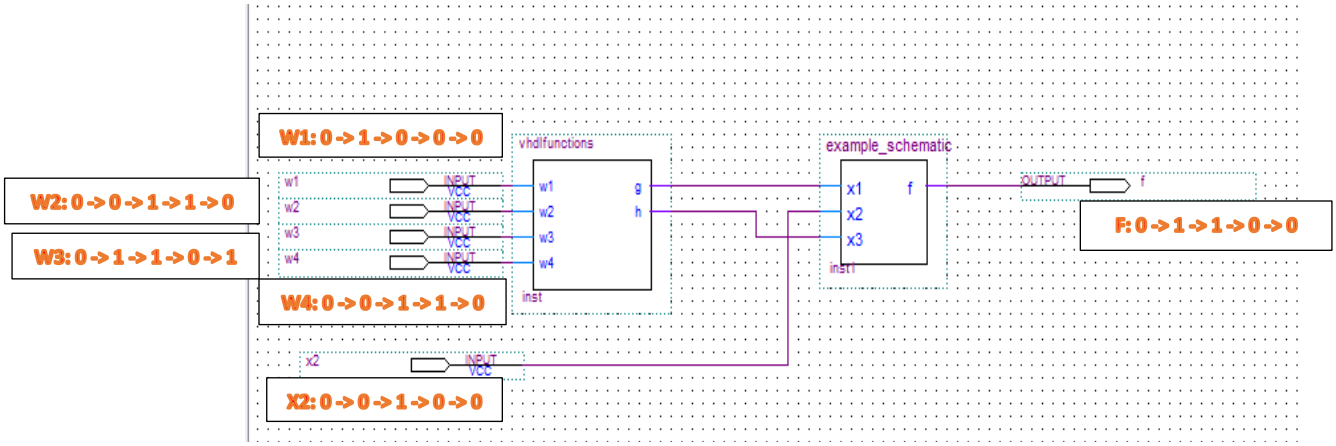


Figure 7 example_mixed1.bdf

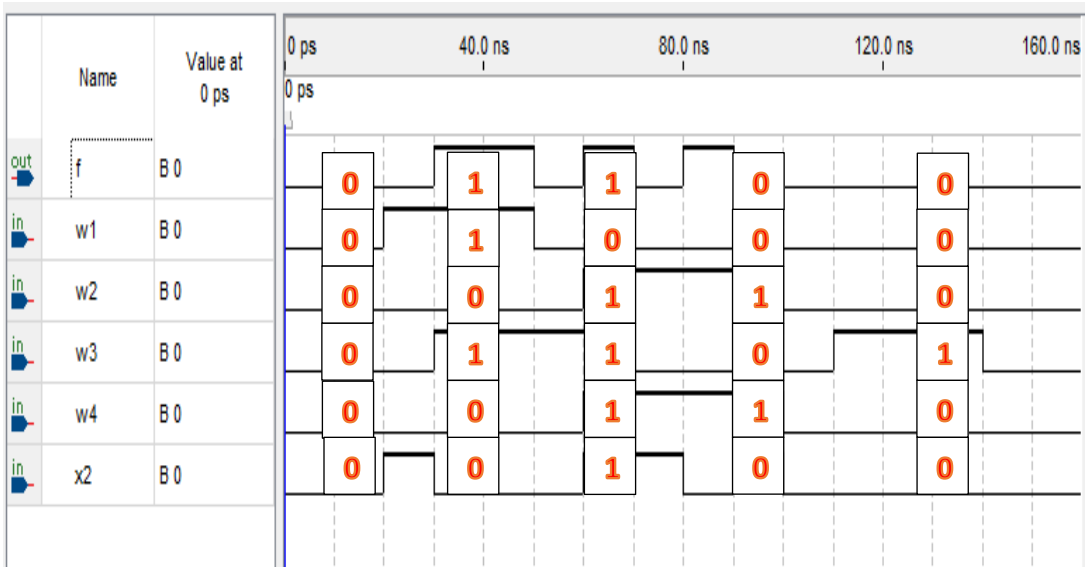


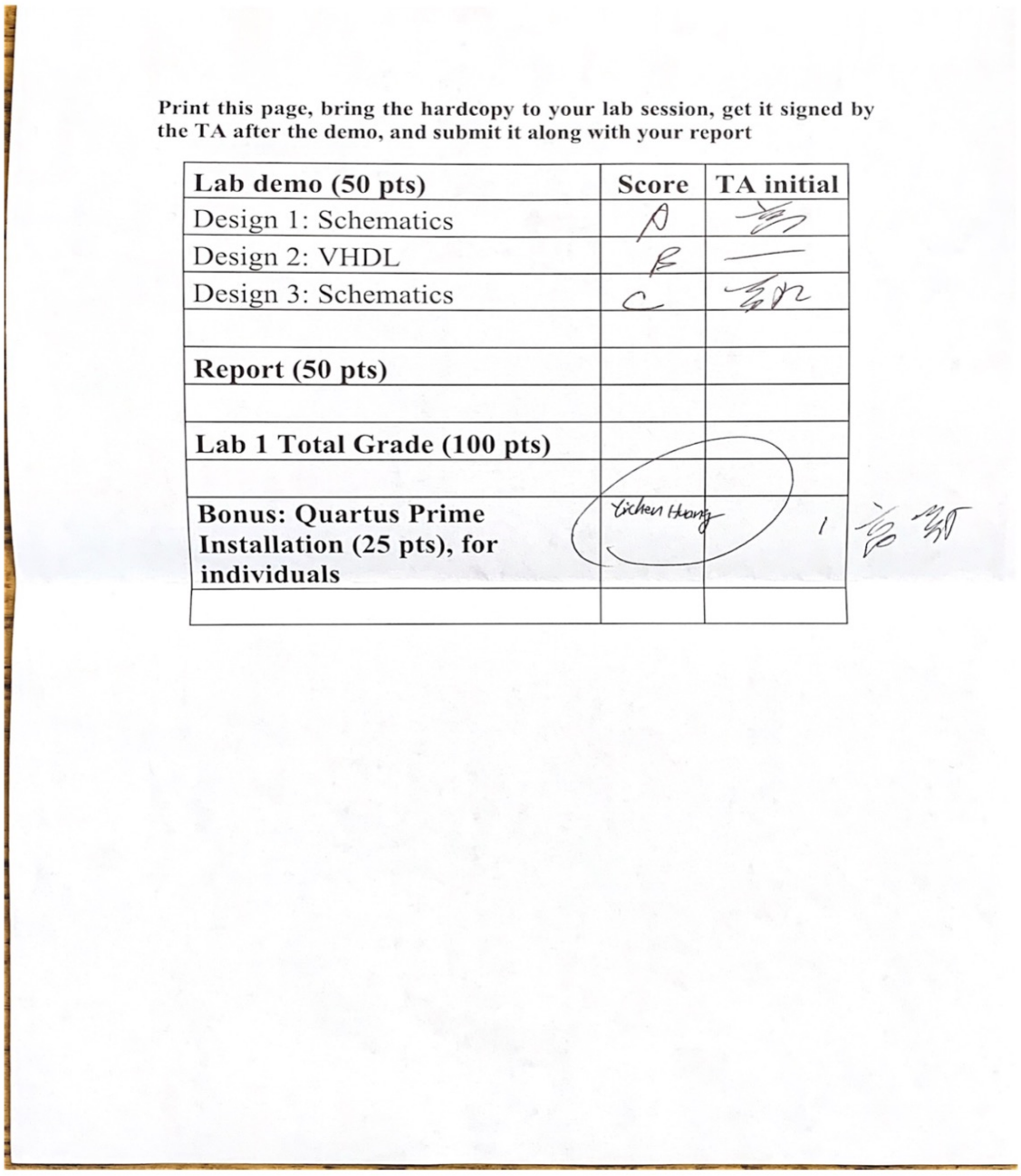
Figure 8 example_mixed1.vwf

Conclusion

During the lab time, we have learned that there are three ways to construct the circuit which are schematic, VHDL and mixed. In the lab, we also get familiar with the software.

Afterword

Attached is a copy of the sheet used to collect information during lab, which has the verification signature on it. (Figure 9)



Print this page, bring the hardcopy to your lab session, get it signed by the TA after the demo, and submit it along with your report

Lab demo (50 pts)	**Score**	**TA initial**
Design 1: Schematics	A	
Design 2: VHDL	B	—
Design 3: Schematics	C	
Report (50 pts)		
Lab 1 Total Grade (100 pts)		
Bonus: Quartus Prime Installation (25 pts), for individuals	Yichen Huang	1

Figure 9 Lab Sheet