ECE380: Pre-Lab #07: Multiplexers and Decoders

In this lab, you will use the Quartus II software package to design and test combinational circuit designs with multiplexers and decoders. You will learn standard IC chips 74151, an 8-to-1 multiplexer, and 74154, a 4-to-16 decoder and use them to implement logic functions. The requirements for this lab consist of completing Quartus II designs and printing any necessary schematic diagrams, performing functional simulations, testing the designs on DE1 board, and submitting a laboratory report.

Prelab tasks:

1. Review the multiplexers and decoders. Read carefully the IC specifications, sn54154.pdf and sn74151a.pdf distributed along with this document, for two standard chips 74154 and 74151. Write one short paragraph to describe a) input/output ports and b) functionality for each chip.

2. **Design A.** Implement the logic function $f(x, y, z) = \bar{x} \oplus z + y\bar{z} + \bar{x}y$ using a single 74151 multiplexer. Draw a schematic diagram as a schematic entry (.bdf file) in Quartus II.

Quartus II has a 74151 device available in the library. Click the "Symbol" icon, follow libraries->others--> maxplus2 to find 74151 in the list. The "Symbol" icon can be found at the top toolbox when you have a .bdf file open.

You can use GND and VCC to set inputs as "0" or "1", if necessary. In Quartus II, you can find them by clicking the "Symbol" icon, and following libraries --> primitives --> other: gnd and vcc. Or after the "Symbol" dialogue window opens, you can search in the Name box for all of three components.

After completing the design, you can compile the project and perform functional simulations. As the function only has three inputs, it is possible to test all the input valuations. You can specify these three inputs as clock signals with different periods to realize all input valuations, in functional simulations. Please refer to Lab 02 for detailed procedures.

3. **Design B.** Consider a circuit that has four inputs x_3, x_2, x_1, x_0. Let $N_1 = x_3x_2$ and $N_2 = x_1x_0$ represent two 2-digit unsigned binary numbers. Design a circuit using a 74154 decoder and two NAND gates that implements two logic functions f_1 and f_2. Function $f_1 = 1$ when two unsigned binary numbers satisfy the relationship $N_1 = N_2 + 1$ (+ represents the arithmetic addition). Otherwise, $f_1 = 0$. Function $f_2 = 1$ when $x_3x_2\ x_1x_0 = 1001$. Otherwise, $f_2 = 0$.

Draw the schematic diagram of the circuit as a schematic entry (.bdf file) in Quartus II.

Note that $N_1 = x_3x_2$ is the input pair of the binary number N_1. It is not the logical AND function of $x_3 \cdot x_2$. Design B acts as a comparator for matching inputs between N_1 and N_2. The output f_1 is high when $N_1 = N_2 + 1$.

Quartus II has a 74154 device available in the library. Click the "Symbol" icon, follow libraries->others--> maxplus2 to find 74154 in the list. You can use GND and VCC to set inputs as "0" or "1", if necessary.

After completing the design, you can compile the project and perform functional simulations. As the function only has four inputs, it is possible to test all the input valuations. You can specify these inputs as clock signals with different periods to realize all input valuations, in functional simulations. Please refer to Lab 02 for detailed procedures.

Prelab requirements:

At the beginning of your lab session, you need to present to the TA

- **Two short paragraphs to describe the standard chips, 74151 and 74154.**
- **Design A and Design B in the forms of Quartus II schematic entries.**

Pre-Lab (30%)	**Score**	**TA initial**
20% Designs		
10% Paragraphs		
Report (70%)		
10% Introduction		
10% Procedures		
20% Results		
30% Conclusions		
Lab Grade (100%)		