ECE 380: Lab 01: Quartus Prime Tutorial

In this lab, students get familiar with VHDL, a hardware description language, and Quartus Prime, CAD software. Students will go through three design methods in the CAD software, Quartus, by following a provided tutorial in this lab.

Quartus Prime contains powerful tools for hardware design and implementation. When progressing through the curriculum, the students will use VHDL and Quartus often. So, this is prerequisite material that students are expected to master.

Lab procedures

Step 1: Learn via Quartus Prime Tutorial
Please read *Tutorial 1 —Using Quartus II CAD Software* (in lab01_quartus_tutorial.pdf). This tutorial from the textbook deals with Quartus II (v 7.0).

Important: You will use Quartus Prime (v 16.0) throughout this semester. Therefore, you need to follow an updated guide, lab1_tutorial_guide.pdf for the interface operation in Quartus Prime (v 16.0).

Introduction to Simulation of VHDL Designs (supplement_quartusii_simulation_vhdl.pdf, in the same folder with this document) will also be helpful.

The major differences are listed as below:

- **Family and Device Settings.** You can choose *Cyclone V(E/GX/GT/SX/SE/ST)* when creating a new project. From the list of available devices, choose the device called *5CSEMA5F31C6*.
- **Using the Compiler.** Click *Processing> Start Compilation* (There is also a toolbar icon for this command, which looks like a purple triangle), instead of *Processing >Compiler Tool* or *Processing > Start > Start Analysis & Synthesis*.
- **Using the Waveform Editor.** Click *File>New>University Program VWF* (If you do not see this option, **University Program** needs to be installed), instead of File> *New >Other files>Vector Waveform File*.
- **Performing the Simulation.** Click *Simulation>Run Functional Simulation* instead of the two steps: *Assignments > Settings* and *Processing > Generate Functional Simulation Netlist*.

Before your lab session with the TA, you need to read *Tutorial 1 – Using Quartus II CAD Software* carefully and go through the tutorial procedures B.1 to B.5.

Step 2: Generate VHDL results:
During your lab session, please demonstrate the procedures of the following three design examples in lab01_quartus_tutorial.pdf to the TA:

- B.3 Design Entry Using Schematic Capture (tutorial1\designstyle1)
- B.4 Design Entry Using VHDL (tutorial1\designstyle2)

- B.5.1 Using Schematic Entry at the Top Level (tutorial1\designstyle3)

Some advice for successful compilation and simulations:

- To start a new design, you should create a new project rather than a new file.
- You need to copy the VHDL codes in their exact forms.
- Entity in your highest level VHDL code should match with your project entity name.

Note: you need to get TA's signature after your successful demo.

Step 3: Lab Report

Please assemble all of the above results into a lab report. A sample report format is attached (supplement_sample_lab_report.pdf). Please submit the report to the TA in the beginning of next lab session (Lab 2).

Include the following items in your lab report:

- Tutorial1\designstyle1: Block design file (*.bdf) of the schematic (example_schematic.bdf)
- Tutorial1\designstyle1: Simulation vector waveform file (.vwf) after the functional simulation of the schematic (example_schematic.vwf)
- Tutorial1\designstyle2: VHDL source file (*.vhd) (example_vhdl.vhd)
- Tutorial1\designstyle2: Simulation vector waveform file (.vwf) after the functional simulation of the VHDL source code (example_vhdl.vwf)
- Tutorial1\designstyle3: VHDL source file (.vhd) (vhdlfunctions.vhd)
- Tutorial1\designstyle3: Block design file (*.bdf) of the schematic (example_mixed1.bdf)
- Tutorial1\designstyle3: Simulation vector waveform file (.vwf) after the functional simulation of the mixed schematic (example_mixed1.vwf)
- Tutorial1\designstyle3: Block symbol file, vhdlfunctions.bsf, generated by Quartus for the sub-circuit represented by vhdlfunctions.vhd

Grades for Lab #1 will be determined according to the following:

Demo (with TA's signature): 50 pts
Report: 50 pts
Total points for Lab #1 = 100 points

Note: The report should at least include the following items:

- (4 pts) example_schematic.bdf
- (4 pts) example_schematic.vwf
- (4 pts) example_vhdl.vhd
- (4 pts) example_vhdl.vwf
- (3 pts) vhdlfunctions.vhd
- (4 pts) example_mixed1.bdf

- (4 pts) example_mixed1.vwf
- (3 pts) vhdlfunctions.bsf

Bonus 25 points: Installation of Quartus Prime

Please download and install "Quartus Prime Lite Edition" through:
http://dl.altera.com/?edition=web

Select "*Release: 16.0*", and "*Combined Files*". This is the same version as the one in the lab. The CD in your textbook is outdated. Please do not use it.

Decompress the downloaded file and install Quartus Prime. You can use free software 7-zip, http://www.7-zip.org/, to decompress the file.

Note that Quartus Prime only supports 64 bit machines.

If you use Mac laptops, you can create a dual boot, where you can establish a Windows operating system. The other option for Apple users is to install in a virtual machine environment. The latter option is slow, as multiple students reported.

Bring your laptop to the lab session and show your installation to the TA. You will get extra 25 points. Each member gets his/her own bonus points for the installation.

Additional materials:

You can also read:

- http://www.altera.com/literature/lit-qts.jsp for Quartus II development software documentation,
- http://esd.cs.ucr.edu/labs/tutorial/ for VHDL basics, and
- *Introduction to Simulation of VHDL Designs*, as attached supplement_quartusii_simulation_vhdl.pdf.
- *Quartus II V15.0 introduction for VHDL users*, as attached supplement_quartusii_v15_intro_vhdl.pdf.

Print this page, bring the hardcopy to your lab session, get it signed by the TA after the demo, and submit it along with your report

Lab demo (50 pts)	**Score**	**TA initial**
Design 1: Schematics		
Design 2: VHDL		
Design 3: Schematics		
Report (50 pts)		
Lab 1 Total Grade (100 pts)		
Bonus: Quartus Prime Installation (25 pts), for individuals		