Lab 04
Multifunctional Logic Circuit

ECE 380-002
University of Alabama

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2019/09/23

Introduction

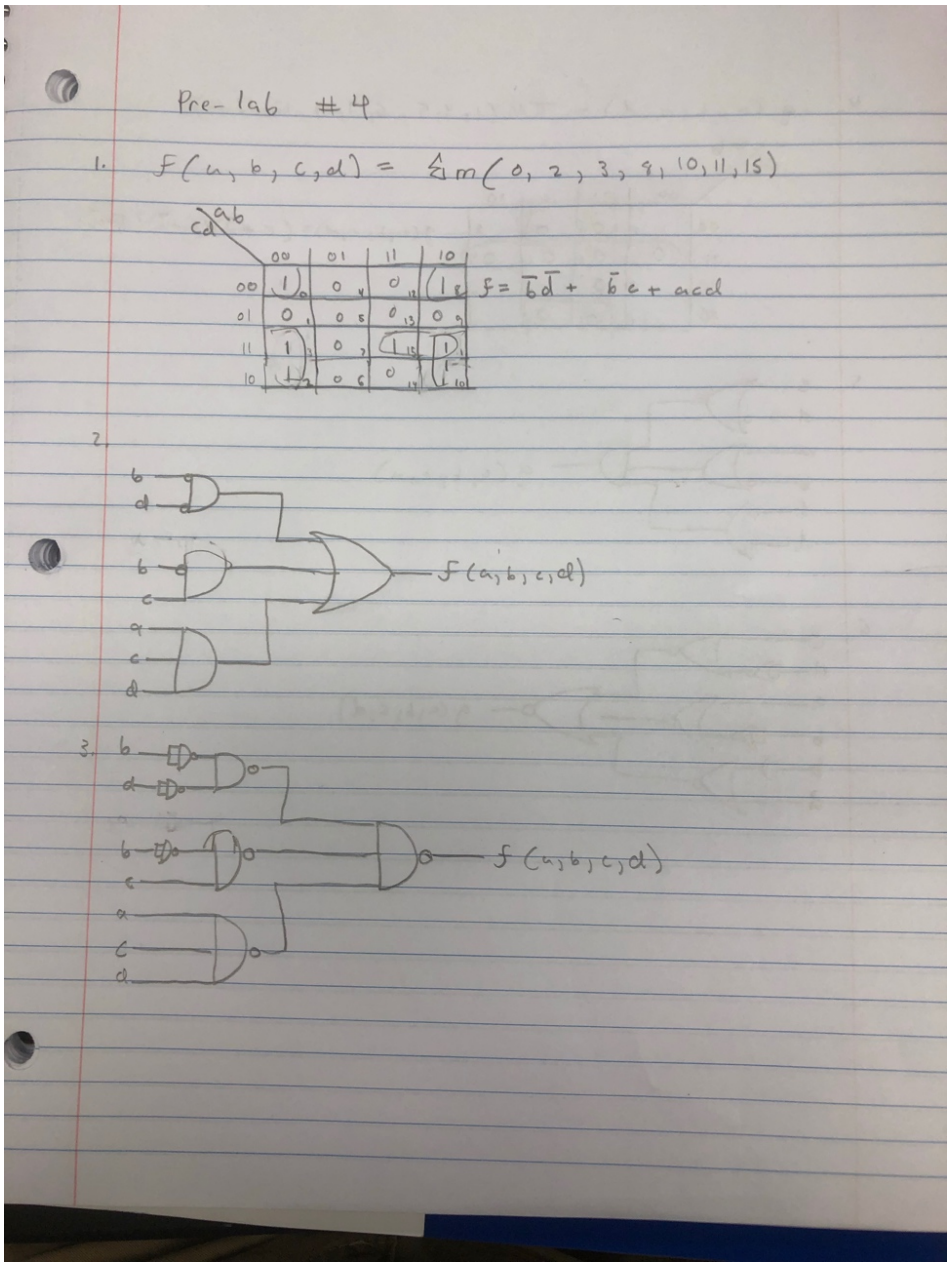
In this lab, we use the Quartus II environment to download designs to programmable devices on the Altera DE1 board. You create several simple designs, using VHDL and schematic entry, which will be downloaded to the Altera DE1 board.

Procedure

a) Prelab

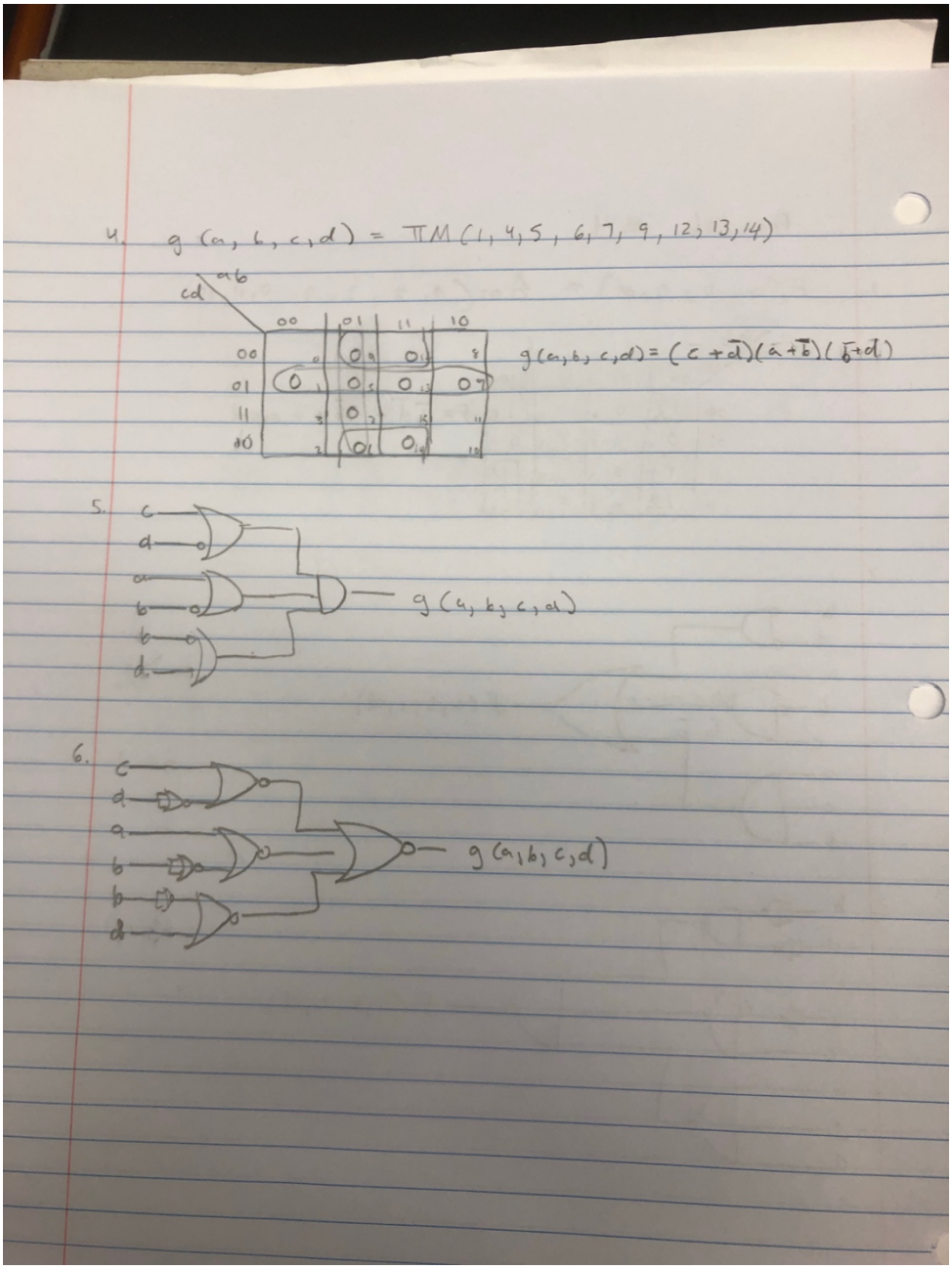
i. SOP Form

In the SOP form, we analyze the problem and create a k-map by the Min-Term method. After we create the k-map, we get an optimized function. Then, we can draw two schematic circuit that first one use AND, NOT, OR Gates and the second one is NAND-Only gate.



ii. POS Form

In the POS form, we draw anther k-map and by Max-Term method. We optimize the function. We also draw two schematic diagram the first one using AND, NOT and OR gates; another is using NOR-only gate.

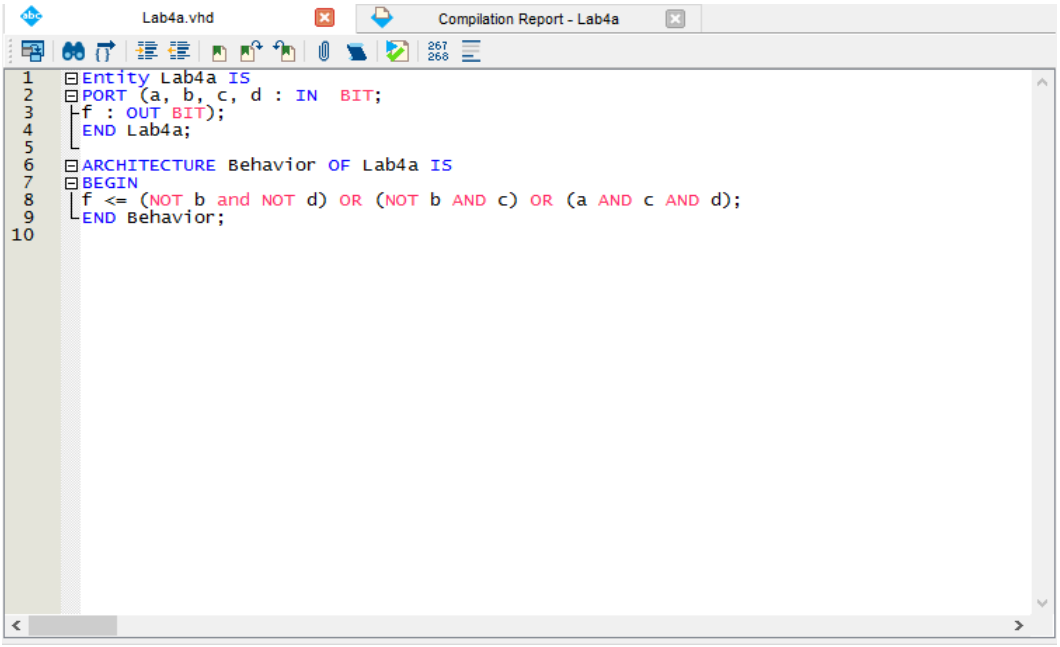


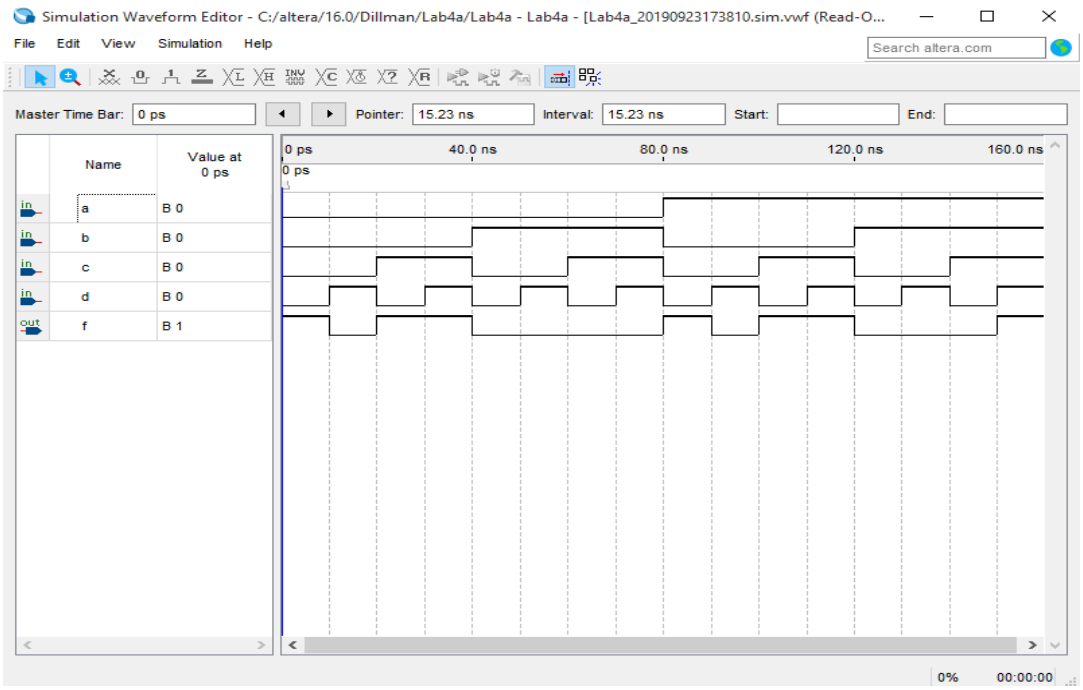
b) During the lab

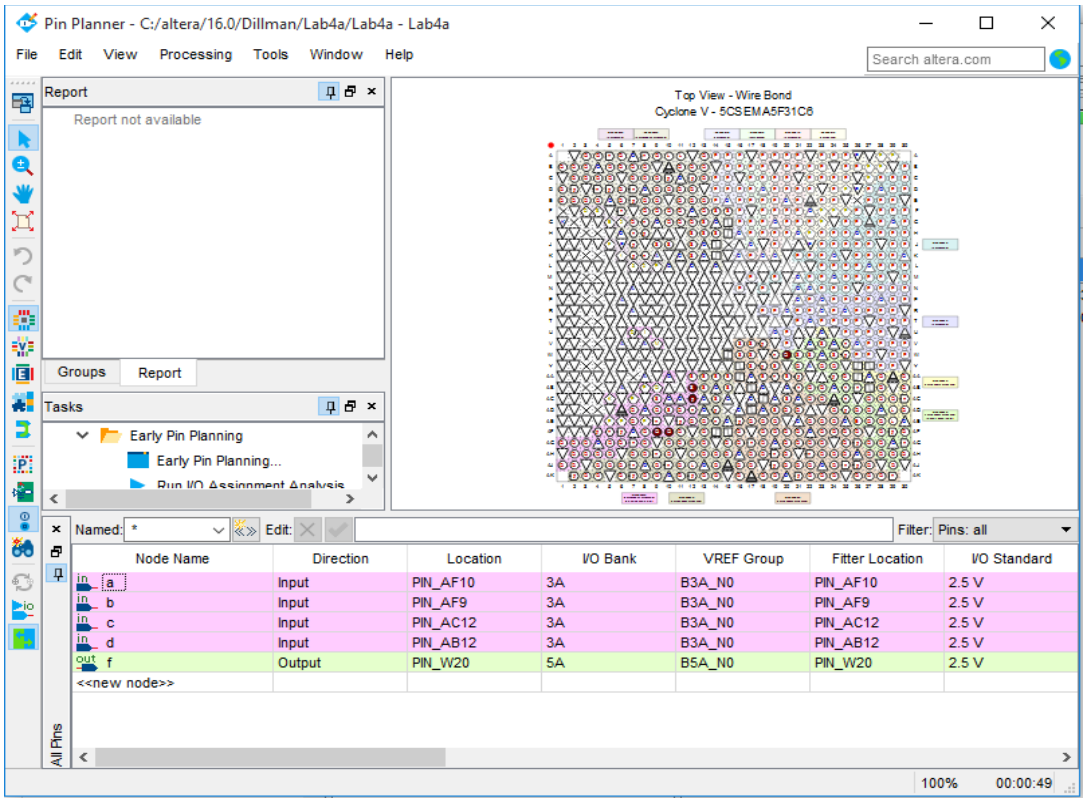
   a. SOP form

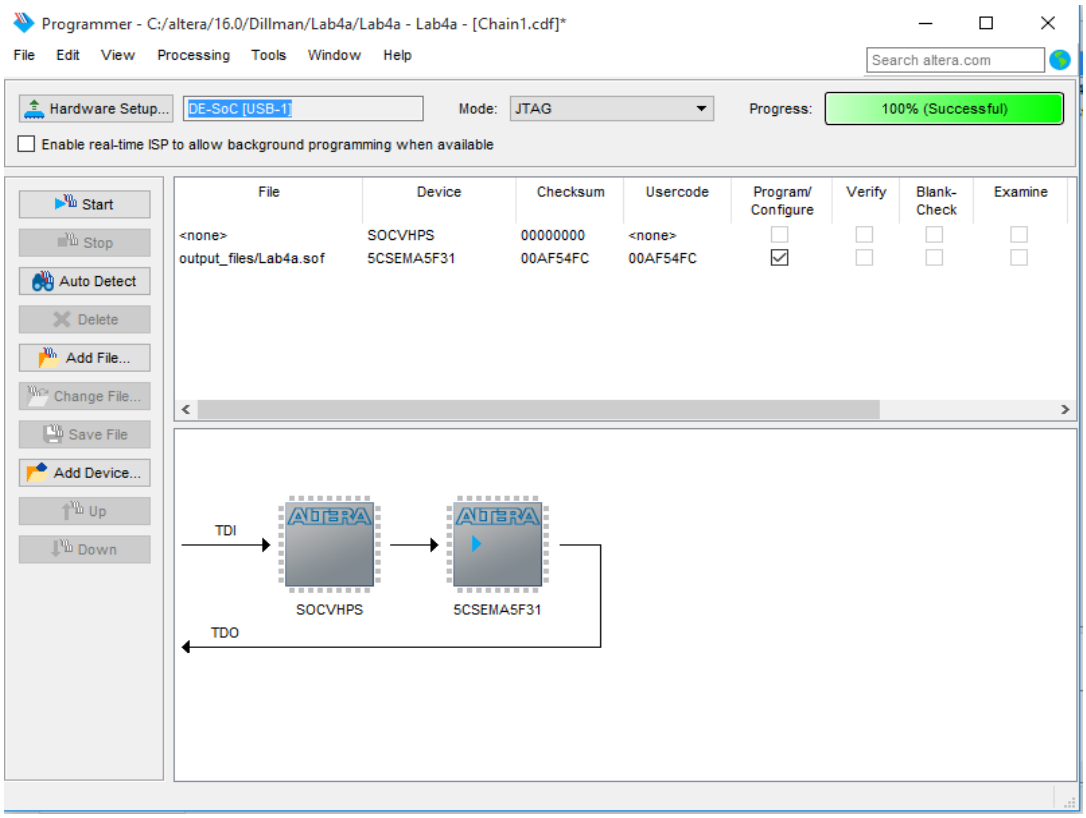
      i. VHDL

Firstly, we write a VHDL file based on the first part of the prelab. The VHDL file describe the function by using AND, OR and Not syntax. After compiling the file, we run a test and set up the switches of the board. Then import the file into the board. We also test the function again through the board.



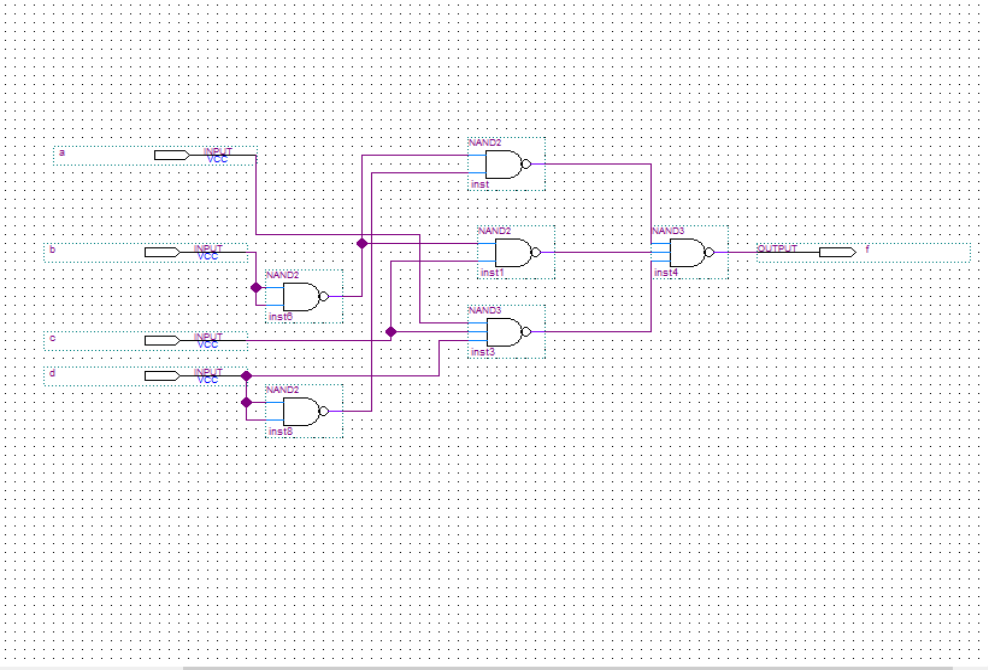


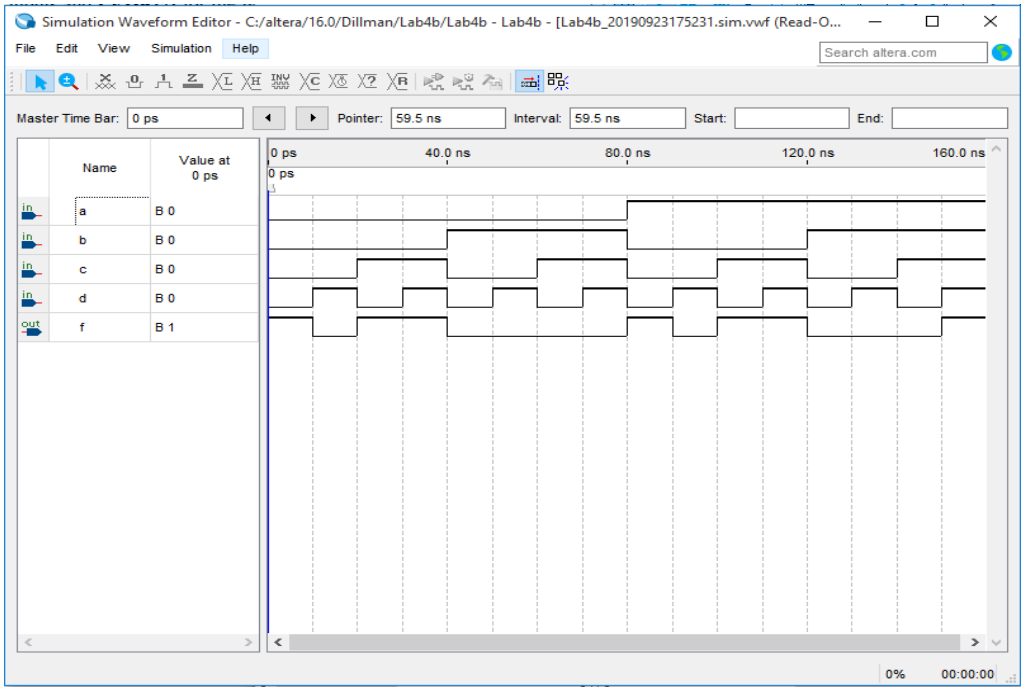

Pin Planner - C:/altera/16.0/Dillman/Lab4a/Lab4a - Lab4a
File Edit View Processing Tools Window Help
Search altera.com
Report
Report not available
Groups Report
Tasks
Early Pin Planning
Early Pin Planning...
Top View - Wire Bond
Cyclone V - 5CSEMA5F31C6
Named: * Edit: Filter: Pins: all
Node Name Direction Location I/O Bank VREF Group Fitter Location I/O Standard
a Input PIN_AF10 3A B3A_N0 PIN_AF10 2.5 V
b Input PIN_AF9 3A B3A_N0 PIN_AF9 2.5 V
c Input PIN_AC12 3A B3A_N0 PIN_AC12 2.5 V
d Input PIN_AB12 3A B3A_N0 PIN_AB12 2.5 V
f Output PIN_W20 5A B5A_N0 PIN_W20 2.5 V
<<new node>>
All Pins
100% 00:00:49

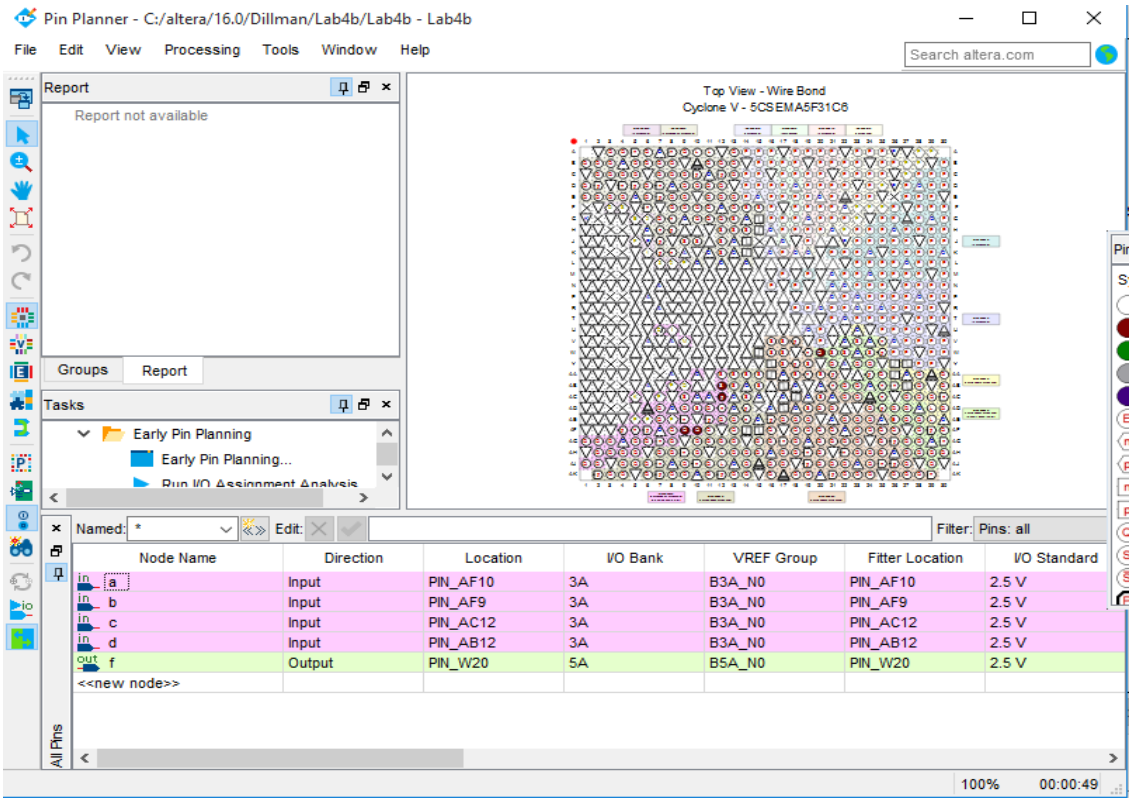

Programmer - C:/altera/16.0/Dillman/Lab4a/Lab4a - Lab4a - [Chain1.cdf]*
File Edit View Processing Tools Window Help
Search altera.com
Hardware Setup... DE-SoC [USB-1] Mode: JTAG Progress: 100% (Successful)
Enable real-time ISP to allow background programming when available
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File Device Checksum Usercode Program/ Configure Verify Blank-Check Examine
<none> SOCVHPS 00000000 <none>
output_files/Lab4a.sof 5CSEMA5F31 00AF54FC 00AF54FC
TDI
SOCVHPS
5CSEMA5F31
TDO

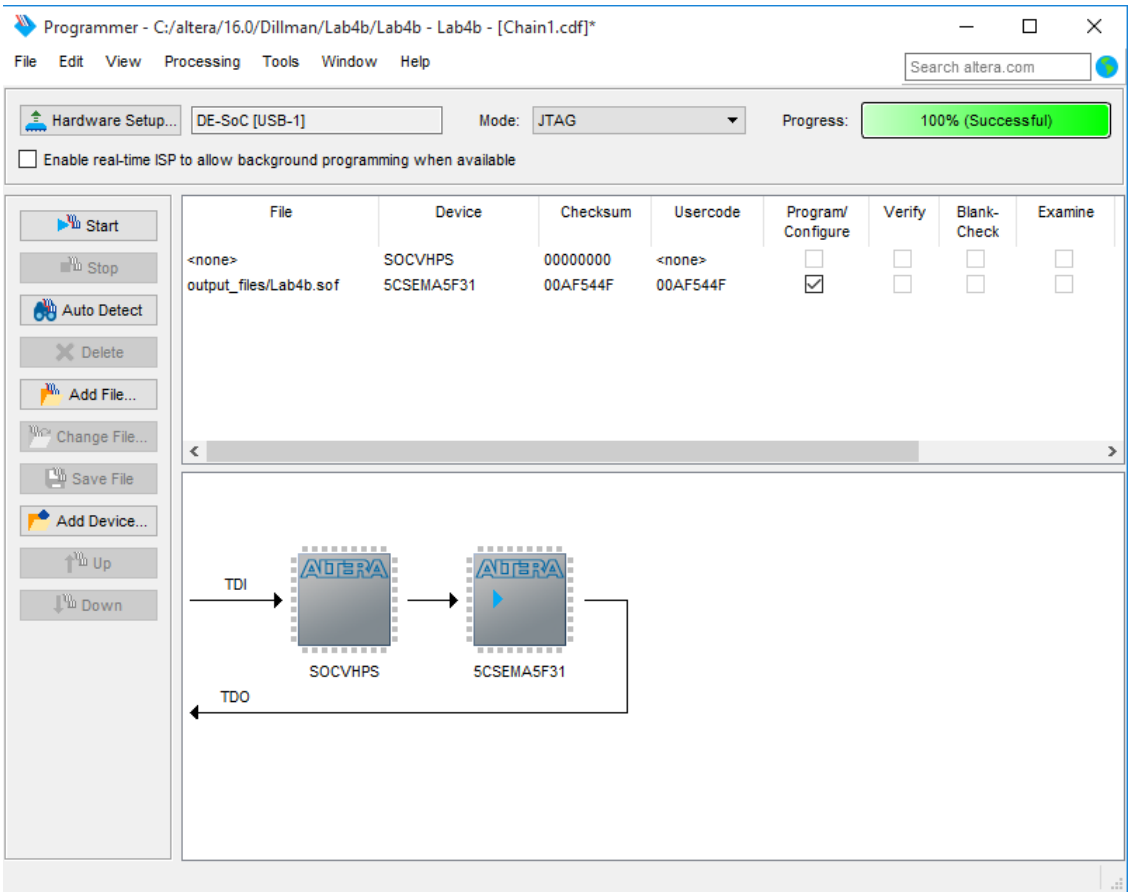
ii. Schematic

We created a body diagram file to draw the NAND-ONLY schematic diagram in the prelab. Then we compiled and test the file and set up switches of the board. After setting, we upload the file to the board and test the board and get the same result of the file.






Pin Planner - C:/altera/16.0/Dillman/Lab4b/Lab4b - Lab4b
File Edit View Processing Tools Window Help
Search altera.com
Report
Report not available
Groups Report
Tasks
Early Pin Planning
Early Pin Planning...
Top View - Wire Bond
Cyclone V - 5CSEMA5F31C6
Named: *
Edit:
Filter: Pins: all
Node Name | Direction | Location | I/O Bank | VREF Group | Fitter Location | I/O Standard
a | Input | PIN_AF10 | 3A | B3A_N0 | PIN_AF10 | 2.5 V
b | Input | PIN_AF9 | 3A | B3A_N0 | PIN_AF9 | 2.5 V
c | Input | PIN_AC12 | 3A | B3A_N0 | PIN_AC12 | 2.5 V
d | Input | PIN_AB12 | 3A | B3A_N0 | PIN_AB12 | 2.5 V
f | Output | PIN_W20 | 5A | B5A_N0 | PIN_W20 | 2.5 V
<<new node>>
All Pins
100% 00:00:49

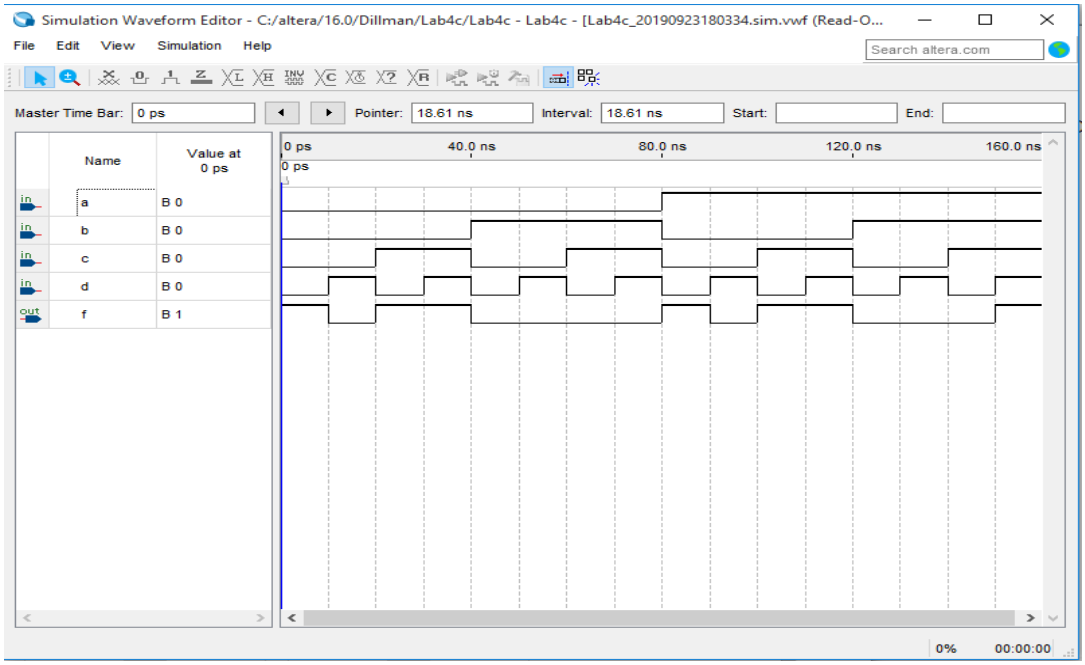

Programmer - C:/altera/16.0/Dillman/Lab4b/Lab4b - Lab4b - [Chain1.cdf]*
File Edit View Processing Tools Window Help
Search altera.com
Hardware Setup... DE-SoC [USB-1] Mode: JTAG Progress: 100% (Successful)
Enable real-time ISP to allow background programming when available
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File | Device | Checksum | Usercode | Program/ Configure | Verify | Blank-Check | Examine
<none> | SOCVHPS | 00000000 | <none>
output_files/Lab4b.sof | 5CSEMA5F31 | 00AF544F | 00AF544F
TDI
SOCVHPS
5CSEMA5F31
TDO

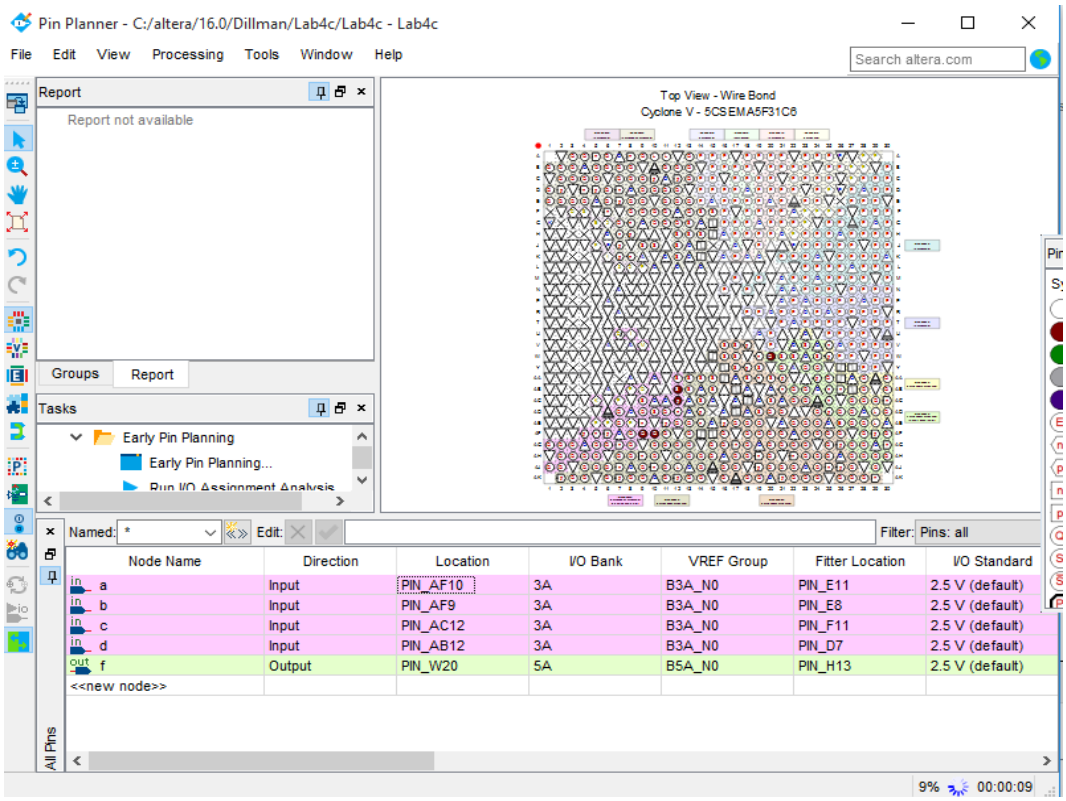
b. POS form

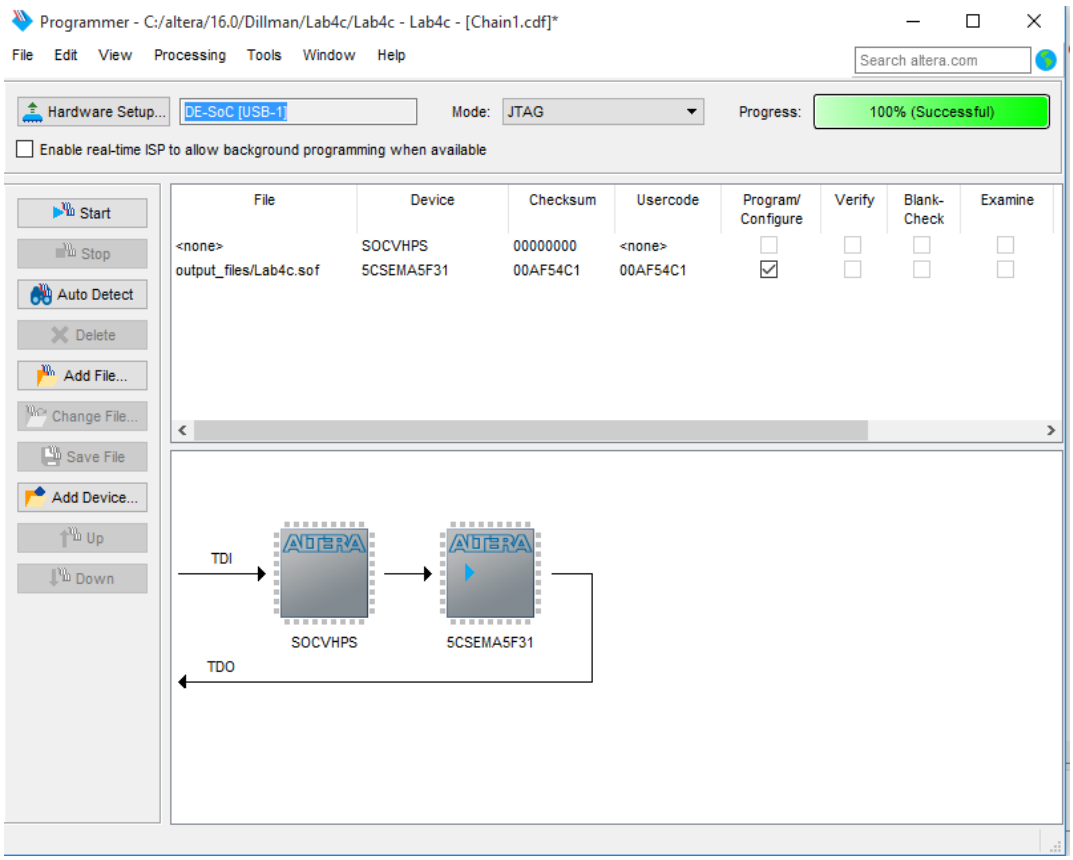
i. VHDL

we write a VHDL file based on the second part of the prelab. The VHDL file describe the function by using AND, OR and Not gate. After compiling the file, we run a test and set up the switches of the board. Then import the file into the board. We also test the function again through the board.

```
1  Entity Lab4c IS
2  PORT (a, b, c, d : IN  BIT;
3        f          : OUT BIT);
4  END Lab4c;
5
6  ARCHITECTURE Behavior OF Lab4c IS
7  BEGIN
8   f <= (c OR NOT d) AND (a OR NOT b) AND (NOT b OR d);
9   END Behavior;
```

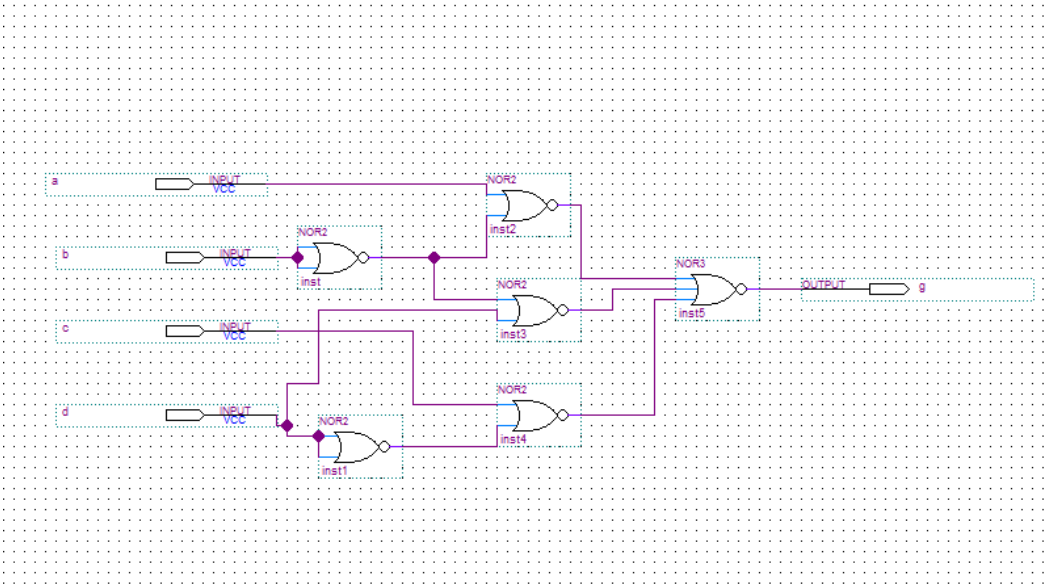


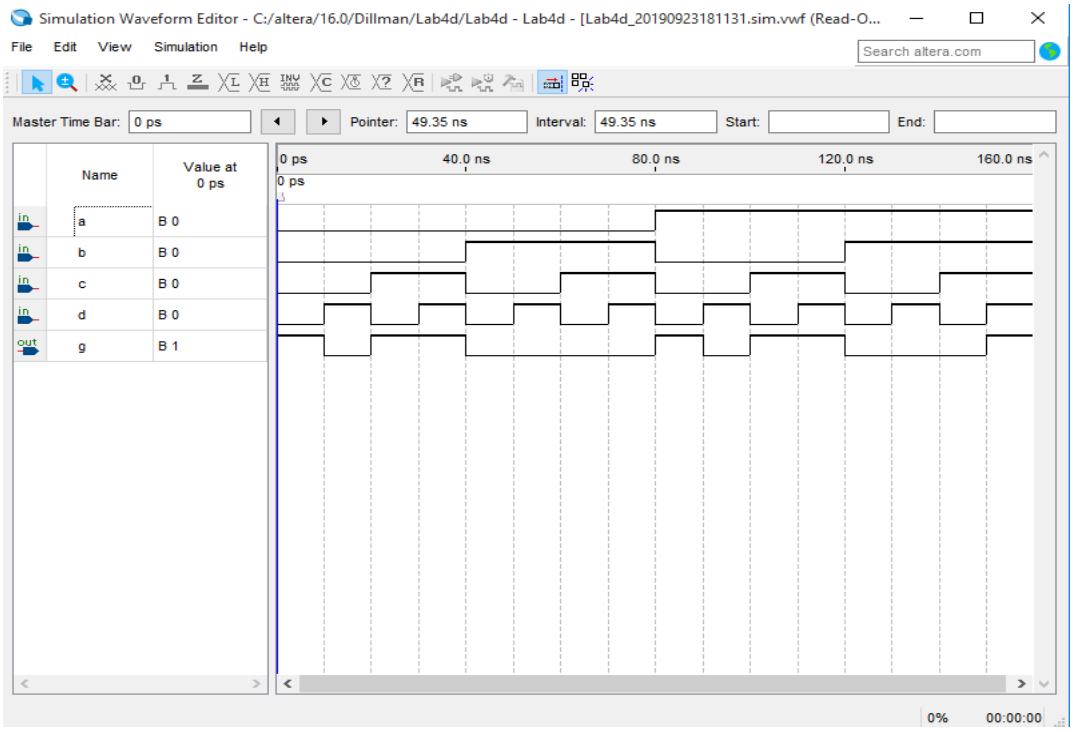

Pin Planner - C:/altera/16.0/Dillman/Lab4c/Lab4c - Lab4c
File Edit View Processing Tools Window Help
Search altera.com
Report
Report not available
Groups Report
Tasks
Early Pin Planning
Early Pin Planning...
Top View - Wire Bond
Cyclone V - 5CSEMA5F31C6
Named: * Edit: Filter: Pins: all
Node Name | Direction | Location | I/O Bank | VREF Group | Fitter Location | I/O Standard
a | Input | PIN_AF10 | 3A | B3A_N0 | PIN_E11 | 2.5 V (default)
b | Input | PIN_AF9 | 3A | B3A_N0 | PIN_E8 | 2.5 V (default)
c | Input | PIN_AC12 | 3A | B3A_N0 | PIN_F11 | 2.5 V (default)
d | Input | PIN_AB12 | 3A | B3A_N0 | PIN_D7 | 2.5 V (default)
f | Output | PIN_W20 | 5A | B5A_N0 | PIN_H13 | 2.5 V (default)
<<new node>>
All Pins
9% 00:00:09

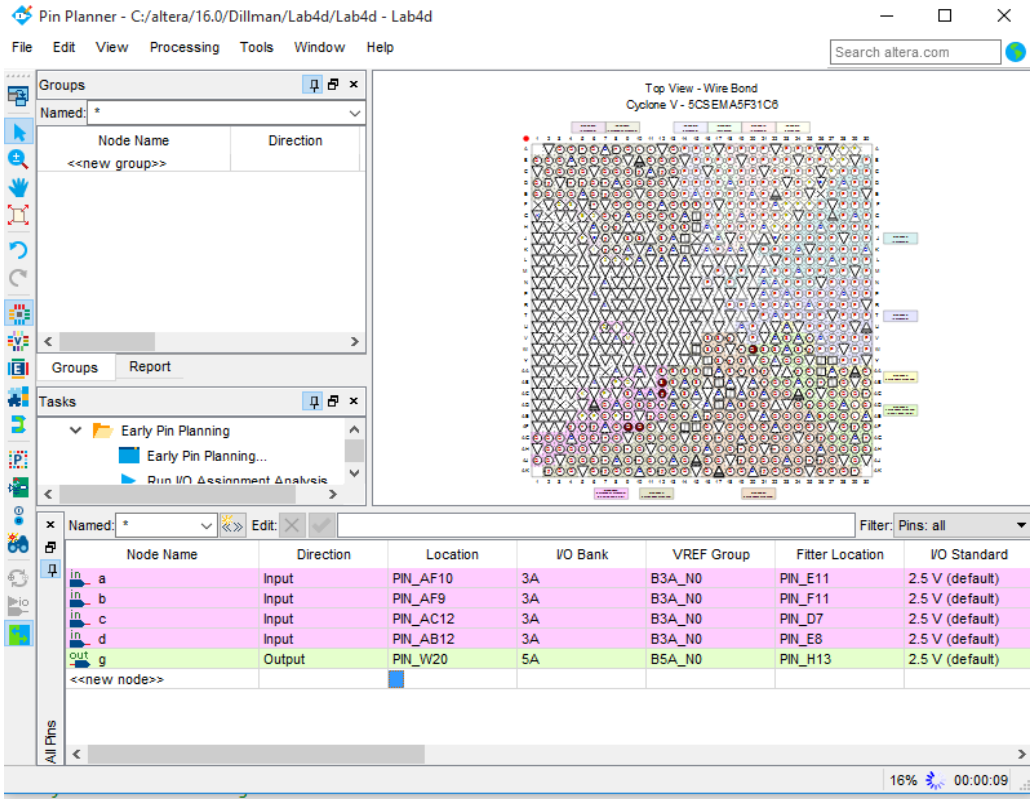

Programmer - C:/altera/16.0/Dillman/Lab4c/Lab4c - Lab4c - [Chain1.cdf]*
File Edit View Processing Tools Window Help
Search altera.com
Hardware Setup... DE-SoC [USB-1] Mode: JTAG Progress: 100% (Successful)
Enable real-time ISP to allow background programming when available
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File | Device | Checksum | Usercode | Program/ Configure | Verify | Blank-Check | Examine
<none> | SOCVHPS | 00000000 | <none>
output_files/Lab4c.sof | 5CSEMA5F31 | 00AF54C1 | 00AF54C1
TDI
SOCVHPS
5CSEMA5F31
TDO

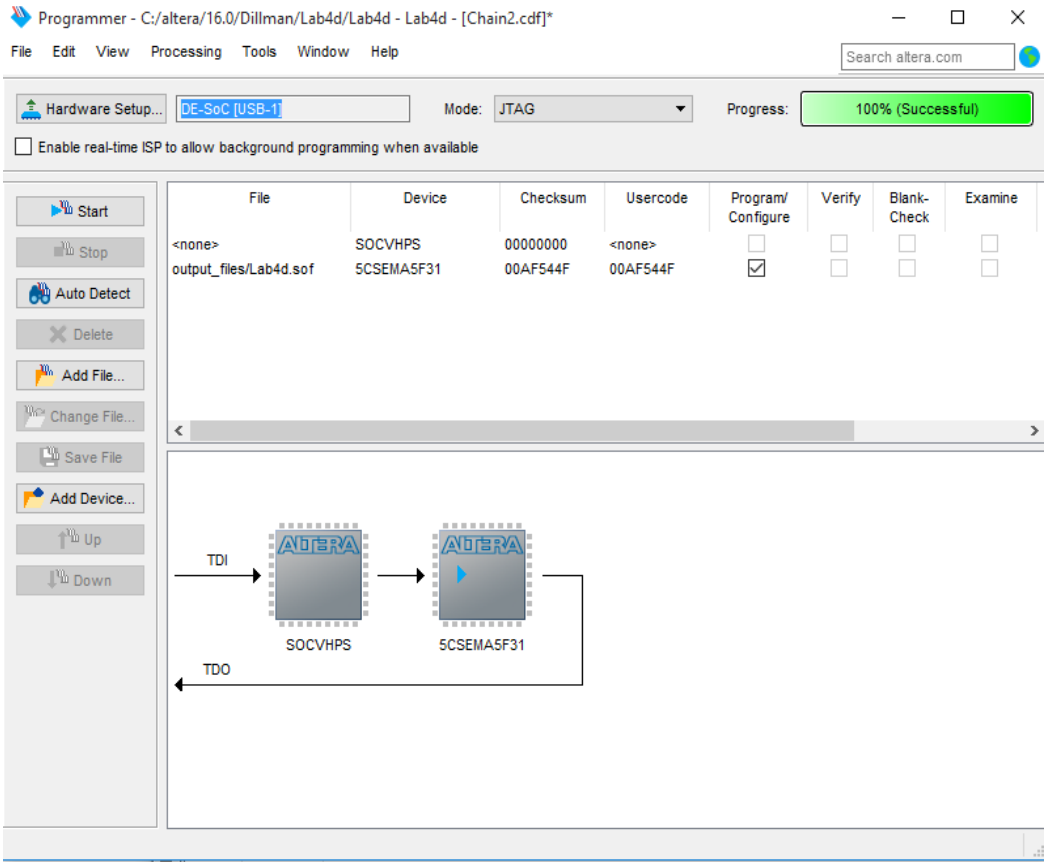
ii. Schematic

We created a body diagram file to draw the NOR-ONLY schematic diagram in the prelab. Then we compiled and test the file and set up switches of the board. After setting, we upload the file to the board and test the board and get the same result of the file.



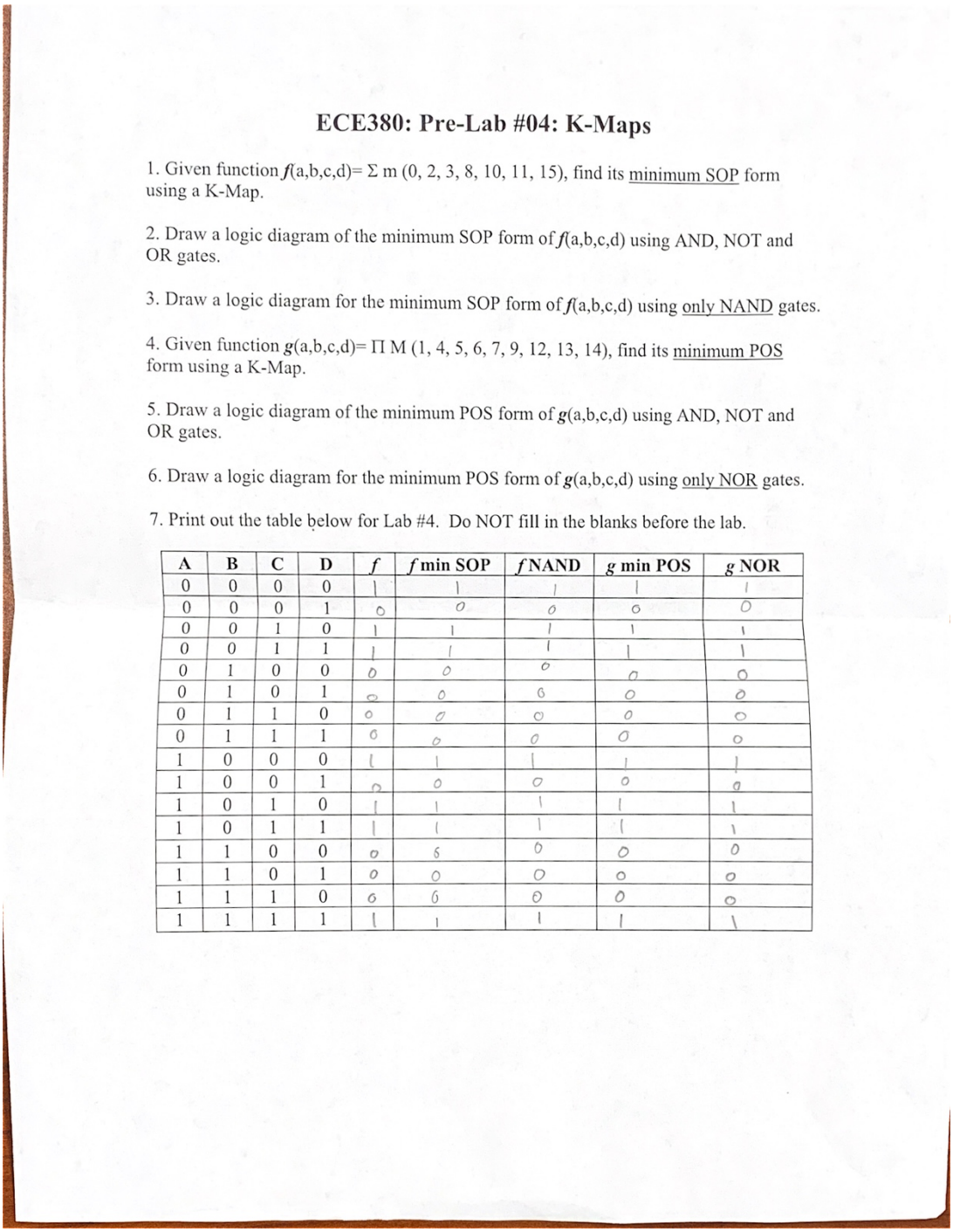



Pin Planner - C:/altera/16.0/Dillman/Lab4d/Lab4d - Lab4d
File Edit View Processing Tools Window Help
Search altera.com
Groups
Named: *
Node Name Direction
<<new group>>
Groups Report
Tasks
Early Pin Planning
Early Pin Planning...
Top View - Wire Bond
Cyclone V - 5CSEMA5F31C6
Named: * Edit: Filter: Pins: all
Node Name Direction Location I/O Bank VREF Group Fitter Location I/O Standard
a Input PIN_AF10 3A B3A_N0 PIN_E11 2.5 V (default)
b Input PIN_AF9 3A B3A_N0 PIN_F11 2.5 V (default)
c Input PIN_AC12 3A B3A_N0 PIN_D7 2.5 V (default)
d Input PIN_AB12 3A B3A_N0 PIN_E8 2.5 V (default)
g Output PIN_W20 5A B5A_N0 PIN_H13 2.5 V (default)
<<new node>>
All Pins
16% 00:00:09


Programmer - C:/altera/16.0/Dillman/Lab4d/Lab4d - Lab4d - [Chain2.cdf]*
File Edit View Processing Tools Window Help
Search altera.com
Hardware Setup... DE-SoC [USB-1] Mode: JTAG Progress: 100% (Successful)
Enable real-time ISP to allow background programming when available
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File Device Checksum Usercode Program/ Configure Verify Blank-Check Examine
<none> SOCVHPS 00000000 <none>
output_files/Lab4d.sof 5CSEMA5F31 00AF544F 00AF544F
TDI
SOCVHPS
5CSEMA5F31
TDO

Result

In the 4 different method, the truth table of each scenario are all same as we predict in the prelab section. The testing by switches are also same as our prediction.



ECE380: Pre-Lab #04: K-Maps

1. Given function f(a,b,c,d)= Σ m (0, 2, 3, 8, 10, 11, 15), find its minimum SOP form using a K-Map.

2. Draw a logic diagram of the minimum SOP form of f(a,b,c,d) using AND, NOT and OR gates.

3. Draw a logic diagram for the minimum SOP form of f(a,b,c,d) using only NAND gates.

4. Given function g(a,b,c,d)= Π M (1, 4, 5, 6, 7, 9, 12, 13, 14), find its minimum POS form using a K-Map.

5. Draw a logic diagram of the minimum POS form of g(a,b,c,d) using AND, NOT and OR gates.

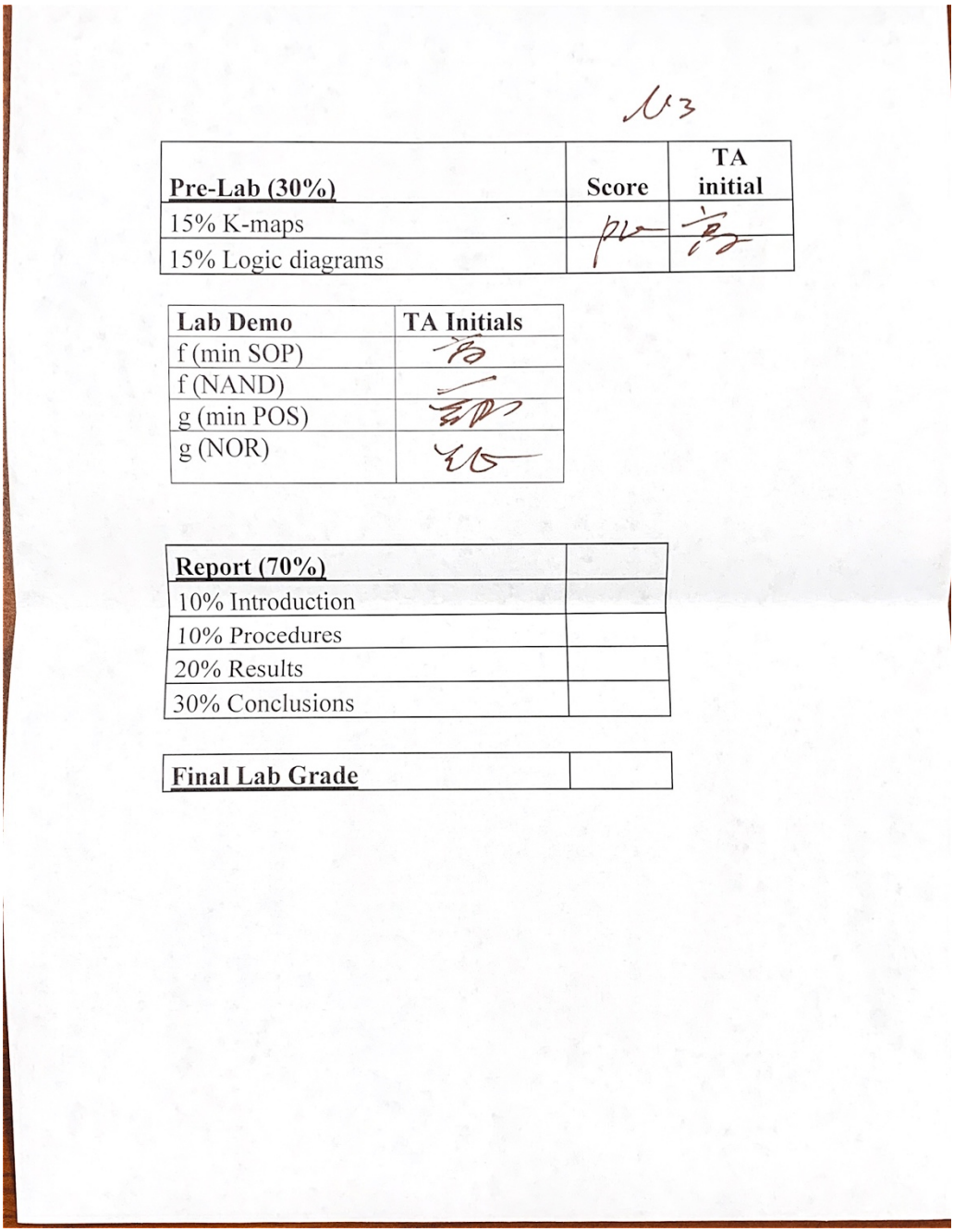
6. Draw a logic diagram for the minimum POS form of g(a,b,c,d) using only NOR gates.

7. Print out the table below for Lab #4. Do NOT fill in the blanks before the lab.

A	B	C	D	f	f min SOP	f NAND	g min POS	g NOR
0	0	0	0	1	1	1	1	1
0	0	0	1	0	0	0	0	0
0	0	1	0	1	1	1	1	1
0	0	1	1	1	1	1	1	1
0	1	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0
0	1	1	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0
1	0	0	0	1	1	1	1	1
1	0	0	1	0	0	0	0	0
1	0	1	0	1	1	1	1	1
1	0	1	1	1	1	1	1	1
1	1	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0
1	1	1	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1

Conclusion

In this lab, we understand how to use K-maps to get an optimized function through SOP method and POS method. We also practiced how to set the switches on the board and learn another testing skill different than waveform method testing.



Pre-Lab (30%)	Score	TA initial
15% K-maps		
15% Logic diagrams		

Lab Demo	TA Initials
f (min SOP)	
f (NAND)	
g (min POS)	
g (NOR)	

Report (70%)	
10% Introduction	
10% Procedures	
20% Results	
30% Conclusions	

Final Lab Grade	