ECE380: Pre-Lab #03: Multifunctional Logic Circuits

In many digital logic applications, a single output that can perform multiple logic functions, for example AND, XOR, XNOR and NOR operations, is desired. In this lab, you will design and test a multifunctional logic circuit capable of implementing multiple logic functions using Altera's DE1 board. You will use the Quartus Prime environment to download and test your design.

Let us consider an output F(C_1, C_0, A, B) that can perform four logic operations when different input conditions are specified.

- When C_1=0 and C_0=0, the output F is the NOR operation of inputs A and B.
- When C_1=0 and C_0=1, the output F is the AND operation of inputs A and B.
- When C_1=1 and C_0=0, the output F is the exclusive NOR operation of inputs A and B. Exclusive NOR of inputs A and B is denoted as F=$\overline{A \oplus B}$. In the SOP form, the exclusive NOR is defined as F=$\overline{A} \cdot \overline{B} + A \cdot B$.
- When C_1=1 and C_0=1, the output is the XOR operation of inputs A and B. Exclusive OR of inputs A and B is denoted as F= $A \oplus B$. In the SOP form, the the exclusive OR is defined as F=$\overline{A} \cdot B + A \cdot \overline{B}$

The table below summarizes the logic operations.

C_1C_0	F
00	$\overline{A + B}$
01	$A \cdot B$
10	$\overline{A \oplus B}$
11	$A \oplus B$

Prior to your lab session, you need to do the following:

1. Draw the 4-input truth table as shown next page with inputs and output column F only. For the logic operations defined in the table above, fill in the values of the outputs under output F. The logic operations will depend on the values of C_1 and C_0. For example, when inputs C_1=0, C_0=1, A=0 and B=0, you need to find the output value that corresponds to the value of a logic function $A \cdot B$.

2. Use the Karnaugh map to obtain the simplest SOP function for F(C_1, C_0, A, B).

3. Draw a NAND-only implementation from the SOP function.

4. Using the text editor of Quartus Prime, write a VHDL code to implement NAND-only logic circuit. Use expressions such as NOT(x1 AND x2 AND x3) for multiple-input NANDs.

5. Using the block editor of Quartus Prime, draw a logic schematic to implement NAND-only logic circuit.

   - Note: Quartus Prime does not have a five input NAND gate. In case you need to use five-input NAND, you can use a six-input NAND gate with input pins 5 and 6 connected to the same signal.

6. Print out the truth table on the next page and fill out the expected values in the output column F and the remaining output columns during your lab session.

Inputs				Outputs				
C_1	**C_0**	**A**	**B**	**F**	**vhd**	**vhd DE1**	**bdf**	**bdf DE1**
0	0	0	0					
0	0	0	1					
0	0	1	0					
0	0	1	1					
0	1	0	0					
0	1	0	1					
0	1	1	0					
0	1	1	1					
1	0	0	0					
1	0	0	1					
1	0	1	0					
1	0	1	1					
1	1	0	0					
1	1	0	1					
1	1	1	0					
1	1	1	1					

Pre-Lab (30%)	**score**	**TA initial**
10% SOP solution		
10% .vhd file		
10% .bdf file		

Report (70%)	
10% Introduction	
10% Procedures	
20% Results	
30% Conclusions	

Lab Grade	