ECE 380: LAB #10: Counter and Finite State Machine

1. Implement Design A. Download the **Design A** to the DE1 board. Use the following inputs: Pushbuttons KEY0 for **Clock** and KEY1 for **Resetn**; toggle switch SW [0] for the input W. Use LEDR [0] to represent the output Z. Compile, assign pins, and download your design to the DE1 board for demonstration to your lab instructor. Print and turn in all VHDL code, simulation results, and FSM design paperwork with your lab report.

2. Implement Design B. Download the **Design B** to the DE1 board. Use the following inputs: Pushbuttons KEY0 for **Clock** and KEY1 for **Resetn**; toggle switch SW [0] for the input W. Use LEDR [0] to represent the output Z. Compile, assign pins, and download your design to the DE1 board for demonstration to your lab instructor. Print and turn in all VHDL code, simulation results, and FSM design paperwork with your lab report.