Lab 04

Multifunctional Logic Circuit

ECE 380-002

University of Alabama

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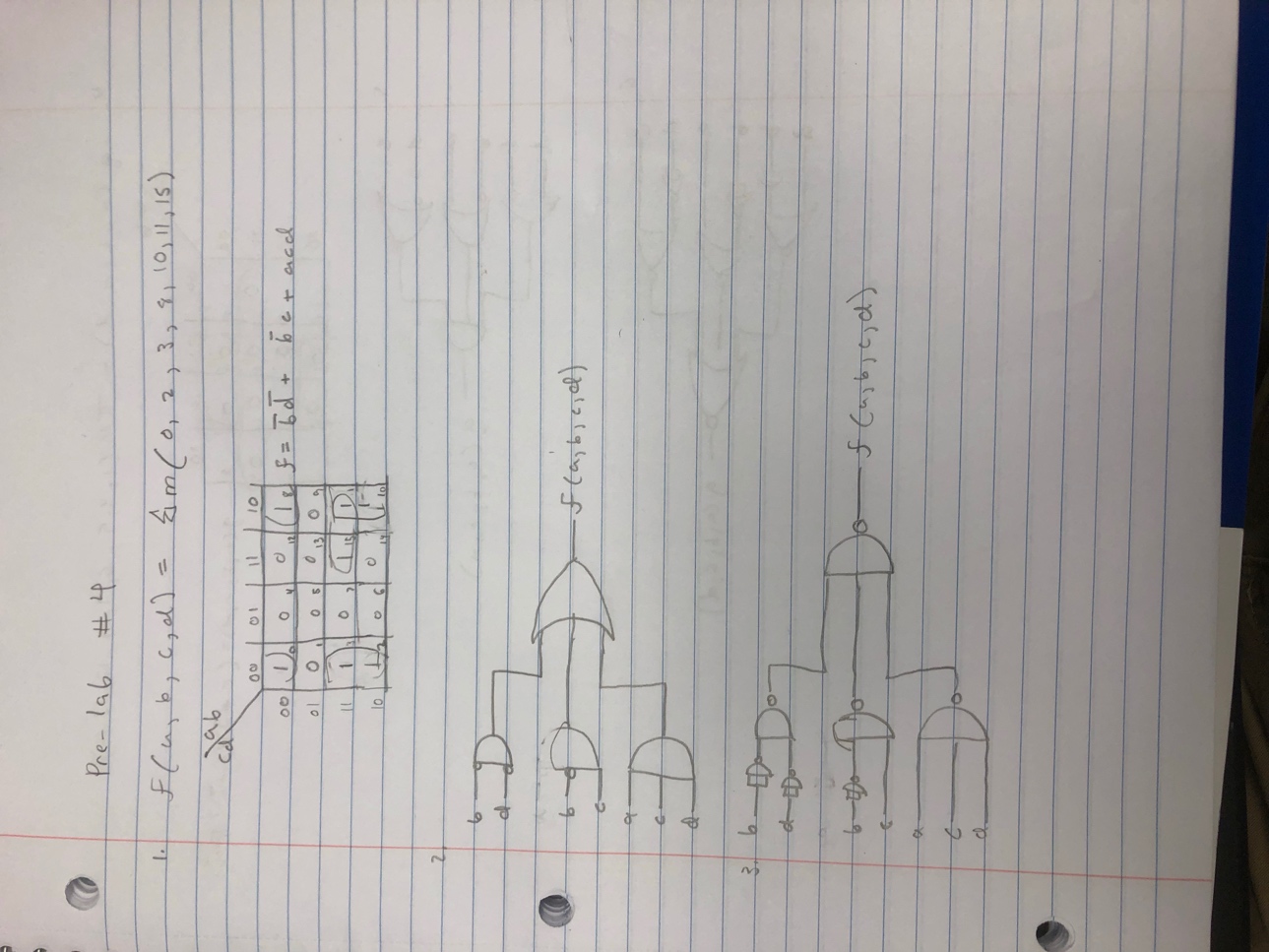
**Introduction**

In this lab, we use the Quartus II environment to download designs to programmable devices on the Altera DE1 board. You create several simple designs, using VHDL and schematic entry, which will be downloaded to the Altera DE1 board.

**Procedure**

1. Prelab
   * 1. SOP Form

In the SOP form, we analyze the problem and create a k-map by the Min-Term method. After we create the k-map, we get an optimized function. Then, we can draw two schematic circuit that first one use AND, NOT, OR Gates and the second one is NAND-Only gate.



* + 1. POS Form

In the POS form, we draw anther k-map and by Max-Term method. We optimize the function. We also draw two schematic diagram the first one using AND, NOT and OR gates; another is using NOR-only gate.

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1. During the lab
   1. SOP form
      1. VHDL

A screenshot of a social media post

Description automatically generatedA screenshot of a cell phone

Description automatically generatedFirstly, we write a VHDL file based on the first part of the prelab. The VHDL file describe the function by using AND, OR and Not syntax. After compiling the file, we run a test and set up the switches of the board. Then import the file into the board. We also test the function again through the board.

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* + 1. Schematic

A screenshot of a video game

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Description automatically generatedWe created a body diagram file to draw the NAND-ONLY schematic diagram in the prelab. Then we compiled and test the file and set up switches of the board. After setting, we upload the file to the board and test the board and get the same result of the file.

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* 1. POS form
     1. VHDL

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Description automatically generatedwe write a VHDL file based on the second part of the prelab. The VHDL file describe the function by using AND, OR and Not gate. After compiling the file, we run a test and set up the switches of the board. Then import the file into the board. We also test the function again through the board.

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* + 1. Schematic

A close up of a map

Description automatically generatedWe created a body diagram file to draw the NOR-ONLY schematic diagram in the prelab. Then we compiled and test the file and set up switches of the board. After setting, we upload the file to the board and test the board and get the same result of the file.

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**Result**

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Description automatically generated In the 4 different method, the truth table of each scenario are all same as we predict in the prelab section. The testing by switches are also same as our prediction.

**Conclusion**

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Description automatically generated In this lab, we understand how to use K-maps to get an optimized function through SOP method and POS method. We also practiced how to set the switches on the board and learn another testing skill different than waveform method testing.