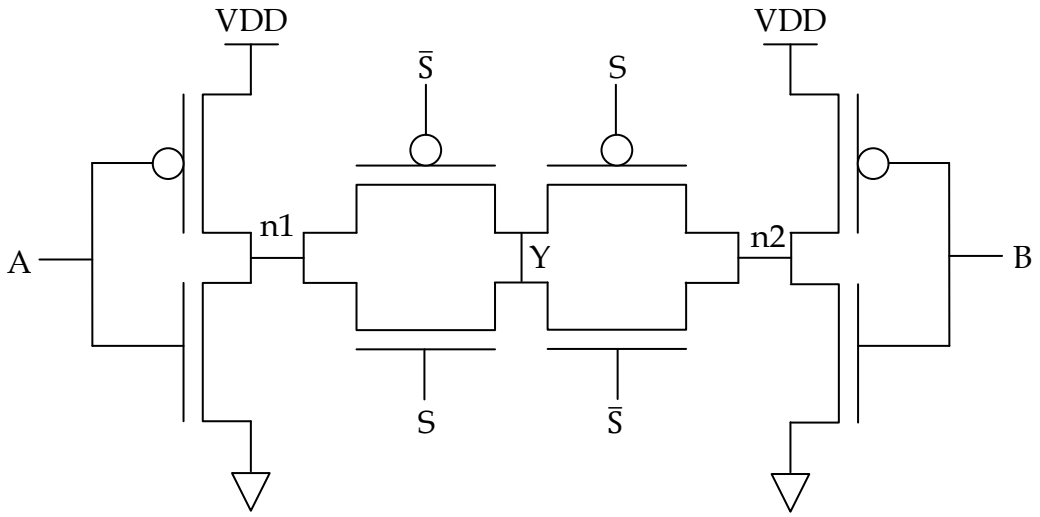
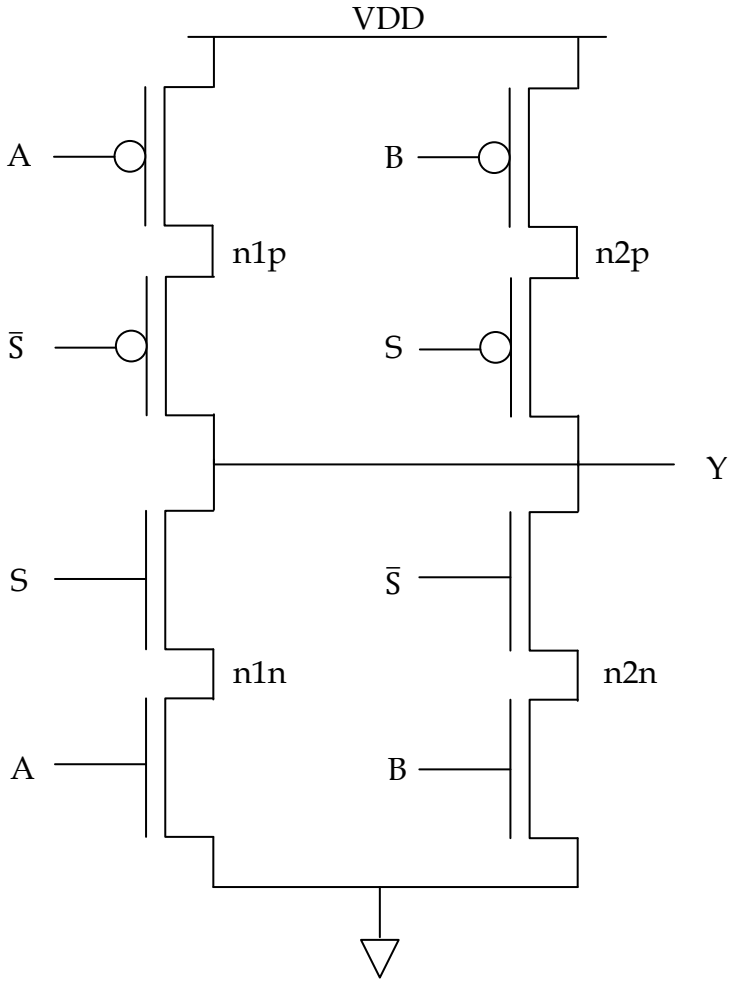
(1)

A. Draw the circuit schematic of the attached layout (a) and (b). Explain which circuit has higher speed.

Here's the circuit of layout(a):

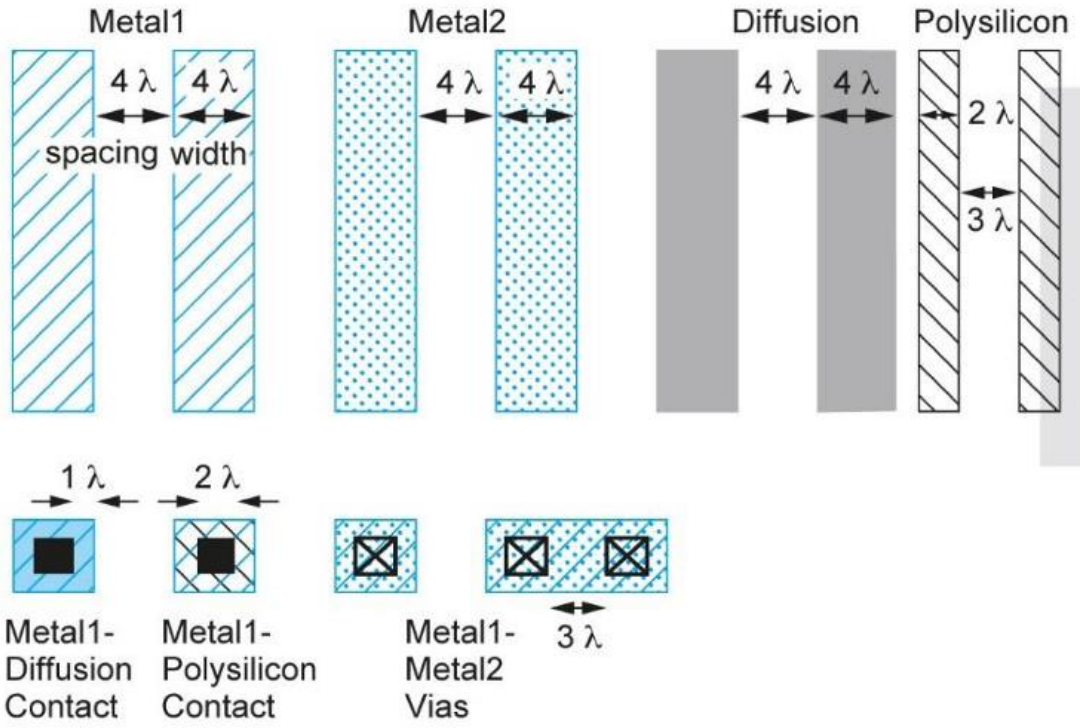


Here's the circuit of layout(b):



以電容的角度來看: Layout(b) 的 diffusion region 是 merged，它的寄生電容會比較小，電容充放電時間比較短，所以速度會變快。
以電阻的角度來看: 距離變短 => 電阻變小 => 電流變大 => 充放電的時間變短 => 速度變快。
綜合以上兩點，可知 layout(b) 的速度會比較快。

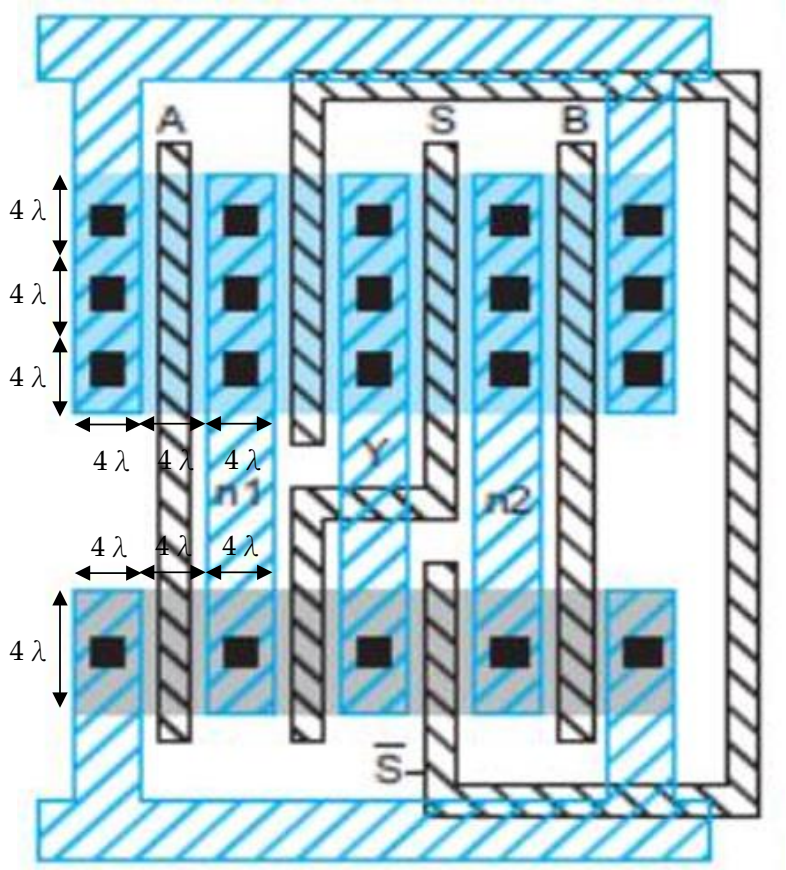
B. Indicate the W/L ratio of each transistors in both (a) and (b) and AD, AS in terms of λ.
我都是照著講義 DIC-Lec4 pp.10 來估大小，請參考下圖:



所以我估長度的方式是:

- contact 算 4 λ
- 兩根 metal 5 之間算 4 λ
- Poly 算 2 λ
- 兩根 poly 之間算 3 λ

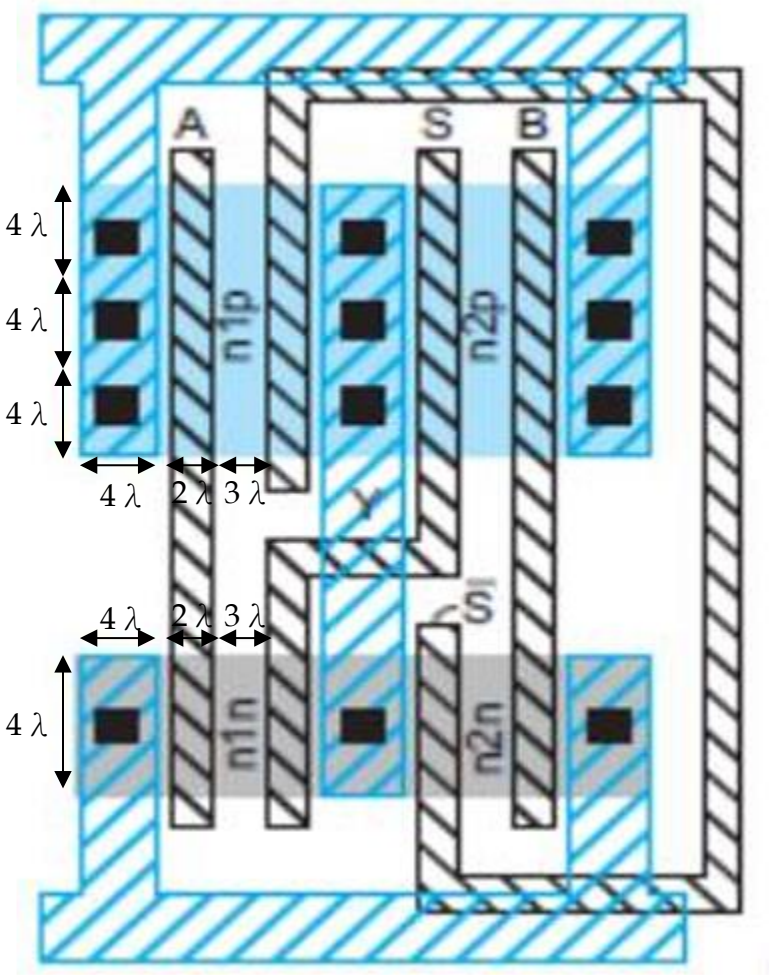
下圖是我具體在 layout(a) 的長度估算方式:



下表是 layout(a) 的每顆 MOS 的 W/L 及其 AD 與 AS:

MOS type	Gate	W	L	W/L	AD	AS
PMOS	A	12λ	2λ	6	$48\lambda^2$	$48\lambda^2$
PMOS	$\bar{S}$	12λ	2λ	6	$48\lambda^2$	$48\lambda^2$
PMOS	S	12λ	2λ	6	$48\lambda^2$	$48\lambda^2$
PMOS	B	12λ	2λ	6	$48\lambda^2$	$48\lambda^2$
NMOS	A	4λ	2λ	2	$16\lambda^2$	$16\lambda^2$
NMOS	S	4λ	2λ	2	$16\lambda^2$	$16\lambda^2$
NMOS	$\bar{S}$	4λ	2λ	2	$16\lambda^2$	$16\lambda^2$
NMOS	B	4λ	2λ	2	$16\lambda^2$	$16\lambda^2$

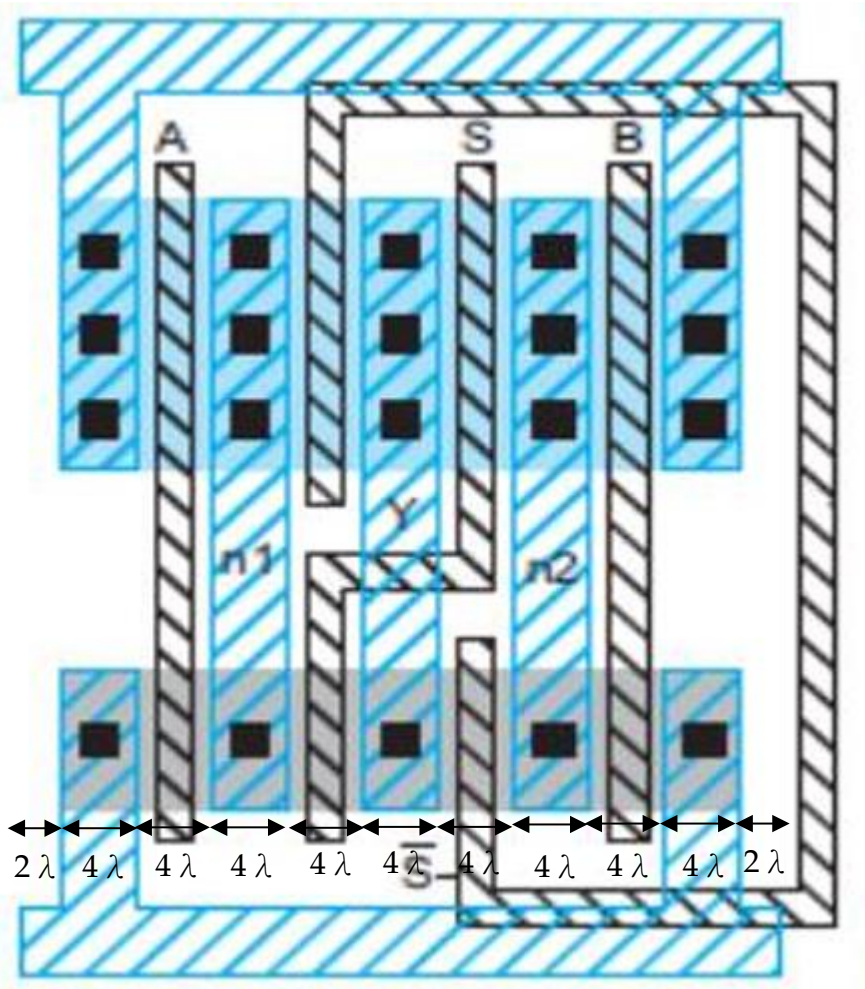
下圖是我具體在 layout(b) 的長度估算方式:



下表是 layout(b) 的每顆 MOS 的 W/L 及其 AD 與 AS:

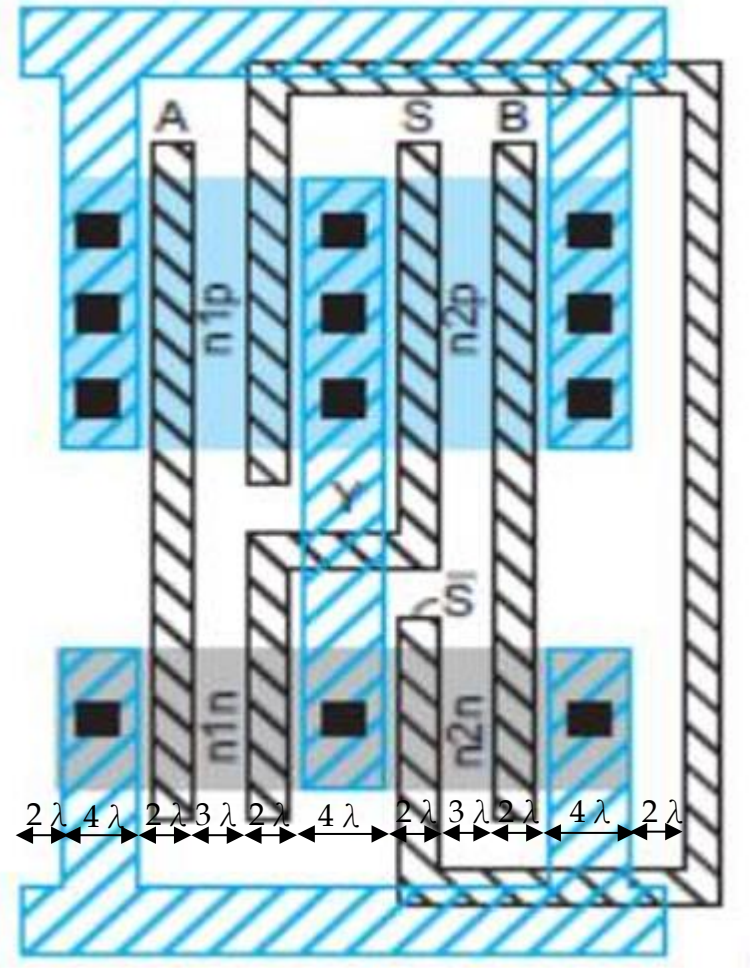
MOS type	Gate	W	L	W/L	AD	AS
PMOS	A	12λ	2λ	6	$36\lambda^2$	$48\lambda^2$
PMOS	$\bar{S}$	12λ	2λ	6	$48\lambda^2$	$36\lambda^2$
PMOS	S	12λ	2λ	6	$48\lambda^2$	$36\lambda^2$
PMOS	B	12λ	2λ	6	$36\lambda^2$	$48\lambda^2$
NMOS	A	4λ	2λ	2	$12\lambda^2$	$16\lambda^2$
NMOS	S	4λ	2λ	2	$16\lambda^2$	$12\lambda^2$
NMOS	$\bar{S}$	4λ	2λ	2	$16\lambda^2$	$12\lambda^2$
NMOS	B	4λ	2λ	2	$12\lambda^2$	$16\lambda^2$

C. Mark the design rules in (a) and (b) that determine the width of this layout.
下圖是我具體在 layout(a)上估長度的方式:



Therefore, the width of the layout(a) is 40λ.

下圖是我具體在 layout(b)上估長度的方式:



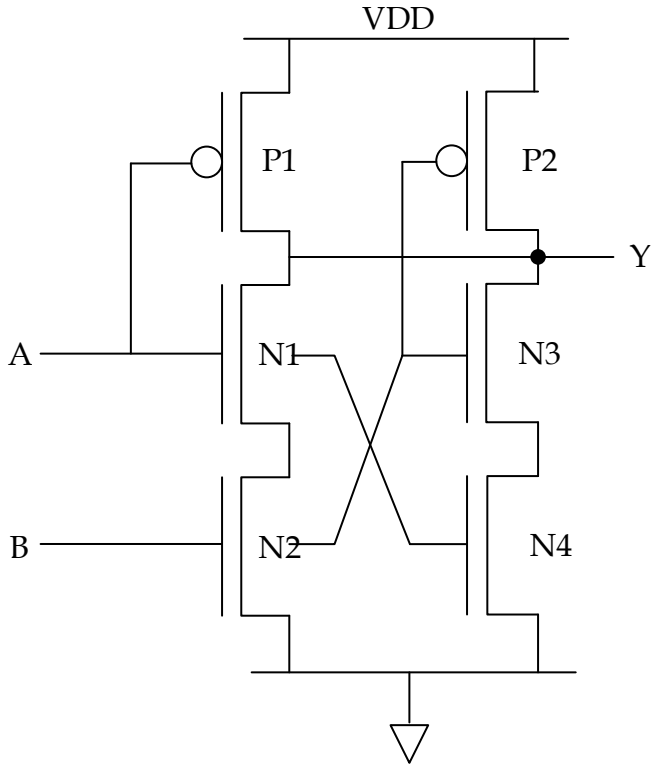
Therefore, the width of the layout(b) is 30λ.

(2)

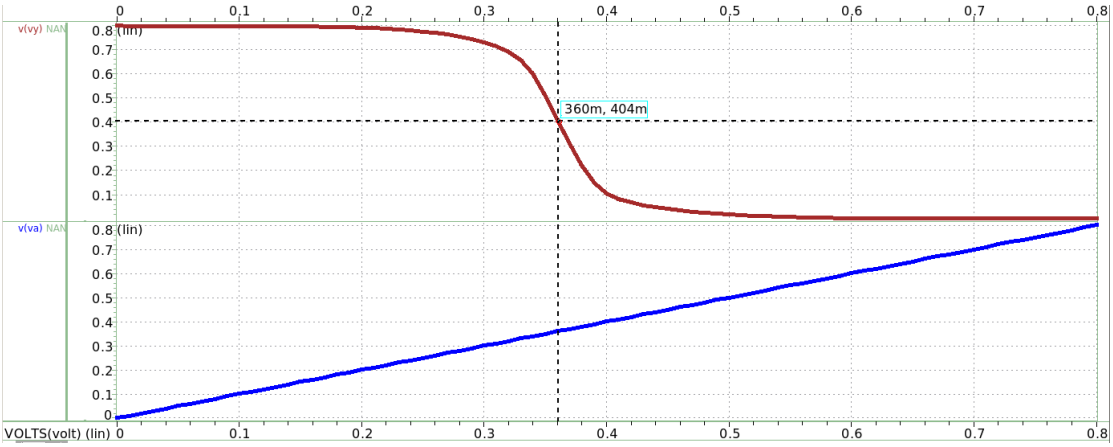
A.

Here's my W/L of PMOS and NMOS:

MOS	W	L	W/L
P1	64n	40n	1.6
P2	64n	40n	1.6
N1	64n	32n	2
N2	64n	32n	2
N3	64n	32n	2
N4	64n	32n	2



Here's the simulation result of VCT:



B.

i. output capacitances and input capacitance of the NAND circuit.

I use ".option captab" to print the input capacitance and output capacitance:

```
.option captab
.op
```

Here's the simulation result:

```
   nodal  capacitance table

   node    =    cap      node    =    cap      node    =    cap

+0:va      = 187.7768a 0:vb      = 187.7768a 0:vdd!    = 313.5648a
+0:vy      = 245.6391a 1:n12     = 160.9708a 1:n34     = 160.9708a
```

Input capacitance = 187.7768 +187.7768 = 375.5536 aF.

Output capacitance = 245.6391 aF.

ii. Leakage power dissipation when Vin = logic 1, and Vout = logic 0.

Here's my code:

```
VVA VA gnd! 0.8
VVB VB gnd! 0.8
.probe power = par('-p(vvdd)')
.tran 0.01n 20n
.meas tran leakagepower AVG power from = 0.01n to = 10n
```

The simulation result:

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
leakagepower=   4.1818n  from=  10.0000p     to=  10.0000n
```

In conclusion, the leakage power dissipation is 4.1818nw when Vin = logic 1, and Vout = logic 0.

iii. Leakage power dissipation when Vin = logic 0, and Vout = logic 1.

Here's my code:

```
VVA VA gnd! 0
VVB VB gnd! 0
.probe power = par('-p(vvdd)')
.tran 0.01n 20n
.meas tran leakagepower AVG power from = 0.01n to = 10n
```

The simulation result:

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
leakagepower=  10.9291n  from=  10.0000p     to=  10.0000n
```

In conclusion, the leakage power dissipation is 10.9291nw when Vin = logic 0,

and Vout = logic 1.

C.

i. A=1 and B changes from 0 to 1.

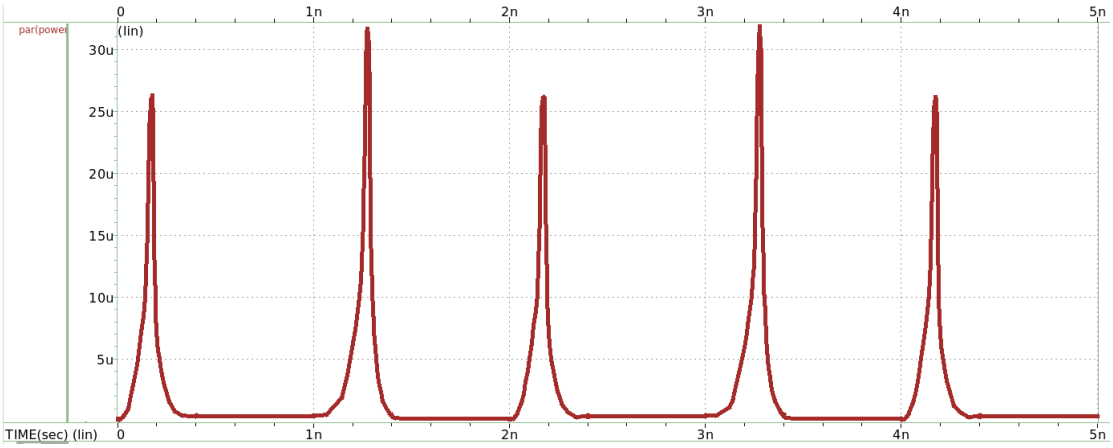
Here's my code:

```
VVA VA gnd! 0.8v
VVB VB gnd! pulse(0 0.8 0ns 0.4ns 0.4ns 0.6ns 2ns)
.meas tran tdr trig v(VB) val='0.45*xvdd' fall=2 targ v(out1) val='0.5*xvdd' rise=2
.meas tran tdf trig v(VB) val='0.45*xvdd' rise=2 targ v(out1) val='0.5*xvdd' fall=2
.tran 10ps 5ns
```

The simulation result of tdr and tdf:

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
tdr=  66.4777p  targ=   3.2865n   trig=   3.2200n
tdf= -22.4084p  targ=   2.1576n   trig=   2.1800n
```

Here's the power waveform:



Here's the average power and peak power:

```
avgpower=   2.2712u  from=  10.0000p     to=   5.0000n
peakpower=  31.7930u    at=   1.2735n
            from=  10.0000p    to=   5.0000n
```

In conclusion:

Parameters	tdr	tdf	Avg power	Peak power
value	66.4777ps	-22.4084ps	2.2712uw	31.7930uw

ii. B=1 and A changes from 0 to 1.

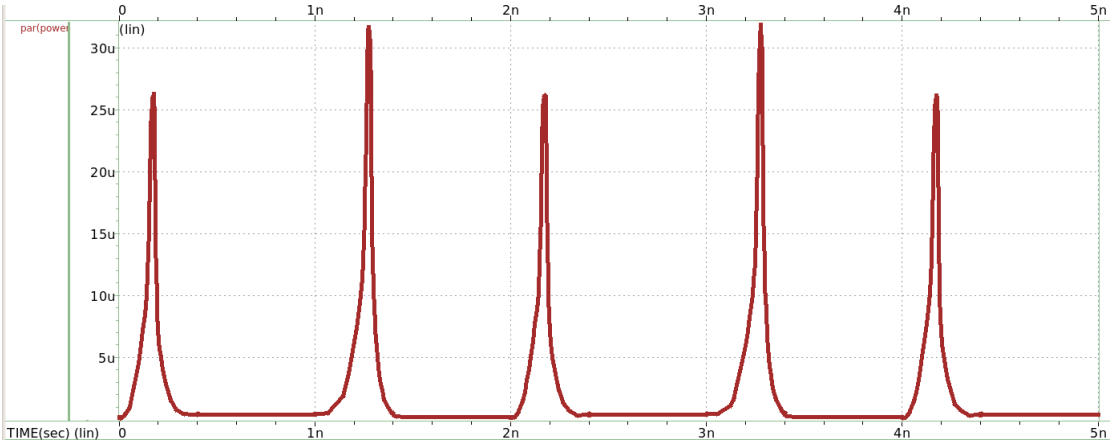
Here's my code:

```
VVA VA gnd! pulse(0 0.8 0ns 0.4ns 0.4ns 0.6ns 2ns)
VVB VB gnd! 0.8v
.meas tran tdr trig v(VA) val='0.45*xvdd' fall=2 targ v(out1) val='0.5*xvdd' rise=2
.meas tran tdf trig v(VA) val='0.45*xvdd' rise=2 targ v(out1) val='0.5*xvdd' fall=2
.probe power = par('-p(vdd)')
.meas tran AvgPower AVG power from = 0.01n to = 5n
.meas tran PeakPower MAX power from = 0.01n to = 5n
.tran 10ps 5ns
```

Here's the simulation result of tdr and tdf:

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
tdr=  66.4777p  targ=   3.2865n   trig=   3.2200n
tdf= -22.4084p  targ=   2.1576n   trig=   2.1800n
```

Here's the power waveform:



Here's the average power and peak power:

```
avgpower=   2.2712u  from=  10.0000p     to=   5.0000n
peakpower=  31.7930u    at=   1.2735n
            from=  10.0000p    to=   5.0000n
```

In conclusion:

Parameters	tdr	tdf	Avg power	Peak power
value	66.4777ps	-22.4084ps	2.2712uw	31.7930uw