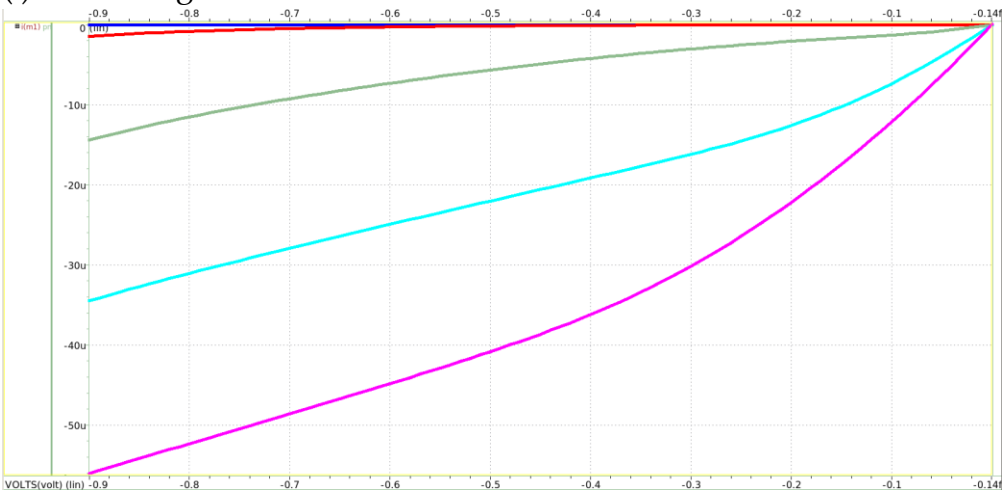
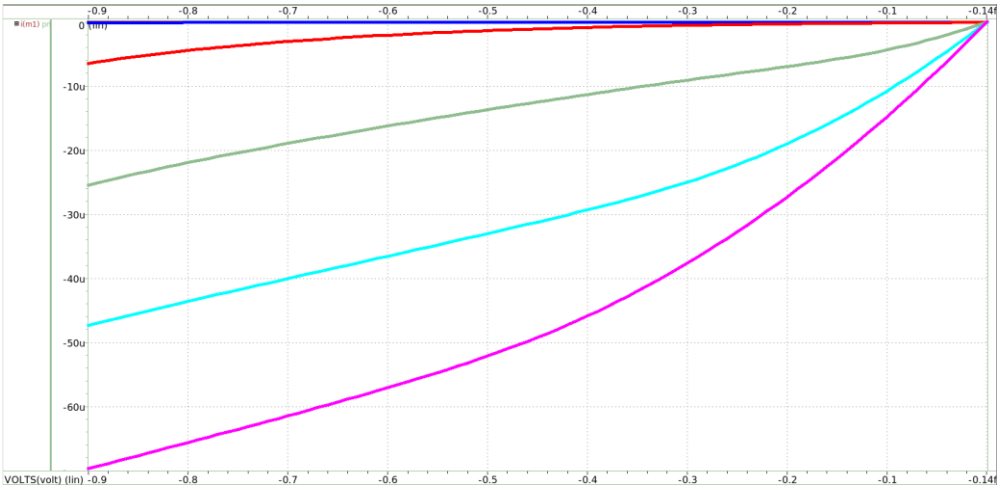
(1) MOS and Inverter with medium threshold voltages (30%)

A. Run SPICE to draw the I-V DC curves for PMOS and NMOS with minimum feature size using High Vt, Medium Vt, and Low Vt respectively. (24%)

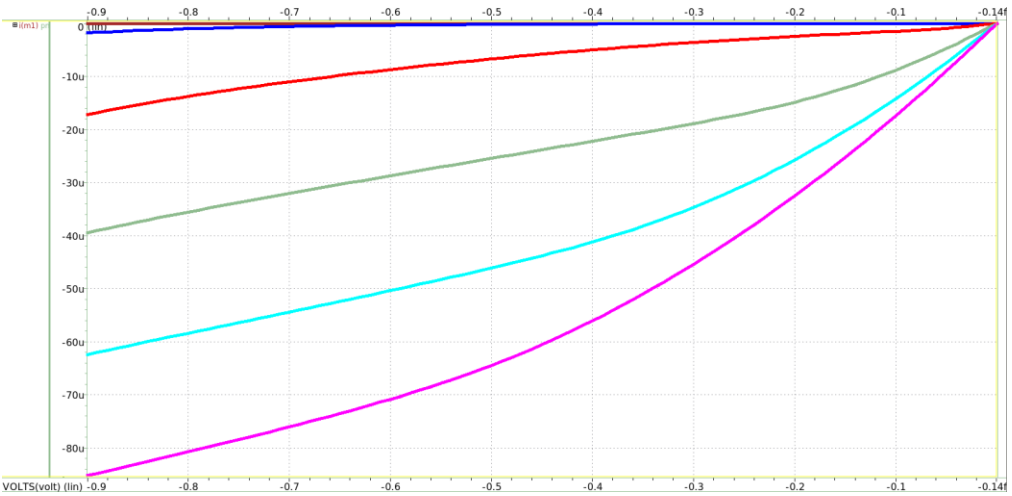
(i) PMOS High V_t



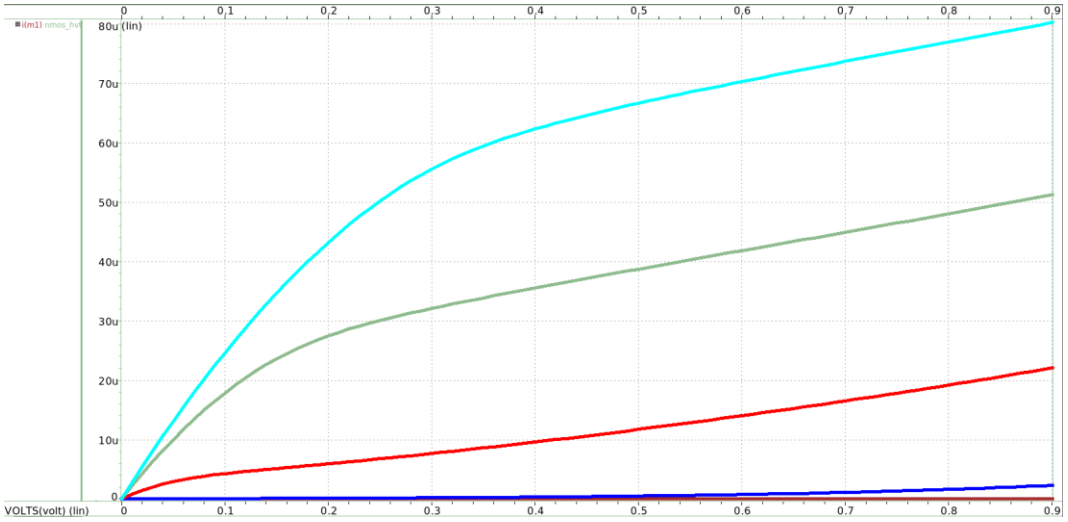
(ii) PMOS Medium V_t



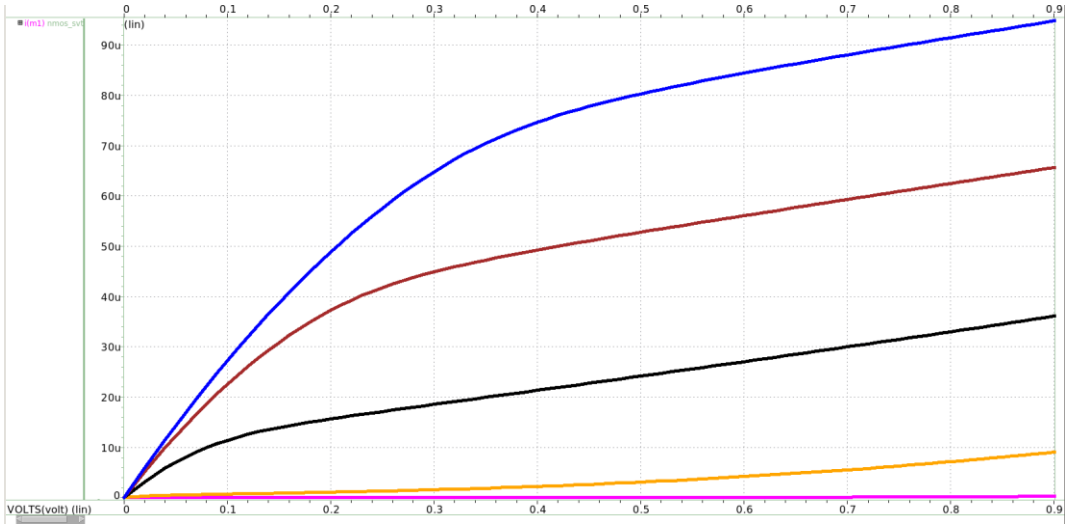
(iii) PMOS Low V_t



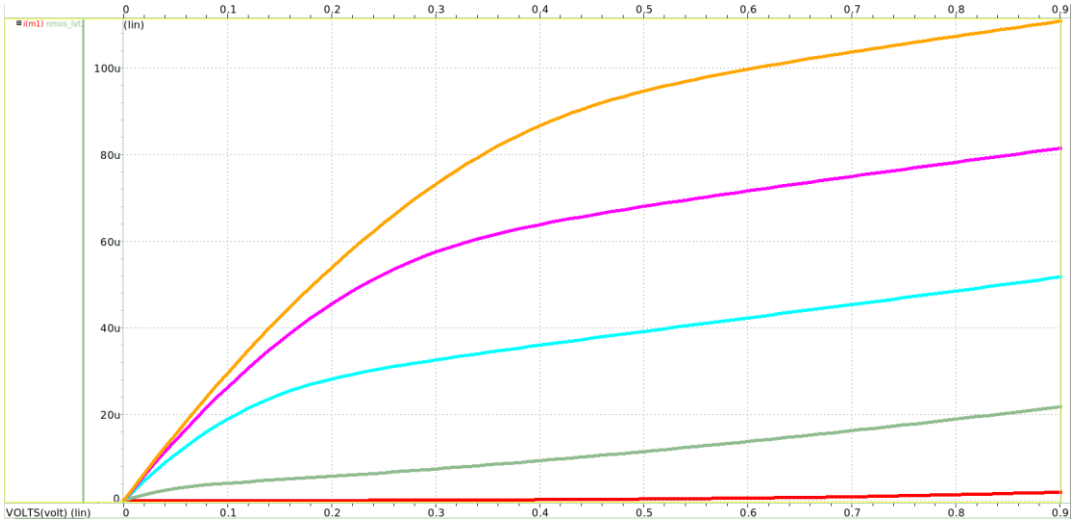
(ix) NMOS High V_t



(x) NMOS Medium V_t



(xi) NMOS Low V_t



B. Keep L equals to L_{min}, design the W of each transistor using medium V_t such that the logic threshold of inverter is at 0.5VDD. Discuss your design procedures and the way you choose your MOS dimensions. Run SPICE to verify your results. (6%)

(i) Discuss my design procedure.

$$\frac{\beta_p}{\beta_n} = \frac{\mu_p}{\mu_n} \times \frac{(t_{ox})_n}{(t_{ox})_p} = \frac{0.014}{0.05} \times \frac{1.15}{1.2} = 0.27$$

上式參數的值我是套製程檔內提供的值。

由上式的手算結果我推斷 NMOS 的 $\frac{W}{L}$ 要是 PMOS 的 0.27 倍。

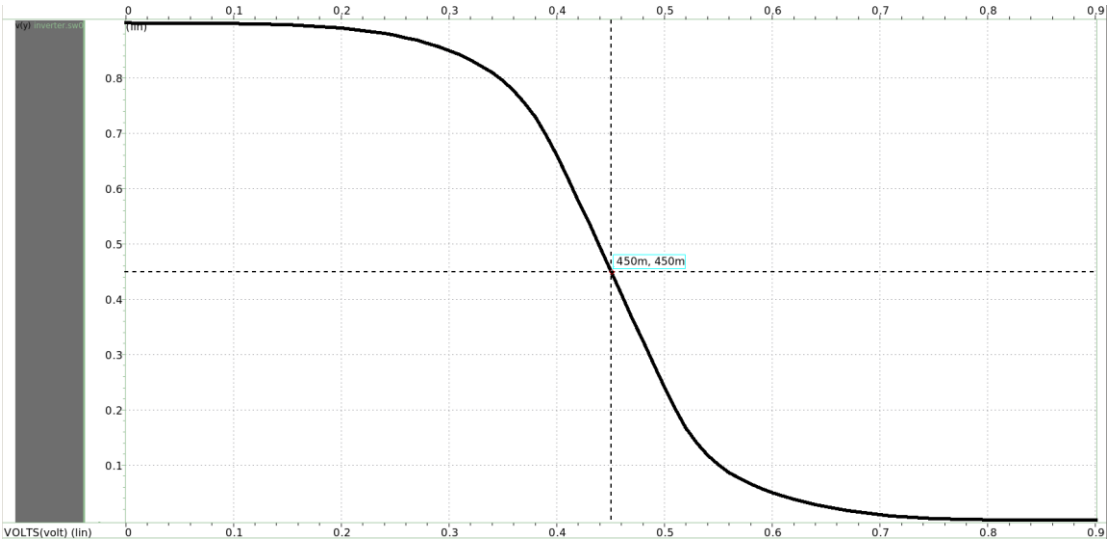
(ii) HSPICE Simulation

下表是我實際跑 HSPICE 模擬時用的參數:

	W	L	W/L
PMOS	115n	32n	3.59
NMOS	64n	32n	2

由上表可知 NMOS 的 $\frac{W}{L}$ 為 PMOS 的 0.55 倍，跟我的手算值 (即 0.27) 有段差距。

下圖是 V_{in} vs V_{out}



(2) Design a CMOS schmitt trigger shown at Fig. 1(b) such that V^+ = 0.54-0.57V and V^- = 0.36-0.33V with CT=VDD (70%)

A. Discuss the difference between Fig. 1(a) and (b). Give the W/L of each device (in table form) of Fig. 1(b) with CT=VDD and discuss your design procedures to determine the size of each transistor using medium V_t. (30%)

(i) Discuss the difference between Fig. 1(a) and (b).

In Fig. 1(b), this circuit is a Schmitt trigger with controllable hysteresis. We can modify V^+ and V^- using V_{CT} even though this circuit has been taped out. However, for the circuit in Fig. 1(a), we have to determine a specific value of V^+ and V^- before taped out. After taped out, the value of V^+ and V^- are fixed and cannot be modified.

(ii) Discuss my design procedures.

Here's the formula of V^- and V^+

$$V^- = \frac{V_{DD} + V_{t_p} + \sqrt{\beta_{n_{eq}}/\beta_{p_{eq}}}V_{t_n}}{1 + \sqrt{\beta_{n_{eq}}/\beta_{p_{eq}}}}$$

$$V^+ = \frac{V_{DD} + V_{t_p} + \sqrt{\frac{\beta_{n_{eq}}}{\beta_{p_{eq}}}}V_{t_n}}{1 + \sqrt{\frac{\beta_{n_{eq}}}{\beta_{p_{eq}}}}} + \frac{\sqrt{\frac{\beta_{n_{eq}}}{\beta_{p_{eq}}}}\left(V_{DD} - V_{t_n}\right)}{\left(1 + \sqrt{K_n}\right)\left(1 + \sqrt{\frac{\beta_{n_{eq}}}{\beta_{p_{eq}}}}\right)}$$

$$= V^- + \frac{\sqrt{\beta_{n_{eq}}/\beta_{p_{eq}}}\left(V_{DD} - V_{t_n}\right)}{\left(1 + \sqrt{K}\right)\left(1 + \sqrt{\beta_{n_{eq}}/\beta_{p_{eq}}}\right)}$$

$$\beta_{n_{eq}} = \frac{\beta_{N1}\beta_{N2}}{\beta_{N1} + \beta_{N2}}, \beta_{p_{eq}} = \frac{\beta_{P1}\beta_{P2}}{\beta_{P1} + \beta_{P2}}, K = \frac{(W/L)_{N1}}{(W/L)_{N3} \parallel (W/L)_{N4}}$$

從上面的兩個式子可知:

想要讓 V^- 變小就要把 $\beta_{n_{eq}}$ 調大，也就是說 N1 及 N2 的 $\frac{W}{L}$ 要調大，且 P1 及 P2 的 $\frac{W}{L}$ 要調小。

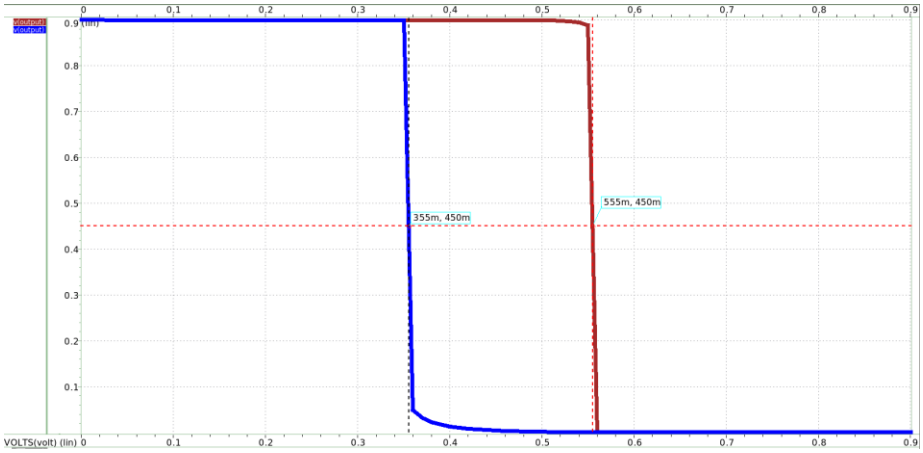
想要讓 V^+ 變大就要把 $\sqrt{K}$ 調小，也就是說 N3 及 N4 的 $\frac{W}{L}$ 要調大，而且要比 N1 的 $\frac{W}{L}$ 還要大。

下表是我每個 MOS 的參數大小

	W	L	W/L
N1	90n	32n	2.8125
N2	50n	32n	1.5625
N3	800n	32n	25
N4	800n	32n	25
P1	64n	80n	0.8
P2	64n	80n	0.8
P3	64n	32n	2
P4	64n	32n	2

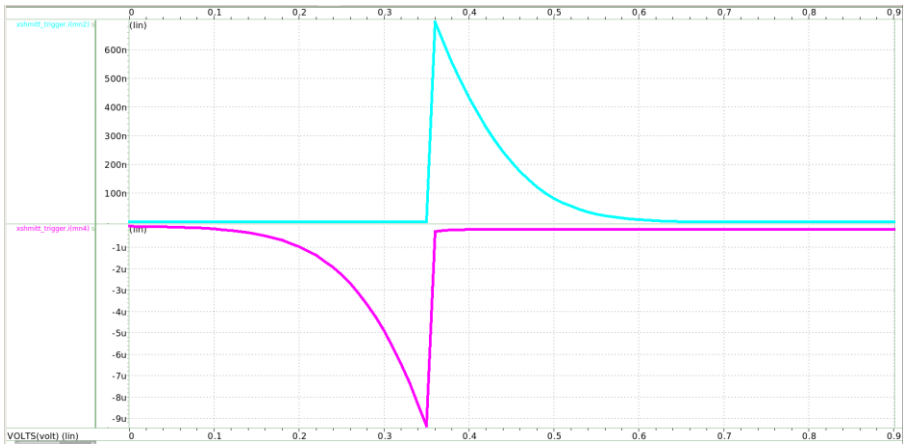
B. Run SPICE to verify your results. Your report must have the figures of VTC, I_{N2} vs V_{in}, and I_{N4} vs V_{in} (20%)

(i) V_{in} vs V_{out}

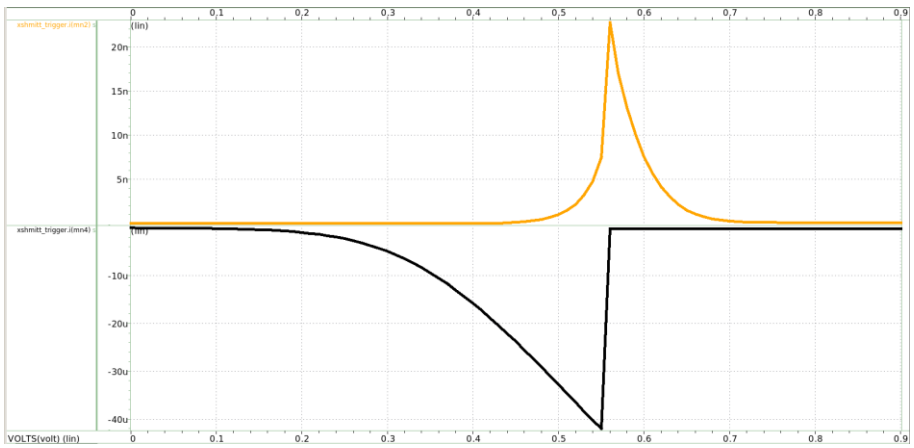


V^-	0.355v
V^+	0.555v

(ii) I_{N2} vs V_{in} & I_{N4} vs V_{in} while V_{in} decreasing from 0.9v to 0v

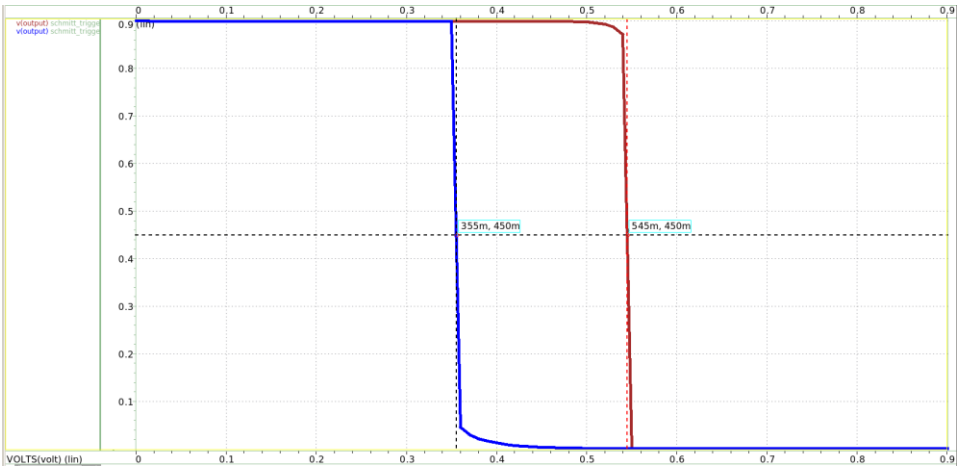


(iii) I_{N2} vs V_{in} & I_{N4} vs V_{in} while V_{in} increasing from 0v to 0.9v



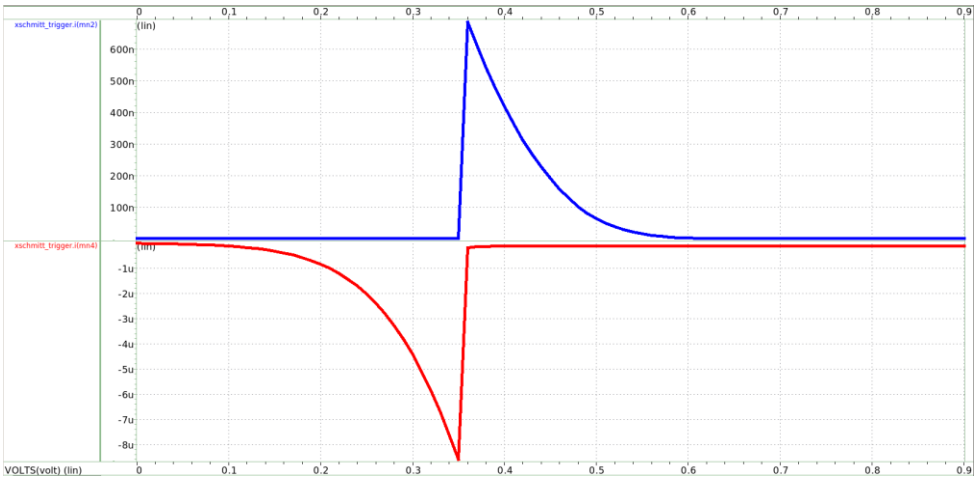
C. Use the same size as in part A, and modify CT to 0.8VDD. Repeat part B to have figures to indicate the new V^- and V^+ (20%)

(i) V_{in} vs V_{out}



New V^-	0.355v
New V^+	0.545v

(ii) I_{N2} vs V_{in} & I_{N4} vs V_{in} while V_{in} decreasing from 0.9v to 0v



(iii) I_{N2} vs V_{in} & I_{N4} vs V_{in} while V_{in} increasing from 0v to 0.9v