Beijing Jiaotong University

Digital system Report Paper

Experiment Title: **Design a four-person responder based on 74SL175**

Date:2019 Year10 Month 29Day **Time:18:00-20:00**

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1.Design requirement.

Firstly, according to the requirements of the responder, the functional requirements of the circuit are analyzed as follows. First, when the moderator presses the main switch, the corresponding lamp should be lit, and after the lamp is turned on, the responder does not need to press the switch for a long time, just press once and the corresponding lamp will light. The circuit can work on its own and keep the light on. Secondly, when one of the answer lights is lit, the subsequent operations of the other responders on the switch will not change the current lighting condition. Finally, after the call is over, the host can turn off the main switch and turn off the circuit. Based on the above analysis, the circuit should have the following functions:

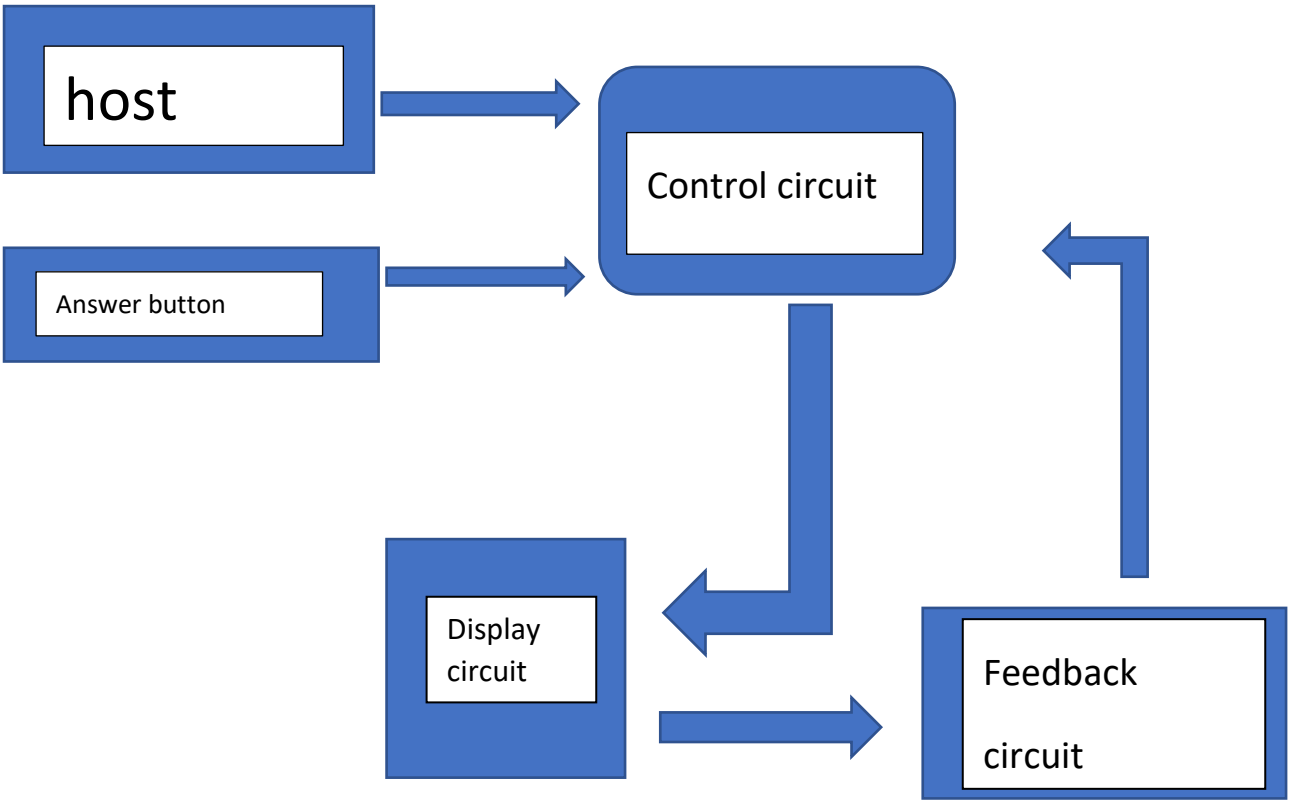
(1) Memory function. This circuit saves the signal of the first person who pressed the switch and keeps the corresponding signal automatically lit for a long time, so that the person answering the question does not need to press the switch for a long time. The signal also acts in the shield circuit.

(2) Shielding function. When the first lamp is lit, the circuit can use the storage signal to block the switching signals of other subsequent responders so that the other lamps are no longer illuminated.

(3) Restore function. The host switch can restore the circuit to its original state.

2.Design idea and diagram.

On request, a 74175-based circuit module plus a 7408-based AND gate and a 7432-based buzzer should be used. Therefore, a basic flow chart can be obtained.
The four-way emergency responder is composed of the host control switch s, emergency responder switch S1-S4, control circuit (74ls175 chip), logic and gate, LED display circuit and other modules.

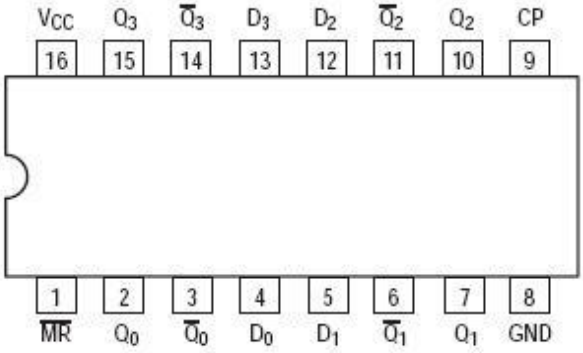


3.Design steps

First design the circuit module based on 74SL175.

SN74LS175

CONNECTION DIAGRAM DIP (TOP VIEW)

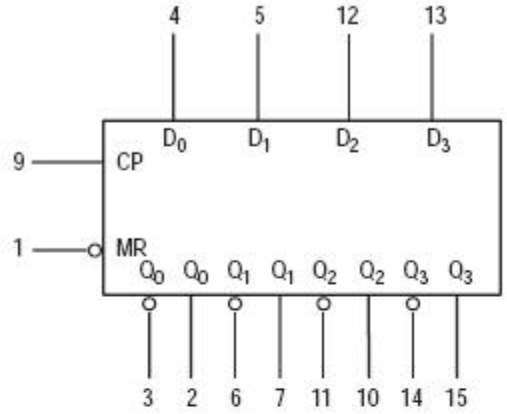


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES		LOADING (Note a) HIGH	LOW
$D_0 - D_3$	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	True Outputs	10 U.L.	5 U.L.
$\overline{Q}_0 - \overline{Q}_3$	Complemented Outputs	10 U.L.	5 U.L.

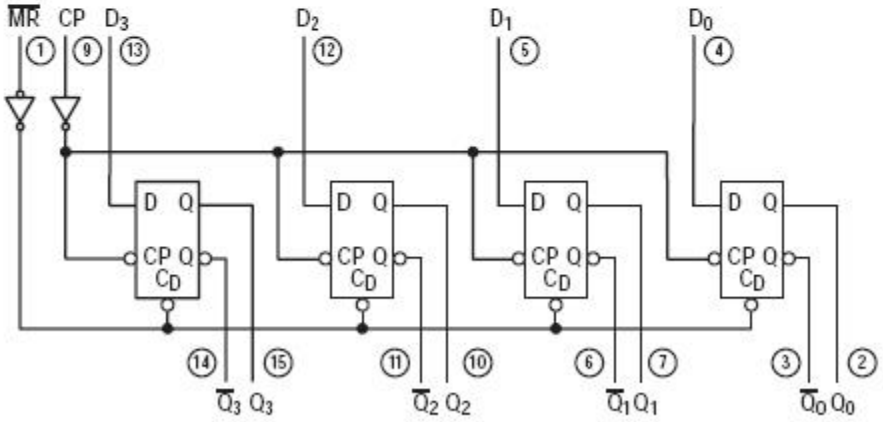
NOTES:
a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

LOGIC DIAGRAM



V_{CC} = PIN 16
GND = PIN 8
○ = PIN NUMBERS

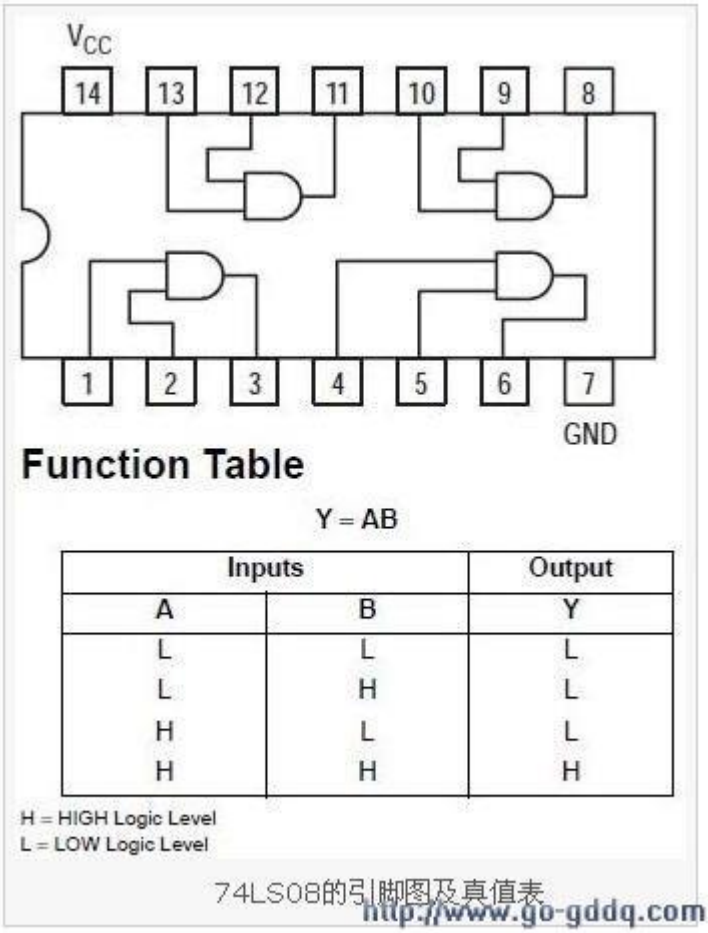
74LS175的功能表

输 入						输 出			
R_D	CP	$1D$	$2D$	$3D$	$4D$	$1Q$	$2Q$	$3Q$	$4Q$
L	×	×	×	×	×	L	L	L	L
H	↑	$1D$	$2D$	$3D$	4D	$1D$	$2D$	$3D$	$4D$
H	H	×	×	×	×	保 持			
H	L	×	×	×	×	保 持			

741s175的真值表

输入				输出	
Sd’	Rd’	CP	D	Qn+1	Qn+1’
0	1	×	×	1	0
1	0	×	×	0	1
0	0	×	×	ϕ	ϕ
1	1	↑	1	1	0
1	1	↑	0	0	1
1	1	↓	×	Qn	Qn’

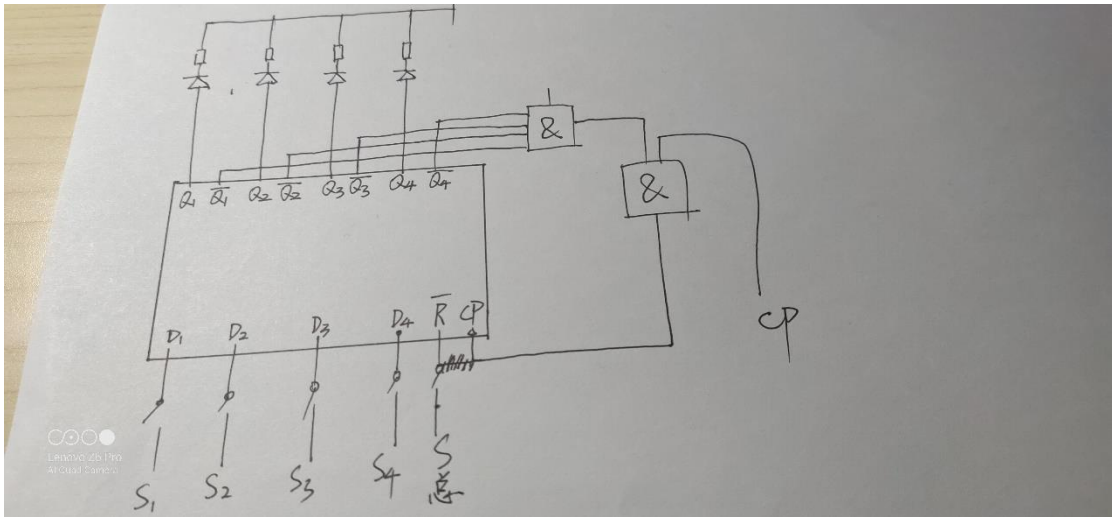
The four outputs are then connected to the AND gate based on the 74SL08.



Then connect the output to the next AND gate.

The pulse is then connected, and the output is linked to the 9th bit of 74175.

4. Present whole logic gate diagram, essential specification and explanation.



As shown, it is an intelligent race response circuit consisting of integrated D triggers. In the figure, chip 3 is the four rising edge D triggers 74LS175: S1,S2,S3,S4 are the answer switch; Q1 ~ Q4 are respectively connected with 4 LED light-emitting diodes; Q1-Q 4 is connected at the same time, and the four input and gate are connected at the same time. Their output and external CP signal are input to the two input and gate, and the two output and input and gate are connected to 74 CP. The working pulse input terminal S of 74LS175 is always the host switch. When the power supply is connected to RD not, RD not = 1 (high voltage, invalid signal).

If all emergency response switches are disconnected from ground (low voltage), Q1-Q4 = 0 (low voltage). The host machine clears the signal and presses the reset switch $S_{总}$. According to the circuit, at this time, output Q1-Q4 of 74ls175 is set to 0 at the same time, and all LEDS are extinguished. At this time, Q 1-Q 4 = 1 and door no. 1 and door no. 2 are open, and the working pulse input terminal CP can receive the external working pulse. When the host announces the beginning, the first judge immediately presses one of the switches s1-s4. At this point, the switch is connected to the power supply, the current will pass through the switch and enter the trigger, and the whole circuit will work. For example, if S1 switch is pressed, D1 = 1 (high level) and Q1 = L, the corresponding LED will be lit up. At the same time, Q 1 = 0, so the output of No.1 and gate is 0, the input of No.2 and gate is 0, and then the external working pulse of No.2 and gate is input. If the CP input signal of 74ls175 is equal to 0 and the working pulse is lost, the edge trigger of 74ls175 will not accept the switch signal of the other three responders. When the S1 switch is turned on, the flip-flop has a storage function. The D1 flip-flop will keep the signal output unchanged, its corresponding lamp will be on for a long time, and there are still tens of thousands of found signals. This will continue until the host presses $S_{总}$ again for the total clear signal.

5.Analyze the principle and the results.

S4	S3	S2	S1	Q4	Q3	Q2	Q1
L	H	H	H	1	0	0	0
H	H	H	H	0	0	0	0
H	H	L	L	0	0	1	1
H	L	H	H	0	1	0	0
L	H	H	L	1	0	0	1
H	H	H	L	0	0	0	1
H	H	L	H	0	0	1	0
H	L	H	L	0	1	0	1

First of all, as far as the circuit design itself is concerned, the circuit design is simple and consists of integrated D flip-flop 74ls175. However, CP working pulse needs to be increased. By contrast, other types of flip-flops, such as basic RS flip-flops and JK flip-flops, can also be used in the design of scrambler circuits without additional CP working pulses, but many gate devices are used in complex circuits. Secondly, as for the application of flip-flop, as long as the memory unit is needed in the circuit design, different types of flip-flop can be used, such as register design, counter design and so on. In a word, the integrated trigger based on 74SL175 is efficient and easy to make.