FPGA Based Acceleration of Canny Edge Detection

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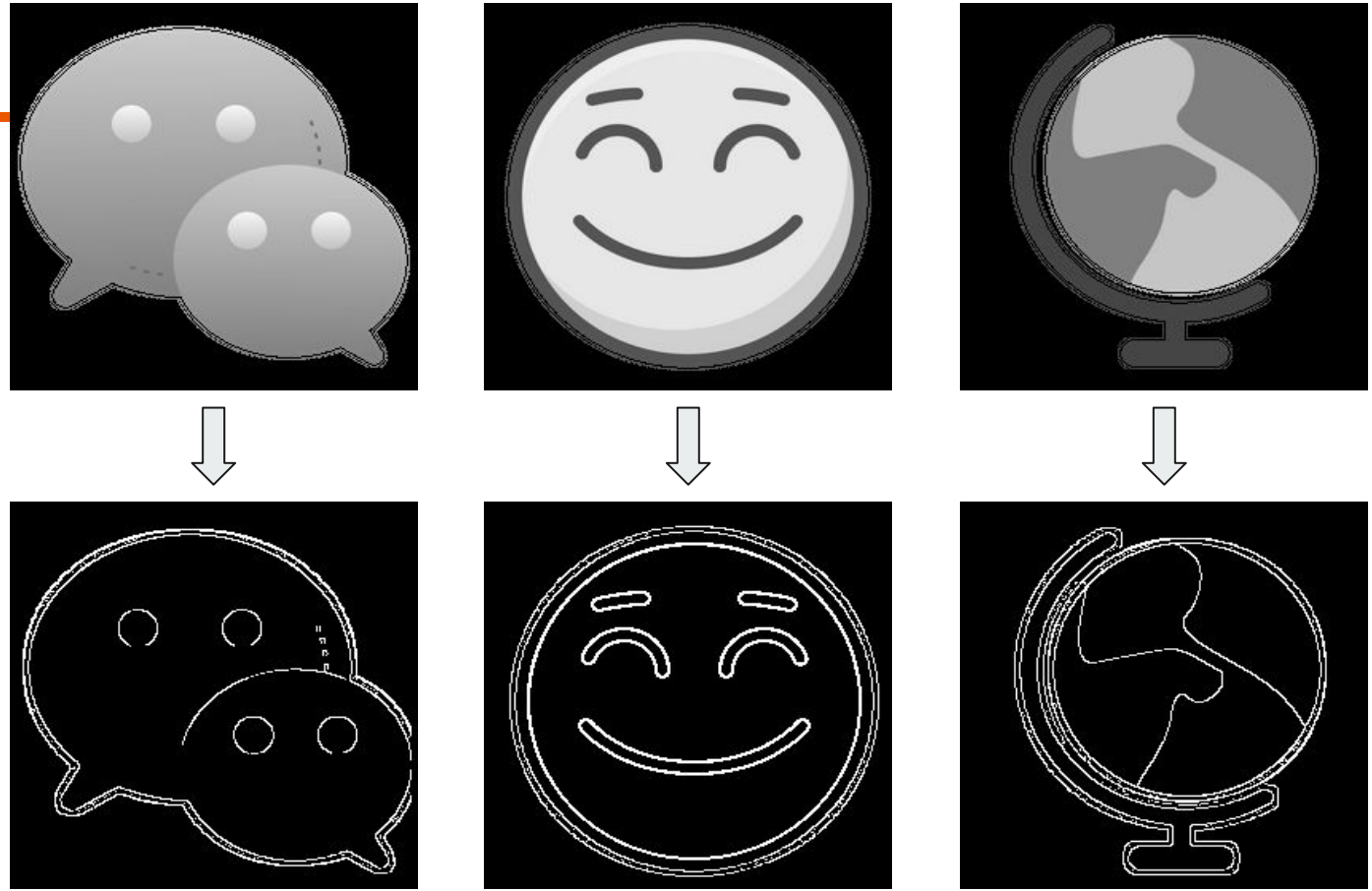
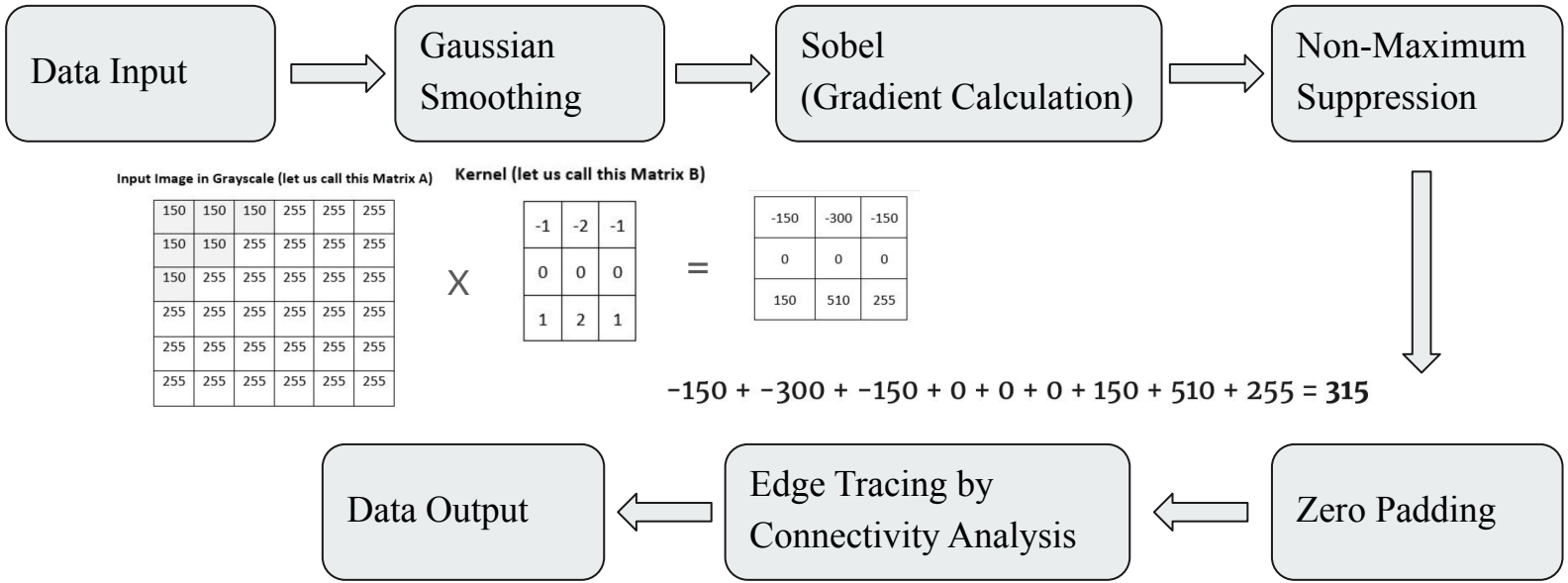
Design Overview

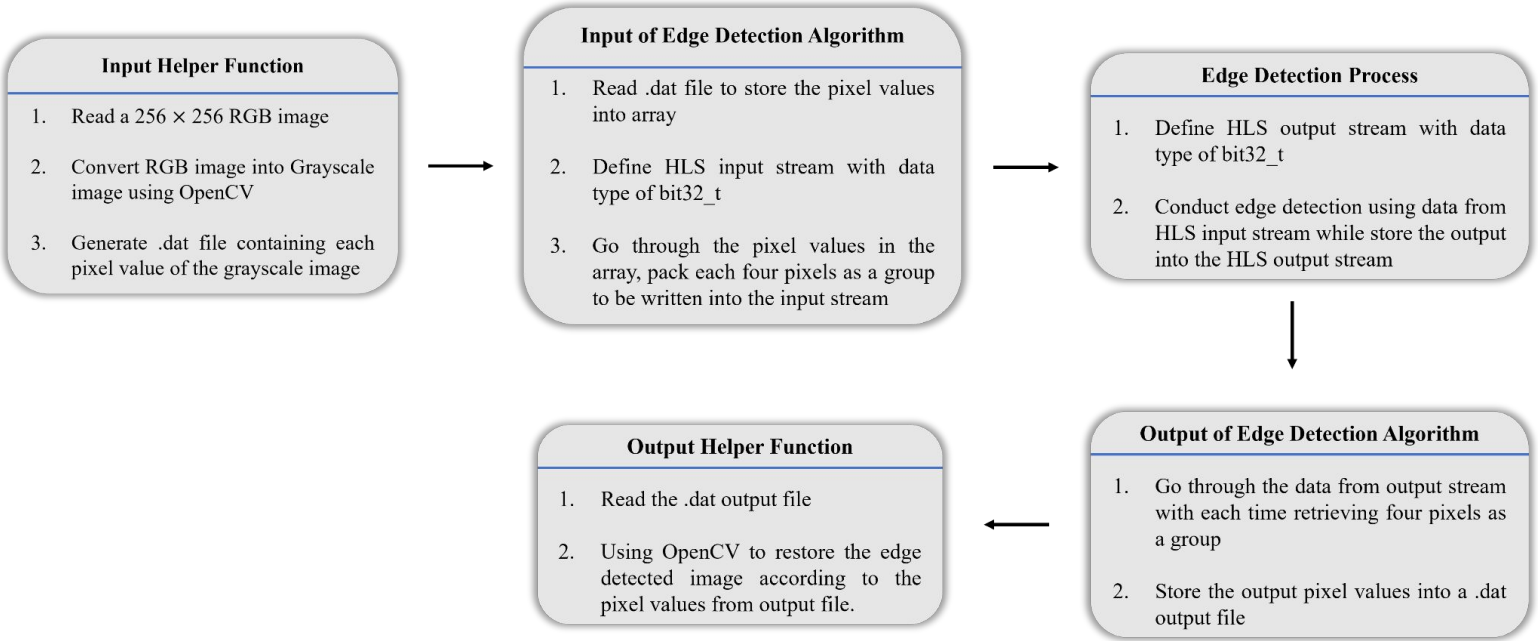
Our ultimate goal is to develop an Canny edge detection project that is not only optimized for performance but also implemented on the Zybo Z7-20 FPGA board.



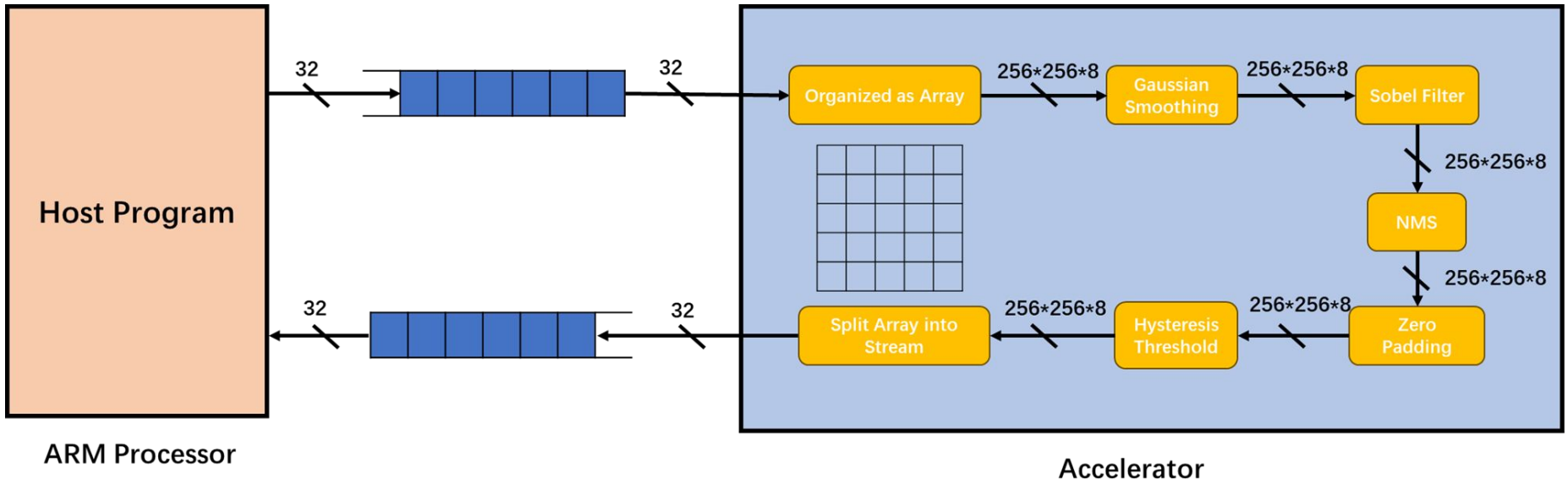
Background(Canny Edge Detection)



Implementation



Baseline Design



Optimization Strategy

Abundant Parallelism:

- Unroll
- Pipeline
- Reshape
- Partition

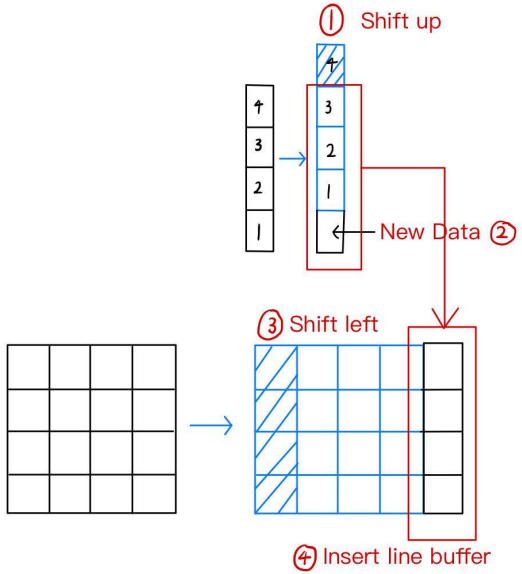
Distributed memory accesses:

- Line buffer
- Window buffer

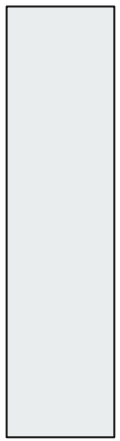
Data Stream with Custom Numeric Types

HLS Line/Window Buffer Design

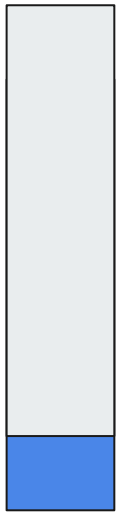
```
//-- line buffer
line_buf.shift_pixels_up(xi);

// write to line buffer
line_buf.insert_bottom_row(new_pixel, xi);

//-- window buffer
window_buf.shift_pixels_left();

// write to window buffer
for(int yw = 0; yw < KERNEL_SIZE; yw++) {
    window_buf.insert_pixel(line_buf.getval(yw,xi),yw,KERNEL_SIZE - 1);
}
```



HLS Line/Window Buffer Design



HLS Line/Window Buffer Design



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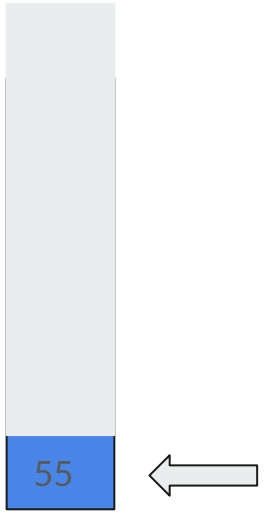

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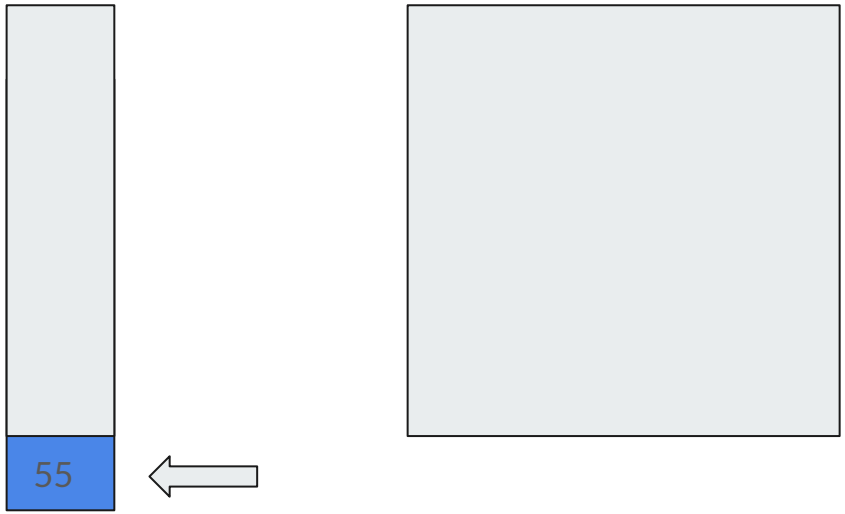

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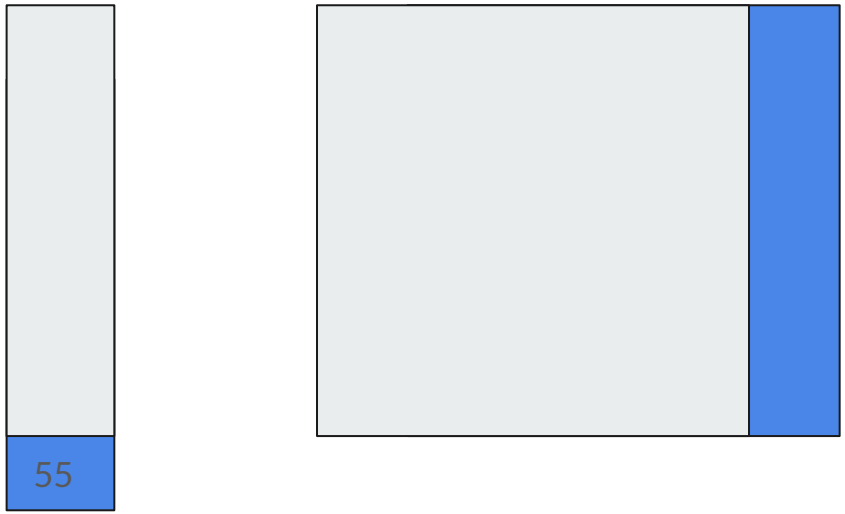

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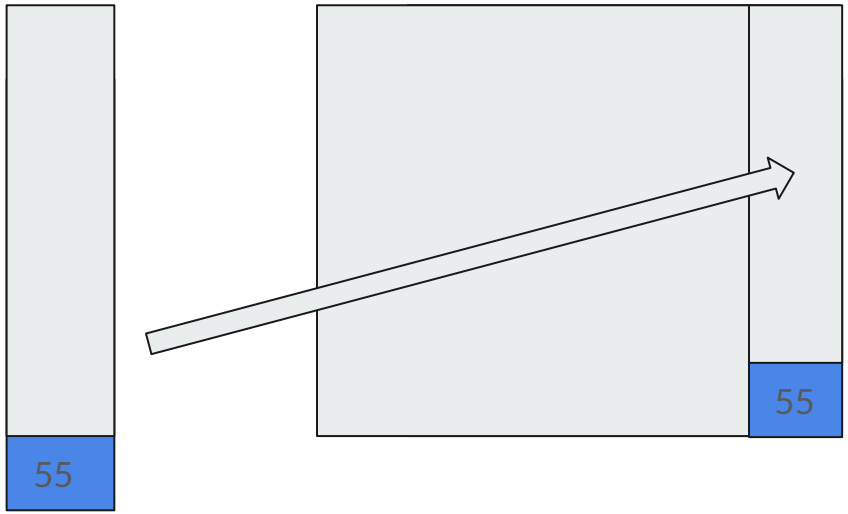
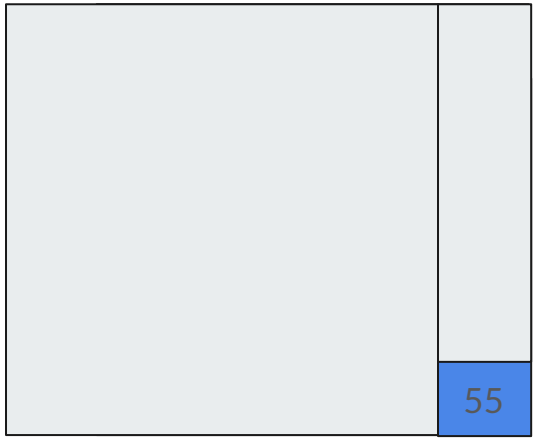
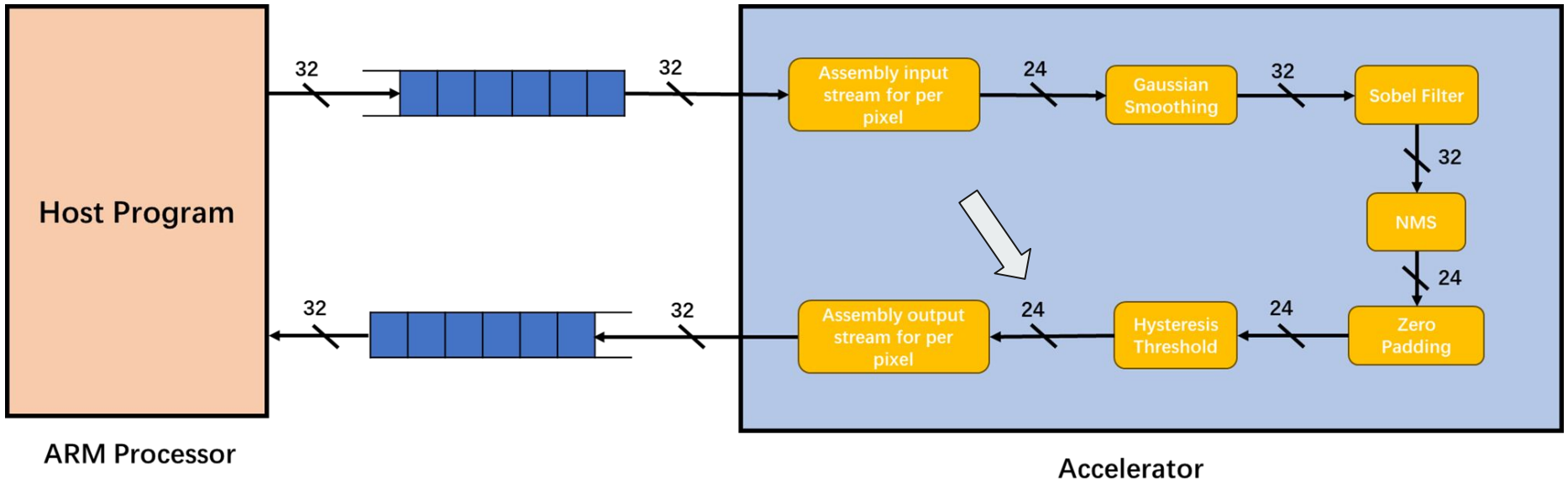


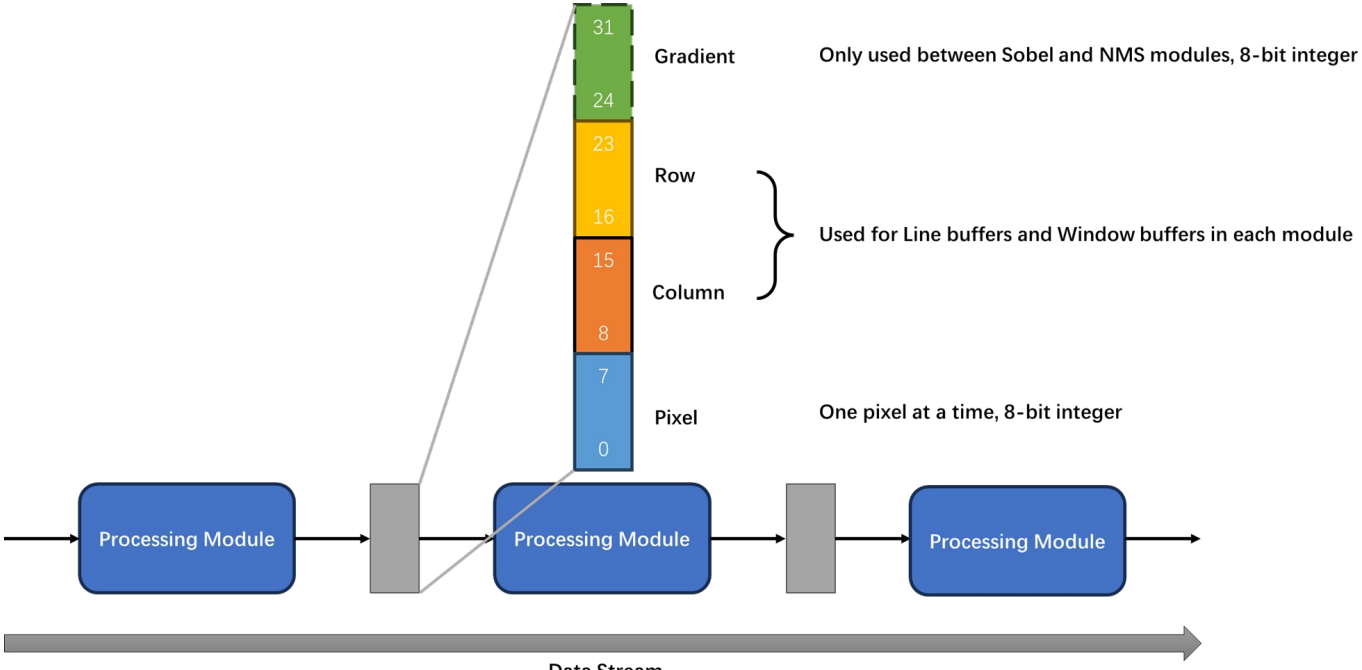
HLS Line/Window Buffer Design



Stream with HLS Line/Window Buffer Design



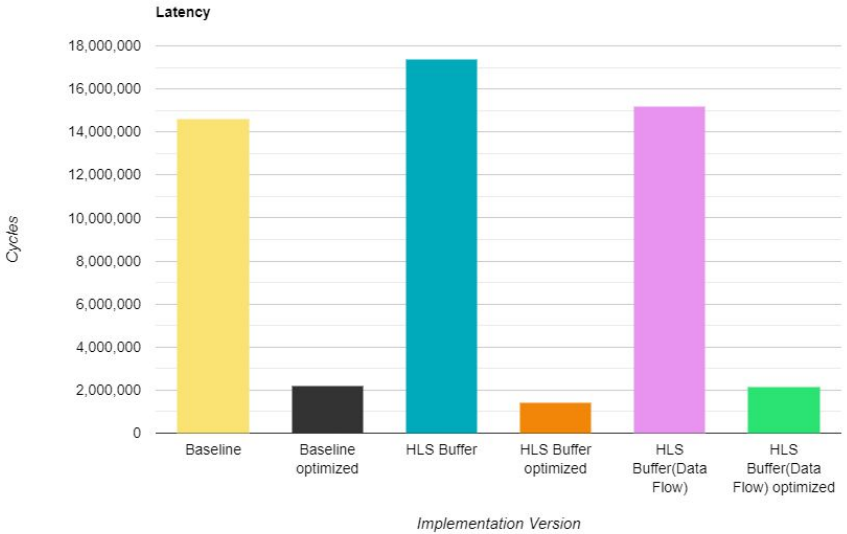
Stream with HLS Line/Window Buffer Design

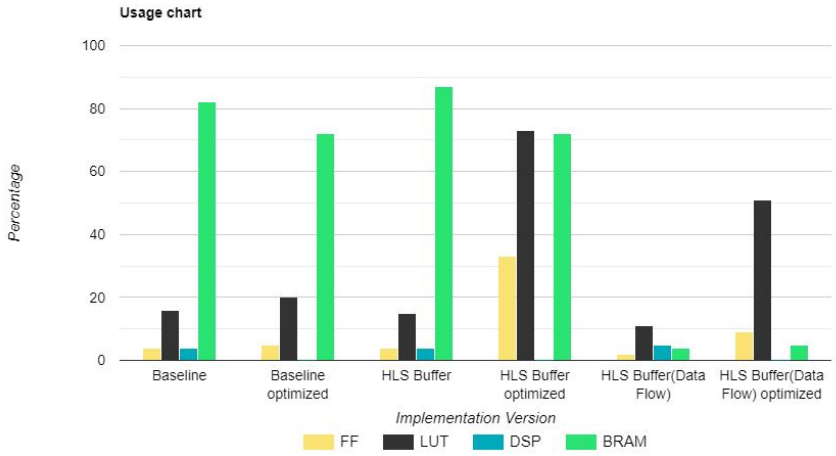


Resource Usage and Performance

	Latency(cycles)	FF	LUT	DSP	BRAM
Baseline	14599614	4	16	4	82
HLS Buffer	17370126	4	15	4	87
HLS Buffer(Data Flow)	15171585	2	11	5	4
Baseline optimized	2210652	5	20	0	72
HLS Buffer optimized	1391886	33	73	0	72
HLS Buffer(Data Flow) optimized	2146305	9	51	0	5

Resource Usage and Performance





Conclusion & Future Design

HLS acceleration

Line buffer & window buffer

Data Flow

Real-time Implementation