Yibo Liu

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Ph.D. new graduate from VLSI lab, University of California, Riverside. Specializing in machine learning acceleration techniques for VLSI reliability modeling and optimization. Experience on VLIS methodologies with machine learning applications, fault-tolerant computing, reliability-aware (EM, BTI, HCI, TBBD) design and management at both circuit and system levels. Experience on STA considering OCV and SSTA.

Education

Ph.D. in Electrical Engineering, University of California, Riverside. 09/2019 ~ Present

M.S. in Computer Engineering, University of California, Riverside. 09/2017 ~ 06/2019

B.E. in Electrical and Computer Engineering, Huazhong University of Science and Technology, China. 09/2013 ~ 07/2017

Techniques & Skills

Programing Skills: Python, TCL, C++, CUDA GPU programming, Verilog, Unix shell;

EDA Skills: Static Timing Analysis (STA), Timing ECO, Spice simulation.

EDA Tools: Synopsys Tools: PrimeTime, VCS, Design Compiler, HSpice; Vivado: HLS;

Machine Learning: Machine learning models, PyTorch, Data mining and information retrieval, Recommender system.

Others: HTML, JMP

Work Experience

R&D Intern - PrimeShield Team, Synopsys Inc. 06/2022 ~ 09/2022

Assist developing an ML accelerated workload-dependent aging-aware static timing analysis (STA) approach with Python and Tcl:

Assist the development of a machine learning-accelerated workload-dependent aging-aware STA approach. The new approach counts in DVFS usage by supporting the scalability of the BTI/HCI aging mission profiles, providing more accurate STA simulation on the actual path, and preventing overly pessimistic aging derates in the current PrimeTime tool. Meanwhile, a one-shot pipeline was developed with Python to overcome the productivity bottleneck from months to one day.

Ph.D. Research Focus on Machine Learning accelerated EDA Reliability Optimization

Machine Learning-Accelerated On-chip Power Grid EM-Aware Voltage Failure Fixing.

1. **Utilized Physics Informed Neural Network (PINN) to develop a model for solving partial differential equation based Korhonen equations, enabling efficient Electromigration(EM) stress analysis.**
2. **Apply generative AI models, including generative adversarial networks (GAN), variational autoencoder (VAE) and Vi-Transformer to fast predict the power grid EM-aware voltage.**
3. **Model EM-aware on-chip power grid fixing scenario as an optimization problem, accelerate the optimization solving process by Machine Learning model acquired sensitivity data (PyTorch AutoGradient) to skip the circuit analysis-based sensitivity calculation.**

Achievement: This ML-based strategy achieved over 100X speedup compared to the conventional matrix-solving approaches. Partial results have been published on TCAD 2022 and ISQED 2024.

Improving Aging (TDDB, BTI/HCI) Reliability On Machine Learning Accelerator with Approximate Computing

Improve machine learning accelerator aging reliability with approximate computing multiplier

1. **Proposed an approximate stochastic computing multiplier, which can compensate for the delay increase caused by BTI/HCI by reducing the demand computation cycles, and mitigating TDDB-induced errors by including error tolerance encoding.**
2. **Embedded the proposed approximate computing multiplier in the neural network accelerator, which enables the neural network accelerator to trade-off among throughput, accuracy, and power during the inference stage by adjusting the bit-width.**
3. **Start from neural network quantization by PyTorch, and implement hardware design on Vivado FPGA with C++.**

Improve device aging reliability and performance with approximate computing divider

1. **Propose a SOTA approximate stochastic computing divider design that achieves the highest accuracy (close to the theoretical upper limit) and the lowest energy cost among all divider designs.**
2. **Implement the proposed divider design with Verilog. Functionality test by Synopsys VCS, Synthesis ASIC design with Synopsys Design Compiler.**

Achievement: Results have been published on ISQED 2021, DAC 2021, TCAD 2024.

Selected Publications

1. **Y. Liu**, S. Yu, M. Tasnim and X. -D. Tan, "Fast and Scaled Counting-Based Stochastic Computing Divider Design", IEEE TCAD, 2024.
2. **Y. Liu**, and X. -D. Tan, "GridVAE: Fast Power Grid EM-Aware IR Drop Prediction and Fixing Accelerated by Variational AutoEncoder", 25th ISQED, 2024.
3. **Y. Liu**, S. Yu, S. Peng and S. X. -D. Tan, "Runtime Long-Term Reliability Management Using Stochastic Computing in Deep Neural Networks", 22nd ISQED, 2021.
4. H. Zhou*, **Y. Liu***, W. Jin, Sheldon X.-D. Tan, "GridNetOpt: Fast Full-Chip EM-Aware IR drop Constrained Power Grid Optimization via Deep Neural Networks", IEEE TCAD, 2022.
5. S. Yu, **Y. Liu**, Sheldon X.-D. Tan, "COSAIM: Counter-based Stochastic-behaving Approximate Integer Multiplier for Deep Neural Networks", DAC 2021.
6. S. Yu, **Y. Liu**, Sheldon X.-D. Tan, "Approximate Divider Design Based on Counting-Based Stochastic Computing Division", MLCAD 2021.