# Yichao Yuan

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## EDUCATION

**Shanghai Jiao Tong University**, Shanghai, China

University of Michigan – Shanghai Jiao Tong University Joint Institute (UM-SJTU JI)
B.S.E in Electrical and Computer Engineering
Overall GPA: 3.80/4.00 Sept. 2017 – Aug. 2021

**University of Michigan**, Ann Arbor, USA

M.S.E in Electrical and Computer Engineering Sept. 2021 – Apr. 2023
Ph.D. in Computer Science and Engineering Sept. 2023 – Now
Overall GPA: 4.00/4.00
Relevant coursework: EECS 470 Computer Architecture (A+), EECS 570 Parallel Computer Architecture (A), EECS 583 Advanced Compilers (A+)

## RESEARCH INTERESTS

Computer Architecture, GPU programming, hardware-software co-design, accelerator design.

## PUBLICATIONS

**Y. Yuan**, A. Iyer, L. Ma, N. Talati, "Vortex: Overcoming Memory Capacity Limitations in GPU-Accelerated Large-Scale Data Analytics" **(Under Review by VLDB 2025)**

J. Pavon, I. Valdivieso, C. Morales, C. Hernandez, M. Aslan, J. Lindegger, **Y. Yuan**, R. Bagué, M. Alser, O. Mutlu, S. Marco-Sola, O. Ergin, N. Talati, M. Valero, O. Unsal, A. Cristal, "QUETZAL: Vector Acceleration Framework for Modern Genome Sequence Analysis Algorithms," at 2024 International Symposium on Computer Architecture **ISCA 2024**.

**Y. Yuan**, H. Ye, S. Vedula, W. Kaza, and N. Talati, "Everest: GPU-Accelerated System for Mining Temporal Motifs," at International Conference on Very Large Databases **VLDB 2024**.

N. Talati, H. Ye, S. Vedula, K-Y Chen, Y. Chen, D. Liu, **Y. Yuan**, D. Blaauw, A. Bronstein, T. Mudge, and R. Dreslinski, "Mint: An Accelerator For Mining Temporal Motifs," accepted to appear at the 55th IEEE/ACM International Symposium on Microarchitecture **MICRO 2022**.

## RELEVANT PROJECTS

**Assessing the Capabilities of Large Language Model in Adaptive Video Streaming**

*University of Michigan, EECS 598 Final Project* Feb. 2024 – Apr. 2024
Design and implement a pipeline to access the capabilities of Large Language Model in Adaptive Video Streaming. Explore different prompt designs and language models. Compare the performance of LLM-based solution with classic rule-based mothods.

**Out-of-Order Superscalar Processor Design**

*University of Michigan, EECS 470 Final Project* Oct. 2021 – Dec. 2021
Design and implement a parameterized out-of-order superscalar processor with SystemVerilog. The superscalar width and other parameters are configurable. Implement additional features for higher performance. Propose the high-level design and organize the team. Also, be responsible for implementation details, integration, and testing.

## TECHNICAL SKILLS

Programming Language/ Tools: C, C++, Python, CUDA, ROCm
Familiar with CPU/GPU architecture and CPU/GPU code optimization.