# Yichao Yuan

E-mail: yichaoy@umich.edu Phone: (+1) 734-450-4291

## EDUCATION

**Shanghai Jiao Tong University**, Shanghai, China

University of Michigan – Shanghai Jiao Tong University Joint Institute (UM-SJTU JI)
B.S.E in Electrical and Computer Engineering
Overall GPA: 3.80/4.00 Sept. 2017 – Aug. 2021

**University of Michigan**, Ann Arbor, USA

M.S.E in Electrical and Computer Engineering
Overall GPA: 4.00/4.00 Sept. 2021 – May. 2023
Ph.D. in Computer Science and Engineering
Aug. 2023 – Now
Graduate Student Research Assistant (GSRA)
May. 2022 – Now
Relevant coursework: EECS 470 Computer Architecture (A+), EECS 570 Parallel Computer Architecture (A), EECS 583 Advanced Compilers (A+)

## RESEARCH INTERESTS

Computer Architecture, hardware-software co-design, accelerator design.

## PUBLICATION

**Y. Yuan**, H. Ye, S. Vedula, W. M Kaza, N. Talati, " Everest: GPU-Accelerated System For Mining Temporal Motifs," Proceedings of the VLDB Endowment, Vol. 17, No. 2, **VLDB 2024**.

N. Talati, H. Ye, S. Vedula, K-Y Chen, Y. Chen, D. Liu, **Y. Yuan**, D. Blaauw, A. Bronstein, T. Mudge, and R. Dreslinski, "Mint: An Accelerator For Mining Temporal Motifs," the 55th IEEE/ACM International Symposium on Microarchitecture **MICRO 2022**.

## RELEVANT PROJECTS

**Prefetching for Graphs on Manycore Architecture**

*University of Michigan, Shepherd Group* Oct. 2021 – Now
Ongoing project. Discuss project specifications with colleagues. Modeling the designed techniques. Aim at designing prefetching methods for graphs on manycore architecture.

**Everest: GPU-Accelerated System For Mining Temporal Motifs**

*University of Michigan, Shepherd Group* May. 2021 – Oct. 2023
Propose a GPU-Accelerated System for Mining Temporal Motifs. Everest includes various techniques to speed up the workload against a baseline GPU implementation by 19x. This work is published in VLDB 2024. Part of the result is also included in a top-tier conference publication at MICRO 2022.

**Out-of-Order Superscalar Processor Design**

*University of Michigan, EECS 470 Final Project* Oct. 2021 – Dec. 2021
Design and implement a parameterized out-of-order superscalar processor with SystemVerilog. The superscalar width and other parameters are configurable. Implement additional features for higher performance. Propose the high-level design and organize the team. Also, be responsible for implementation details, integration, and testing.

## EXTRACURRICULAR ACTIVITIES

**Teaching Assistant for VLSI Design**
*Shanghai Jiao Tong University* May. 2021 – Aug. 2021
**Teaching Assistant for Semiconductor Devices**
*Shanghai Jiao Tong University* Sept. 2019 – Dec. 2019

## TECHNICAL SKILLS

*Programming languages and tools*
C, C++, Python, CUDA, Julia, SystemVerilog, Matlab, LLVM, Murphi, Git, Design Compiler, Nsight Compute, x86 SIMD, LaTeX, RISCV Spike, Vivado, Verilator

## REFERENCES

Prof. Ronald Dreslinski, Morris Wellman Faculty Development Associate Professor, Computer Science and Engineering, University of Michigan, Ann Arbor, MI. E-mail: rdreslin@umich.edu

Prof. Trevor Mudge, Bredt Family Professor, Computer Science and Engineering, University of Michigan, Ann Arbor, MI. E-mail: tnm@umich.edu

Dr. Nishil Talati, Assistant Research Scientist (Research Faculty), Computer Science and Engineering, University of Michigan, Ann Arbor, MI. E-mail: talatin@umich.edu