

Example Circuit A — Simple Circuit

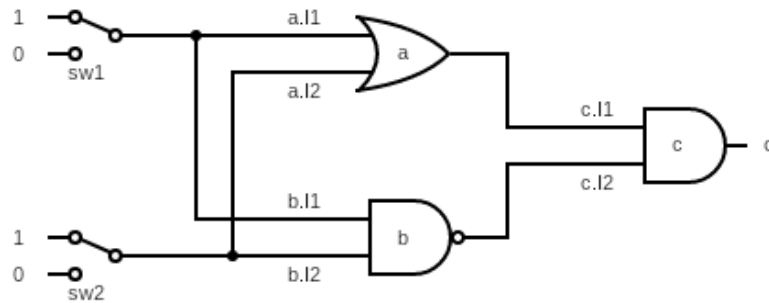


Figure 1: XOR Gate

```

1      #Example circuit - Simple circuit (As per first interim report);
2      #XOR gate;
3
4      devices(
5          a is OR;
6          b is NAND;
7          c is AND;
8          sw1, sw2 are SWITCH;
9      )
10
11     initialise(
12         sw1, sw2 are HIGH;
13         a, b, c have 2 inputs;
14     )
15
16     connections(
17         a(
18             sw1 is connected to a.I1;
19             sw2 is connected to a.I2;
20         )
21
22         b(
23             sw1 is connected to b.I1;
24             sw2 is connected to b.I2;
25         )
26
27         c(
28             a is connected to c.I1;
29             b is connected to c.I2;
30         )
31     )
32
33     monitors(
34         c;
35     )

```

Example Circuit B — Complex Circuit

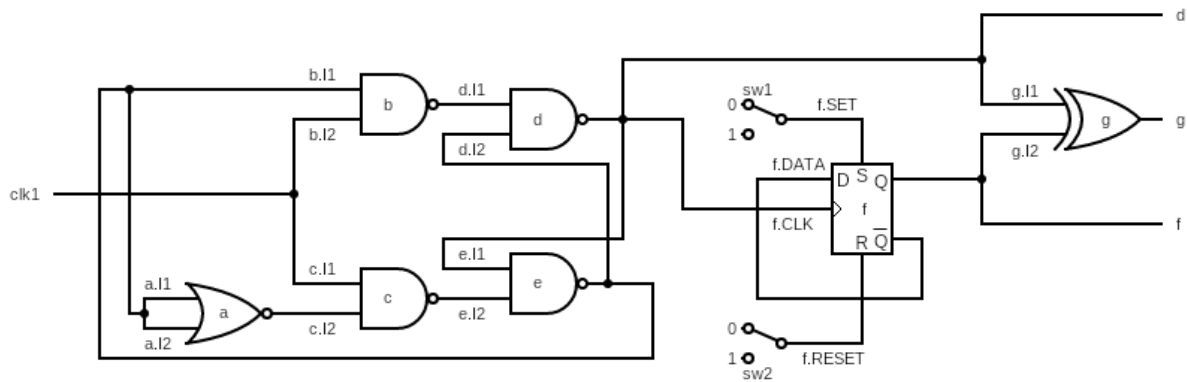


Figure 2: 2 Bit Counter with Outputs XOR

```

1  #Example circuit - Complex circuit (As per first interim report);
2  #2 bit counter with outputs XOR;
3
4  devices(
5      a is NOR;
6      b, c, d, e are NAND;
7      f is DTYPE;
8      g is XOR;
9      sw1, sw2 are SWITCH;
10     clk1 is CLOCK;
11 )
12
13 initialise(
14     a, b, c, d, e, g have 2 inputs;
15     sw1, sw2 are LOW;
16     clk1 cycle length 5;
17 )
18
19 connections(
20     a(
21         e to a.I1;
22         e to a.I2;
23     )
24
25     b(
26         e to b.I1;
27         clk1 to b.I2;
28     )
29
30     c(
31         clk1 to c.I1;

```

```

32         a to c.I2;
33     )
34
35     d(
36         b to d.I1;
37         e to d.I2;
38     )
39
40     e(
41         d to e.I1;
42         c to e.I2;
43     )
44
45     f(
46         f.QBAR to f.DATA;
47         d to f.CLK;
48         sw1 to f.SET;
49         sw2 to f.CLEAR;
50     )
51
52     g(
53         d to g.I1;
54         f.Q to g.I2;
55     )
56 )
57
58 monitors(
59     d, f.Q, g;
60 )

```

Example Circuit C — 50 Switches

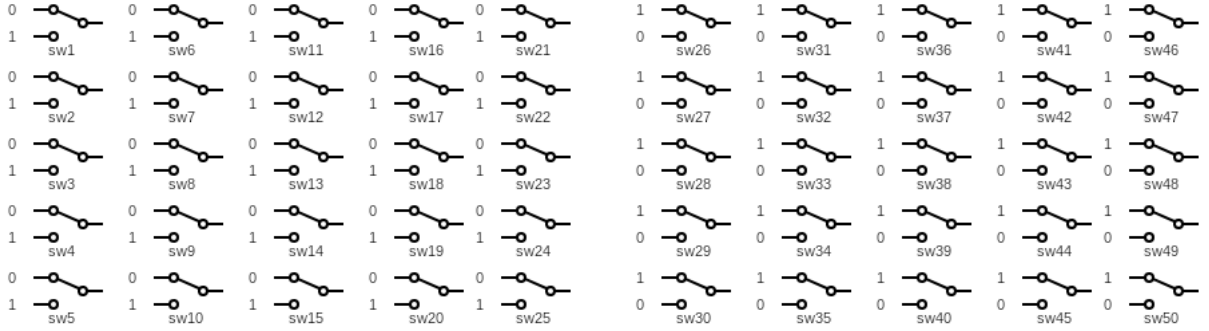


Figure 3: 50 Switches

```

1      #Example circuit - 50 switches;
2
3      devices(
4          sw1, sw2, sw3, sw4, sw5, sw6, sw7, sw8, sw9, sw10,
5          sw11, sw12, sw13, sw14, sw15, sw16, sw17, sw18, sw19, sw20,
6          sw21, sw22, sw23, sw24, sw25, sw26, sw27, sw28, sw29, sw30,
7          sw31, sw32, sw33, sw34, sw35, sw36, sw37, sw38, sw39, sw40,
8          sw41, sw42, sw43, sw44, sw45, sw46, sw47, sw48, sw49, sw50 are SWITCH;
9      )
10
11     initialise(
12         sw1, sw2, sw3, sw4, sw5, sw6, sw7, sw8, sw9, sw10,
13         sw11, sw12, sw13, sw14, sw15, sw16, sw17, sw18, sw19, sw20,
14         sw21, sw22, sw23, sw24, sw25 are LOW;
15         sw26, sw27, sw28, sw29, sw30, sw31, sw32, sw33, sw34, sw35,
16         sw36, sw37, sw38, sw39, sw40, sw41, sw42, sw43, sw44, sw45,
17         sw46, sw47, sw48, sw49, sw50 are HIGH;
18     )
19
20     connections(
21     )
22
23     monitors(
24         sw1, sw2, sw3, sw4, sw5, sw6, sw7, sw8, sw9, sw10,
25         sw11, sw12, sw13, sw14, sw15, sw16, sw17, sw18, sw19, sw20,
26         sw21, sw22, sw23, sw24, sw25, sw26, sw27, sw28, sw29, sw30,
27         sw31, sw32, sw33, sw34, sw35, sw36, sw37, sw38, sw39, sw40,
28         sw41, sw42, sw43, sw44, sw45, sw46, sw47, sw48, sw49, sw50;
29     )
30

```

Example Circuit D — SR Bistable

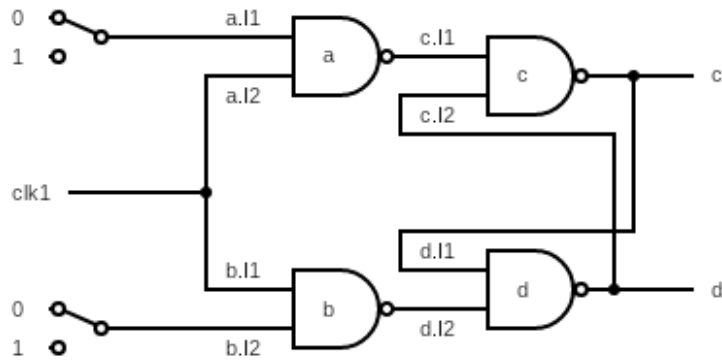


Figure 4: SR Bistable

```

1  #Example circuit - SR bistable;
2
3  devices(
4      a, b, c, d are NAND;
5      sw1, sw2 are SWITCH;
6      clk1 is CLOCK;
7  )
8
9  initialise(
10     sw1, sw2 are LOW;
11     a, b, c, d have 2 inputs;
12     clk1 cycle 5;
13 )
14
15 connections(
16     a(
17         sw1 to a.I1;
18         clk1 to a.I2;
19     )
20
21     b(
22         clk1 to b.I1;
23         sw2 to b.I2;
24     )
25
26     c(
27         a to c.I1;
28         d to c.I2;
29     )
30
31     d(
32         c to d.I1;

```

```
33         b to d.I2;
34     )
35 )
36
37 monitors(
38     c, d;
39 )
```

Example Circuit E — Divide by 3 Circuit

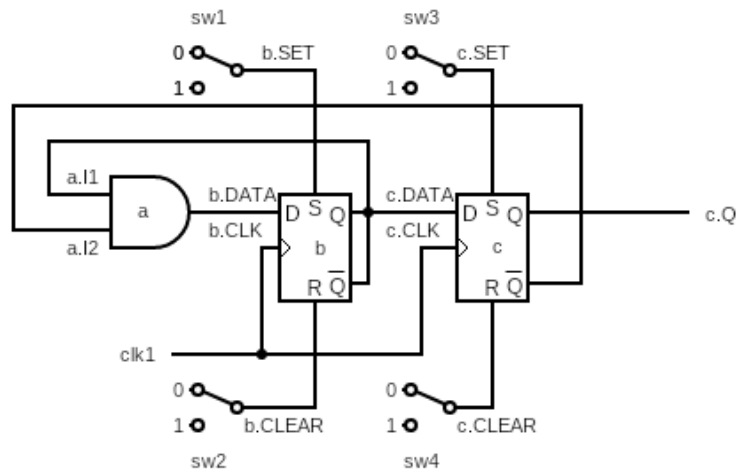


Figure 5: Divide by 3 Circuit

```

1  #Example circuit - divide (clock frequency) by 3;
2
3  devices(
4      a is AND;
5      b, c are DTYPE;
6      sw1, sw2, sw3, sw4 are SWITCH;
7      clk1 is CLOCK;
8  )
9
10 initialise(
11     a has 2 inputs;
12     sw1, sw2, sw3, sw4 are LOW;
13     clk1 cycle 9;
14 )
15
16 connections(
17     a(
18         b.QBAR to a.I1;
19         c.QBAR to a.I2;
20     )
21
22     b(
23         a to b.DATA;
24         clk1 to b.CLK;
25         sw1 to b.SET;
26         sw2 to b.CLEAR;
27     )
28
29     c(

```

```
30         b.Q to c.DATA;
31         clk1 to c.CLK;
32         sw3 to c.SET;
33         sw4 to c.CLEAR;
34     )
35 )
36
37 monitors(
38     c.Q;
39 )
```


Example Circuit F — Blank Circuit

```
1      #Example circuit - Blank circuit;
2
3      devices(
4      )
5
6      initialise(
7      )
8
9      connections(
10     )
11
12     monitors(
13     )
```

Alternatively, a blank .txt file will also suffice