Example Circuit A — Simple Circuit

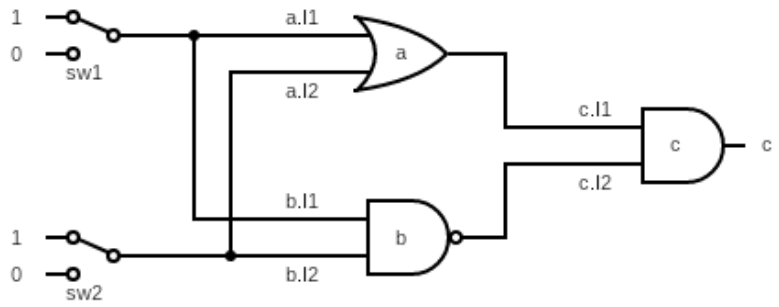

Figure 1: XOR Gate

```
#Example circuit - Simple circuit (As per first interim report);
#XOR gate;

devices(
    a is OR;
    b is NAND;
    c is AND;
    sw1, sw2 are SWITCH;
)

initialise(
    sw1, sw2 are HIGH;
    a, b, c have 2 inputs;
)

connections(
        sw1 is connected to a.I1;
        sw2 is connected to a.I2;

        sw1 is connected to b.I1;
        sw2 is connected to b.I2;

        a is connected to c.I1;
        b is connected to c.I2;
)

monitors(
    c;
)
```

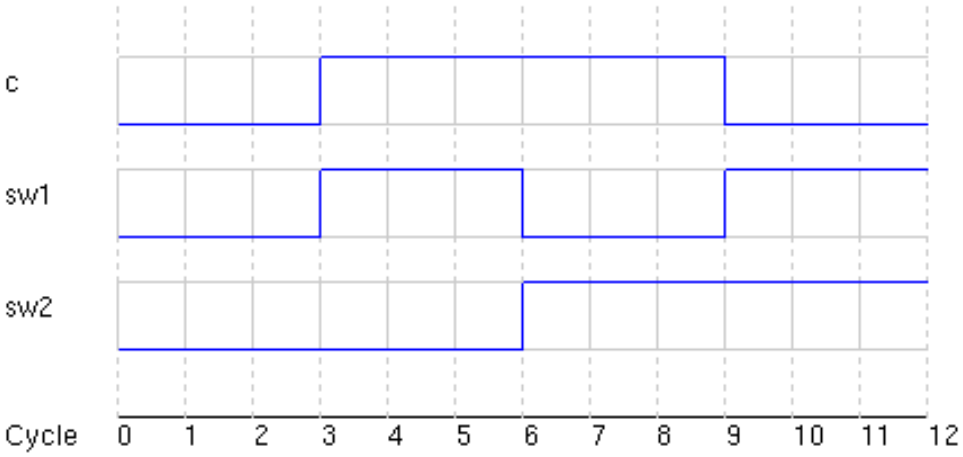

Figure 2: XOR Gate Output

Example Circuit B — Complex Circuit

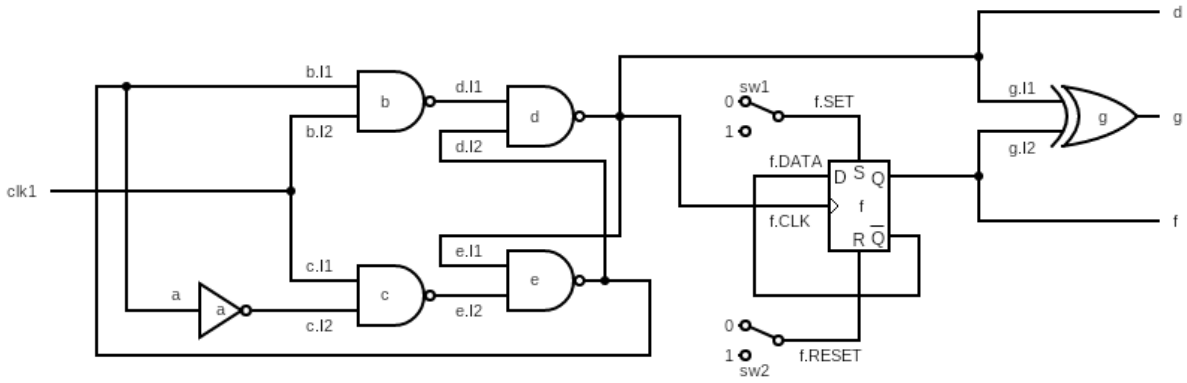

Figure 3: 2 Bit Counter with Outputs XOR

```
#Example circuit - Complex circuit (As per first interim report);
#2 bit counter with outputs XOR;

devices(
    a is NOT;
    b, c, d, e are NAND;
    f is DTYPE;
    g is XOR;
    sw1, sw2 are SWITCH;
    clk1 is CLOCK;
)

initialise(
    b, c, d, e, g have 2 inputs;
    sw1, sw2 are LOW;
    clk1 cycle length 5;
)

connections(
        e to a;

        e to b.I1;
        clk1 to b.I2;

        clk1 to c.I1;
        a to c.I2;

        b to d.I1;
        e to d.I2;

        d to e.I1;
```

```
32              c to e.I2;
33
34              f.QBAR to f.DATA;
35              d to f.CLK;
36              sw1 to f.SET;
37              sw2 to f.CLEAR;
38
39              d to g.I1;
40              f.Q to g.I2;
41      )
42
43      monitors(
44          d, f.Q, g;
45      )
```

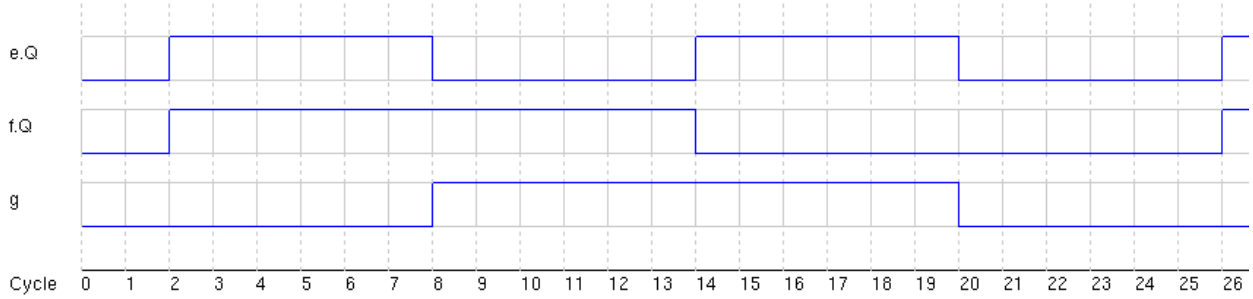

Figure 4: 2 Bit Counter Output

Example Circuit C — SR Bistable

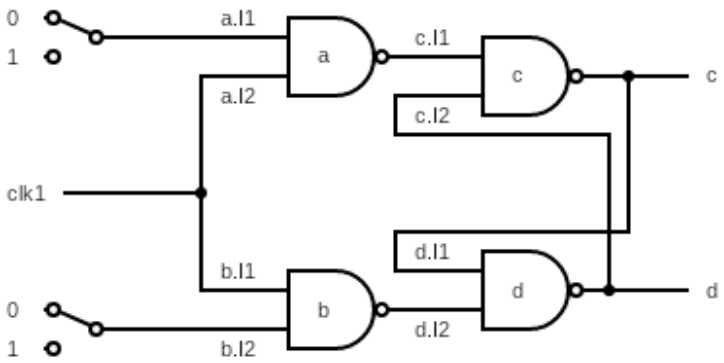

Figure 5: SR Bistable

```
#Example circuit - SR bistable;

devices(
    a, b, c, d are NAND;
    sw1, sw2 are SWITCH;
    clk1 is CLOCK;
)

initialise(
    sw1, sw2 are LOW;
    a, b, c, d have 2 inputs;
    clk1 cycle 5;
)

connections(
        sw1 to a.I1;
        clk1 to a.I2;

        clk1 to b.I1;
        sw2 to b.I2;

        a to c.I1;
        d to c.I2;

        c to d.I1;
        b to d.I2;
)

monitors(
    c, d;
)
```

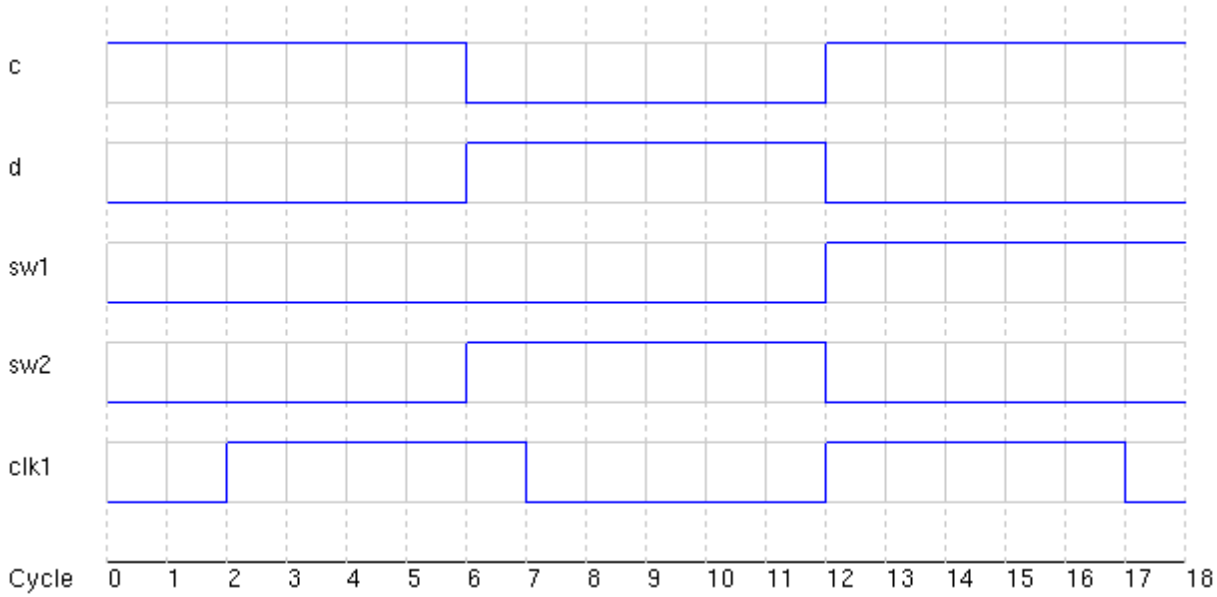

Figure 6: SR Bistable Output

Example Circuit D — Divide by 3 Circuit

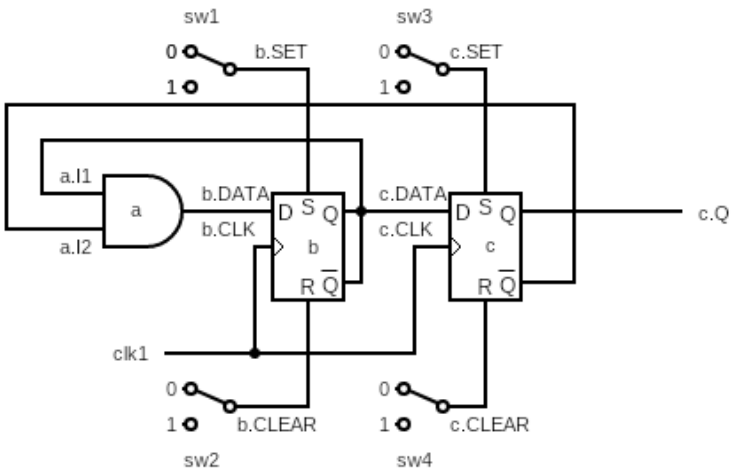

Figure 7: Divide by 3 Circuit

```
#Example circuit - divide (clock frequency) by 3;

devices(
    a is AND;
    b, c are DTYPE;
    sw1, sw2, sw3, sw4 are SWITCH;
    clk1 is CLOCK;
)

initialise(
    a has 2 inputs;
    sw1, sw2, sw3, sw4 are LOW;
    clk1 cycle 9;
)

connections(
        b.QBAR to a.I1;
        c.QBAR to a.I2;

        a to b.DATA;
        clk1 to b.CLK;
        sw1 to b.SET;
        sw2 to b.CLEAR;

        b.Q to c.DATA;
        clk1 to c.CLK;
        sw3 to c.SET;
        sw4 to c.CLEAR;
)
```

```
30
31      monitors(
32          c.Q;
33      )
```

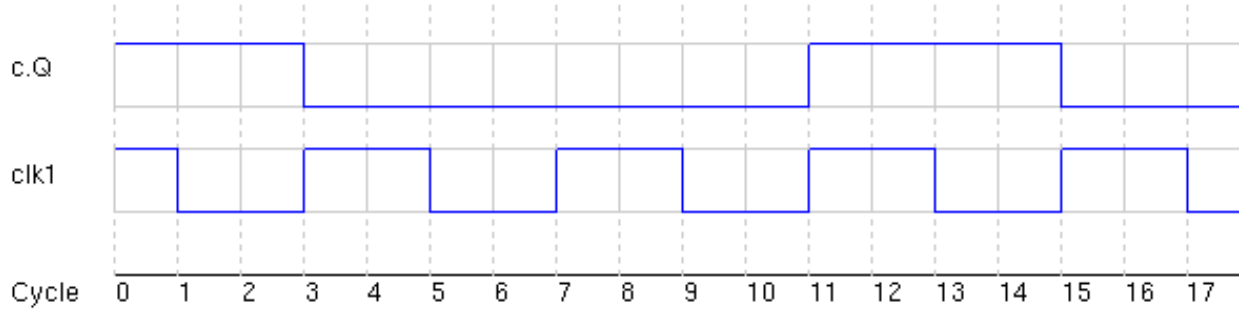

Figure 8: Divide by 3 Circuit Output

Example Circuit E — Ring Oscillator

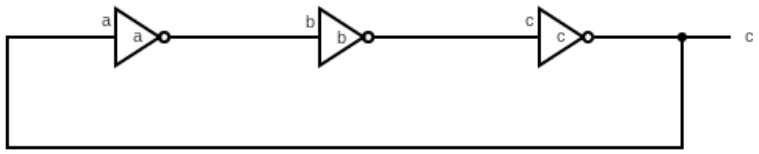

Figure 9: Ring Oscillator

```
#Example circuit - Ring Oscillator;

devices(
    a, b, c are NOT;
)

initialise(
)

connections(
        c to a;

        a to b;

        b to c;
)

monitors(
    c;
)
```

Note that this circuit will not be able to be simulated as it involves oscillating signals.