EECT 7325

PROJECT #2: 4*4 Bit Multiplier

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I. Introduction

The project 2 indicates to design the layout manually by using the cells we designed in the project 1 and do any type of design. Moreover, the size of the layout is probably about 100 cells. After the design, the correct simulation result is necessary and LVS and DRC result of the final layout should show no error. I chose a 4*4 bit multiplier for my topic and it was composed of 2 bits full adder and 4 bits full adder. The total layout are about 140 cells.

II. 2 Bit Full Adder

Layout

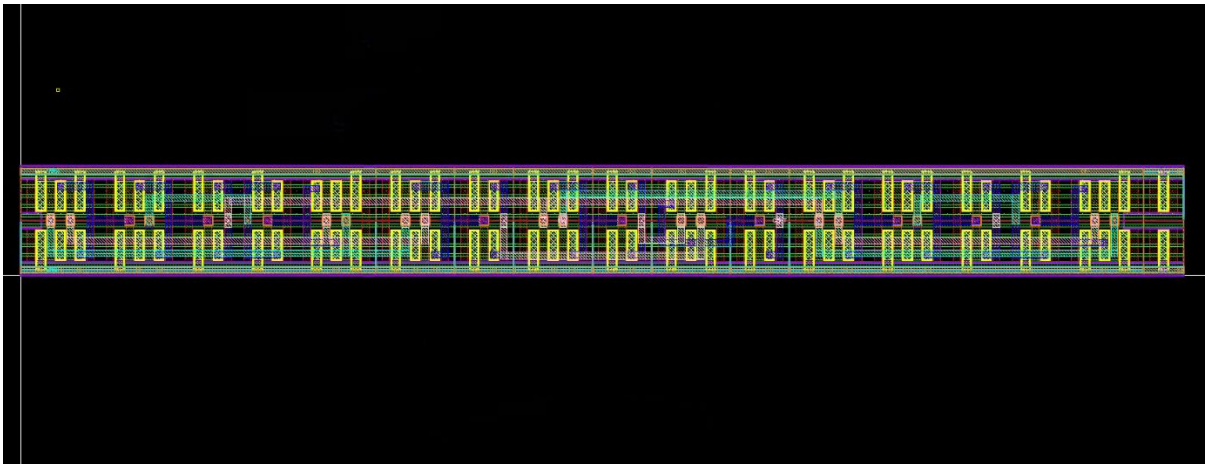

Fig 1-1. 2Bit Full Adder layout

Template Table

PMOS Width	NMOS Width	Cell Height	Cell Width	Cell Area
0.081um(3 Fins)	0.081um(3 Fins)	0.288um	3.078um	0.89um^2
Total Cells				
8 (2 XOR+ 2 NAND + 1NOR +3 Inverter)				

Schematic & Simulation

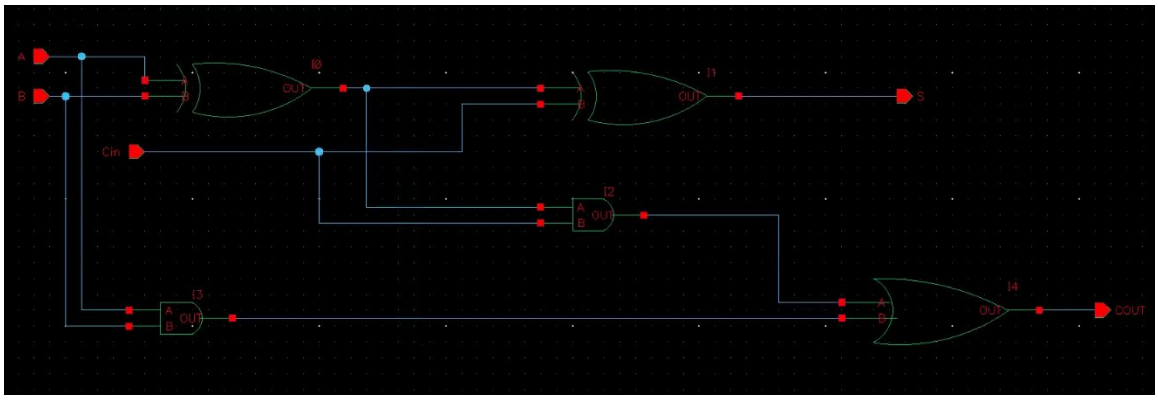

Fig 1-2. 2 Bit Full Adder Schematic

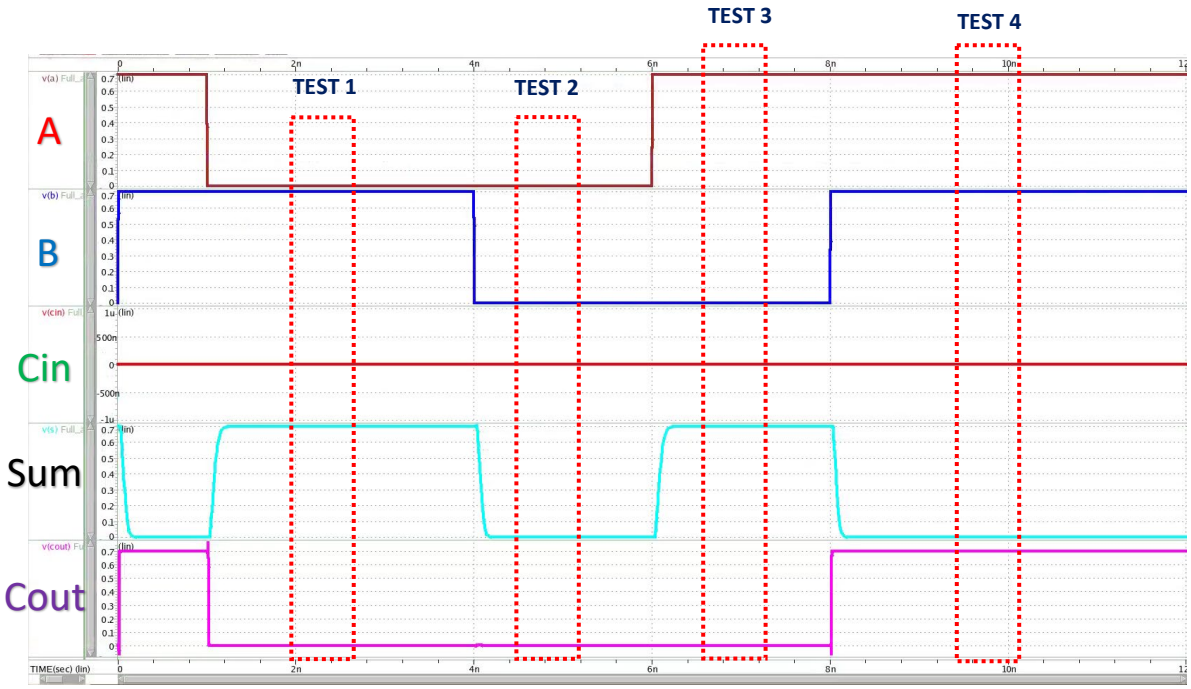

Fig 1-3. 2 Bit Full Adder Simulation

Testing Table

	TEST 1	TEST 2	TEST 3	TEST 4
Input	A : 0 B : 1	A : 0 B : 0	A : 1 B : 0	A : 1 B : 1
Value	1	0	1	2
Output	Sum:1 Cout:0	Sum:0 Cout:0	Sum:1 Cout:0	Sum:0 Cout:1

III. 4 Bit Full Adder

Layout

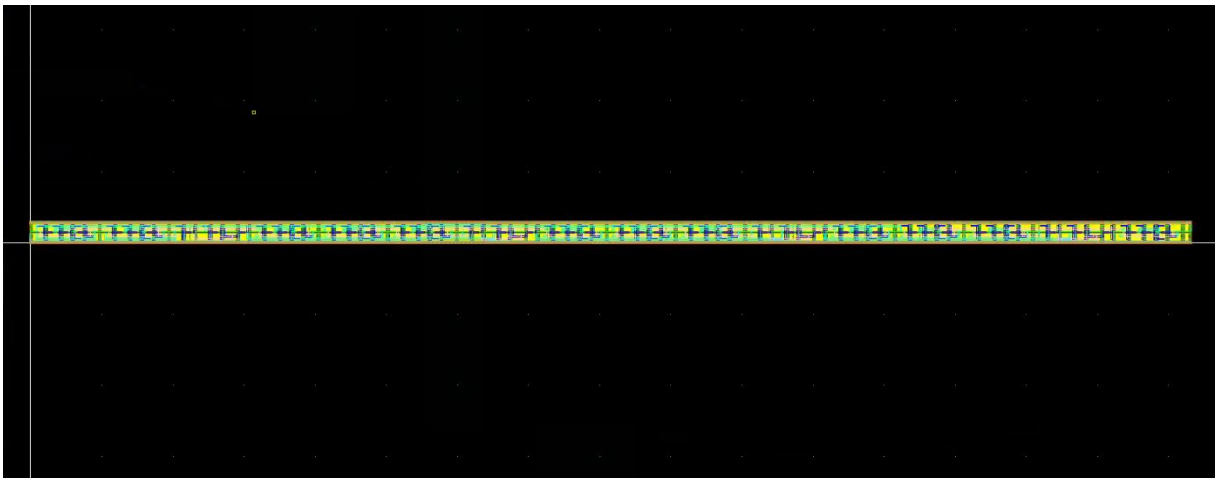

Fig 2-1. 4 Bit Full Adder Layout

Template Table

PMOS Width	NMOS Width	Cell Height	Cell Width	Cell Area
0.081um(3 Fins)	0.081um(3 Fins)	0.288um	16.2um	4.66um^2
Total Cells				
36 (4 XOR + 4 2bits full adder)				

Schematic & Simulation

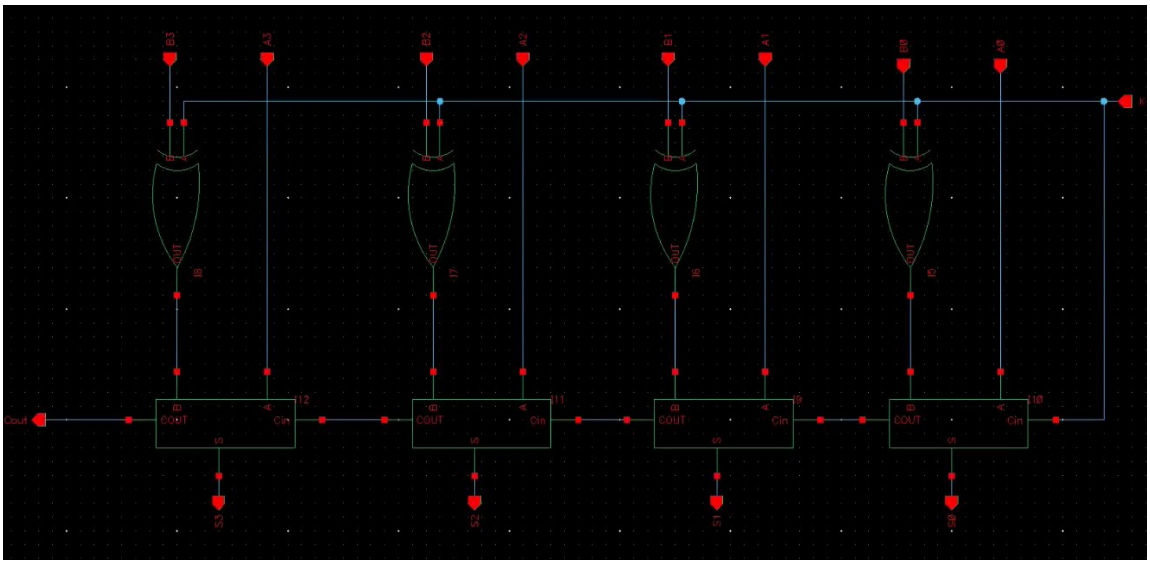

Fig 2-2. 4 Bit Full Adder Schematic

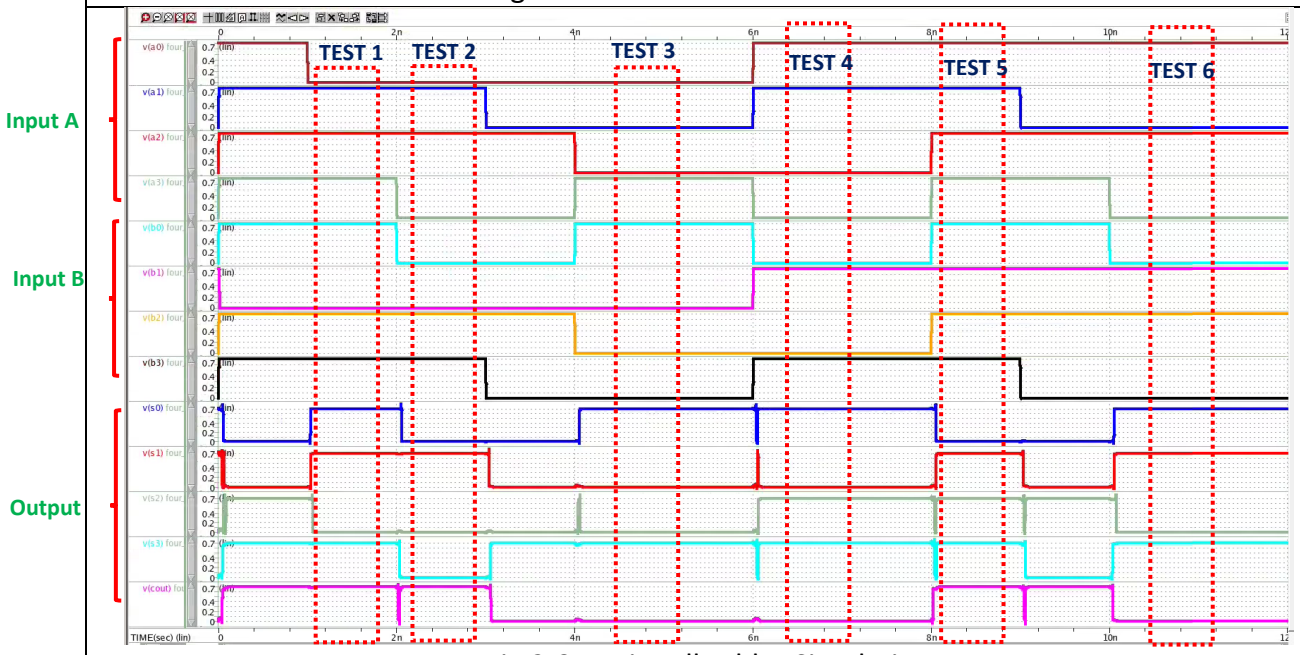

Fig 2-3. 4 Bit Full Adder Simulation

Testing Table

	TEST 1	TEST 2	TEST 3	TEST 4	TEST 5	TEST 6
Input	A : 1110 B : 1101	A : 0110 B : 1100	A : 1000 B : 0001	A : 0011 B : 1010	A : 1111 B : 1111	A : 0101 B : 0110
Value	14+13 = 27	6+12 = 18	8+1 = 9	3+10 = 13	15+15 = 30	5+6 = 11
Output	1011,Cout=1 =11+16= 27	0010,Cout=1 =2+16=18	1001,Cout=0 =9	1101,Cout=0 =13	1110,Cout=1 =14+16=30	1011,Cout=0 =11

IV. 4*4 Bit Multiplier

Layout

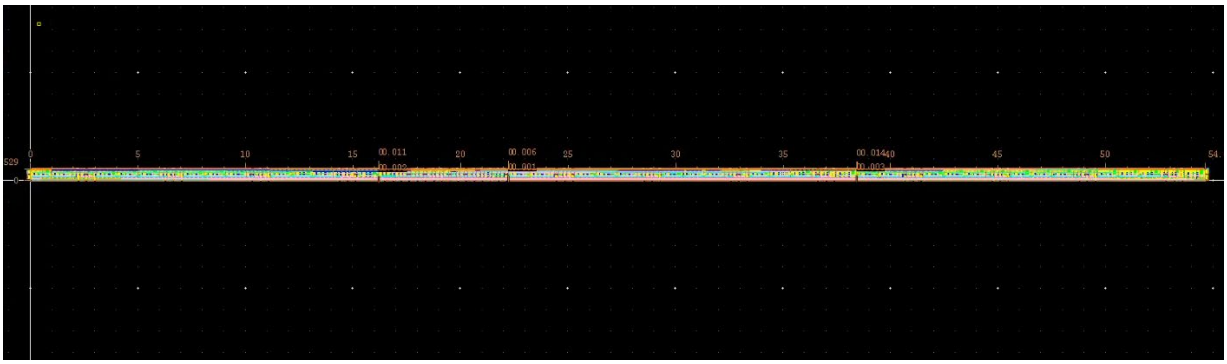

Fig 3-1. 4*4 Bit Multiplier layout

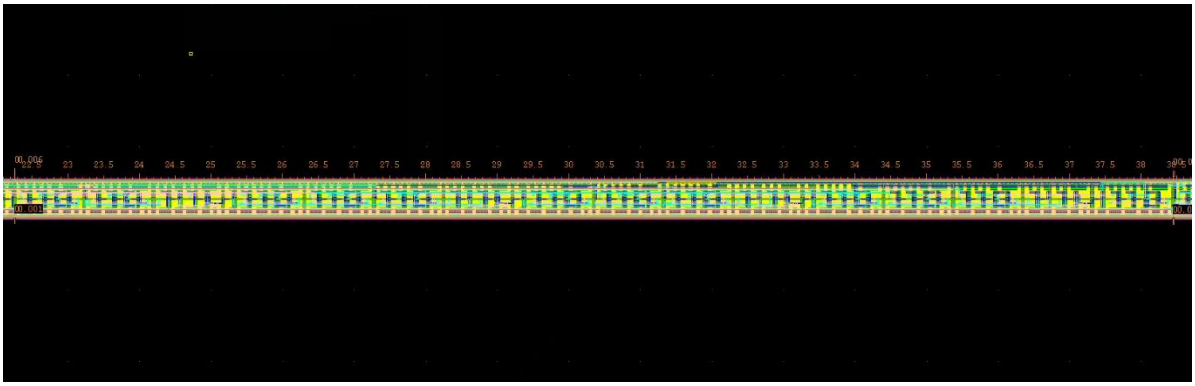

Fig 3-2. Part 1 of Multiplier – First 4 Bits Full adder

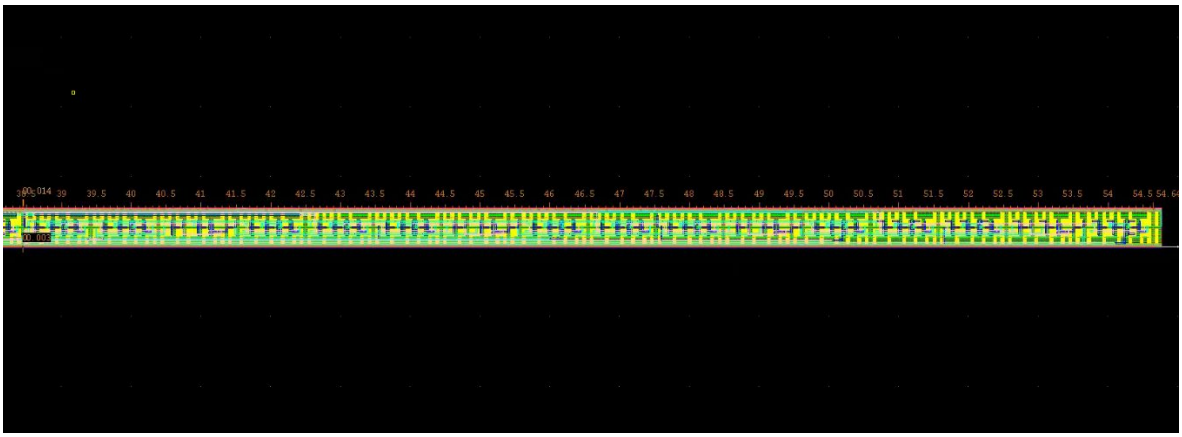

Fig 3-3. Part 2 of Multiplier – Second 4Bits Full adder

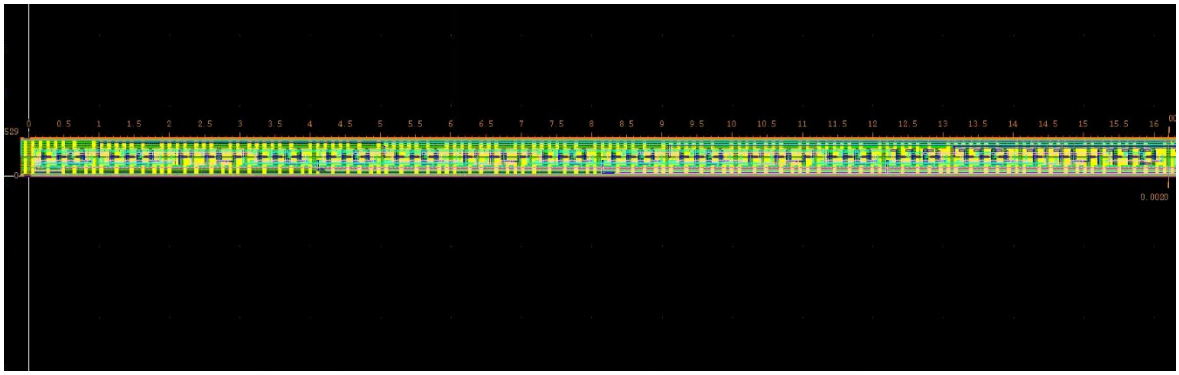

Fig 3-4. Part 3 of Multiplier – Third 4Bits Full adder

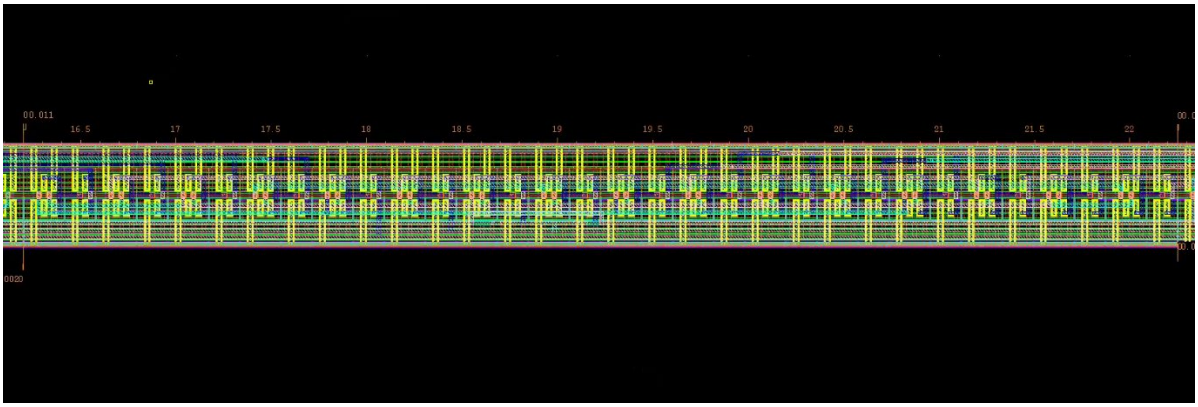

Fig 3-5. Part 4 of Multiplier – And Gate

Template Table				
PMOS Width	**NMOS Width**	**Cell Height**	**Cell Width**	**Cell Area**
0.081um(3 Fins)	0.081um(3 Fins)	0.529um	54.648um	30um^2
Total Cells				
140 (3 4Bits Full Adder + 16 NAND +16 Inverter)				

DRC & LVS Match

Fig 3-6. Multiplier DRC

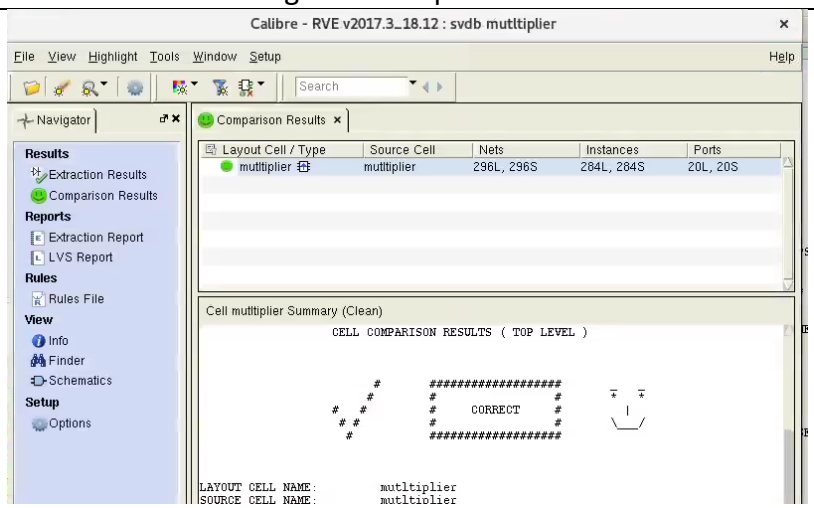

Fig 3-7. Multiplier LVS

Schematic

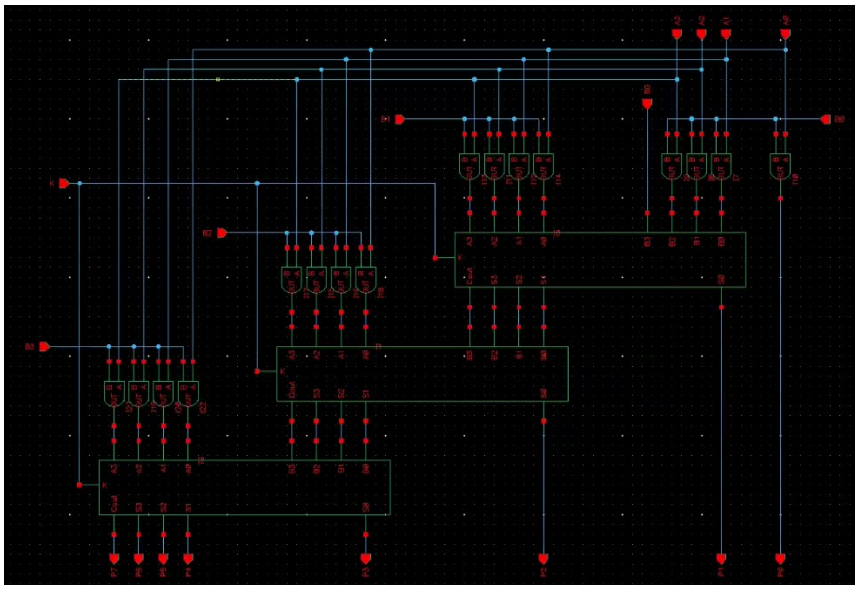

Fig 3-8. 4*4 Bit Multiplier Schematic

V. Simulation and Testing Table

Simulation

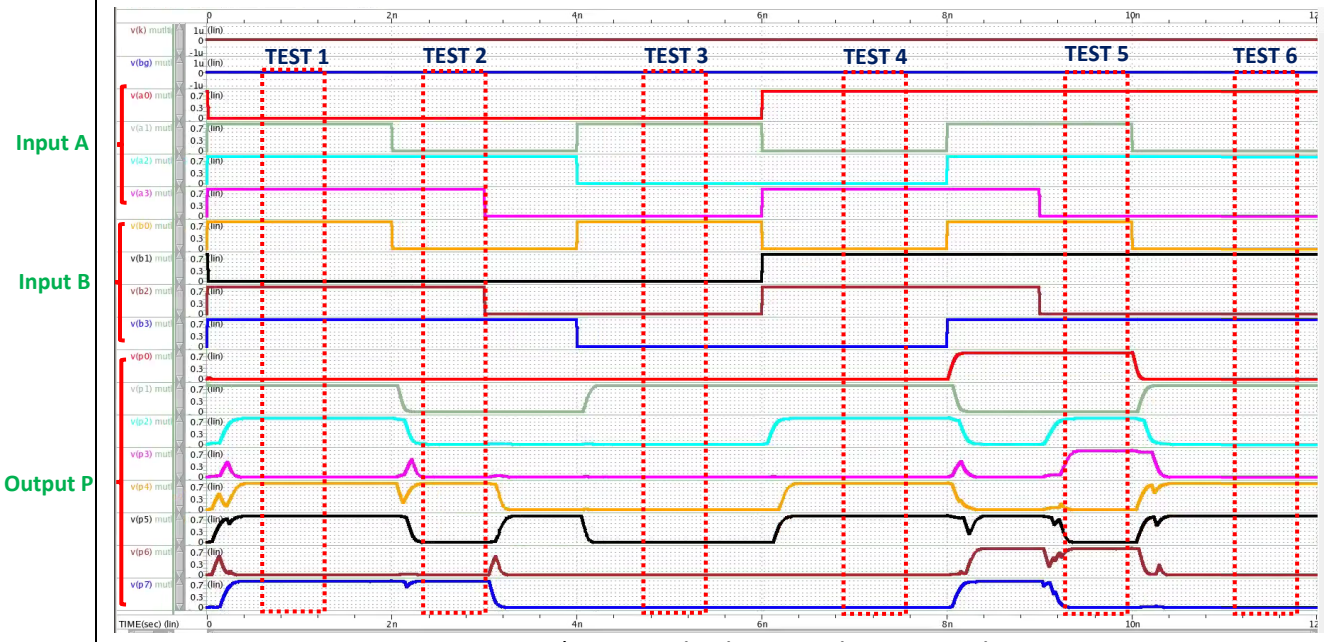

Fig 3-9. 4*4 Bit Multiplier Simulation Result

Testing Table

K	BG	A0	A1	A2	A3	B0	B1	B2	B3	P0	P1	P2	P3	P4	P5	P6	P7
Cin	0	2^0	2^1	2^2	2^3	2^0	2^1	2^2	2^3	2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7

	TEST 1	TEST 2	TEST 3	TEST 4	TEST 5	TEST 6
Input	A : 1110 B : 1101	A : 1100 B : 1100	A : 0010 B : 0001	A : 1001 B : 0110	A : 0111 B : 1011	A : 0101 B : 1010
Value	14*13 = 182	12*12 = 144	2*1 = 2	9*6 = 54	7*11 = 77	5*10 = 50
Output	1011 0110 = 182	1001 0000 = 144	0000 0010 = 2	0011 0110 = 54	0100 1101 = 77	0011 0010 = 50

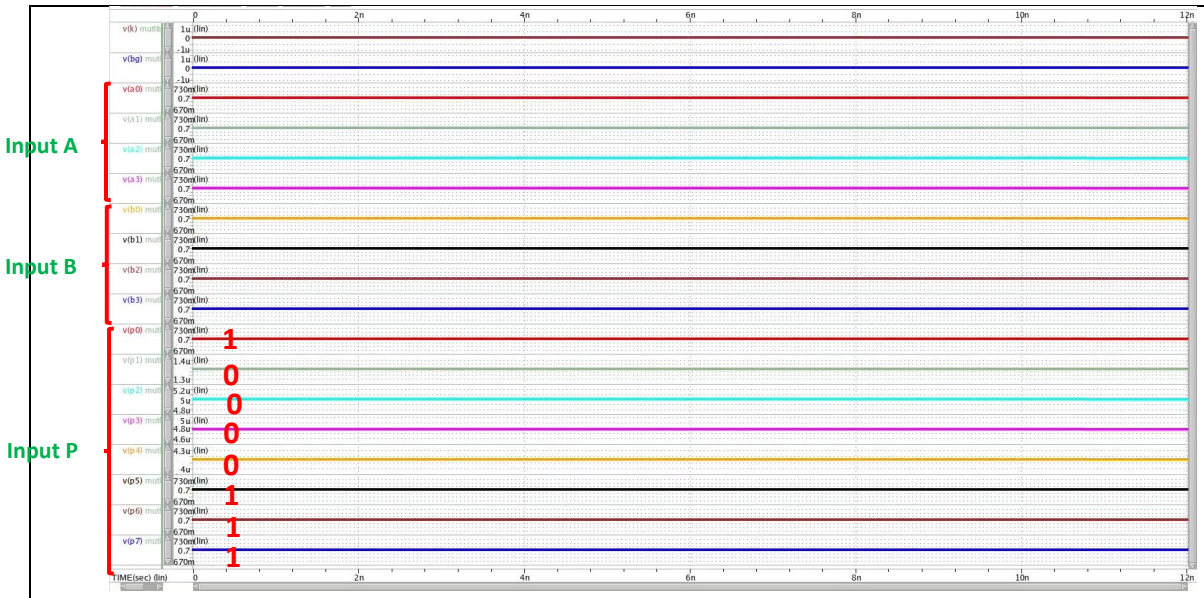

Fig 3-10. 4*4 Bit Multiplier Simulation Result

Testing Table	
Input	1111 + 1111
Value	15*15 =225
Output	1110 0001 =225

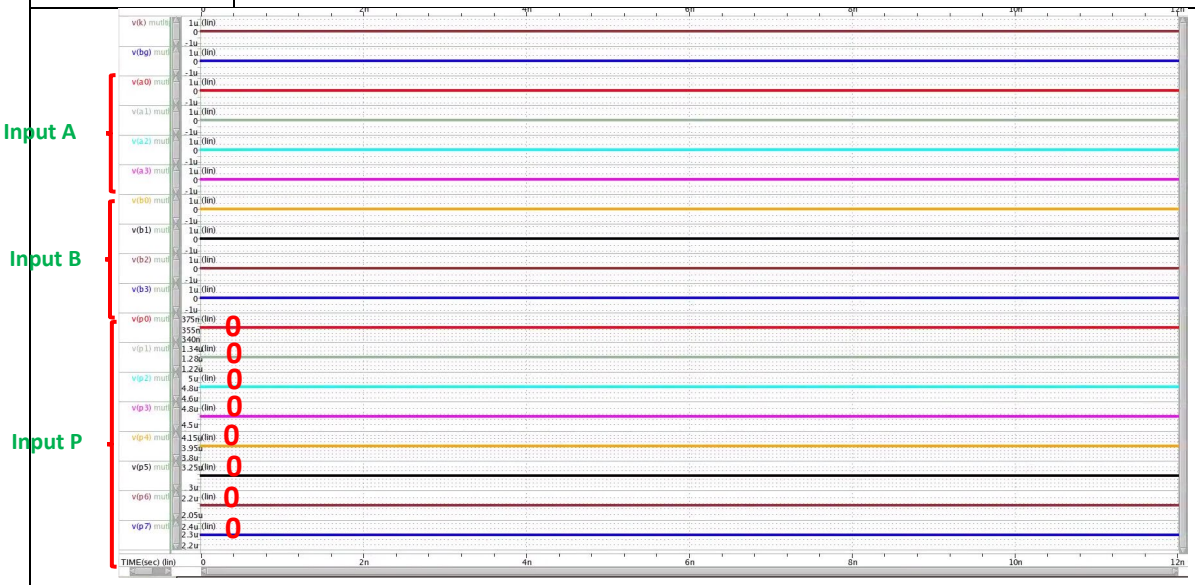

Fig 3-11. 4*4 Bit Multiplier Simulation Result

Testing Table	
Input	0000 * 0000
Value	0*0 =0
Output	0000 0000 = 0

VI. Tradeoffs

The 4*4 multiplier can give product of 8-bit size by using the input number of 4-bit size. The maximum of the number is 15*15 =225. This multiplier is Combinational Multiplier. It performs multiplication of two unsigned binary numbers and the advantage is that it can generate intermediate products easily. The disadvantage is that it needs more layout area.

VII. Conclusion

The final project needs to design a larger and complicated layout system than before. I learned how to place the metal wiring in less space to decrease the layout area. After completing the layout design, LVS match was big challenge because the layout was large. I must check the total layout many times to reduce the mismatch to the schematic. I am glad that I can learn much more simulation skills and use the knowledge what I learn in this class when I do this project.

VIII. Reference

- Class Note
- Asap7_tutorial word file