

EECT 7325
PROJECT #1: Cell Library for 7nm

Name: YI CHIEN CHIANG
UTD ID: 2021477769

Table of Contents

I.	Introduction.....	3
II.	7nm Design Rules.....	3
III.	Inverter.....	4
IV.	NAND2.....	7
V.	NOR2.....	10
VI.	XOR2.....	13
VII.	MUX2:1.....	16
VIII.	OAI21.....	19
IX.	OAI22.....	23
X.	AOI21.....	26
XI.	AOI22.....	30
XII.	DFF.....	33
XIII.	Final Layout.....	36
XIV.	Conclusion.....	37
XV.	Reference.....	37

I. Introduction

This project outlines the 7nm layout design of the different logic gate using the concepts learned in EECT 7325. In order to design first I need to understand the design rules of 7nm layout and complete ten cells in this project. After finishing the cells layout, simulating the cells to get the result is necessary. All parts of the cells must be correct and should be lined up side by side next to each other. Finally, I need to create and transfer the layout files to .lib files to finish this project.

II. 7nm Design Rules

Layout Design Rules			
Gate Width	0.02um	SDT to Gate	0.005um
Gate Pitch	0.054um	LIG to GCut	0.014um
Fin Width	0.007um	Cell Height	0.288um
Fin pitch	0.027um	SDT Width	0.024um
Gate to Gate	0.034um	Minimum M1,M2,M3 Width	0.018um
Fin to Gate	0.019um	V0,V0,V2 Area	0.018um*0.018um

Fig 1. 7nm Layout Rule

III. Inverter

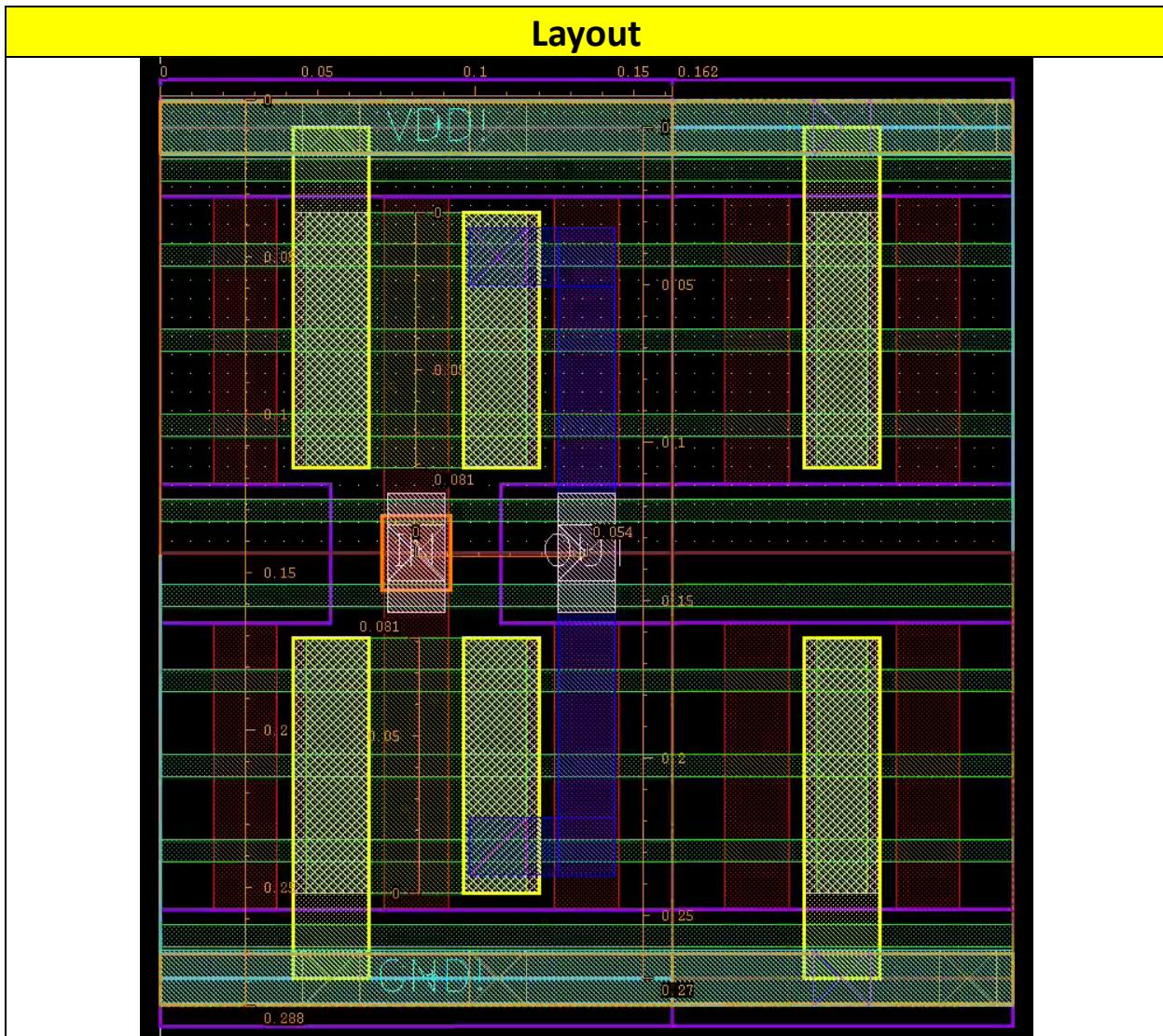


Fig 2-1. Inverter layout

Template Table

PMOS Width	NMOS Width	Cell Height	Cell Width	Cell Area
0.081um(3 Fins)	0.081um(3 Fins)	0.288um	0.162um	0.046656um ²
Pin(IN) to Pin(OUT)		Pin(VDD!) to Pin(GND!)		
0.054um		0.27um		

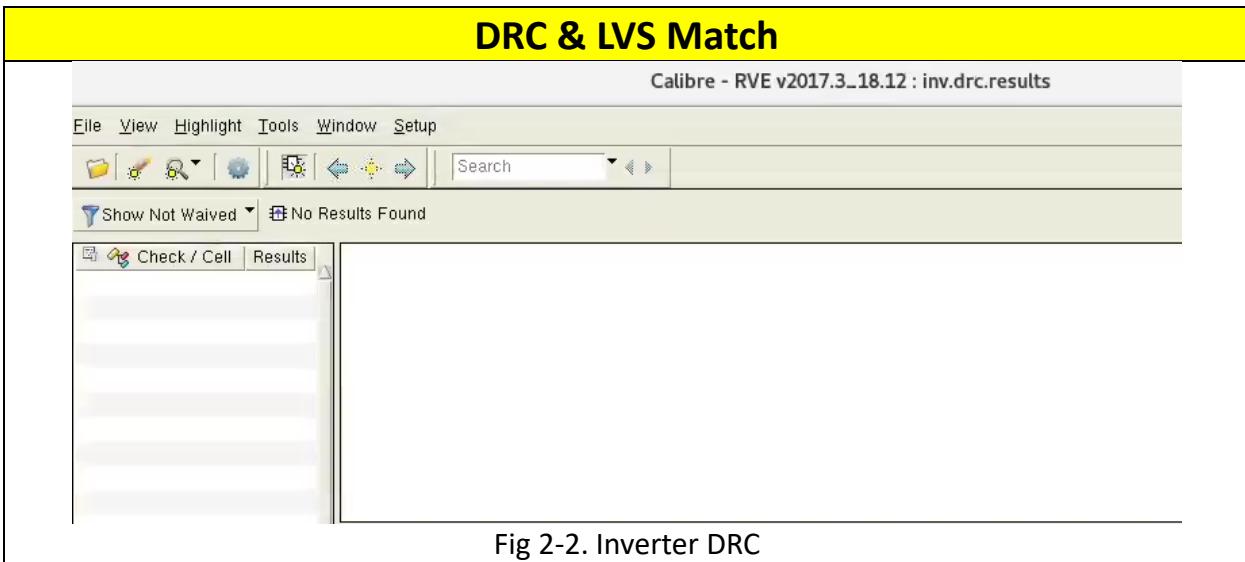


Fig 2-2. Inverter DRC

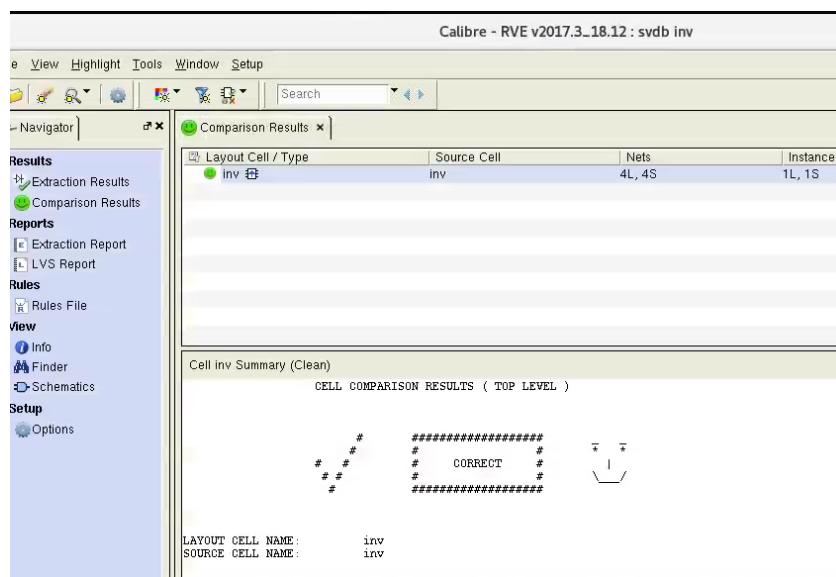


Fig 2-3. Inverter LVS

Schematic & Simulation

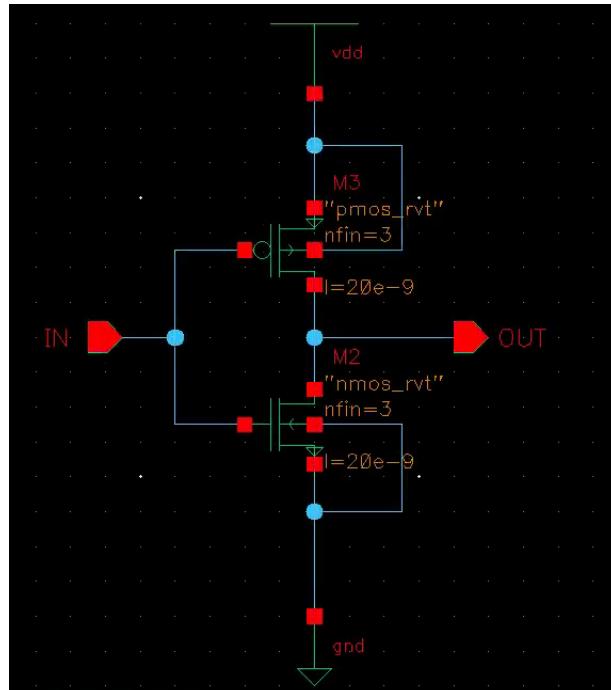


Fig 2-4. Inverter Schematic

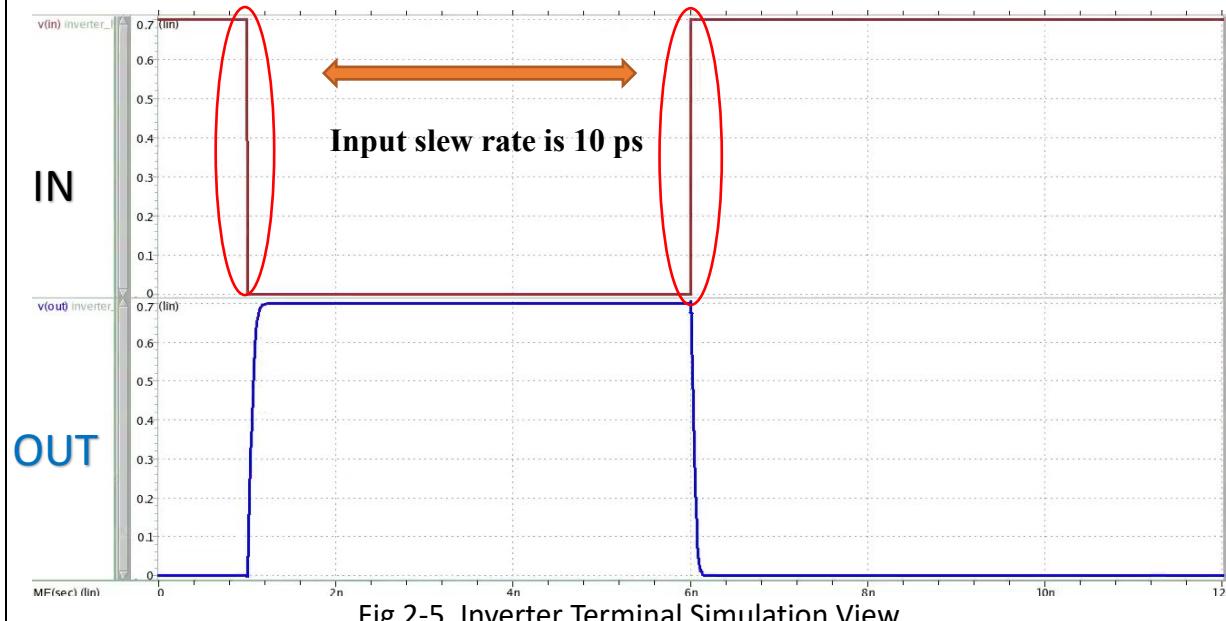


Fig 2-5. Inverter Terminal Simulation View

IV. NAND2

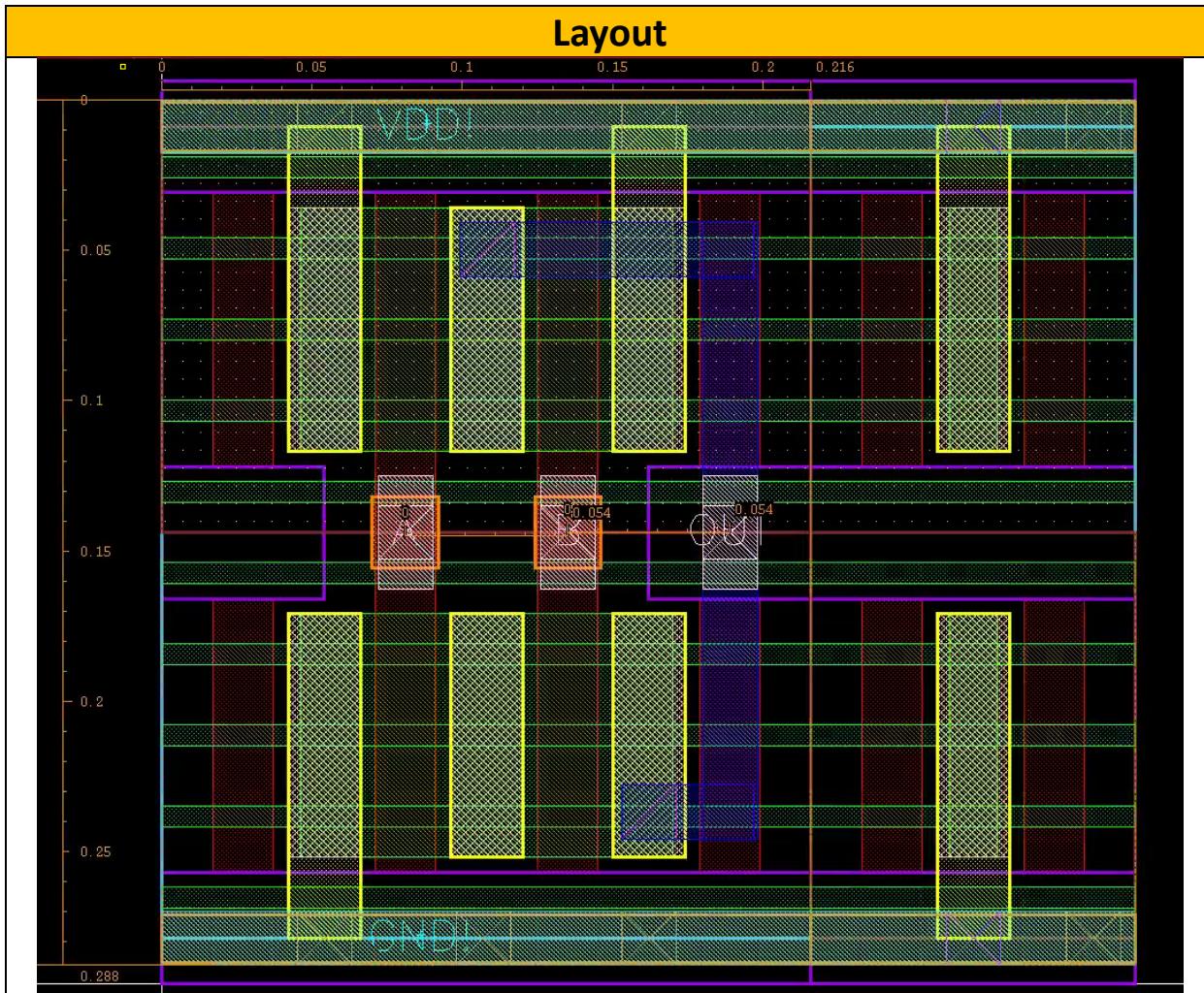


Fig 3-1. NAND2 layout

Template Table

PMOS Width	NMOS Width	Cell Height	Cell Width	Cell Area
0.081um(3 Fins)	0.081um(3 Fins)	0.288um	0.216um	0.062208um ²
Pin(A) to Pin(B)		Pin(VDD!) to Pin(GND!)		Pin(B) to Pin(OUT)
0.054um		0.27um		0.054um

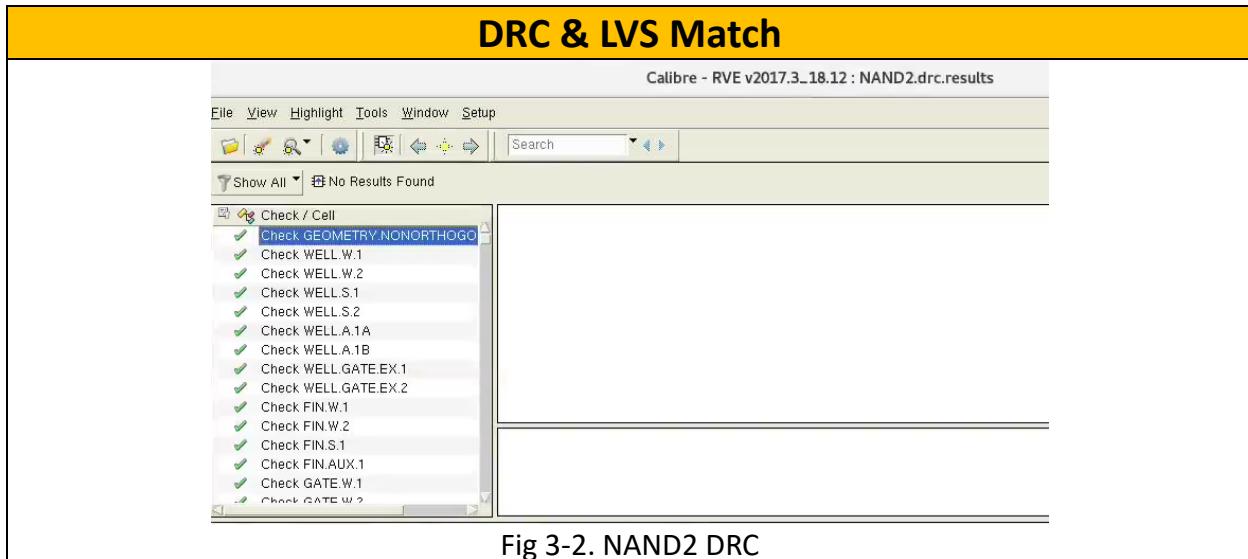


Fig 3-2. NAND2 DRC

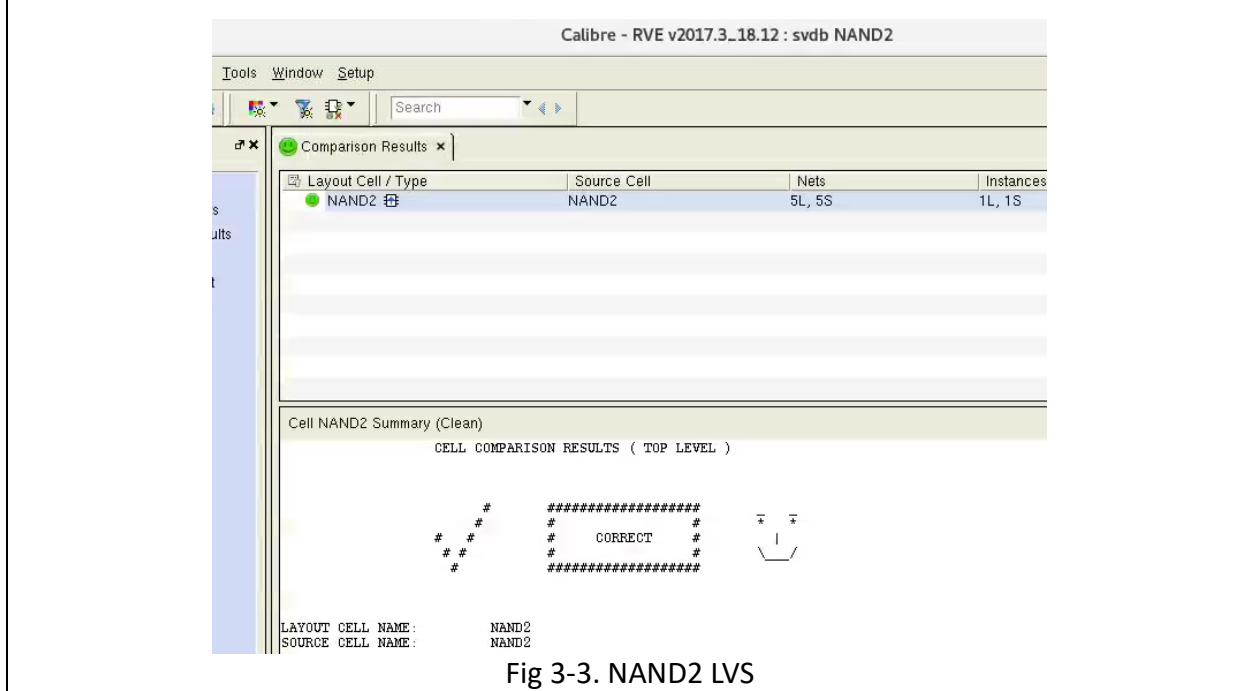
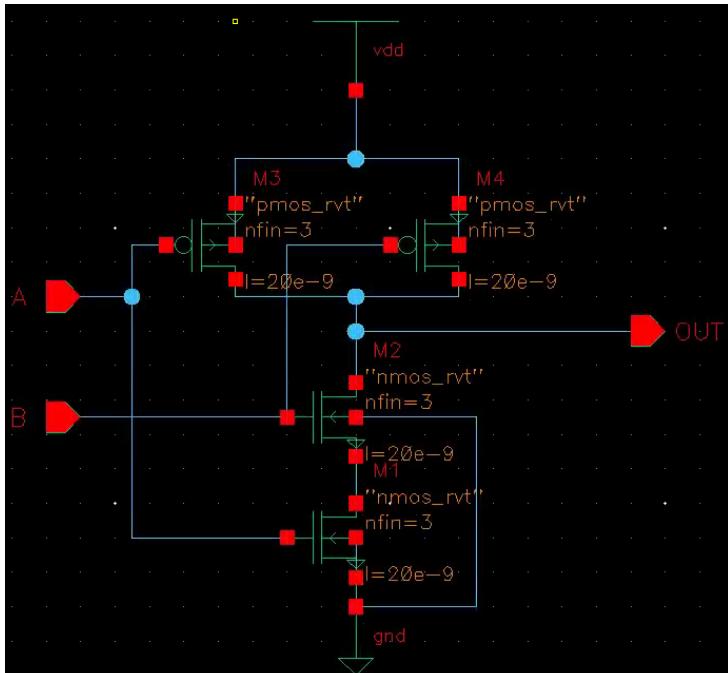


Fig 3-3. NAND2 LVS

Schematic & Simulation



NAND2

A	B	OUT
0	0	1
0	1	1
1	0	1
1	1	0

Fig 3-4. NAND2 Schematic

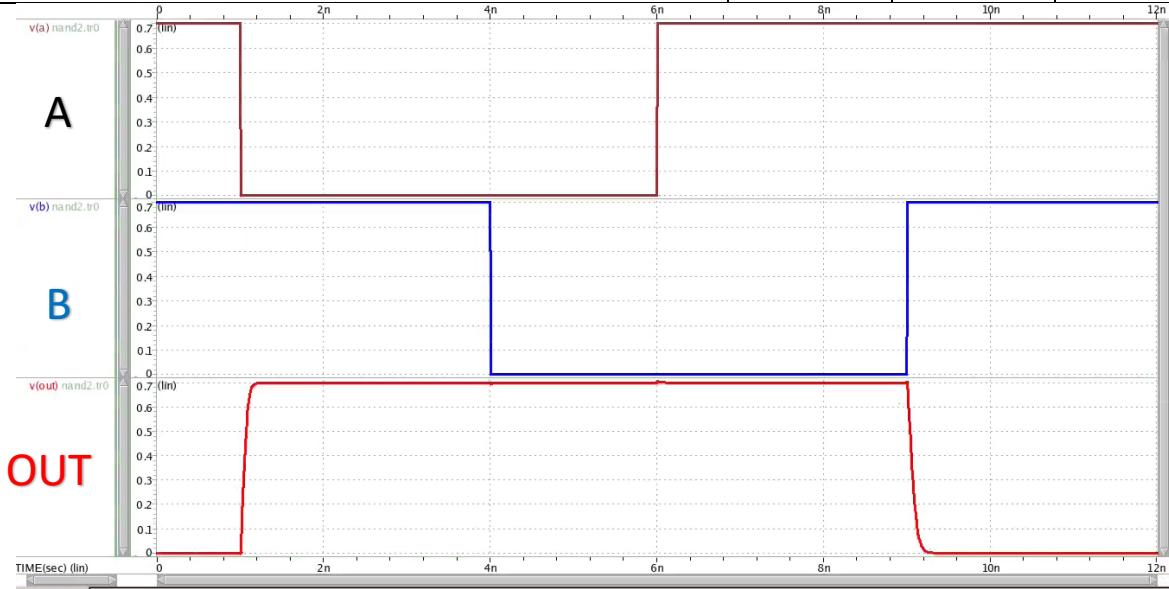


Fig 3-5. NAND2 Terminal Simulation View

V. NOR2

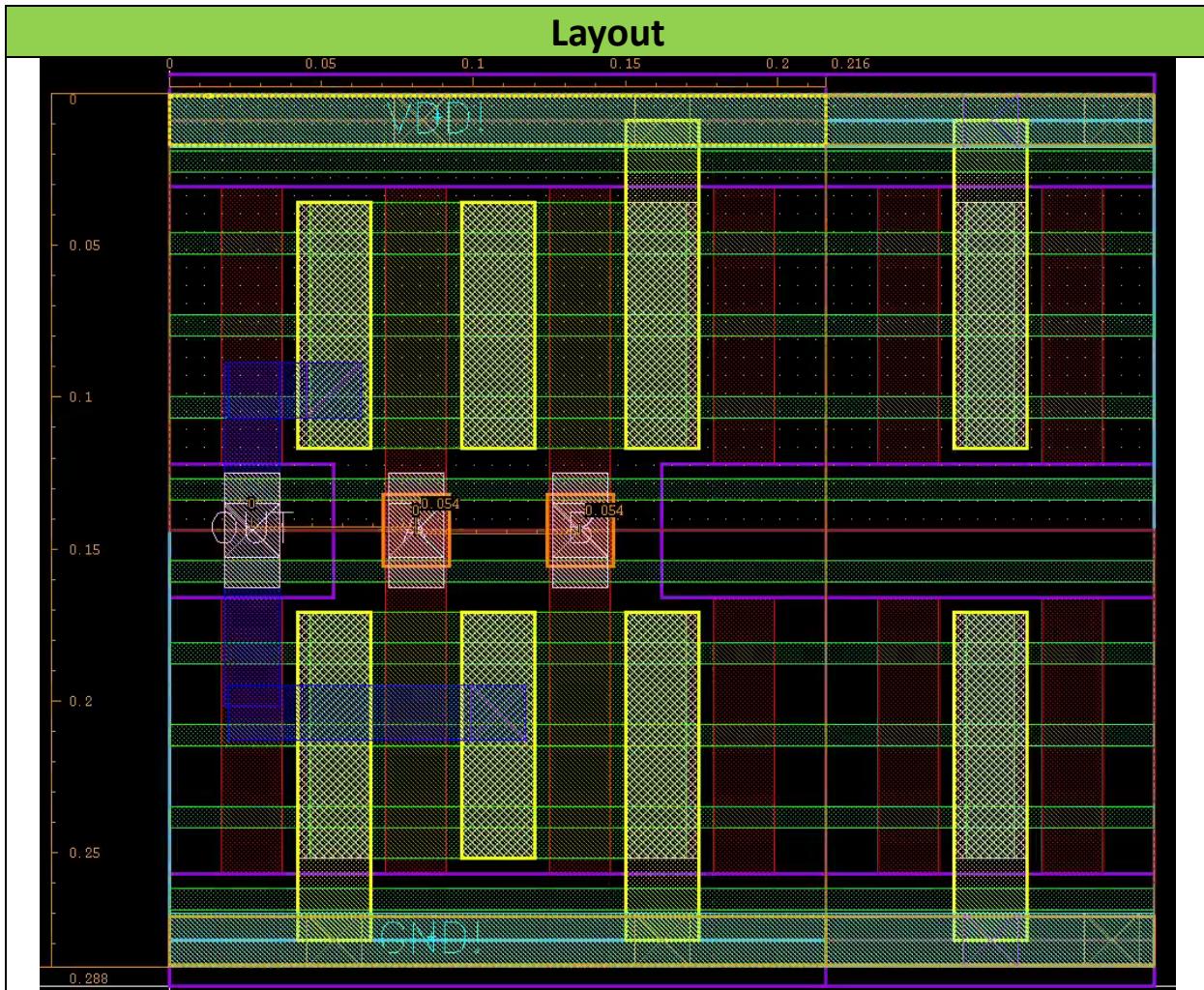


Fig 4-1. NOR2 layout

Template Table

PMOS Width	NMOS Width	Cell Height	Cell Width	Cell Area
0.081um(3 Fins)	0.081um(3 Fins)	0.288um	0.216um	0.062208um ²
Pin(A) to Pin(B)		Pin(VDD!) to Pin(GND!)		Pin(A) to Pin(OUT)
0.054um		0.27um		0.054um

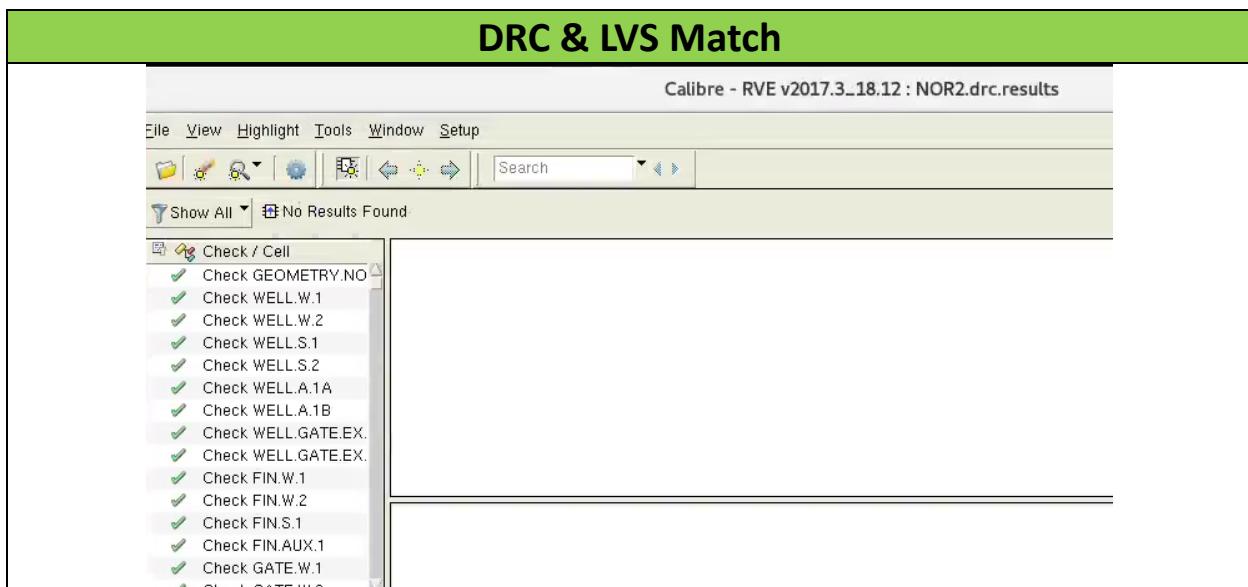


Fig 4-2. NOR2 DRC

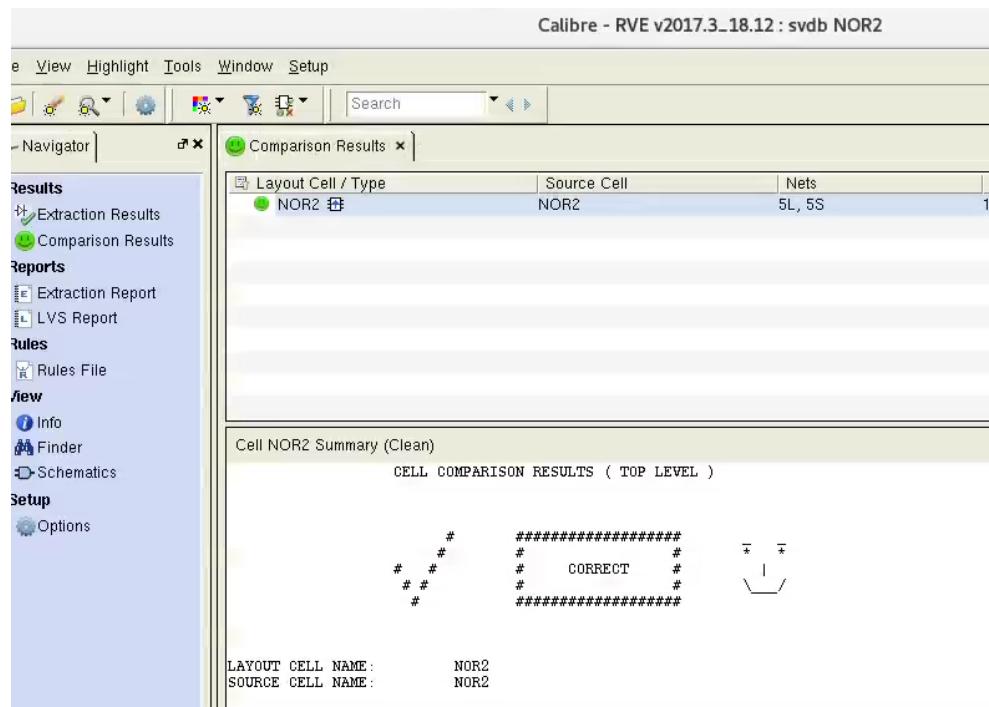


Fig 4-3. NOR2 LVS

Schematic & Simulation

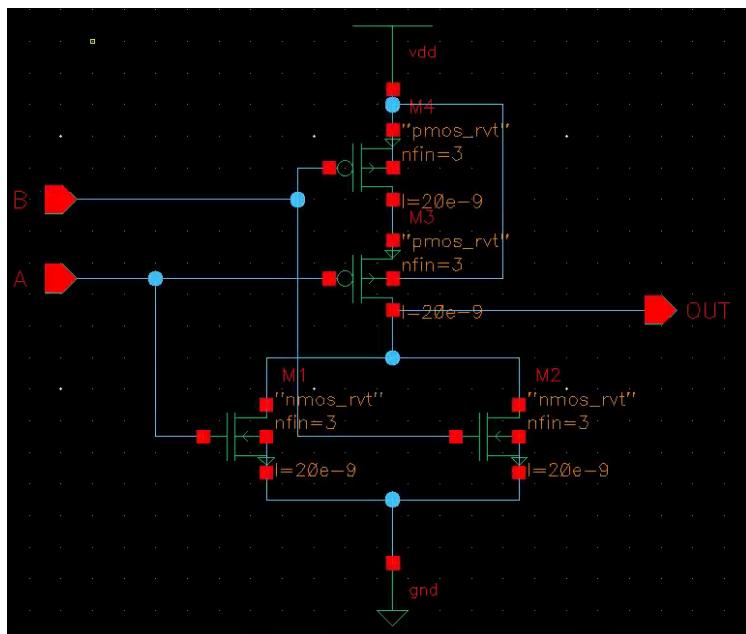


Fig 4-4. NOR2 Schematic

NOR2

A	B	OUT
0	0	1
0	1	0
1	0	0
1	1	0

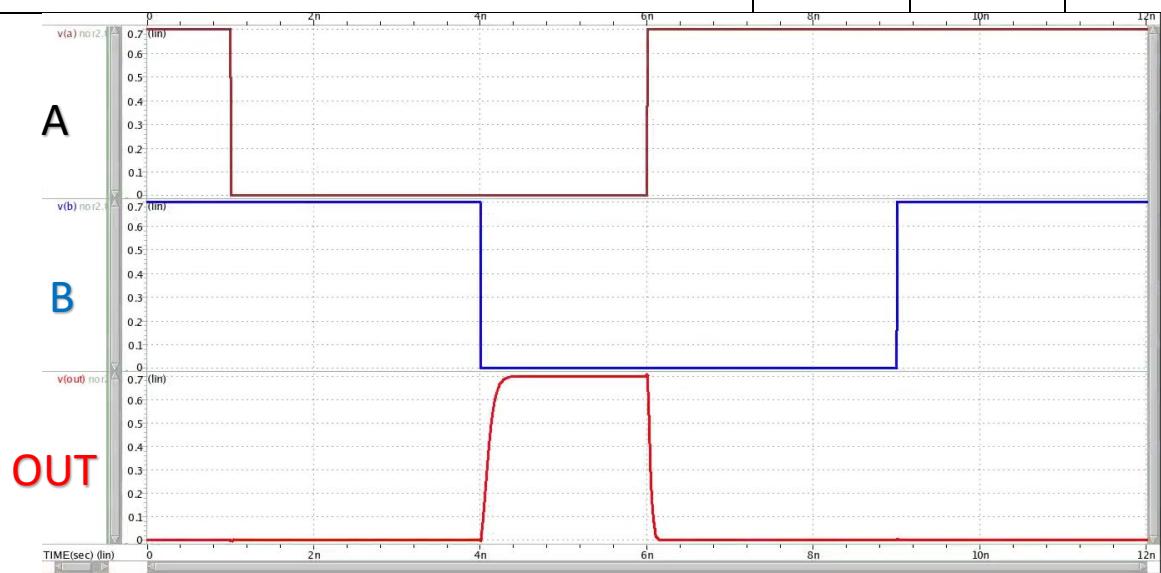


Fig 4-5. NOR2 Terminal Simulation View

VI. XOR2

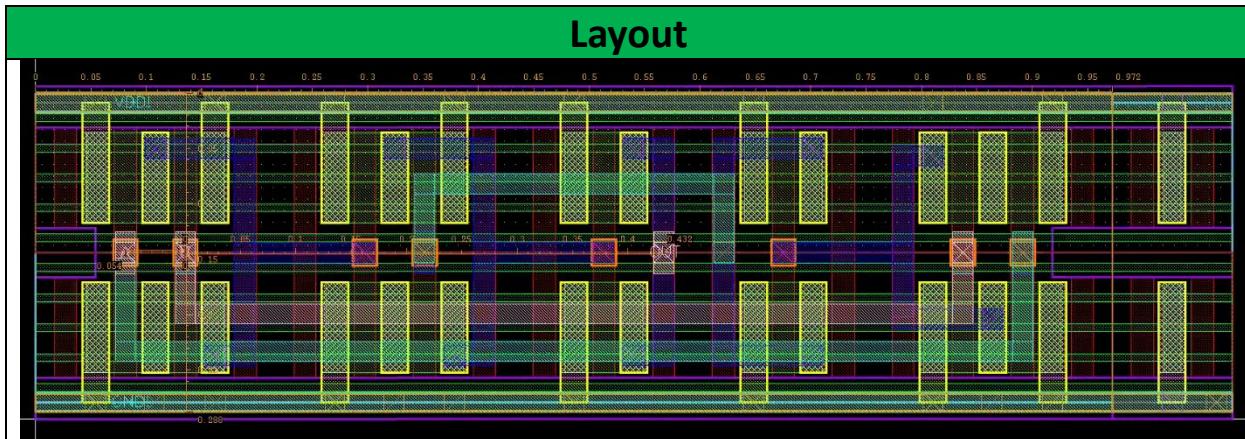


Fig 5-1. XOR2 layout

Template Table				
PMOS Width	NMOS Width	Cell Height	Cell Width	Cell Area
0.081um(3 Fins)	0.081um(3 Fins)	0.288um	0.972um	0.279936um ²
Pin(A) to Pin(B)		Pin(VDD!) to Pin(GND!)		Pin(B) to Pin(OUT)
0.054um		0.27um		0.432um

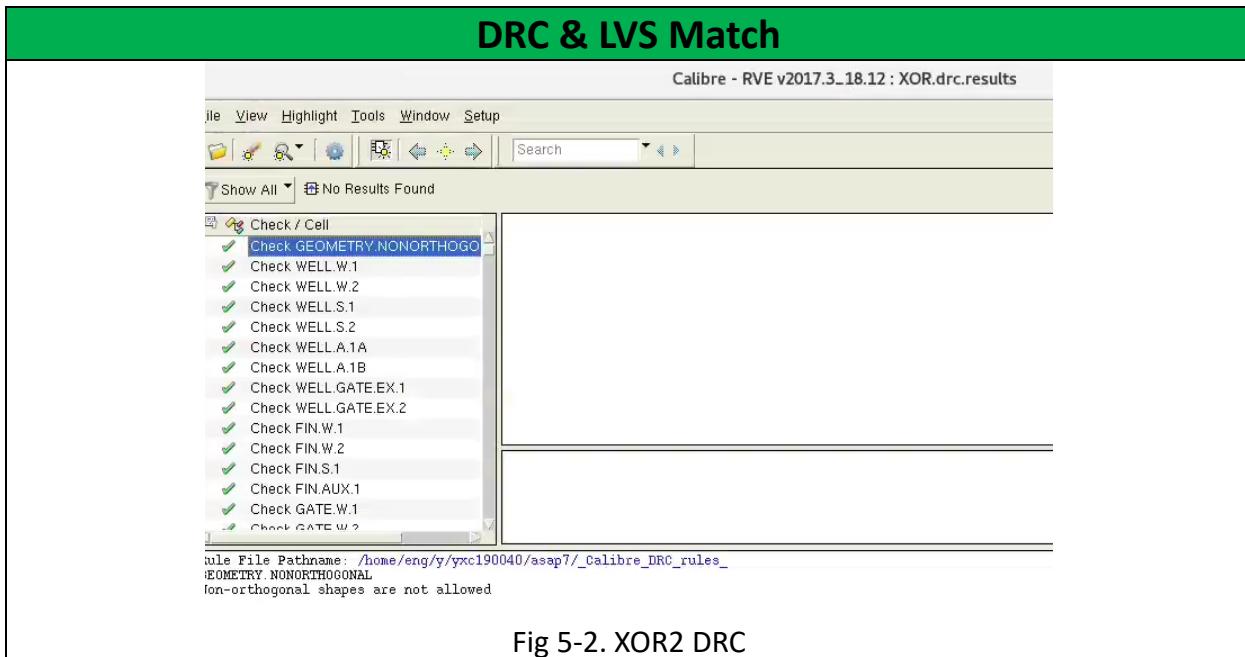


Fig 5-2. XOR2 DRC

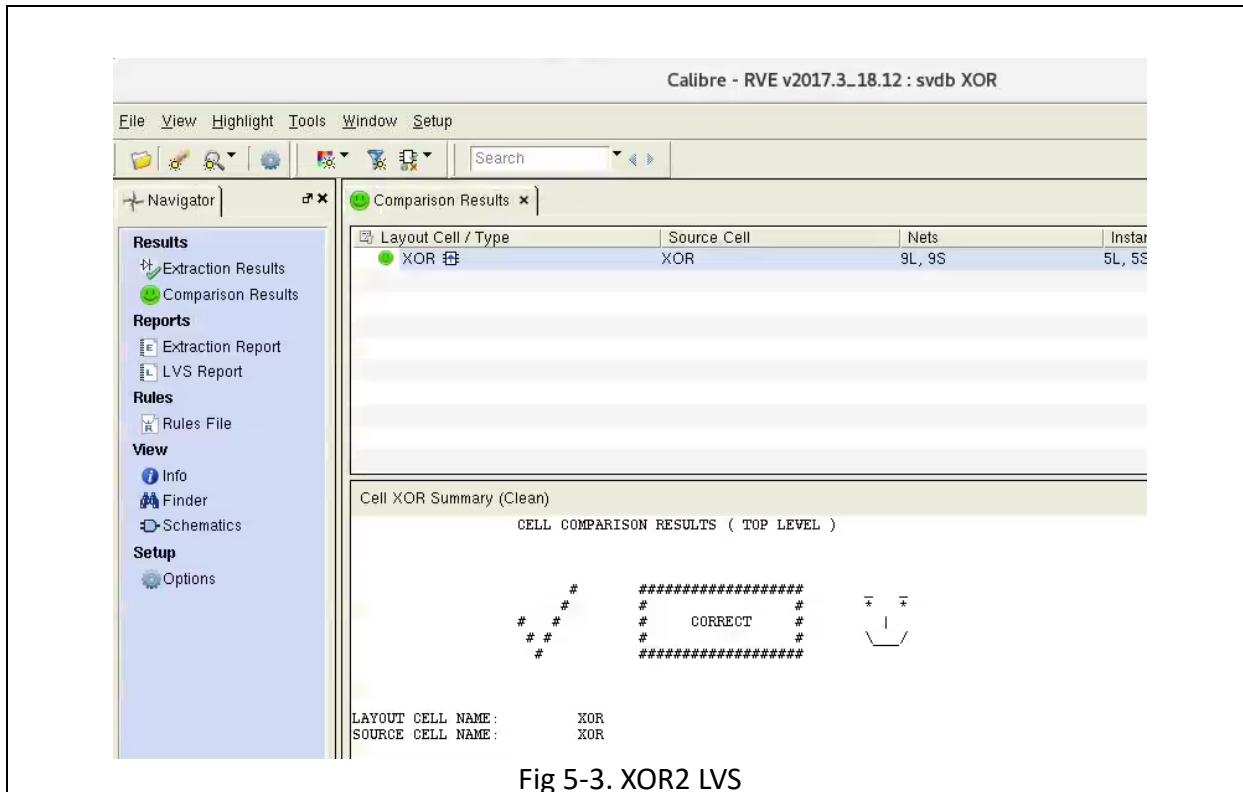


Fig 5-3. XOR2 LVS

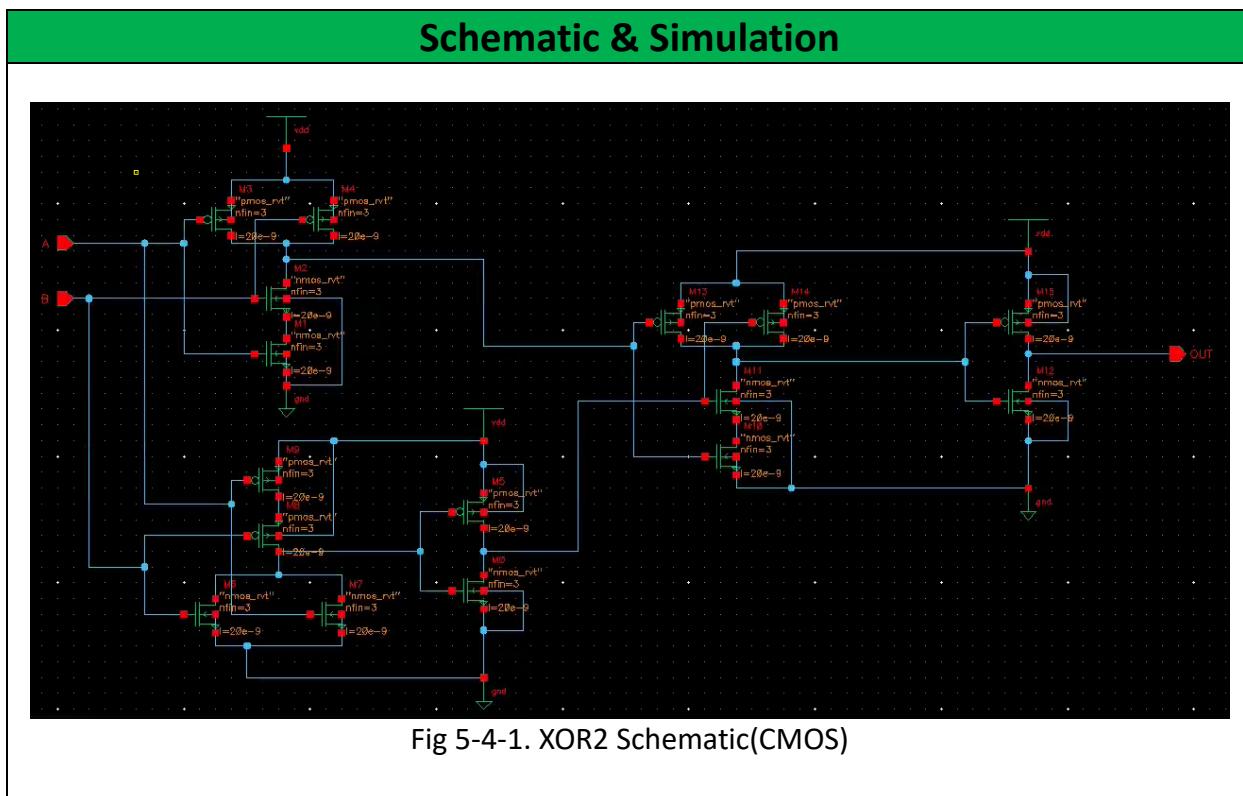


Fig 5-4-1. XOR2 Schematic(CMOS)

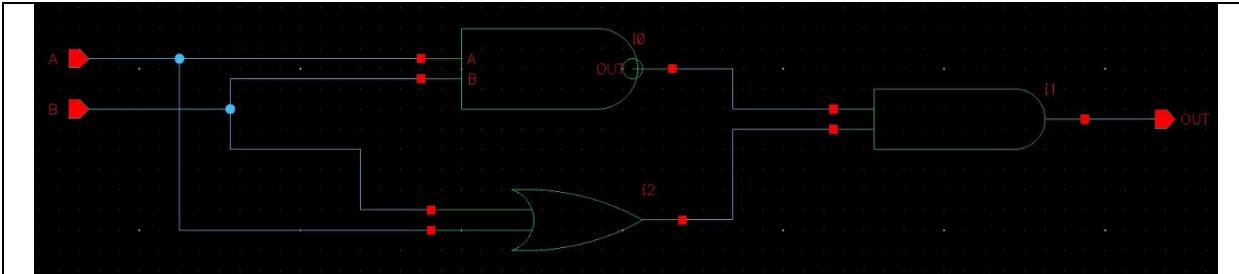


Fig 5-4-2. XOR2 Schematic(Logic Gate)

XOR2 Logic

A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	0

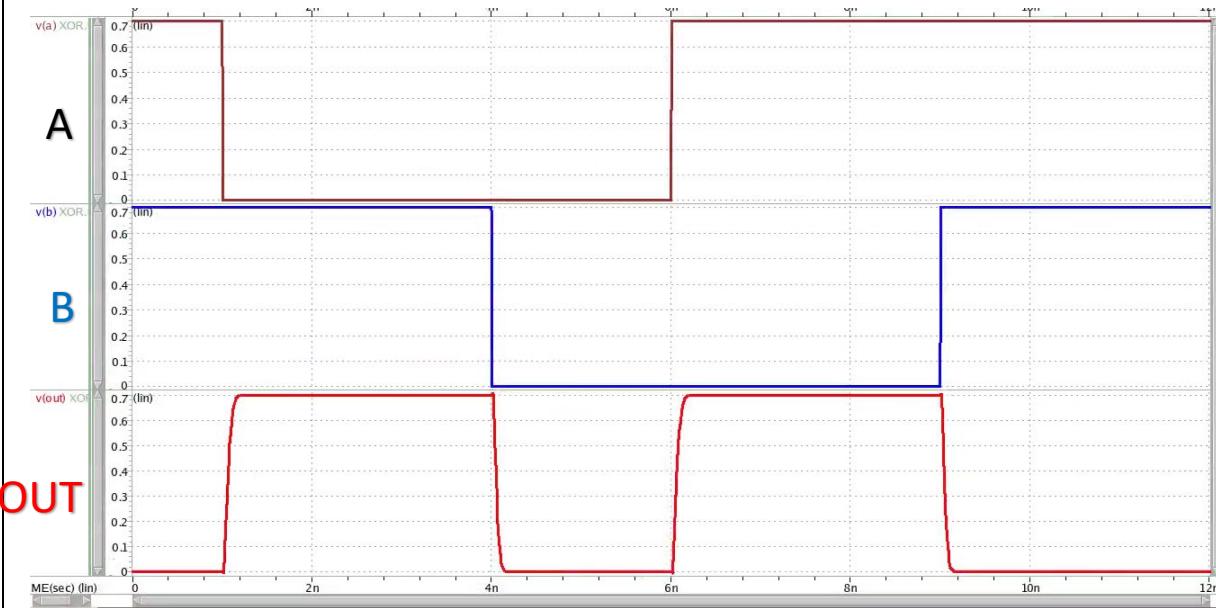


Fig 5-5. XOR2 Terminal Simulation View

VII. MUX2:1

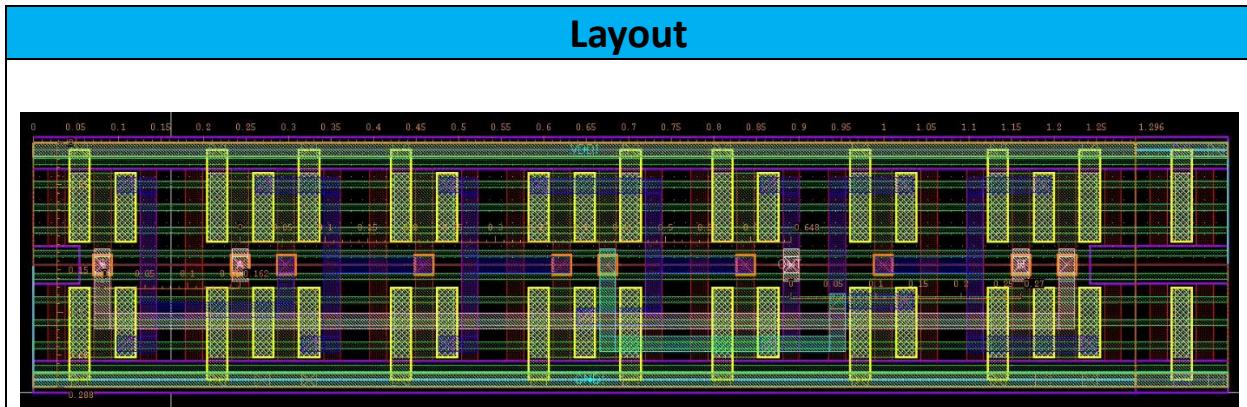


Fig 6-1. MUX2:1 layout

Template Table				
PMOS Width	NMOS Width	Cell Height	Cell Width	Cell Area
0.081um(3 Fins)	0.081um(3 Fins)	0.288um	1.296um	0.373248um ²
Pin(S) to Pin(A)	Pin(A) to Pin(OUT)	Pin(VDD!) to Pin(GND!)	Pin(B) to Pin(OUT)	
0.162um	0.648um	0.27um	0.27um	

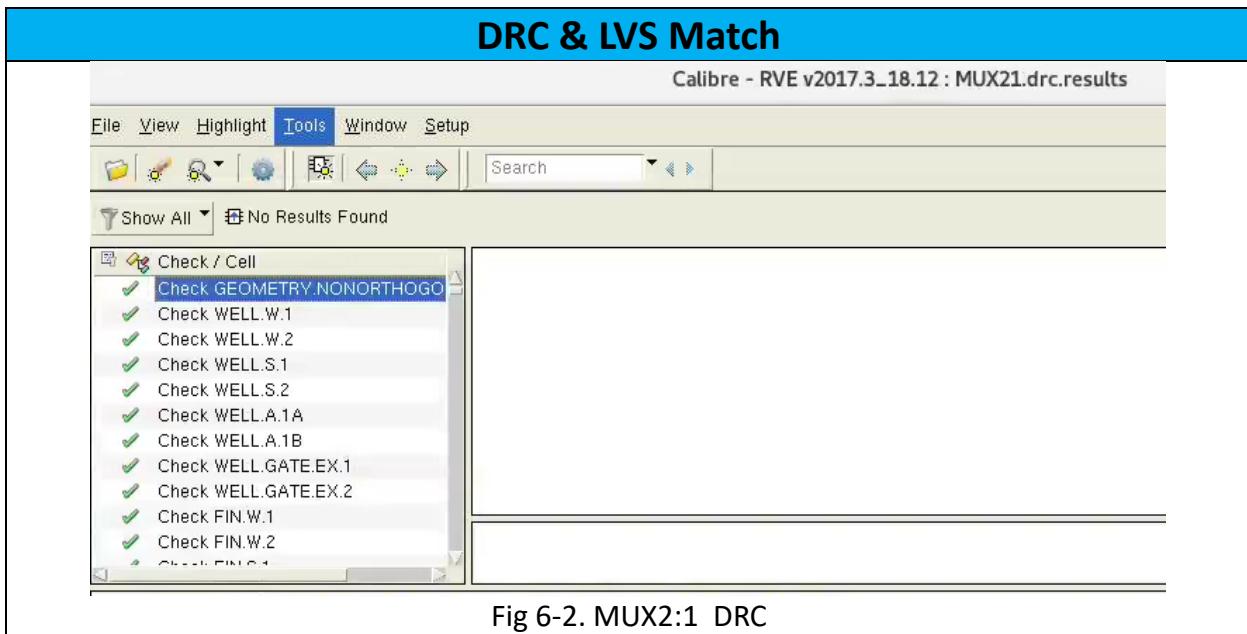


Fig 6-2. MUX2:1 DRC

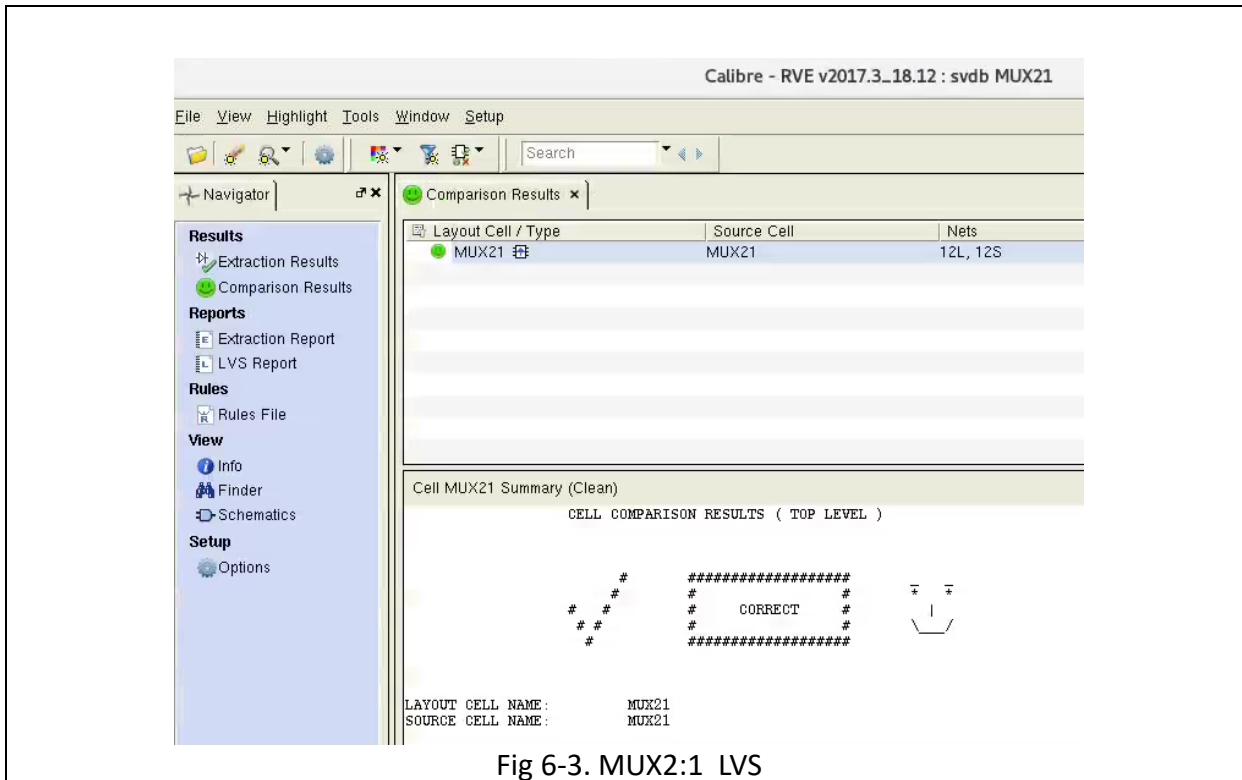


Fig 6-3. MUX2:1 LVS

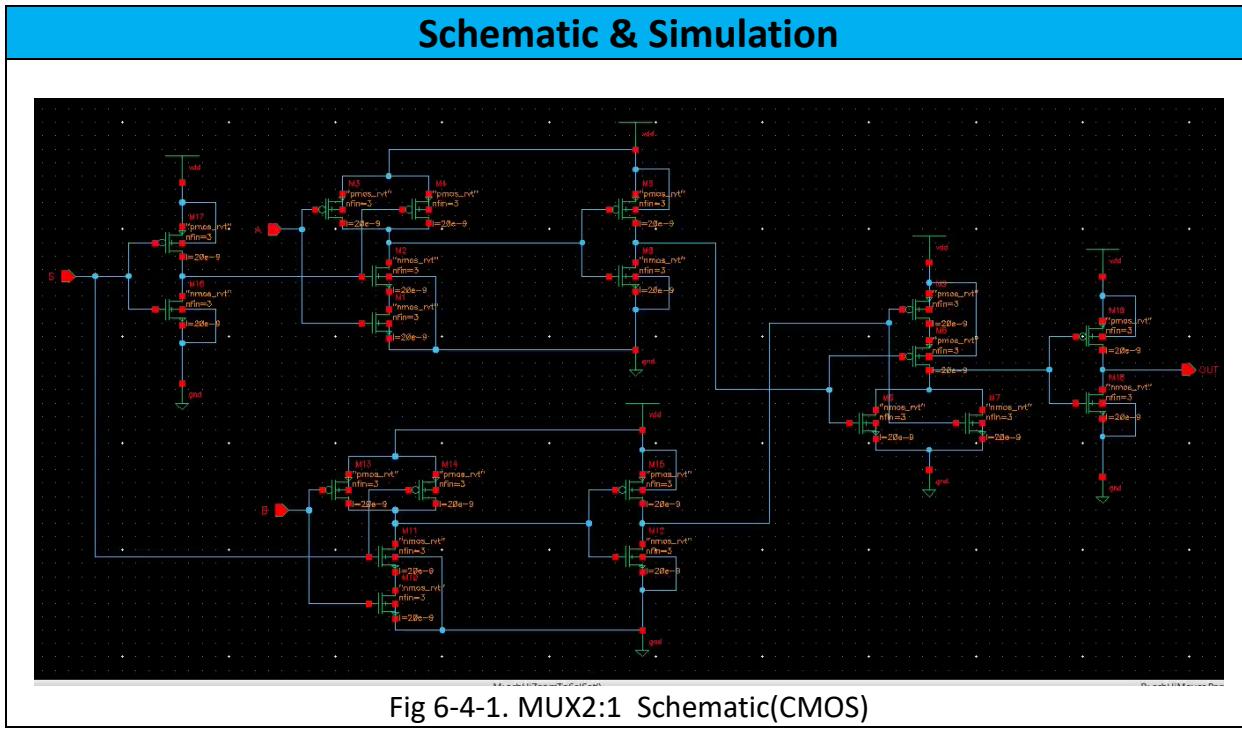


Fig 6-4-1. MUX2:1 Schematic(CMOS)

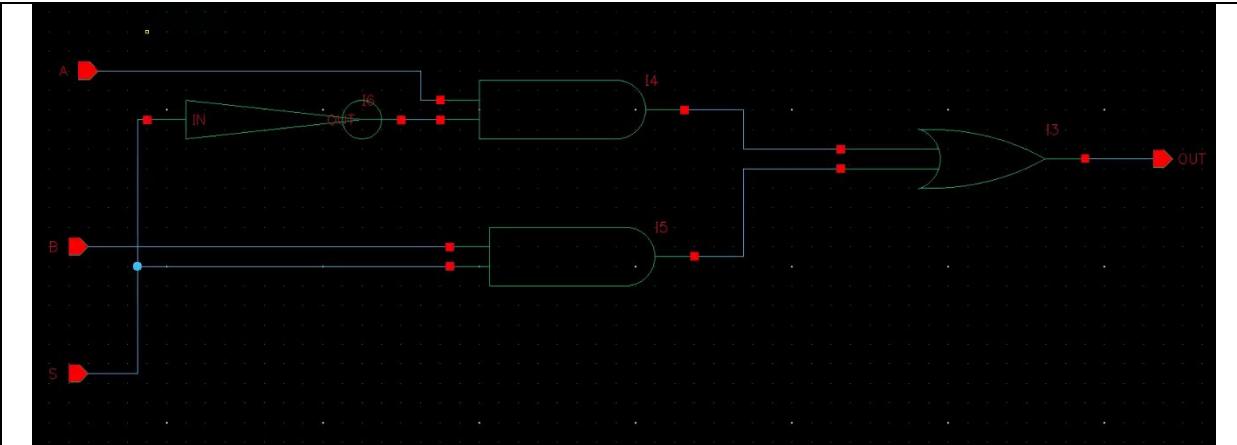


Fig 6-4-2. MUX2:1 Schematic(Logic Gate)

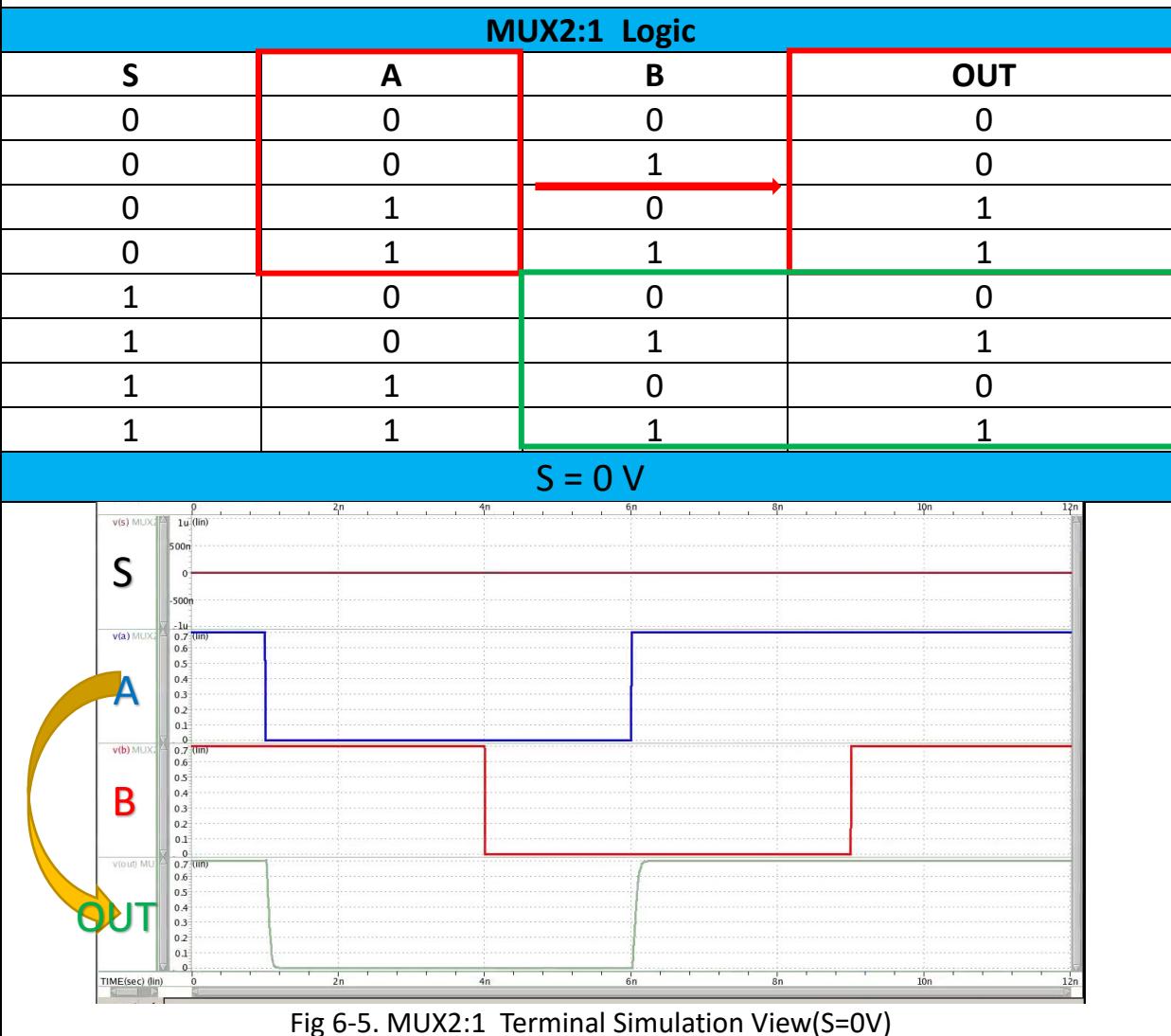


Fig 6-5. MUX2:1 Terminal Simulation View(S=0V)

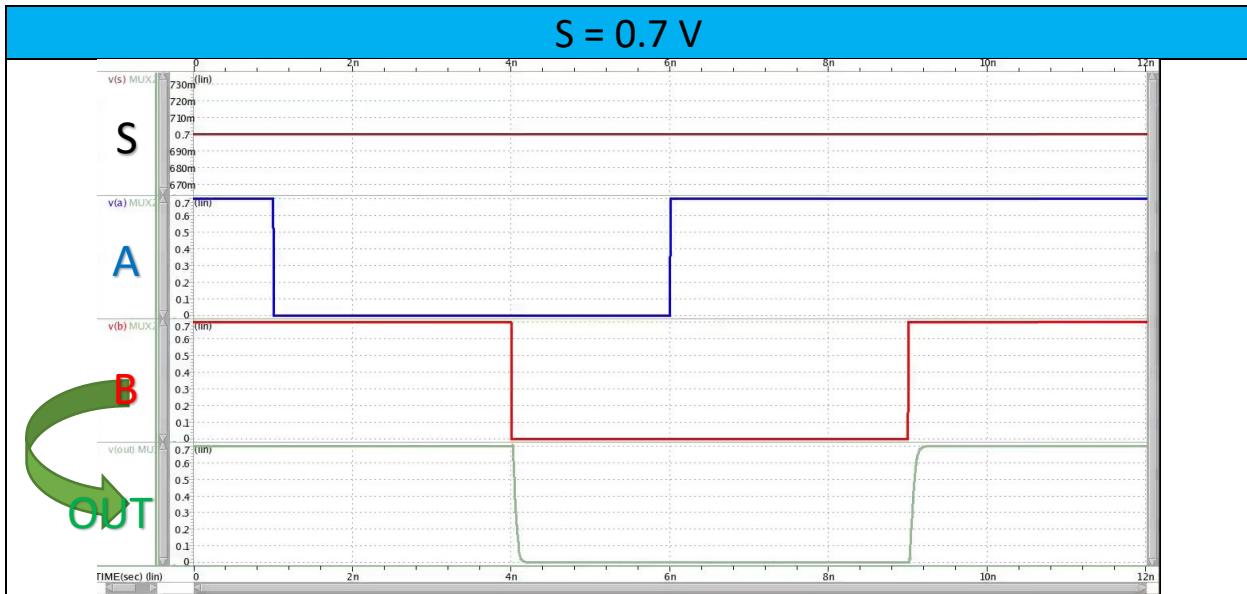


Fig 6-6. MUX2:1 Terminal Simulation View($S=0.7\text{V}$)

Simulation Analysis

- If $S=0\text{v} \Rightarrow$ The output signal follows the A input signal
- If $S=0.7\text{v} \Rightarrow$ The output signal follows the B input signal

VIII. OAI21

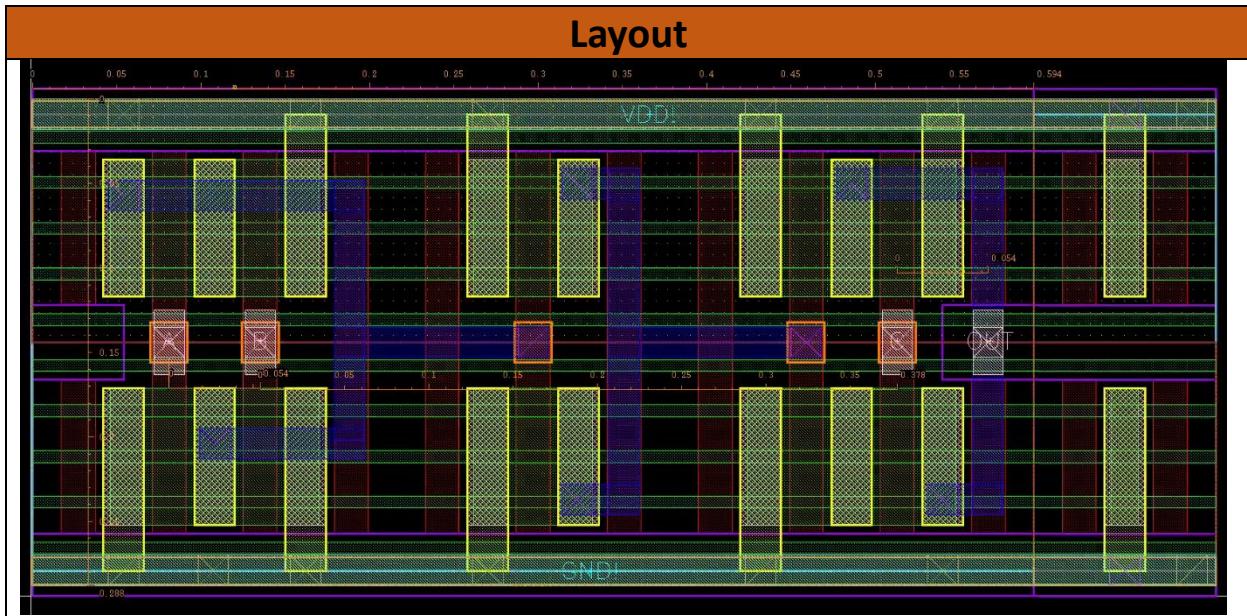
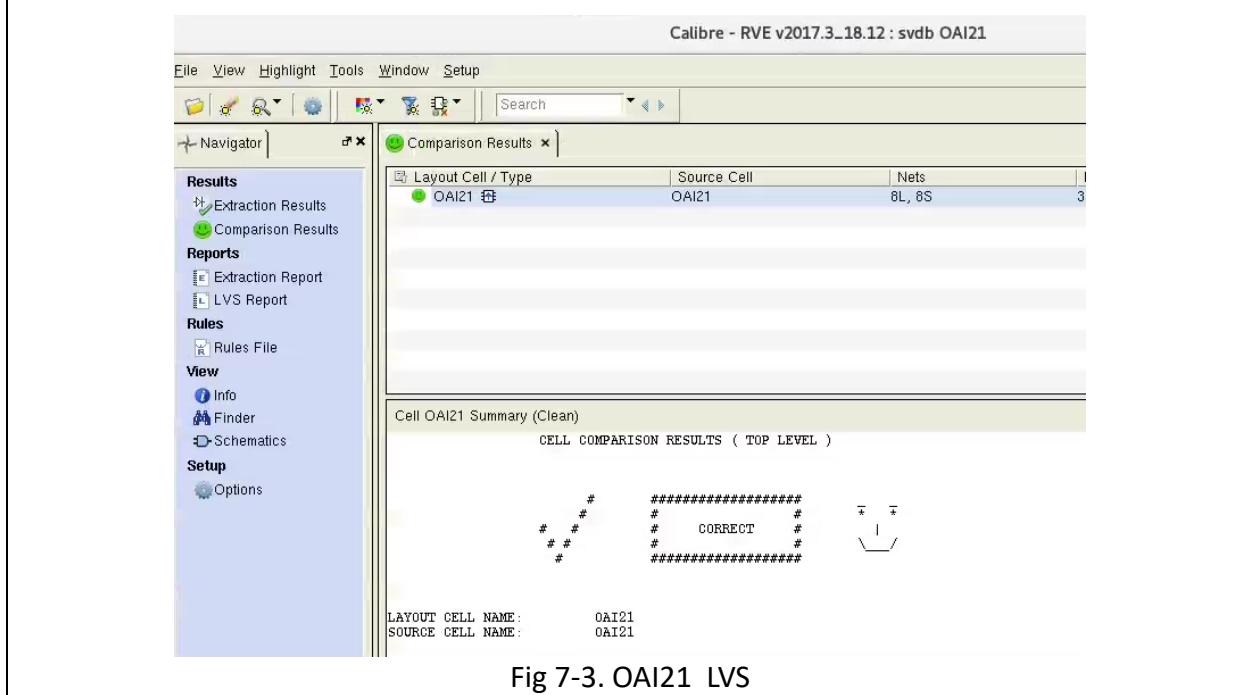
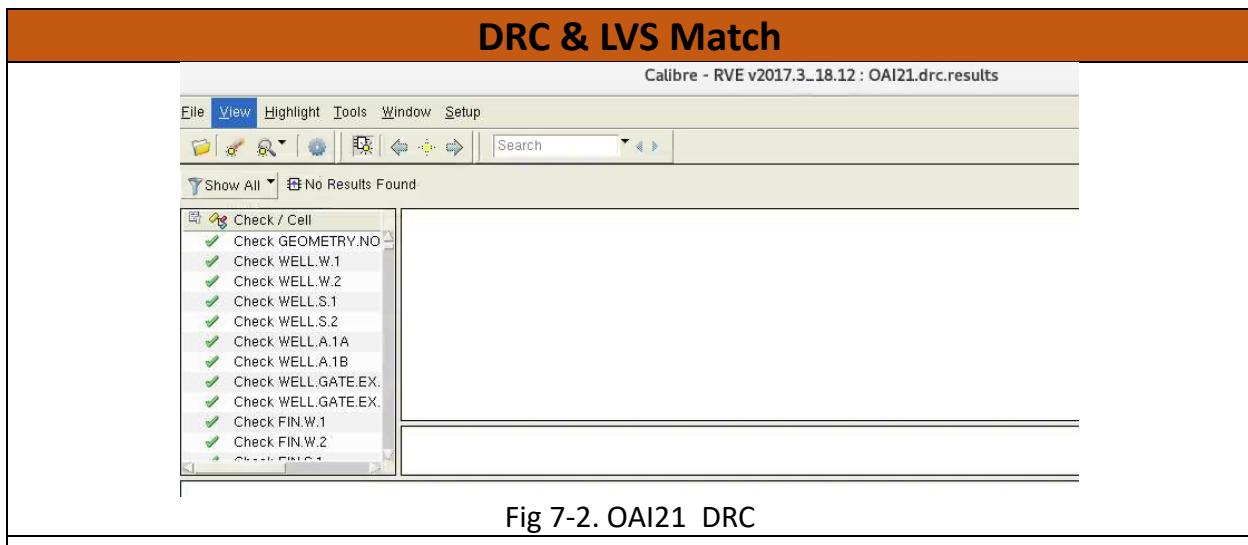


Fig 7-1. OAI21 layout

Template Table				
PMOS Width	NMOS Width	Cell Height	Cell Width	Cell Area
0.081um(3 Fins)	0.081um(3 Fins)	0.288um	0.594um	0.171072um ²
Pin(A) to Pin(B)	Pin(B) to Pin(C)		Pin(VDD!) to Pin(GND!)	Pin(C) to Pin(OUT)
0.054um	0.378um		0.27um	0.054um



Schematic & Simulation

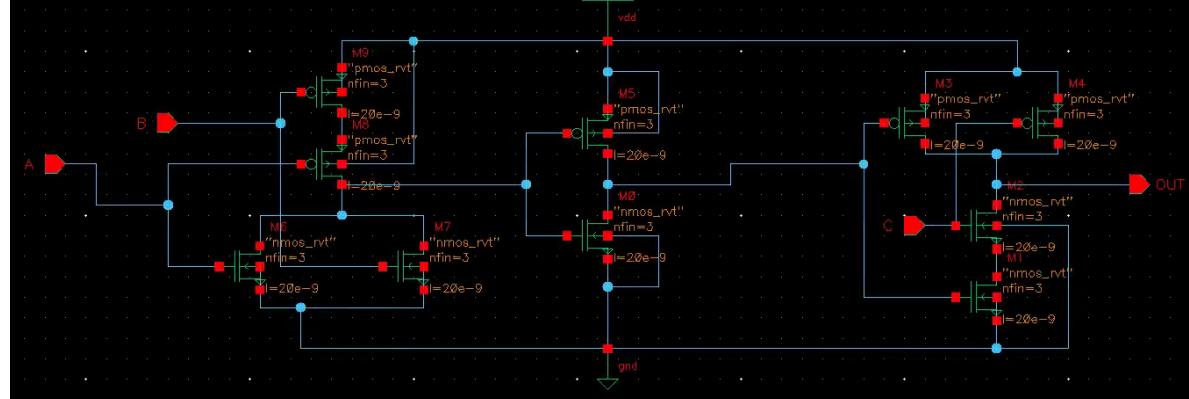


Fig 7-4-1. OAI21 Schematic(CMOS)

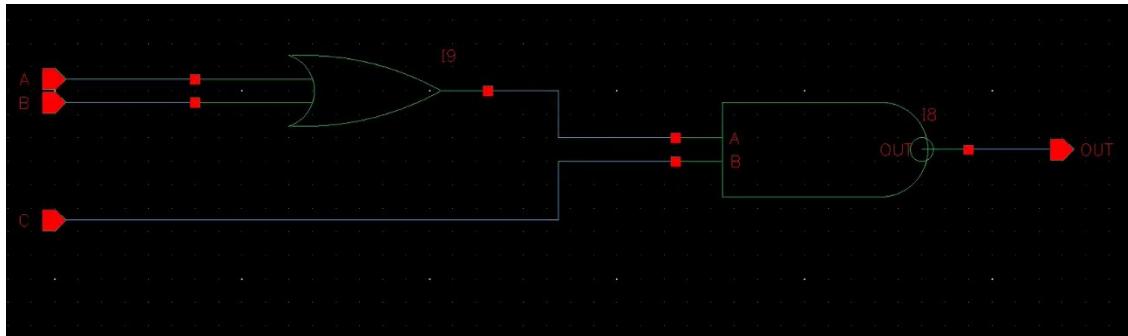


Fig 7-4-2. OAI21 Schematic(Logic Gate)

OAI21 Logic

A	B	C	OUT
0	0	0	1
0	1	0	1
1	0	0	1
1	1	0	1
0	0	1	1
0	1	1	0
1	0	1	0
1	1	1	0

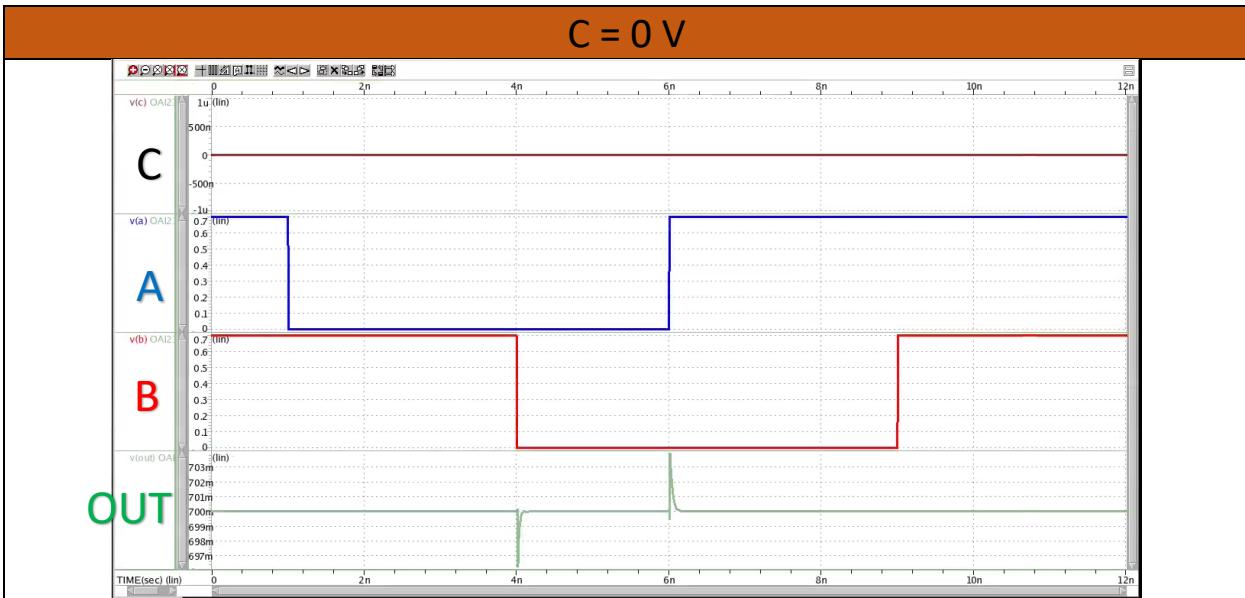


Fig 7-5. OAI21 Terminal Simulation View($C=0\text{V}$)

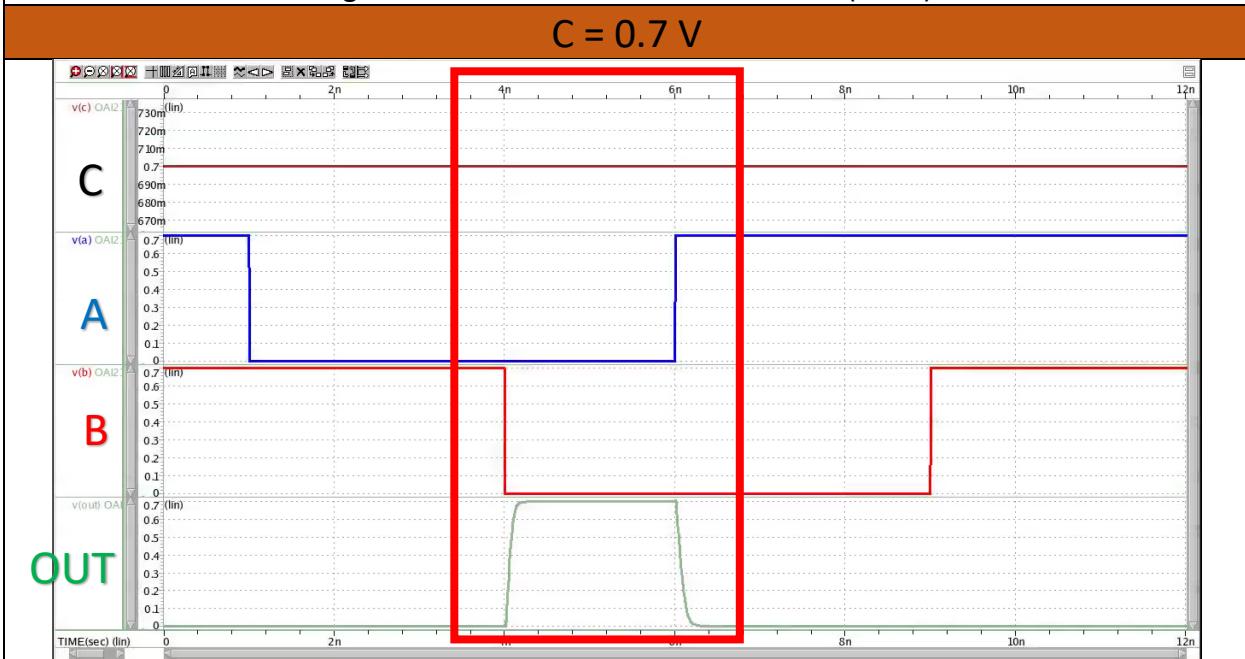


Fig 7-6. OAI21 Terminal Simulation View($C=0.7\text{V}$)

Simulation Analysis

- If $C=0\text{v} \Rightarrow$ The output signal remain 0.7v
- If $C=0.7\text{v} \Rightarrow$ The output signal remain 0v except A & B = 0v

IX. OAI22

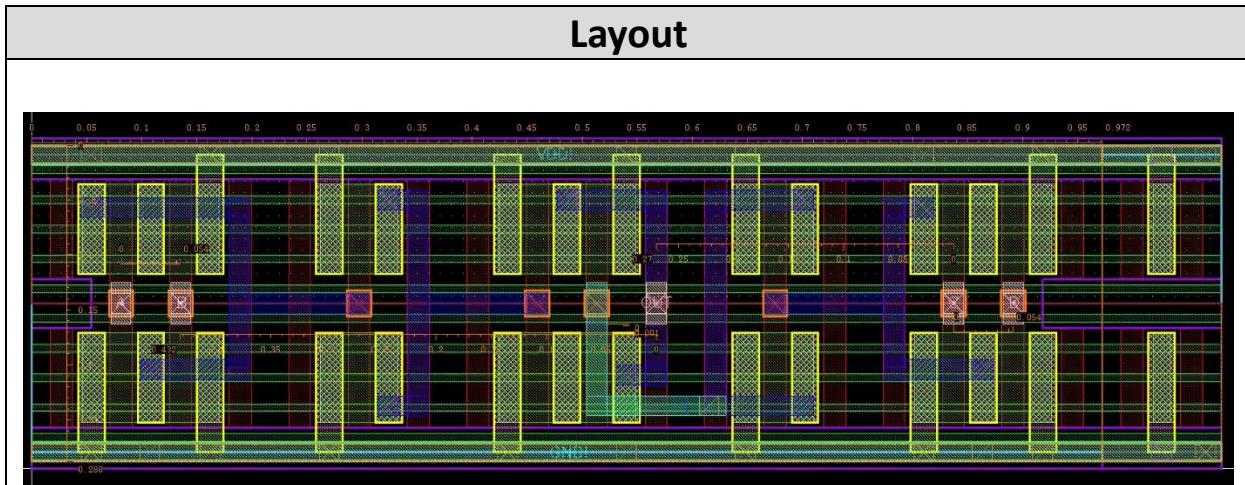


Fig 8-1. OAI22 layout

Template Table

PMOS Width	NMOS Width	Cell Height	Cell Width	Cell Area
0.081um(3 Fins)	0.081um(3 Fins)	0.288um	0.972um	0.279936um ²
Pin(A) to Pin(B)	Pin(B) to Pin(OUT)	Pin(VDD!) to Pin(GND!)	Pin(OUT) to Pin(C)	Pin(C) to Pin(D)
0.054um	0.432um	0.27um	0.27um	0.054um

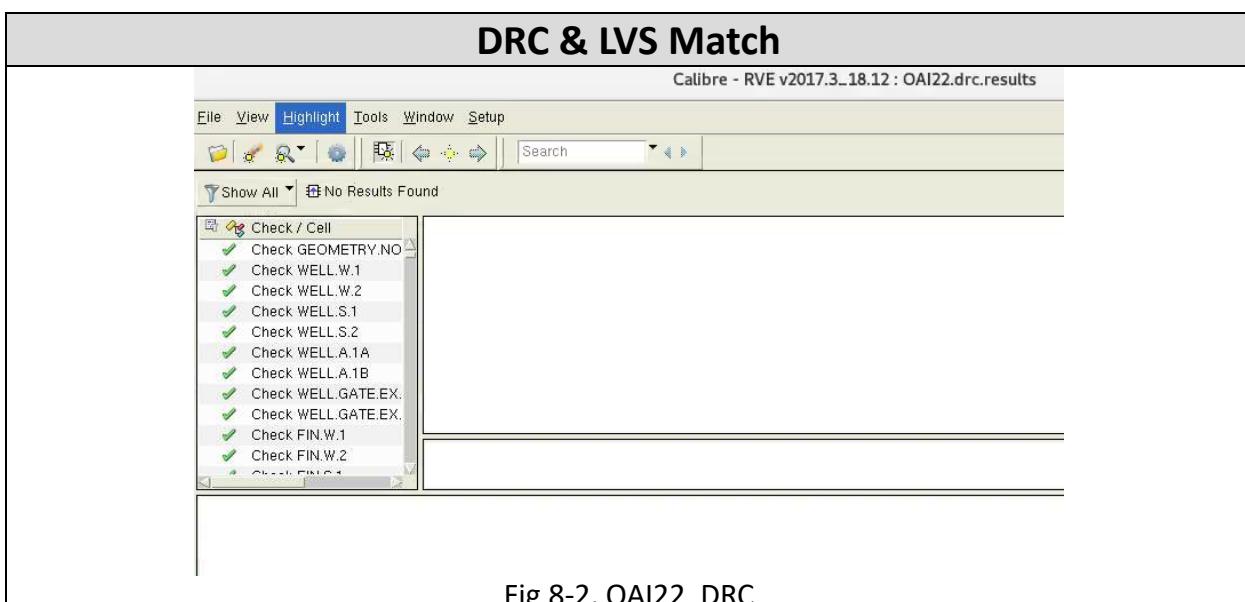
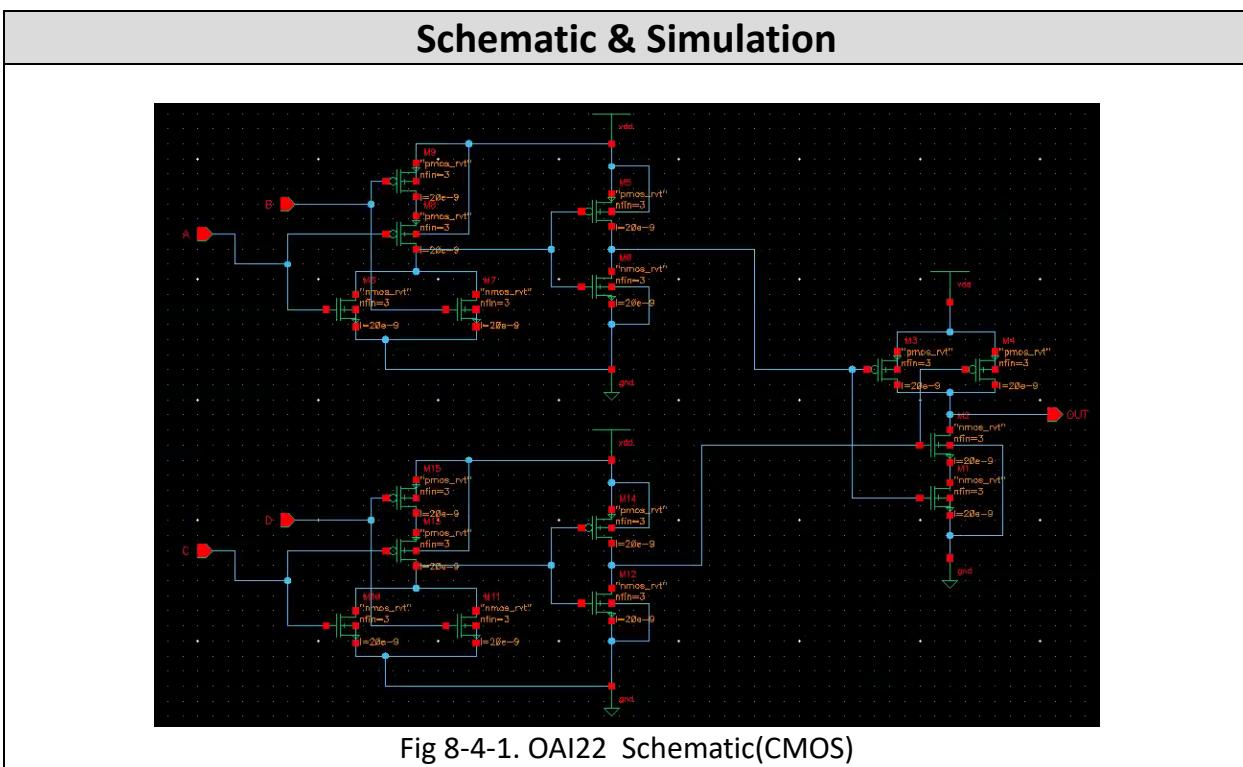
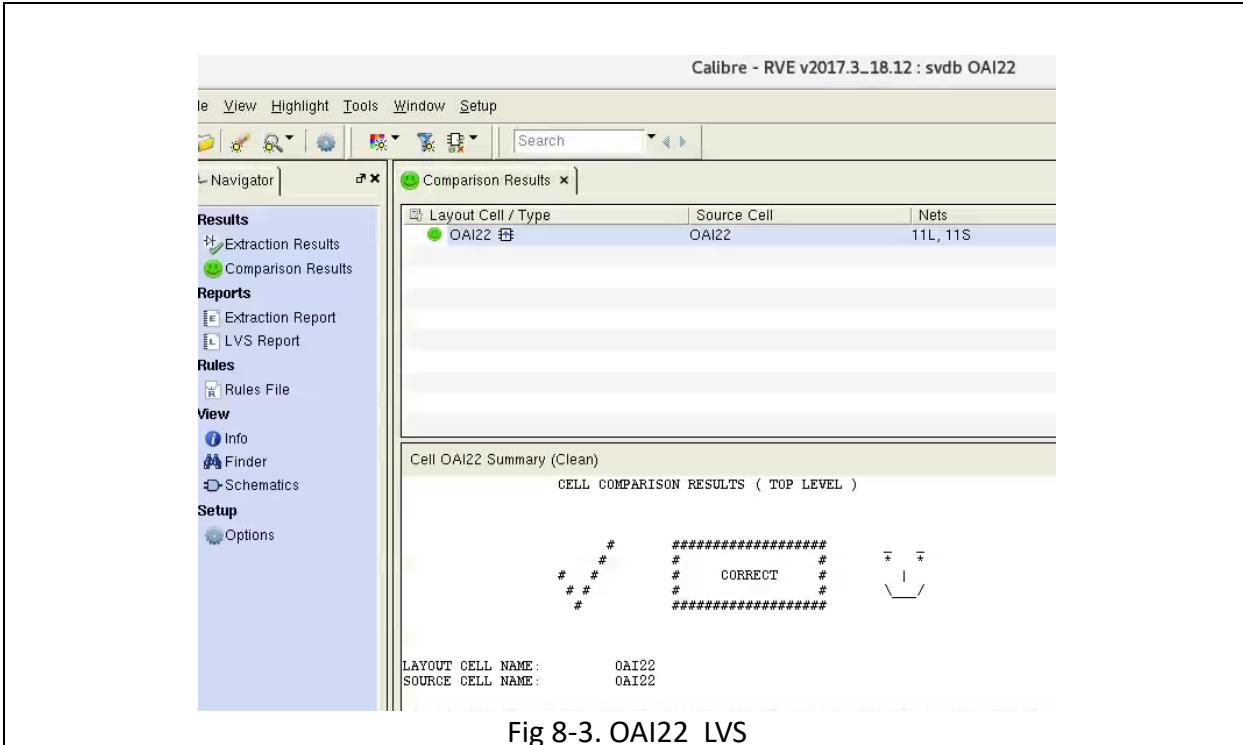


Fig 8-2. OAI22 DRC



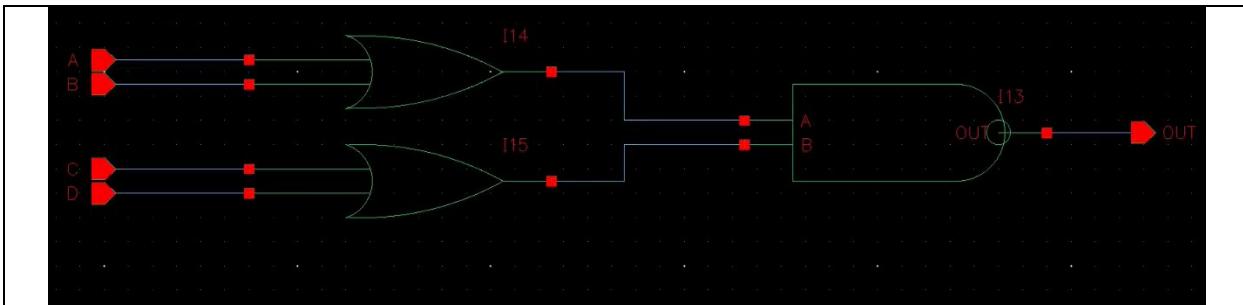


Fig 8-4-2. OAI22 Schematic(Logic Gate)

OAI22 Logic

A	B	C	D	OUT
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	1	0	0	1
0	0	1	1	1
0	1	1	0	0
0	1	0	1	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	1
1	0	1	1	0
1	1	1	0	0
1	1	0	1	0
1	1	1	1	0

A = 0 V

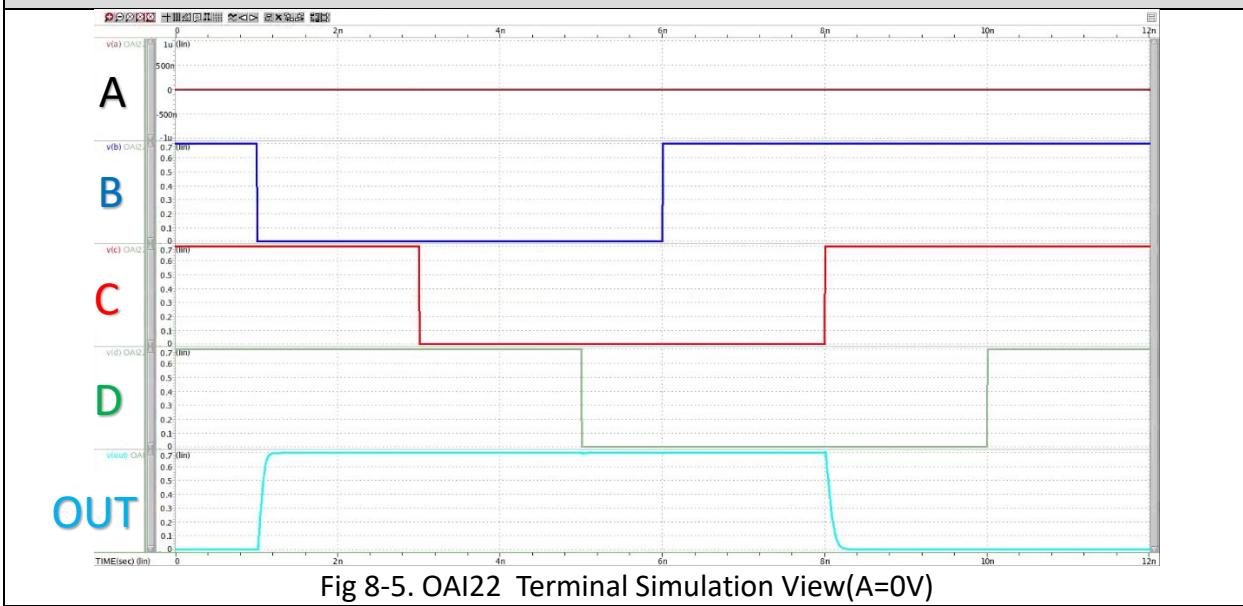


Fig 8-5. OAI22 Terminal Simulation View(A=0V)

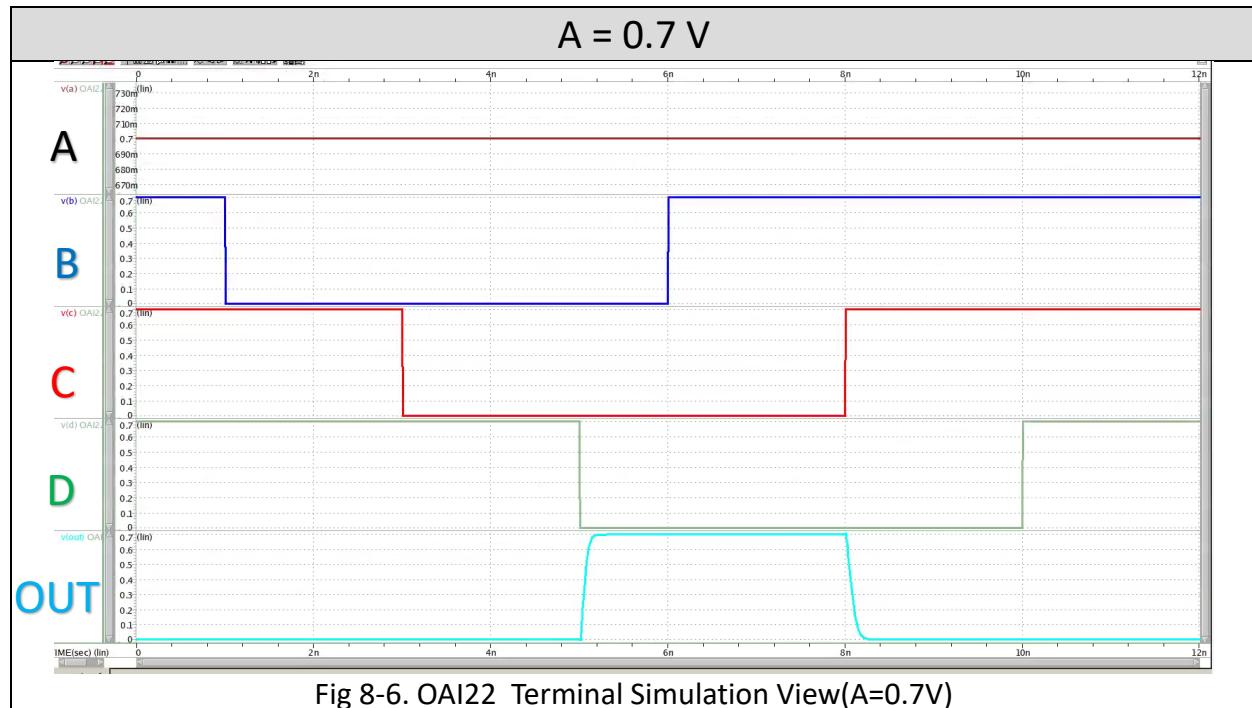


Fig 8-6. OAI22 Terminal Simulation View(A=0.7V)

X. AOI21

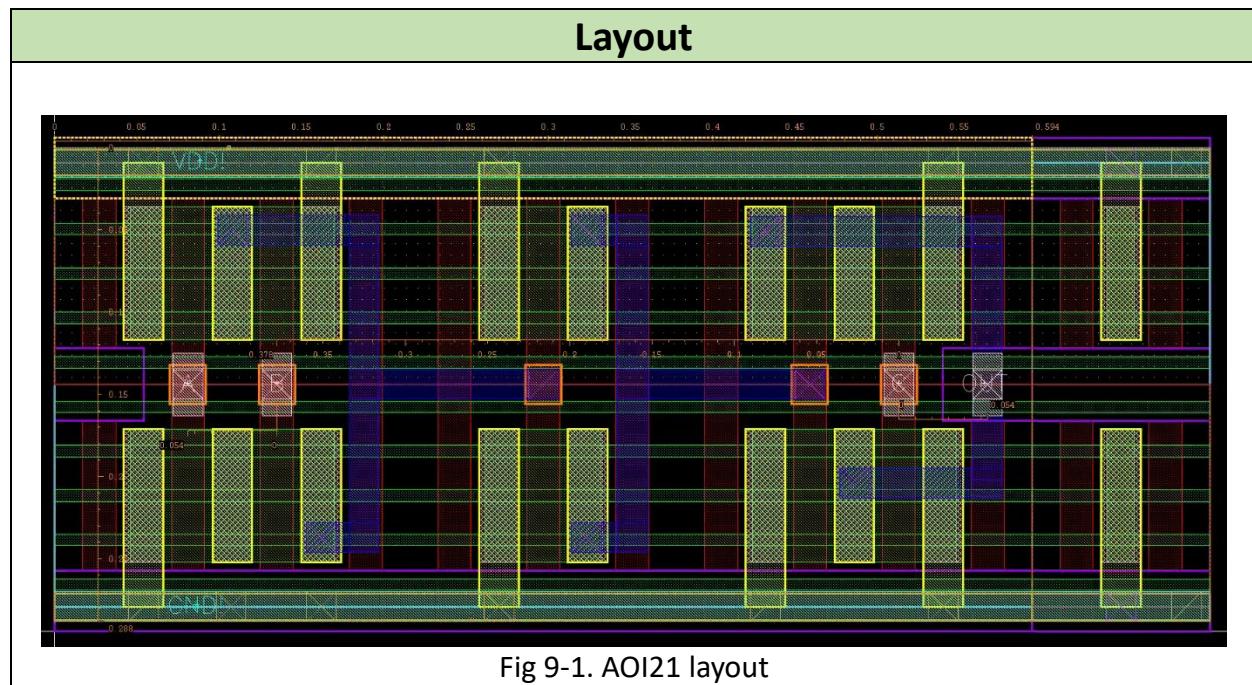


Fig 9-1. AOI21 layout

Template Table

PMOS Width	NMOS Width	Cell Height	Cell Width	Cell Area
0.081um(3 Fins)	0.081um(3 Fins)	0.288um	0.594um	0.171072um ²
Pin(A) to Pin(B)	Pin(B) to Pin(C)	Pin(VDD!) to Pin(GND!)	Pin(C) to Pin(OUT)	
0.054um	0.378um	0.27um	0.054um	

DRC & LVS Match

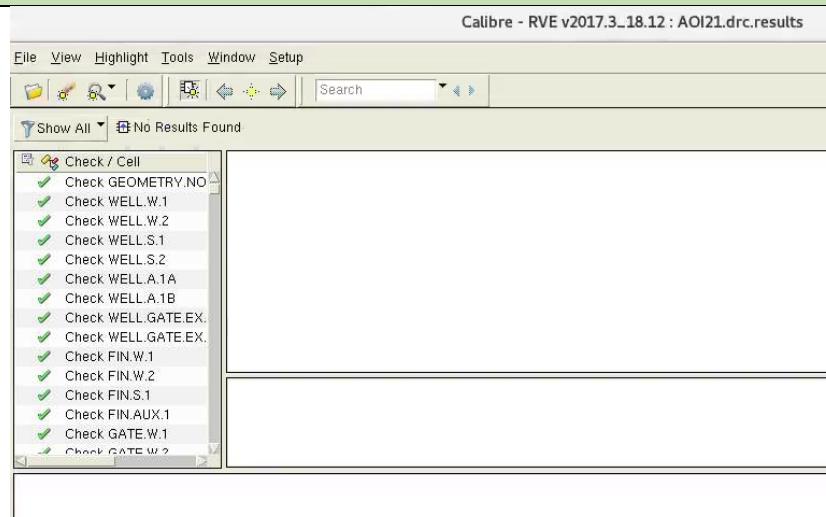


Fig 9-2. AOI21 DRC

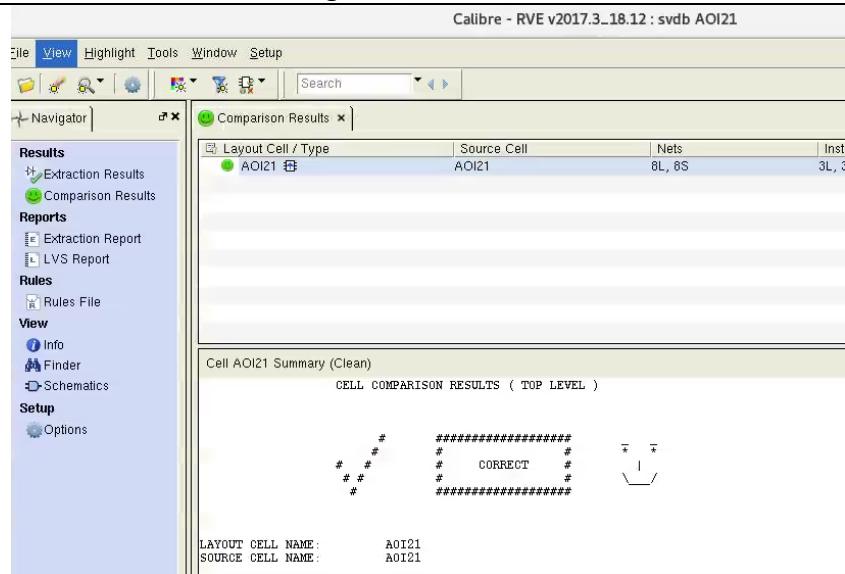


Fig 9-3. AOI21 LVS

Schematic & Simulation

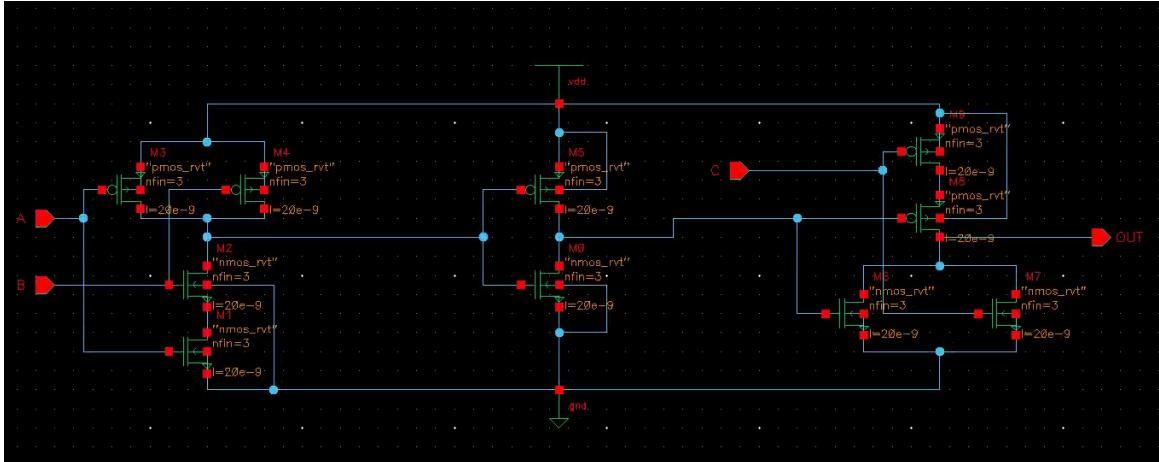


Fig 9-4-1. AOI21 Schematic(CMOS)

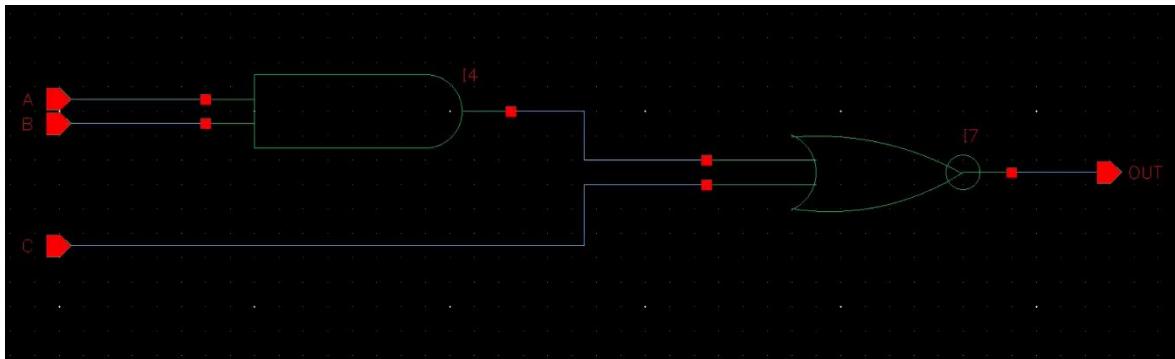


Fig 9-4-2. AOI21 Schematic(Logic Gate)

AOI21 Logic

A	B	C	OUT
0	0	0	1
0	1	0	1
1	0	0	1
1	1	0	0
0	0	1	0
0	1	1	0
1	0	1	0
1	1	1	0

$C = 0.7 \text{ V}$

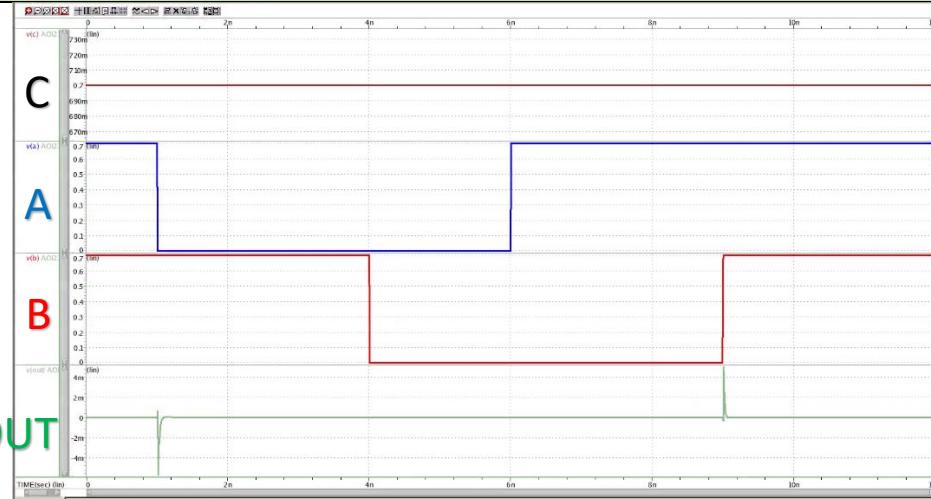


Fig 9-5. AOI21 Terminal Simulation View($C=0\text{V}$)

$C = 0 \text{ V}$



Fig 9-6. AOI21 Terminal Simulation View($C=0.7\text{V}$)

Simulation Analysis

- If $C=0.7\text{v} \Rightarrow$ The output signal remain 0v
- If $C=0\text{v} \Rightarrow$ The output signal remain 0.7v except A & B = 0.7v

XI. AOI22

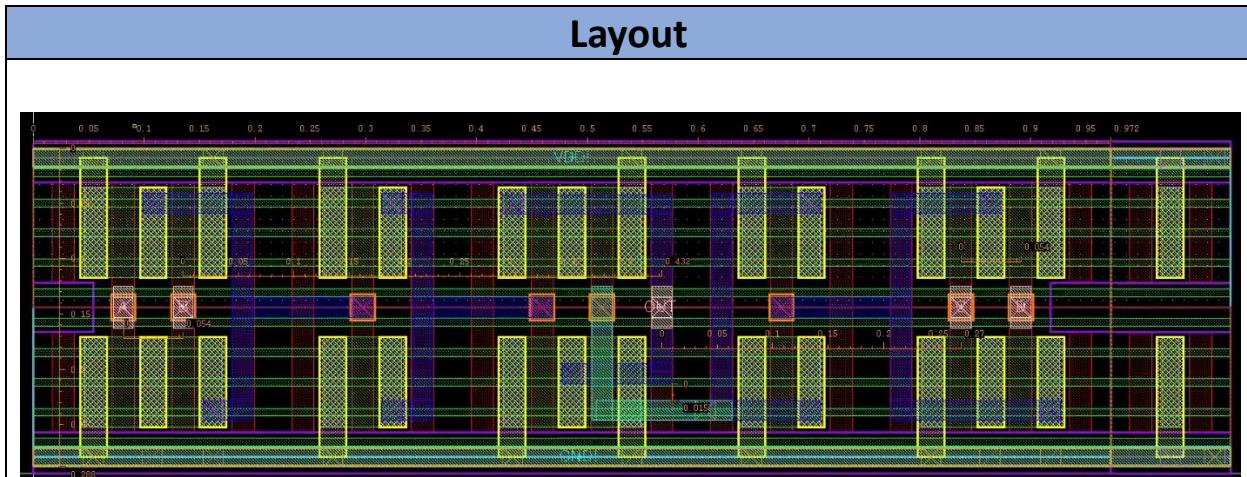


Fig 10-1. AOI22 layout

Template Table				
PMOS Width	NMOS Width	Cell Height	Cell Width	Cell Area
0.081um(3 Fins)	0.081um(3 Fins)	0.288um	0.972um	0.279936um ²
Pin(A) to Pin(B)	Pin(B) to Pin(OUT)	Pin(VDD!) to Pin(GND!)	Pin(OUT) to Pin(C)	Pin(C) to Pin(D)
0.054um	0.432um	0.27um	0.27um	0.054um

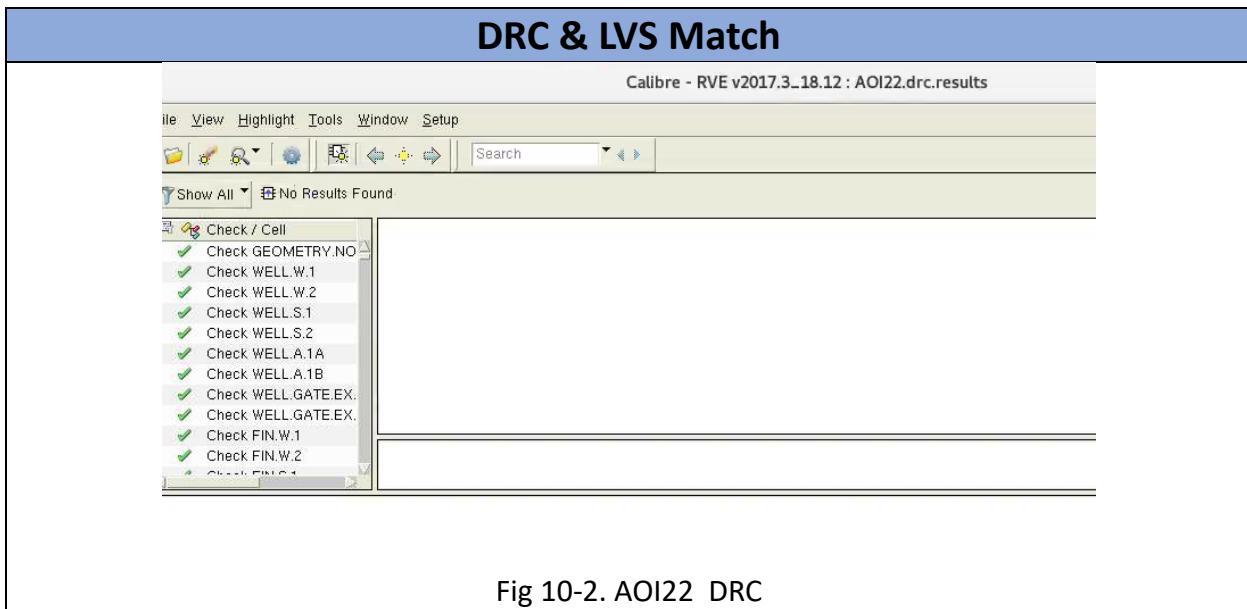


Fig 10-2. AOI22 DRC

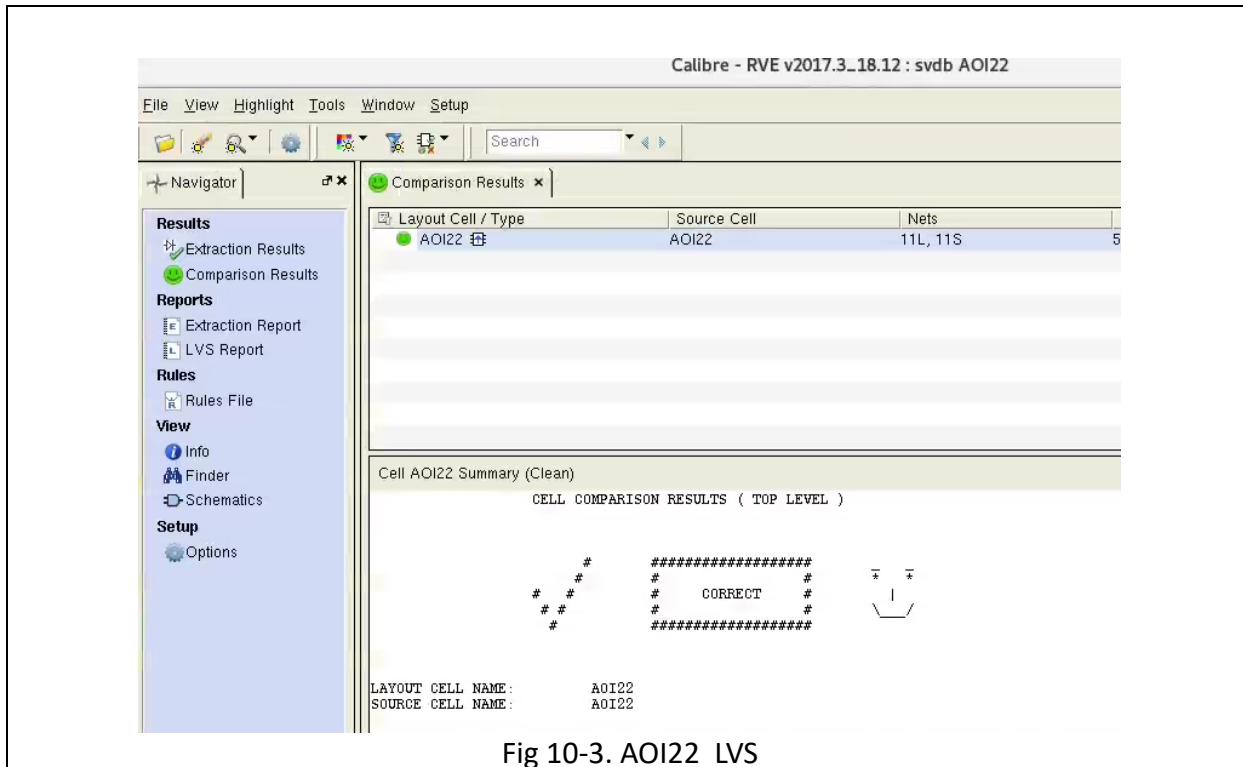
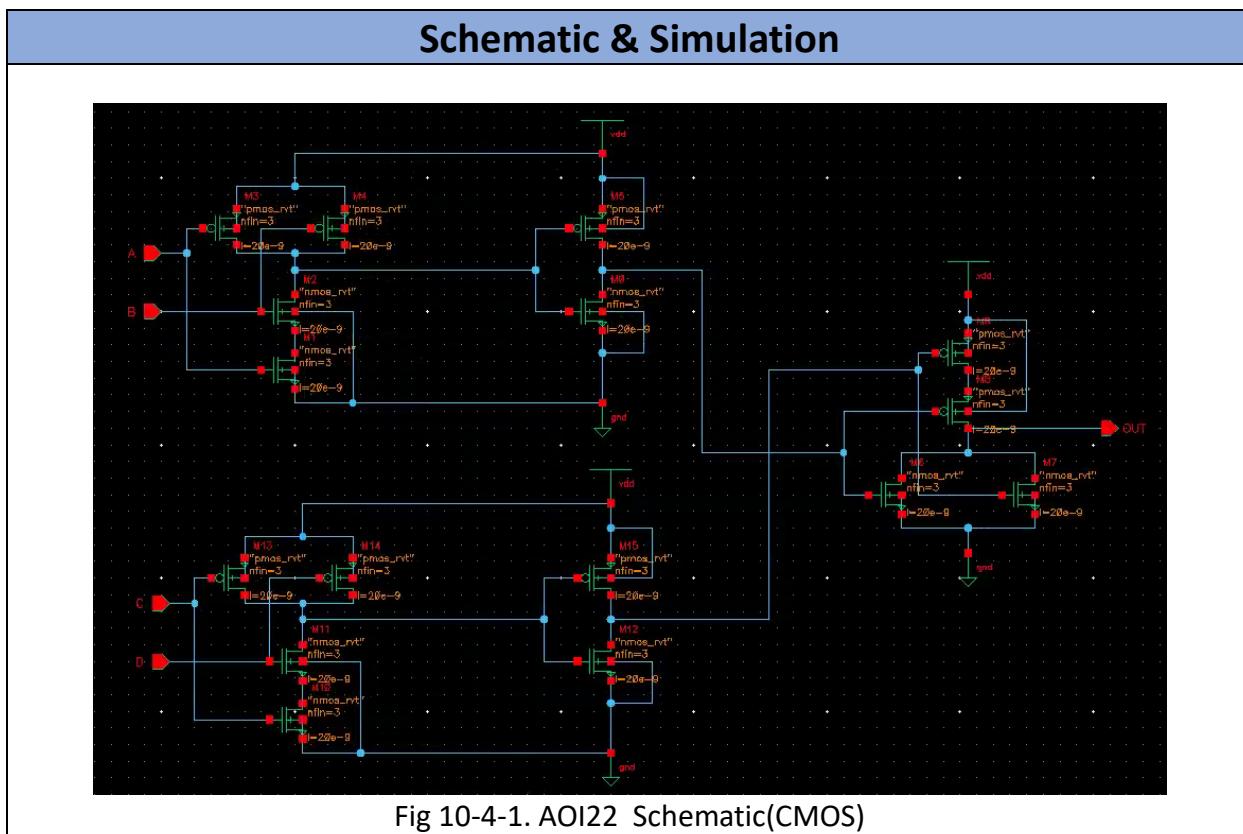


Fig 10-3. AOI22 LVS



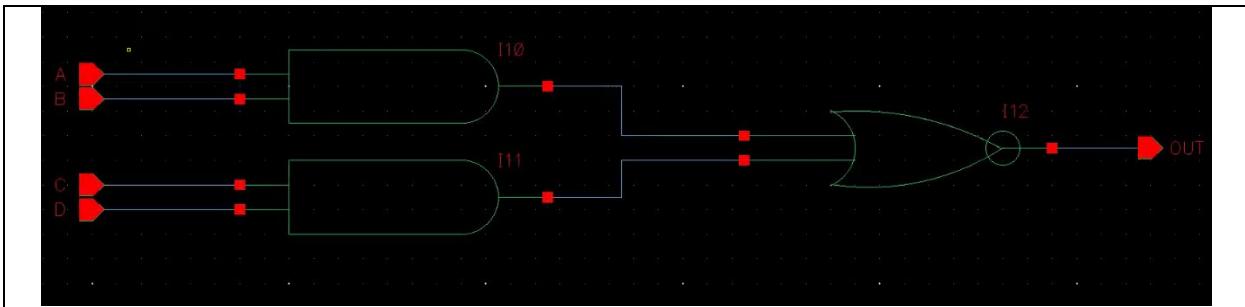


Fig 10-4-2. AOI22 Schematic(Logic Gate)

AOI22 Logic

A	B	C	D	OUT
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	1	0	0	1
0	0	1	1	0
0	1	1	0	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	0
1	1	0	1	0
1	1	1	1	0

A = 0 V

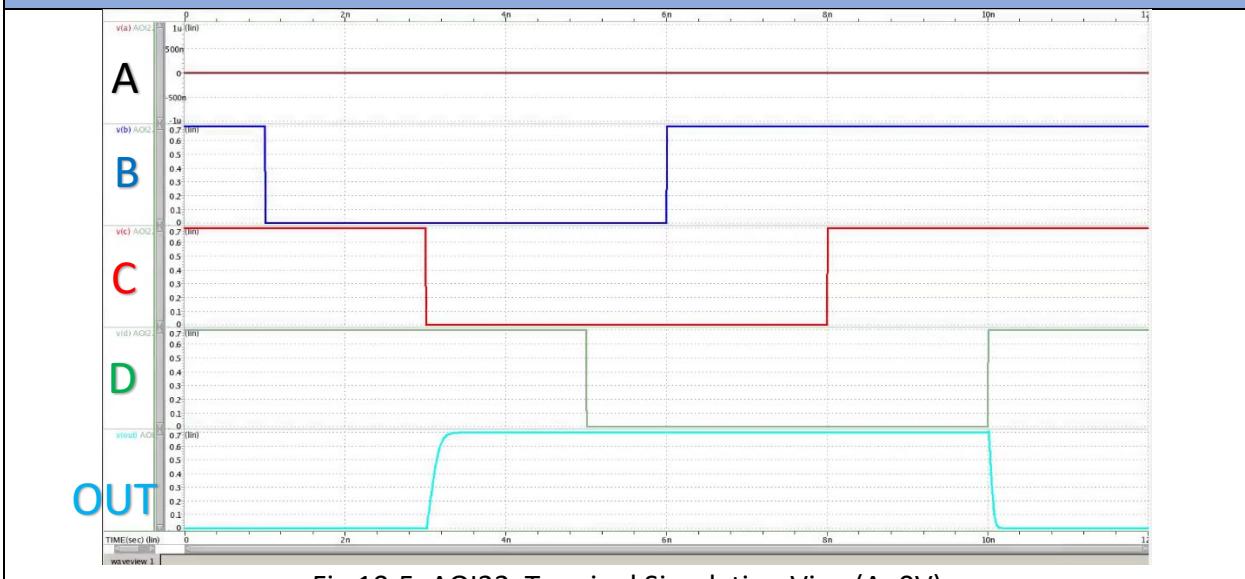


Fig 10-5. AOI22 Terminal Simulation View(A=0V)

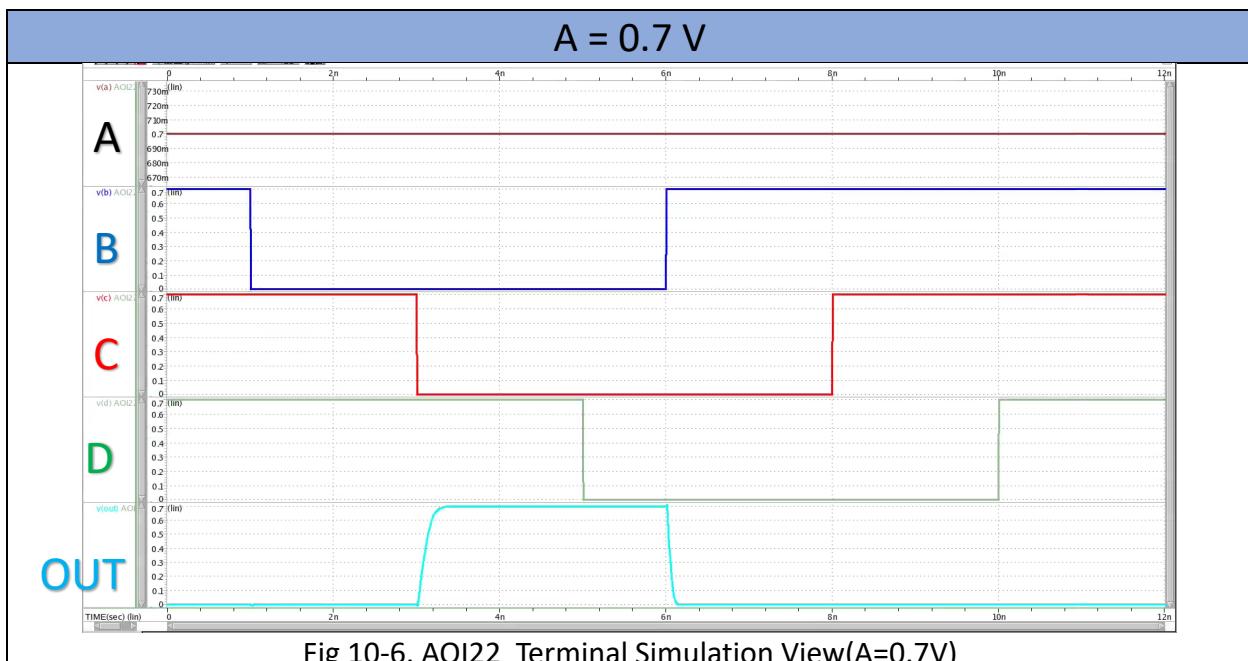


Fig 10-6. AOI22 Terminal Simulation View(A=0.7V)

XII. DFF

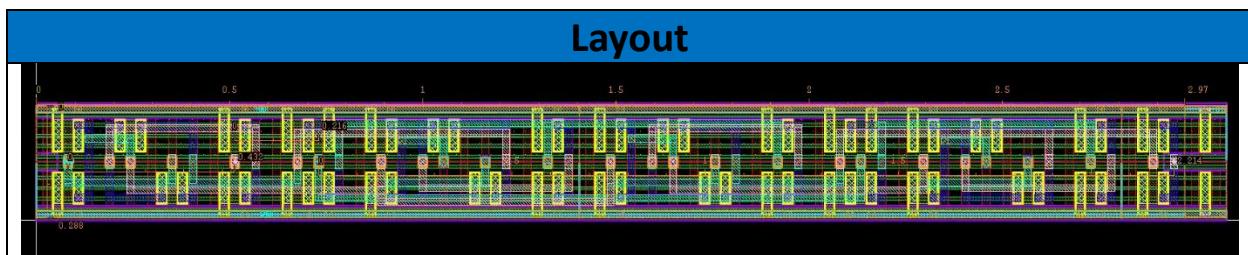


Fig 11-1-1. DFF layout(Full DFF)

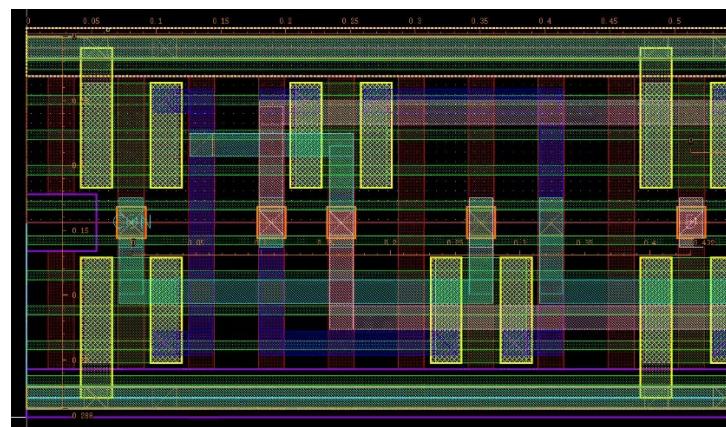


Fig 11-1-2. DFF layout(CON to D)

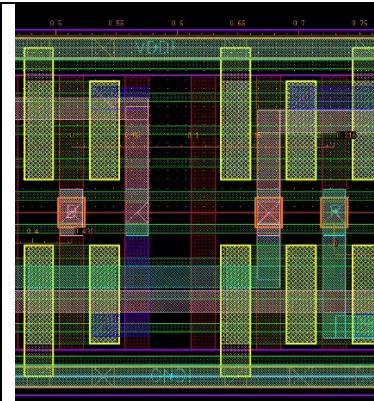


Fig 11-1-3. DFF layout(D to R)

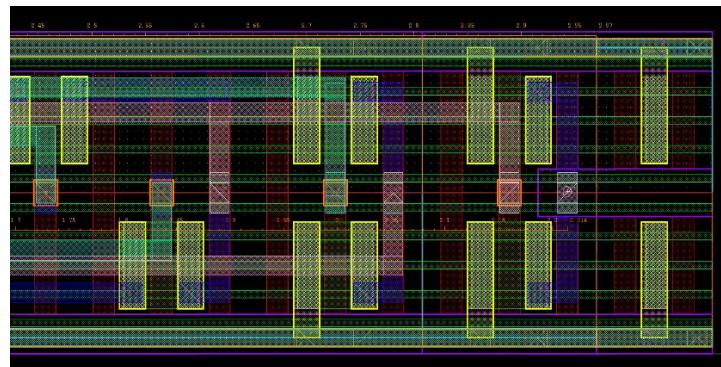


Fig 11-1-4. DFF layout(R to Q)

Template Table

PMOS Width	NMOS Width	Cell Height	Cell Width	Cell Area
0.081um(3 Fins)	0.081um(3 Fins)	0.288um	2.97um	0.85536um ²
Pin(CON) to Pin(D)	Pin(D) to Pin(R)		Pin(VDD!) to Pin(GND!)	Pin(R) to Pin(Q)
0.432um	0.216um		0.27um	2.214um

DRC & LVS Match

Calibre - RVE v2017.3_18.12 : DFF.drc.results

File View Highlight Tools Window Setup

Show All ▾ No Results Found

Check / Cell

- ✓ Check GEOMETRY.NO
- ✓ Check WELL.W.1
- ✓ Check WELL.W.2
- ✓ Check WELL.S.1
- ✓ Check WELL.S.2
- ✓ Check WELL.A.1A
- ✓ Check WELL.A.1B
- ✓ Check WELL.GATE.EX.
- ✓ Check WELL.GATE.EX.
- ✓ Check FIN.W.1
- ✓ Check FIN.W.2
- ✓ Check FIN.G1

Fig11-2. DFF DRC

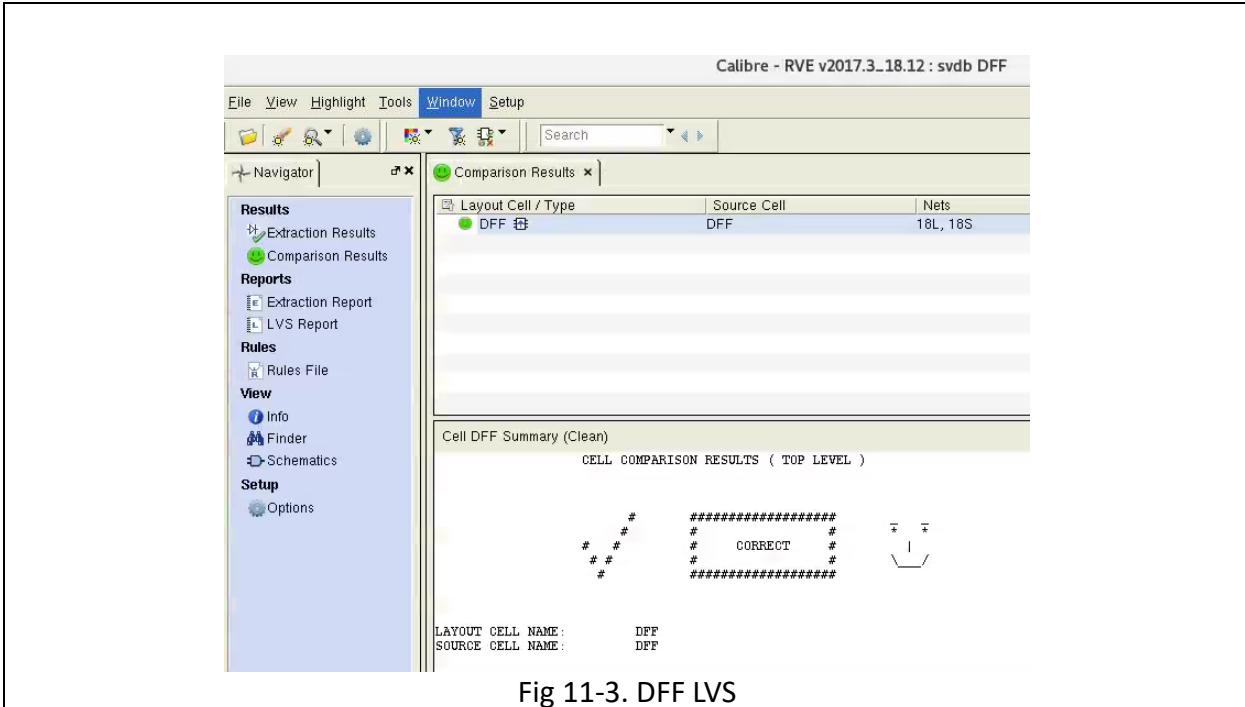


Fig 11-3. DFF LVS

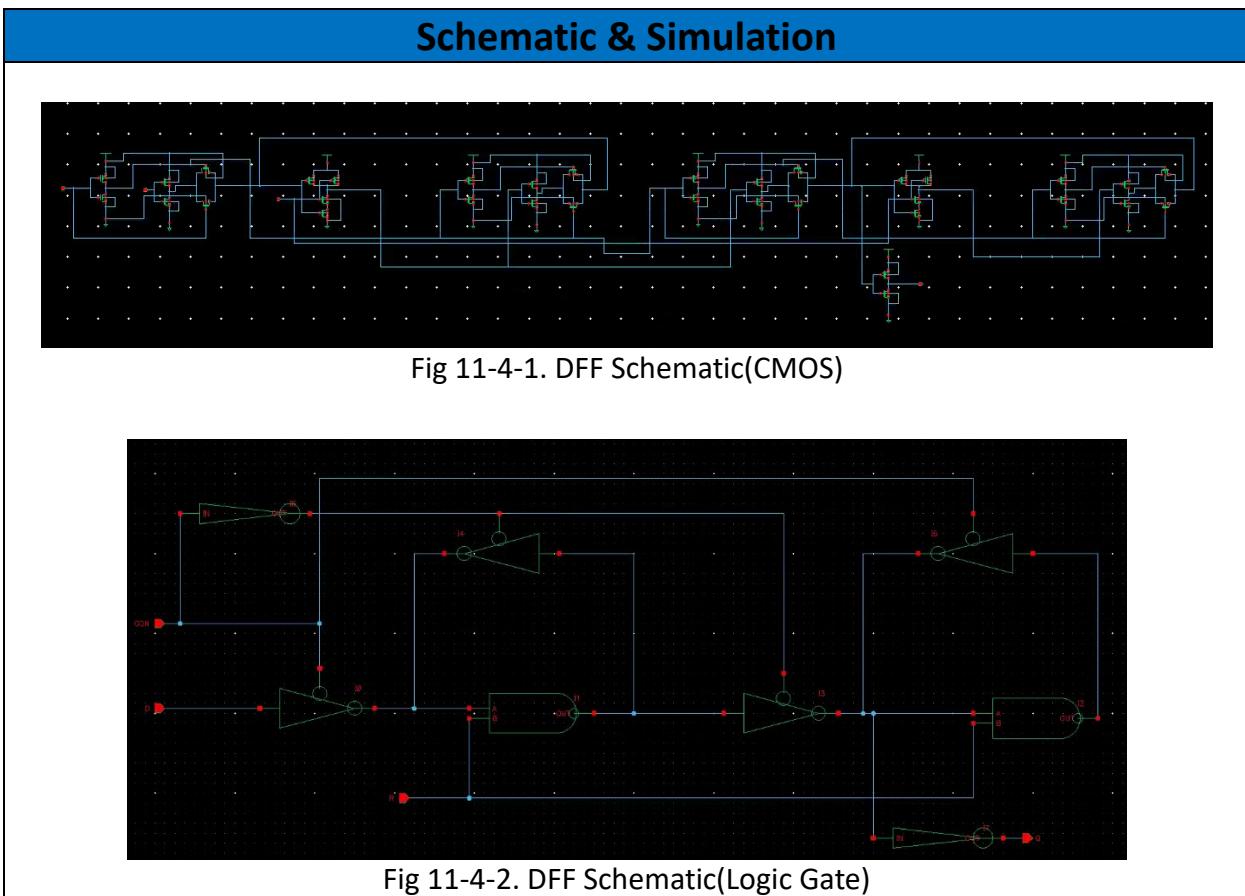


Fig 11-4-1. DFF Schematic(CMOS)

Fig 11-4-2. DFF Schematic(Logic Gate)

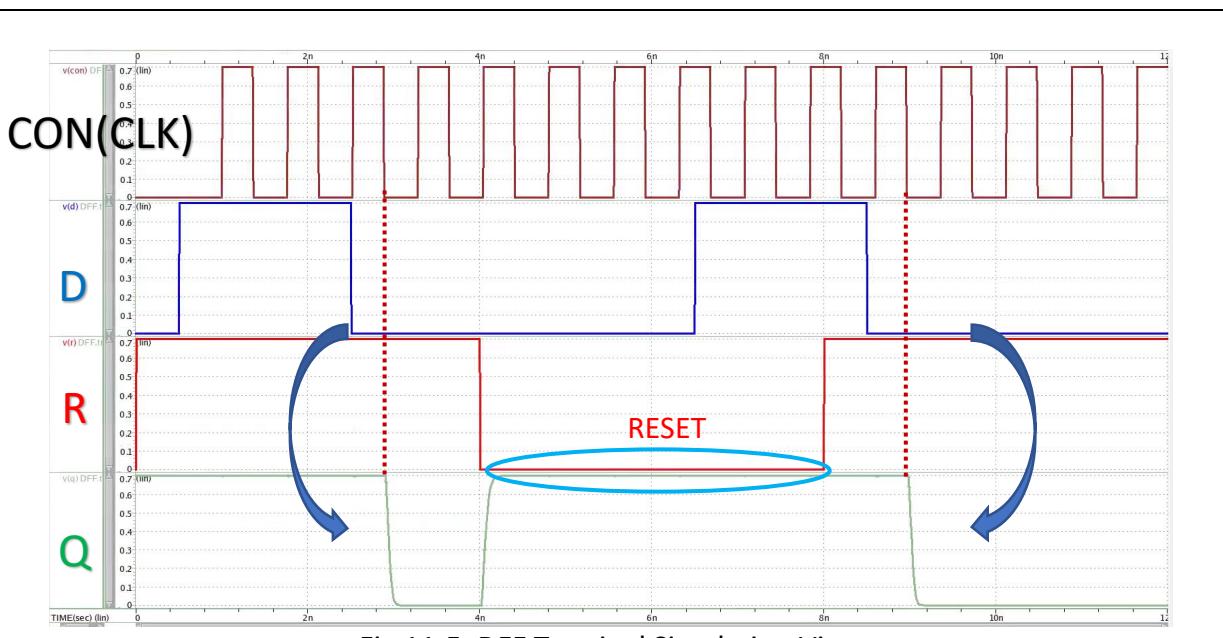


Fig 11-5. DFF Terminal Simulation View

Simulation Analysis

- This is a negative edge triggered D flip flop
- If CLK get down and D signal is different from Q signal, Q will follow D signal
- When Reset=0v, Q will reset to initial state(0.7v)

XIII. Final Layout

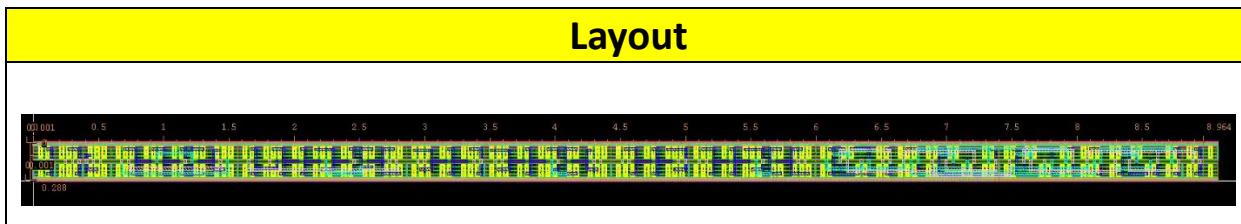


Fig 12-1. All Cells layout

Template Table

PMOS Width	NMOS Width	Cell Height	Cell Width	Cell Area
0.081um(3 Fins)	0.081um(3 Fins)	0.288um	8.964um	2.581632um ²

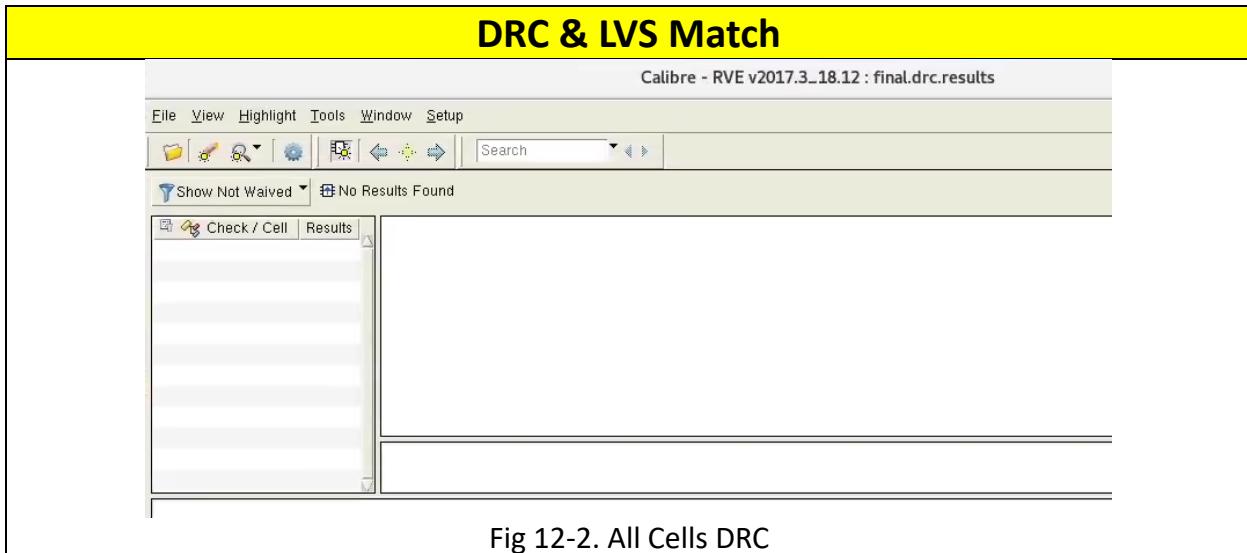


Fig 12-2. All Cells DRC

XIV. Conclusion

After completing this project, I learned the rules about the 7nm cells library and how to create the 7nm layout. The composition is different from the 130nm layout, but most of layout skills are similar. Thus, I can create the layout more quickly than I designed the 130nm layout at the first time. I am glad that I could learn much more simulated skills and used the knowledge what I learned in this class when I did this project.

XV. Reference

- Class note
- Asap7_tutorial word file