EECT 6326 Analog Integrated Circuit Design

Design of an Operational Amplifier

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I. Introduction

For this project, we need to design a differential input single-ended output single-stage amplifier. I can use 2V power supply and only one idea current source to design the op amplifier in TSMC 0.35-um technology. However, the gain of the single stage op amplifier must over 85dB. This specification is not difficult if we use two stage op amplifier. Thus, I choose the Telescopic Cascode Op Amplifier as our design. I can increase the gain value by Cascode circuit to match the gain what I want.

II. Design Requirements

1. Differential voltage gain: Avd $\geq$ 85 dB.

2. Output voltage swing range: OVSR = Vo(max) – Vo(min) $\geq$ 1.3 V.

3. Average slew rate: SR $\geq$ 10 V/us (Average slew rate = (SR+ + SR-)/2).

4. Common mode rejection ratio: CMRR $\geq$ 80 dB.

5. Unity-gain bandwidth: GBW $\geq$ 8 MHz.

6. Phase margin: f(GBW) $\geq$ 60°.

7. Power dissipation (VDD): Pdiss $\leq$ 0.5 mW (2V) including power dissipation from all current mirrors and the current source.

8. Capacitive load: 3 pF

III. Value Table

Specifications	Required	Obtained
Avd	≥ 85 dB	86.87dB
OVSR	≥ 1.3 V	1.307V
SR	≥ 10 V/us	8.907 V/us
CMRR	≥ 80 dB	87.57dB
GBW	≥ 8 MHz	10.2MHz
PM	≥ 60°	61.52°
P_{diss}	≤ 0.5 mW (2V)	0.125mW(2V)

IV. Circuit Schematic and symbol

Amplifier Schematic

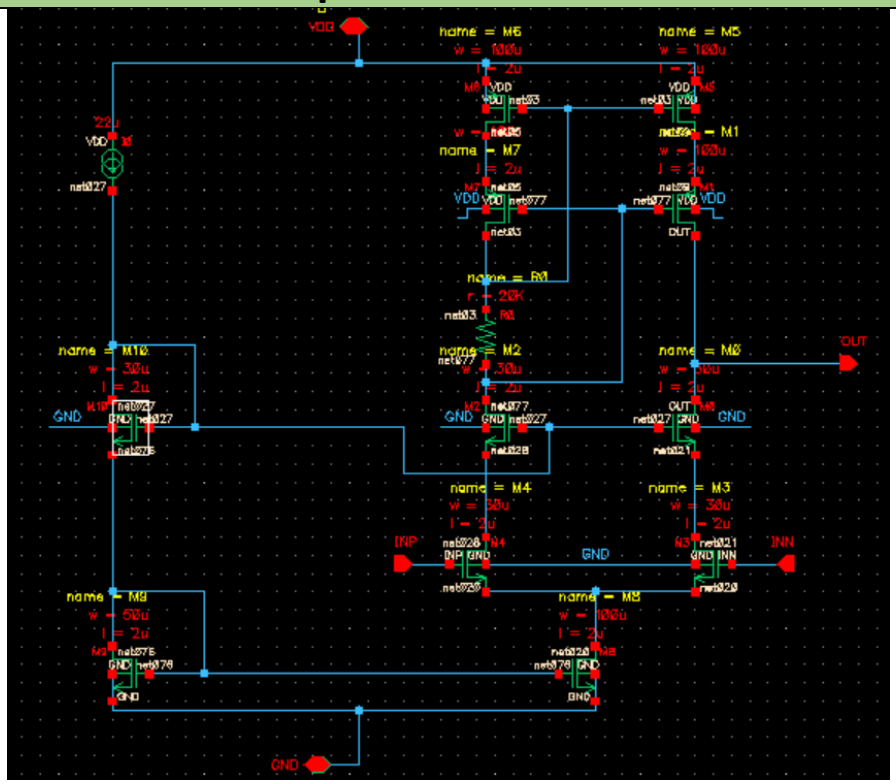

Fig. 1 Amplifier Schematic

Parameter Table			
Transistor	Width(W)	Length(L)	Current
M0(NMOS)	30um	2um	20.43uA
M1(PMOS)	100um	2um	20.43uA
M2(NMOS)	30um	2um	20.43uA
M3(NMOS)	30um	2um	20.43uA
M4(NMOS)	30um	2um	20.43uA
M5(PMOS)	100um	2um	20.43uA
M6(PMOS)	100um	2um	20.43uA
M7(PMOS)	100um	2um	20.43uA
M8(NMOS)	100um	2um	40.87uA
M9(NMOS)	50um	2um	22.0uA
M10(NMOS)	30um	2um	22.0uA
Current Source			22uA
Load Capacitance	3pF		0
R0	20kΩ		20.43uA

Node voltage and Current

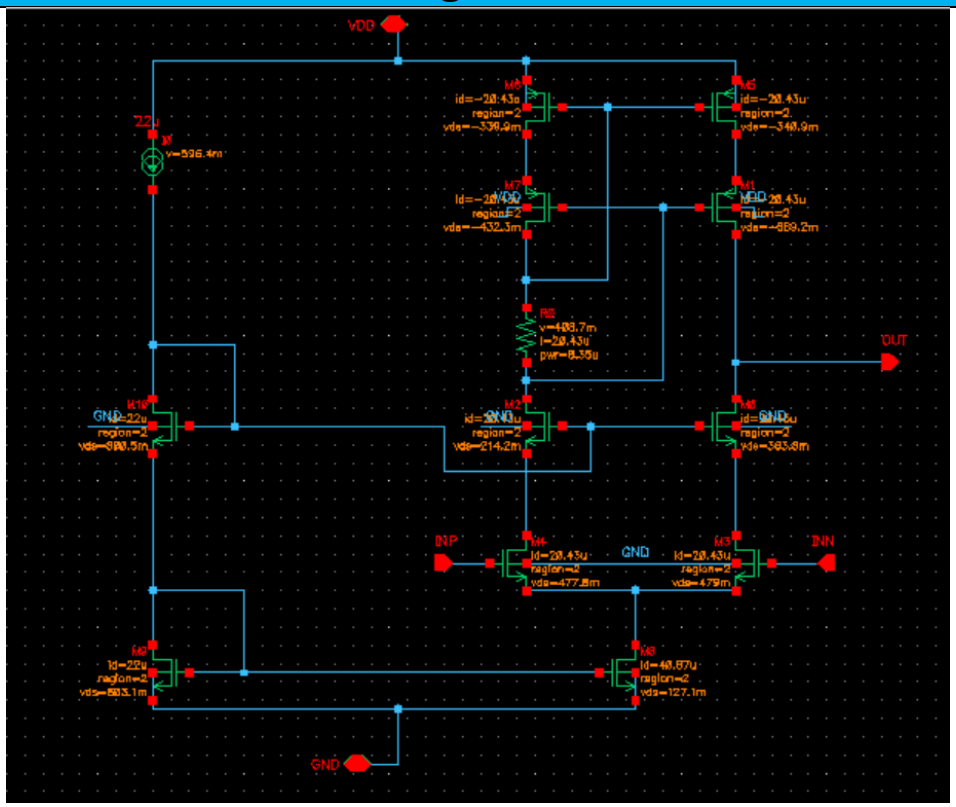

Fig. 2 Amplifier Node voltage and Current

V. Simulation Result

Symbol of amplifier

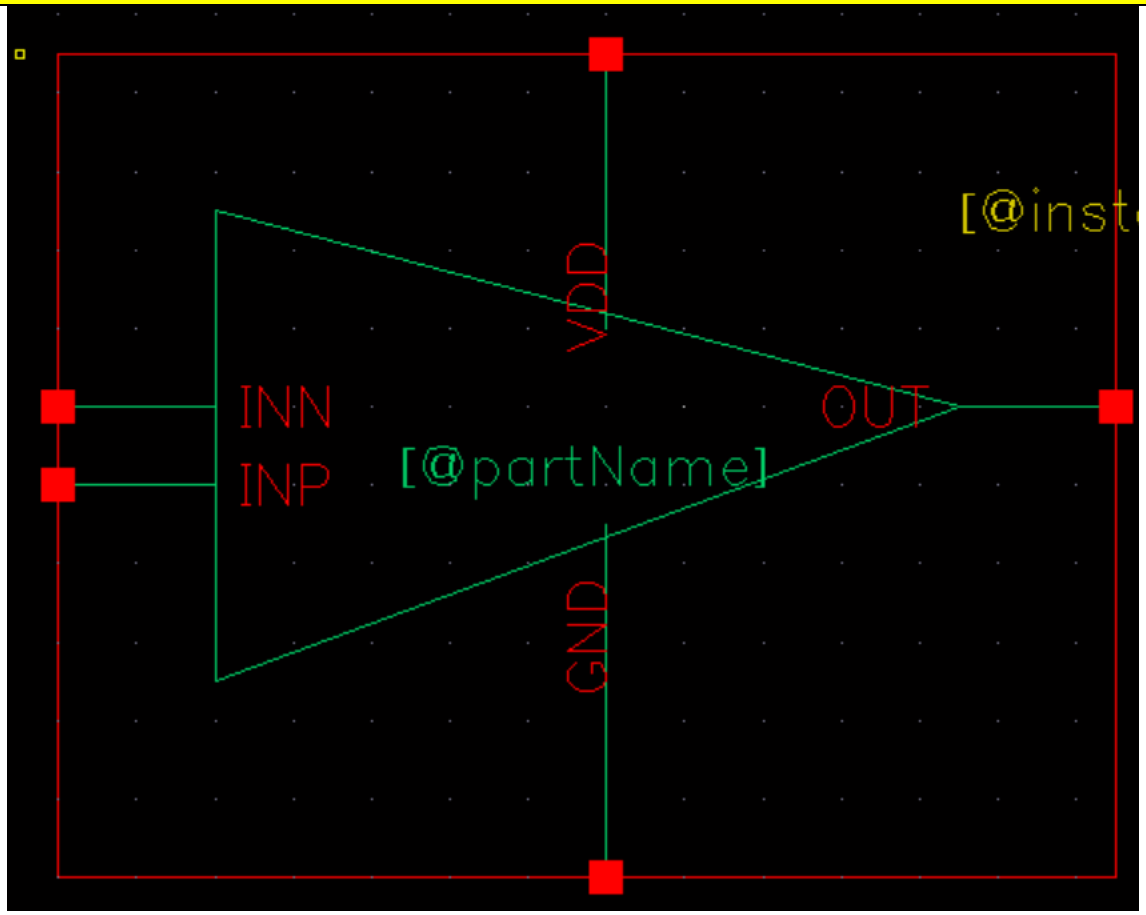

Fig. 3 Amplifier of symbol

Operating region(All Saturation Region)

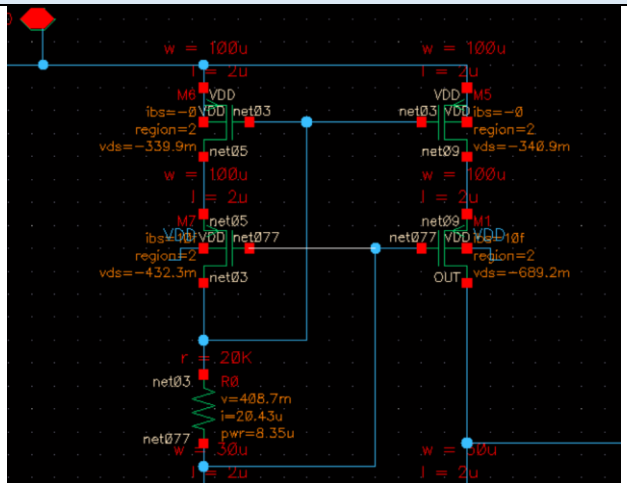

Fig. 4-1 Pmos Region

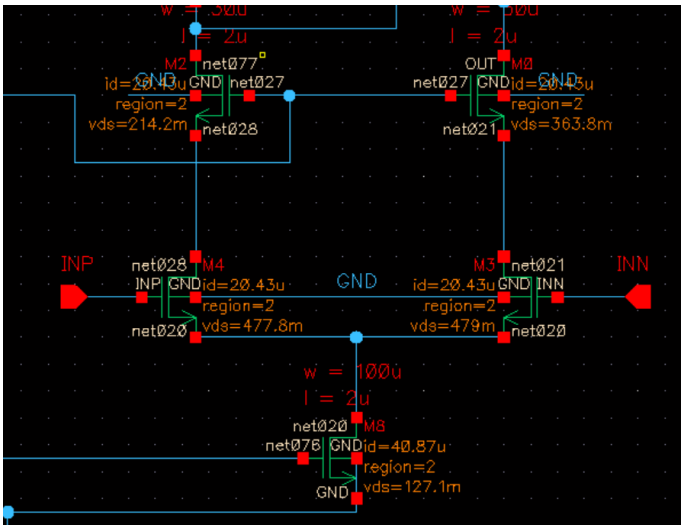

Fig. 4-2 Nmos Region

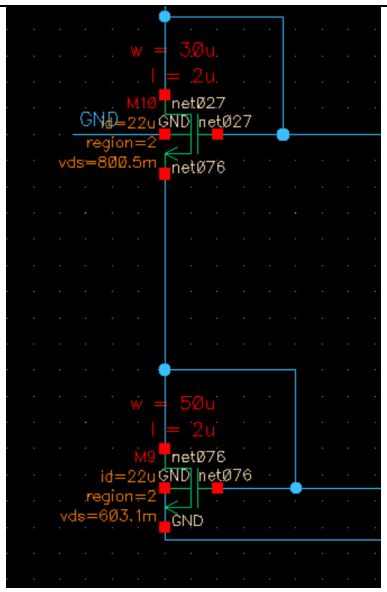

Fig. 4-3 Current Source Region

Region=2 show the MOS is in Saturation Region

Differential Voltage Gain A_{vd}

Simulation circuit

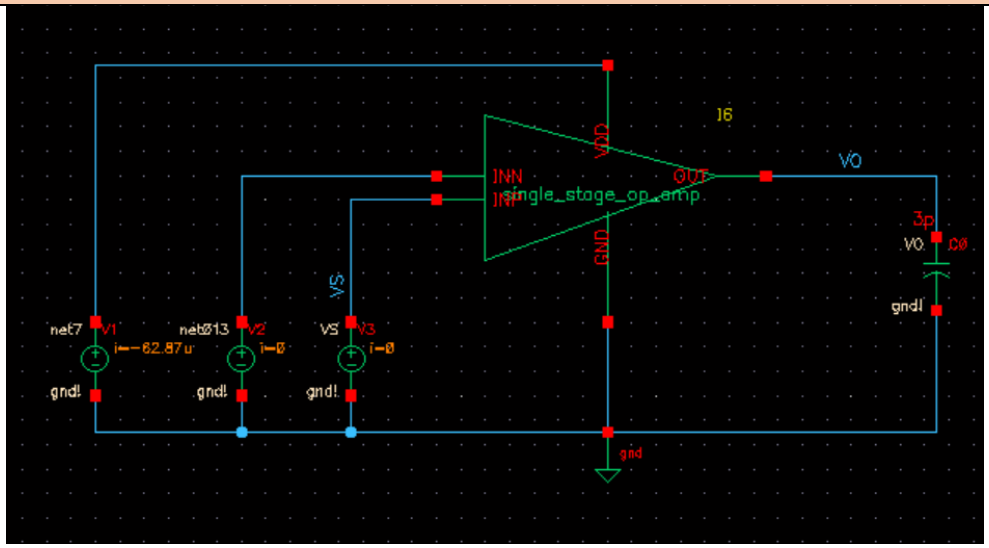

Fig. 5 Gain simulation Schematic

Simulation (A_{vd})

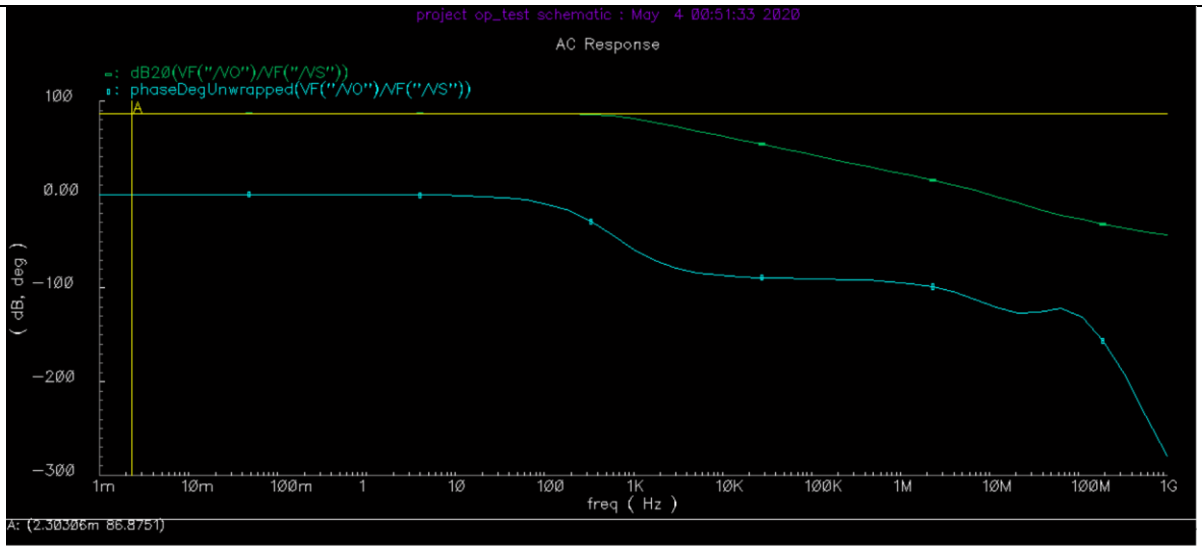

Fig. 6 A_{vd} simulation result

A_{vd}=86.8751dB

Unity-gain bandwidth (GBW)

Simulation (GBW)

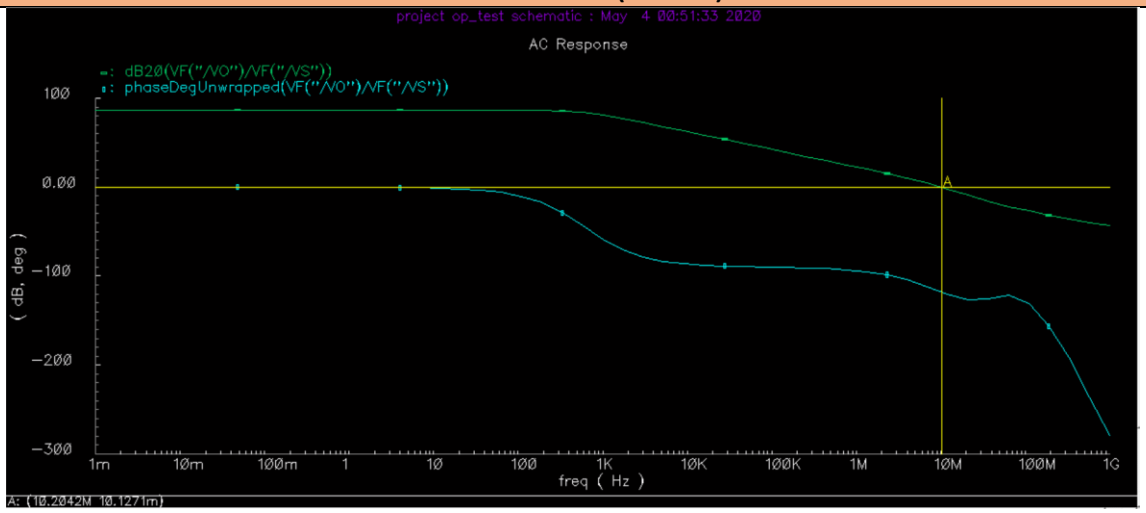

Fig. 7 GBW simulation result

GBW=10.2042MHz

Phase Margin (PM)

Simulation (PM)

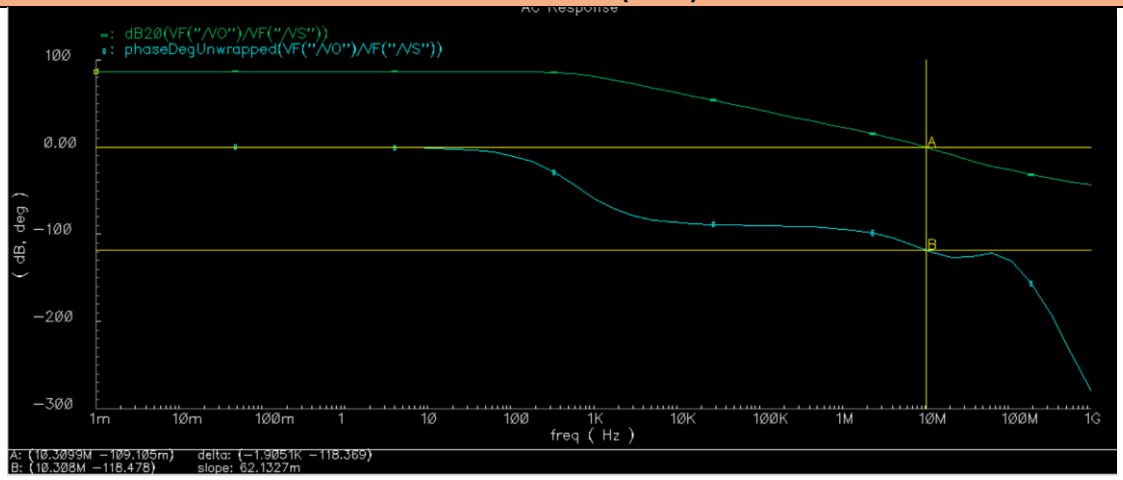

Fig. 8 PM simulation result

PM = 180°-118.478° = 61.522°

Common Mode Rejection Ratio (CMRR)

Simulation (CMRR)

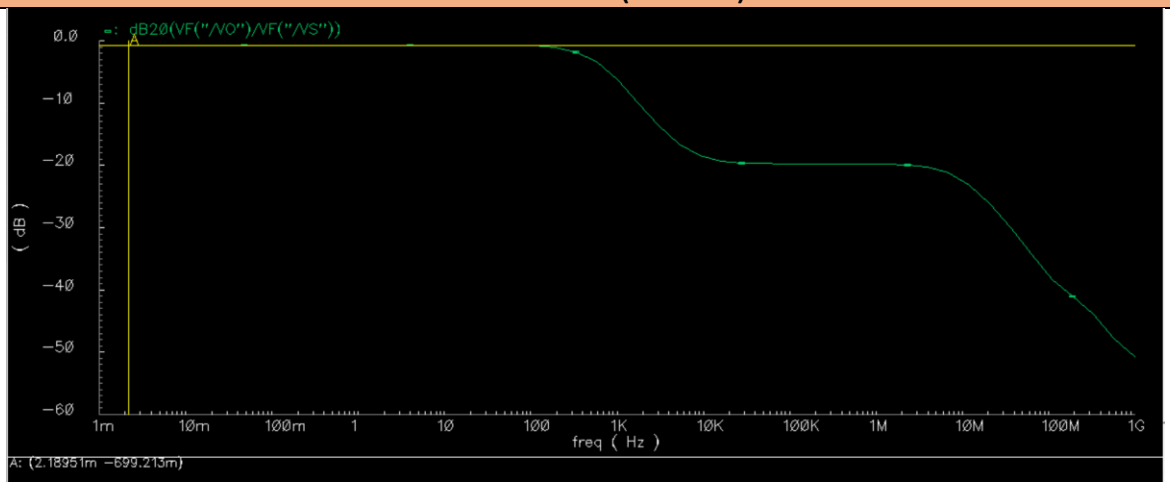

Fig. 9 CMRR simulation result

CMRR = $\frac{Avd}{Acm}$= 86.87dB-(-0.699dB) = 87.571dB

Output Voltage Swing Range (OVSR)

Simulation circuit

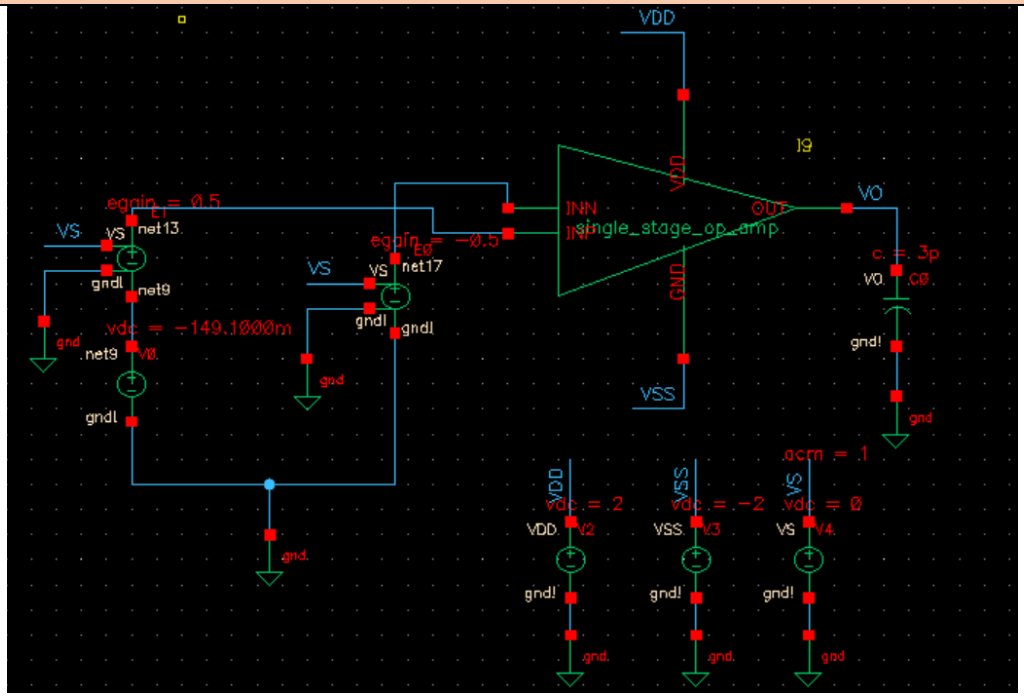

Fig. 10 OVSR simulation Schematic

Simulation (OVSR)

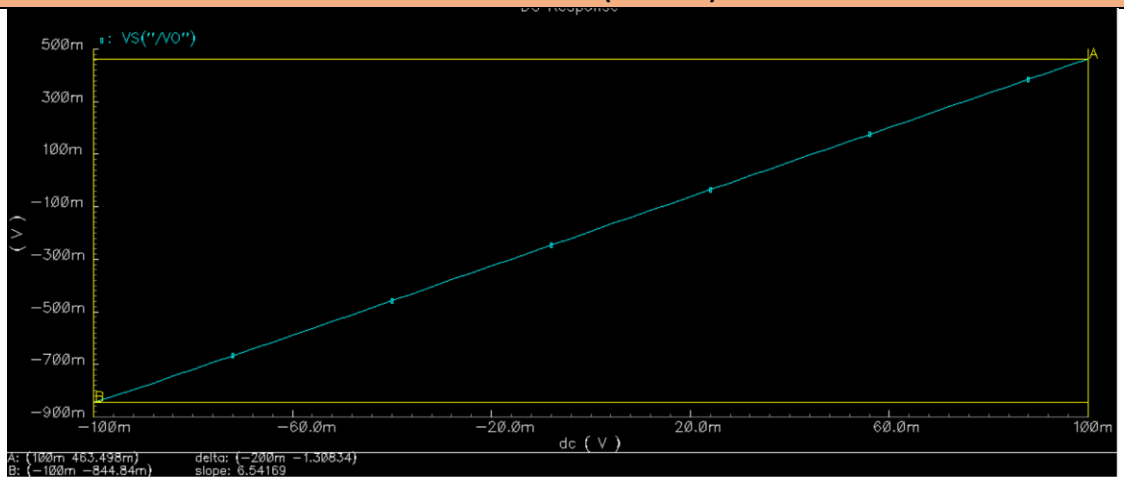

Fig. 11 OVSR simulation result

OVSR=Vo(max)-Vo(min)=0.463-(-0.844) = 1.307V

Average Slew Rate(SR)

Simulation circuit

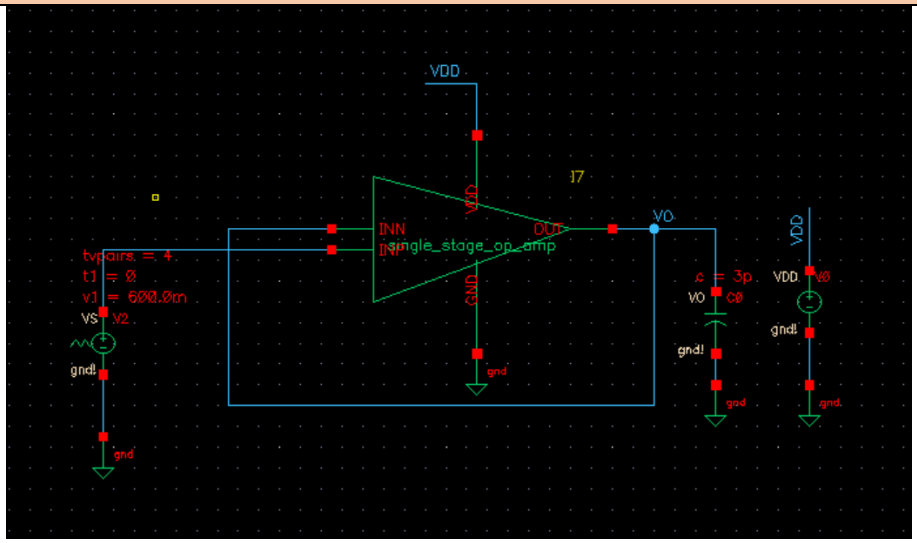

Fig. 12 SR simulation Schematic

Simulation (SR)

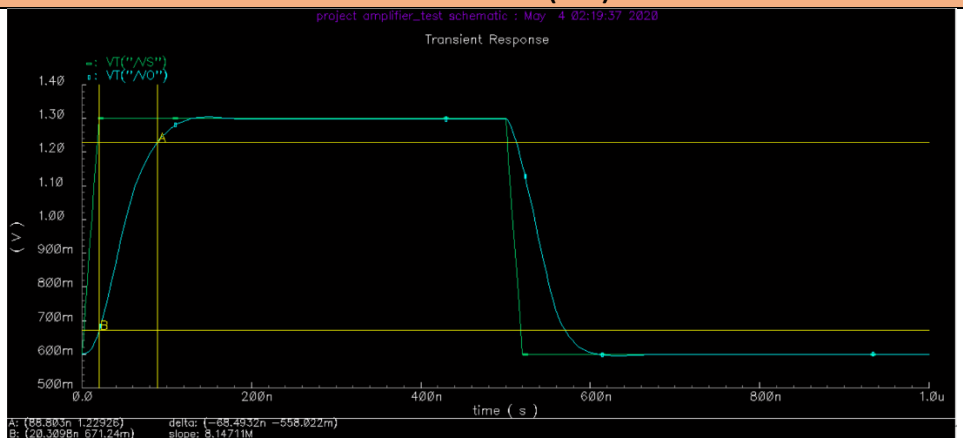

Fig. 13-1 SR simulation result(rise)

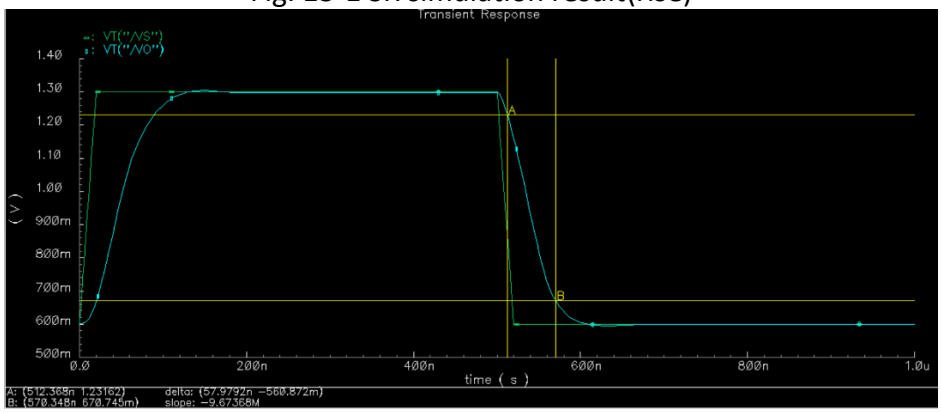

Fig. 13-2 SR simulation result(fall)

$$SR = \frac{SR+ + SR-}{2} = \frac{8.1471+9.673}{2} = 8.907\ V/us$$

Power dissipation (VDD)

Simulation Schematic (P_{diss})

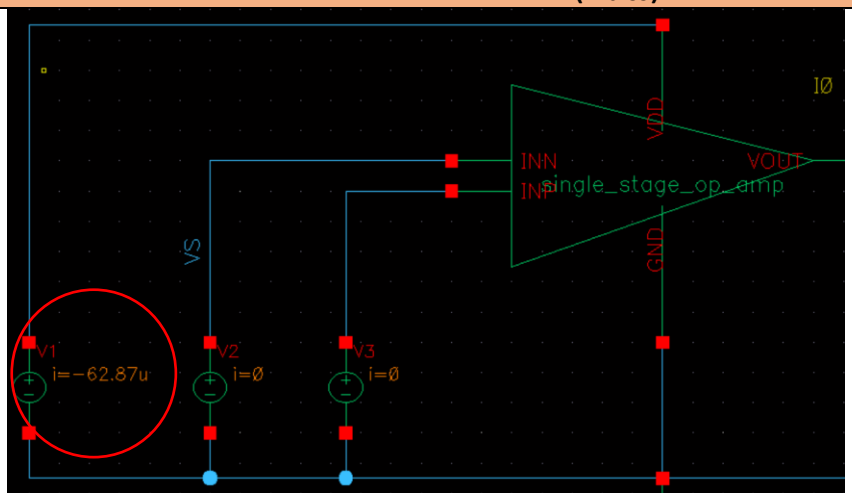

Fig. 14 P_{diss} simulation Schematic

P_{diss} = VDD * Total Current = 2V * 62.87uA= 0.125mW

VI. Score Calculation

$$\text{Score= min } [15,15(\frac{86.87dB}{85dB})]+\text{min } [10,10(\frac{1.307V}{1.3V})]+ \text{ min } [10,10(\frac{8.907V/us}{10V/us})]+$$

$$\text{min } [10,10(\frac{87.571dB}{80dB})]+\text{min } [20,20(\frac{10.2MHz}{8MHz})]+ \text{ min } [10,10(\frac{61.53°}{60°})]+ \text{ min } [15,15(\frac{0.5mW}{0.125mW})] = 80$$

VII. Conclusion

After this project, I think that it is not easy to match all specifications. I redesigned and modified my circuit many times because when my design met some requirements, some other requirements are unmatched. The single-stage op amplifier is not two-stage op amplifier, it is not difficult to get high gain in two-stage op amplifier. If I want to get high gain in single-stage, I must focus on cascode design. At first, my gain value was only 43dB, so I added a two NMOS into the circuit to increase the gain. As a result of the current unmatched, I spent several days to modify it and succeeded. I am glad that I can learn much more simulation skills and use the knowledge what I learn in this class when I do this project.

VIII. Reference

- Class notes in elearning
- Design of Analog CMOS Integrated Circuits 2nd Edition, by Behzad Razavi, McGraw-Hill, 2017.