RF Low Noise Amplifier Project

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Introduction

This project outlines the design and implementation of the RF low noise amplifier (LNA) in Figure 1 using concepts learned in EERF 6355. The amplifier itself is intended for use as a front-end amplifier. As the front end of a receiver the amplifier input will be a relatively small current that must be amplified into a useable voltage signal while increasing SNR as much as possible.

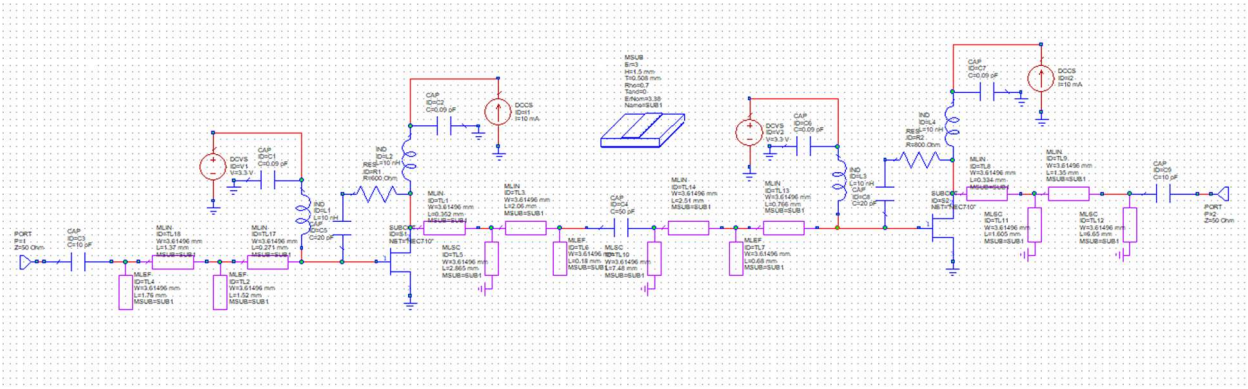

Figure 1: LNA Schematic

The LNA was designed to meet the specifications in table 1 below.

Parameter	Value
Center Frequency	10 GHz
Bandwidth B_{3dB} Bandwidth B_{20dB}	Min: 3GHz Max: 4 GHz Min:4 GHz Max: 6 GHz
NF	<2 dB
Gain	>18 dB@ 10GHz <-2dB outside B_{20dB}
Output Return Loss	>12 dB@10GHz
Stability	Unconditional for all frequencies
Vcc	+3.3V

Table 1: LNA Performance Specifications

Gain And Noise Figure Budget

To begin gain design, the necessary gain of the amplifiers stages will be determined based off the gain and noise figure budget shown in table 2 below.

	Input Match	FET Stage 1	Interstage Match	FET Stage 2	Output Match	Total
Gain(dB)	-0.25	10	-1	12	-1	19.75
Gain(Linear)	0.944	10.000	0.794	15.849	0.794	94.406
Noise Figure(dB)	0.25	1.3	1	2	1	1.865
Noise Figure(Linear)	1.059	1.349	1.259	1.585	1.259	1.536

Table 2: Gain and Noise Figure Budget

The most notable values in the table above are the input match noise figure, and the input stage noise figure. This is because the noise figure of the entire device is most effected by these two elements, and in order to get a good overall noise figure these elements must be considered very carefully. This is why the stage 1 gain is lower than the stage 2 gain, because it is very likely that to guarantee very low noise figure in stage 1 some gain will have to be lost. This is because in order to guarantee good noise figure the input impedance will not be matched for maximum power transfer but instead for minimum noise figure. The low noise figure of the input match also shows that the input match will need to be relatively small, using only 1 or 2 L networks to minimize the loss and noise figure. These losses incurred in the first stage by focusing on noise figure are then recovered by somewhat higher gain in the second stage, which will be conjugate matched at the input and output for maximum power transfer. As well as better, higher order matching networks used in between stages and at the output which will increase the device bandwidth.

Matching Network Design

To begin the matching network design, the input matching network was prioritized as this stage is the most important when it comes to noise figure. To determine what input impedance was necessary for the transistor, noise figure circles were plotted for the device at 10GHz shown in figure 2, and the input impedance was then matched close to the center of the NF circles.

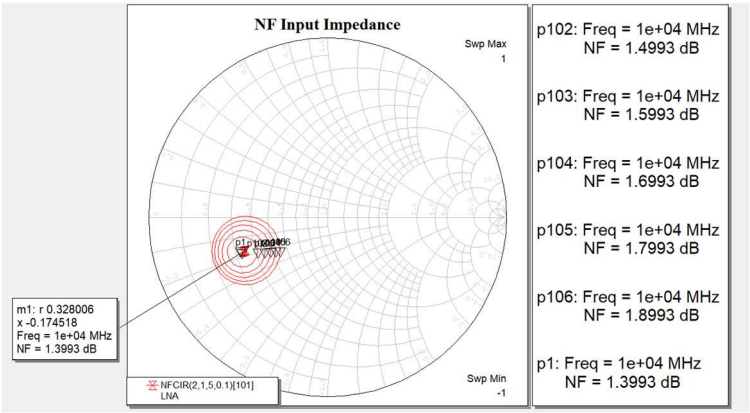

Figure 2: Input Stage Noise Figure Circles

In order to guarantee the bandwidth of the device while keeping the input matching network noise figure low a 2 segment microstrip line L network was designed MWO as shown in figure 3, however due to some modeled non-idealities the values were tuned somewhat to more accurately match to the needed value as shown in figure 4.

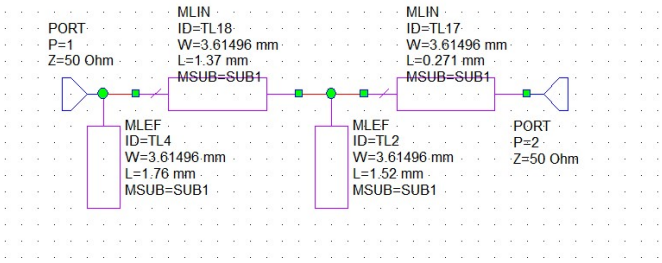

Figure 3: MWO Input Matching Network Schematic

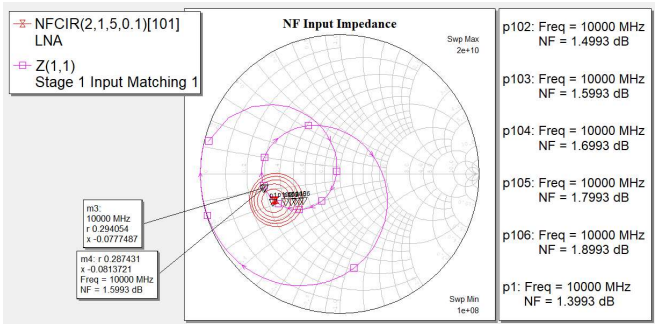

Figure 4: Input Matching Network MWO Validation

After completing the input matching network for stage 1, the following schematic was used to determine the output impedance of the stage.

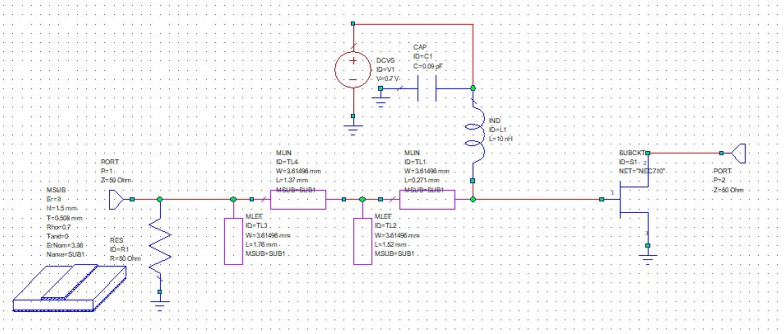

Figure 5: Stage 1 Output Impedance Schematic

Then in order to obtain a larger bandwidth as well as to simplify the design, the output impedance of stage 1 was conjugately matched to the conjugate of the input impedance of the second stage. The design was implemented in MWO as shown in figure 6 shows the MWO implementation. The IMN used more components to increase the bandwidth of the match and overall increase the bandwidth that the amplifier is able to perform at. Figure 7 shows the output return loss of the first stage to verify the efficacy of the IMN. Since the output return loss around 15dB the match is good.

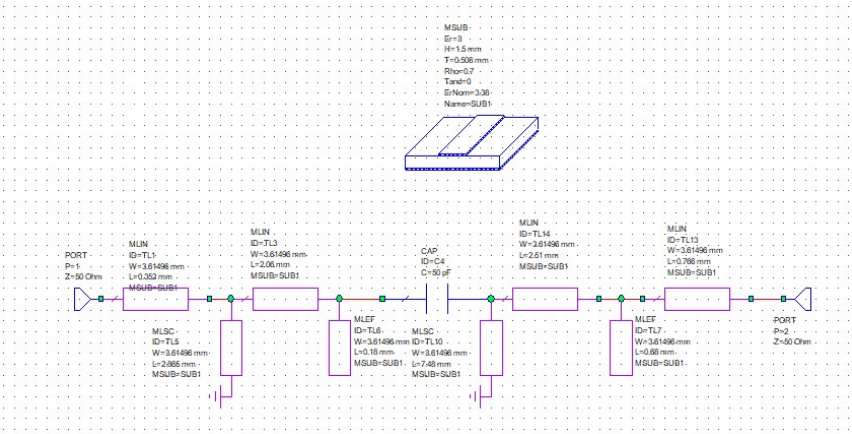

Figure 6: IMN Schematic

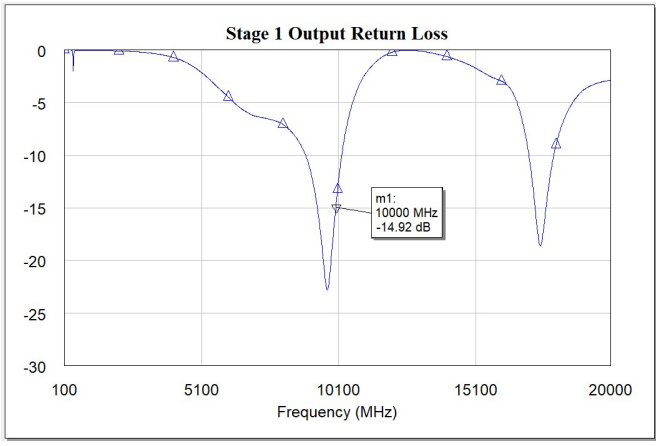

Figure 7: Stage 1 Output Return Loss

Finally, just like with the first stage, the second stages output impedance was measured via MWO. From there the output matching network was designed using MWO to conjugately match the output impedance of the second stage to the 50 ohm system impedance. Figure 8 below shows the designed output matching network, and figure 9 shows the output return loss of the full amplifier to guarantee that the output matching network is working well enough for the design.

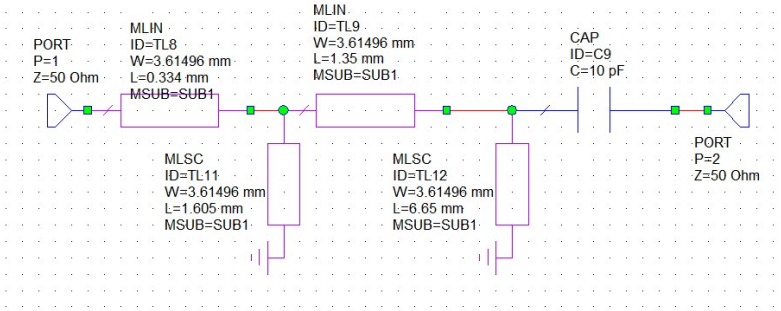

Figure 8: Output Matching Network Schematic

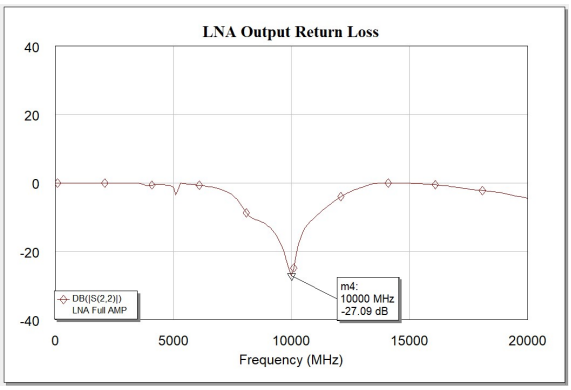

Figure 9: LNA Output Return Loss

After verifying that the output return loss meets the specification, it was determined that the output matching network was functioning properly.

Bias Network Design

After concluding the matching network design, the biasing of the device was implemented by using 10nH choke inductors, 10pF blocking caps, and 0.09pF supply bypass caps. These values were chosen specifically so they would not affect the matching networks very much at all. This is because at 10GHz the 10nH inductors have an impedance of around 628 ohms. Compared to the small values (<30 ohms) matched to at the inputs and outputs of both stages, the inductors behave fairly close to open circuits. Similarly the 10pF capacitors have an impedance of around 1.6 ohms at 10GHz which is fairly close to a short circuit compared to the other impedances matched to in the circuit. Thanks to the chosen values of the capacitor and the inductor the matching network impedances did not change by a meaningful amount so we were able to continue with the design.

Circuit Stability

In order to guarantee the amplifiers operation over the desired frequency range, we want to guarantee each stage is unconditionally stable over the frequency range (0.1-20GHz). This was done by analyzing the stability circles (input and output) of each stage. Initially without any feedback methods in place neither stage was unconditionally stable over the frequency range, so an RC feedback network was added. The capacitor value was chosen to be 20pF, large enough to not change the input and output impedances too much, but still block dc from passing. For both stages a 600 ohm resistance seemed to be the best compromise to get unconditional stability while maintaining proper noise figure and gain performance. The addition of the feedback network did not change the necessary input impedance by a meaningful amount, however the output impedance did need to be changed slightly. The change was fairly small so the MWO circuit tuner was used to change the output networks to get a proper match once again after the addition of the feedback network. Figures 10 and 11 show the input and output stability circles of stage 1 respectively, and figures 12 and 13 show the input and output stability circles of stage 2 respectively. The plots are expanded somewhat to show that none of the circles intersect the

smith chart which shows, along with the less than 1 input return loss, that both stages are unconditionally stable over the measured frequency range with the feedback added.

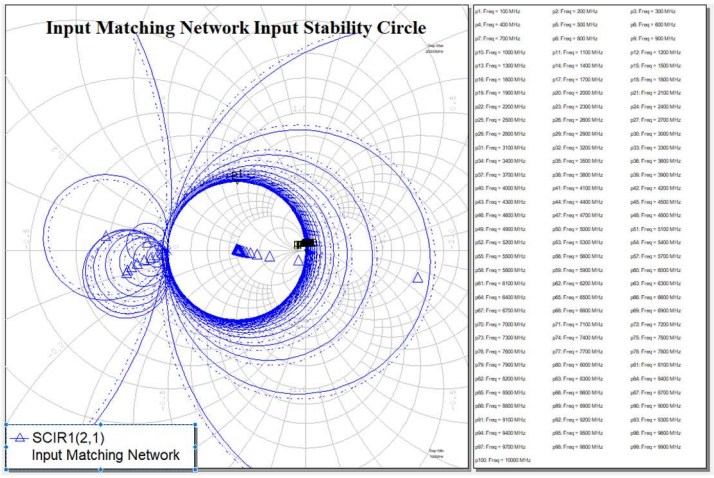

Figure 10: Input Matching Network Input Stability Circles

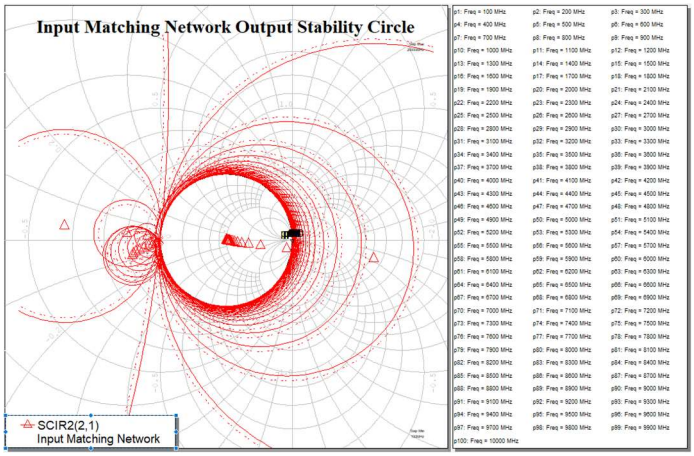

Figure 11: Input Matching Network Output Stability Circles

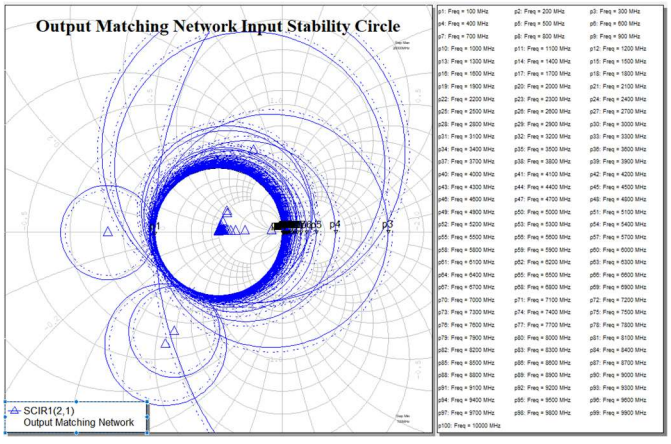

Figure 12: Output Matching Network Input Stability Circles

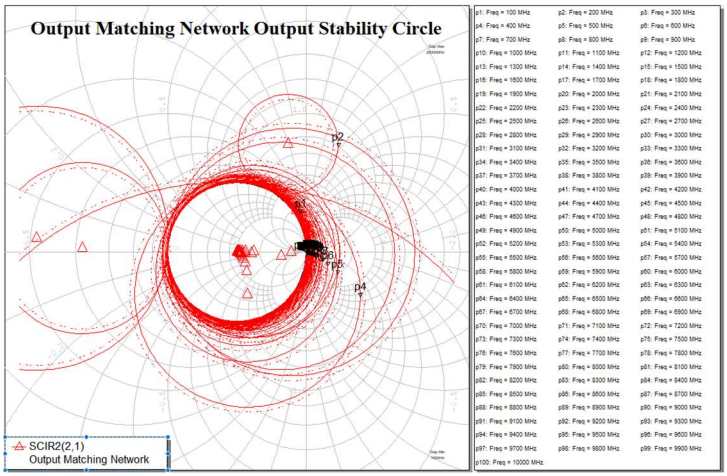

Figure 13: Output Matching Network Output Stability Circles

Circuit Performance

After finalizing the design and stability of the circuit, the performance was characterized using MWO simulations for each of the specifications listed in table 1. The first simulation in figure 14 run shows the amplifier s-parameters as well as noise figure over the amplification frequency range.

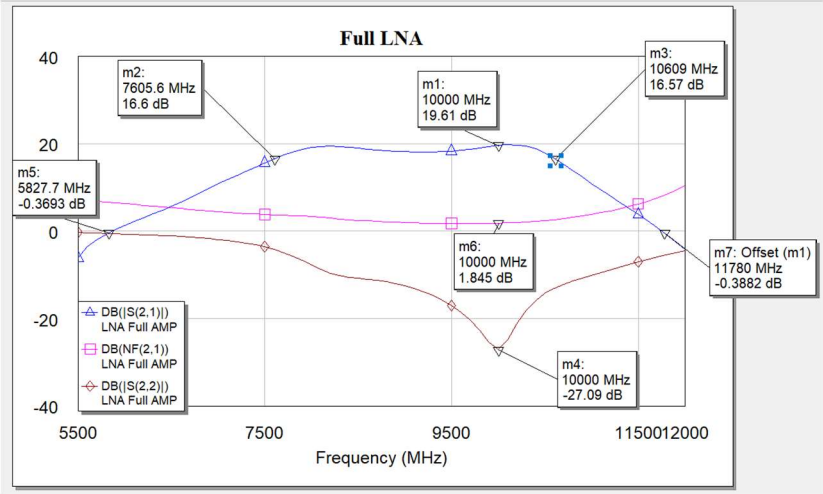

Figure 14: Relevant Amplifier S-parameters and NF

The plot above shows the amplifiers gain performance over the entire frequency band, as well as the output return loss, and noise figure of the device. From this the 3dB and 20dB bandwidths, gain, noise figure, and output return loss performance can be determined and compared to the specification. Also the amplifier was proven to be unconditionally stable in the circuit stability section. As a summary, table 3 shows a compliance matrix for the amplifier with all the specifications listed, and shows that with this design all of the specifications were met.

Parameter	Specificaiton	Simulated Result	Compliant Y/N
Bandwidth B3dB	min:3GHz max:4GHz	3.004GHz	Y
Bandwidth B20dB	min:4GHz max:6GHz	5.9293GHz	Y
NF	<2dB	1.845dB	Y
Gain	>18dB @10GHz <-2 outside B20dB	19.61dB	Y
Output Return Loss	>12dB @10GHz	27.09dB	Y
Stability	Unconditionally Stable	Unconditionally Stable	Y
Vcc	3.3V	3.3V	Y

Table 3: LNA Compliance Matrix

Conclusion

The design procedure followed, as explained in the project guidelines, worked very well for us. We were worried initially because of how much back tracking and how long the process was before any simulation results could be seen, but thanks to the rigorous designing of the amplifier very few large scale changes needed to be made to the actual foundation of the device after getting it designed. Thanks to that we were able to get a good amplifier immediately. The only issue we ran into was that initially we were not very thorough with working out the matching networks by hand so we had to tune them more, which took up some time. If we were to do the project again being much more critical during the initial by hand smith chart design of the matching networks would save a good amount of time and effort down the line.