Assignment 3

CMPT 215
Due: Aug 10^{th}, 2017

August 16, 2017

Total: 30
Please show all your work to get full marks

Problem 1.
(4 marks) Describe the modifications to the single clock cycle datapath that would be needed to implement the jal instruction and give the control signal setting that would be required for this instruction.

solution:

Bonus marks!

Give a single cycle datapath that can perform R and I instructions the modifications needed would be:

- Add a multiplexor between instruction memory and register file (this will already be in place if assumed it can handle I and/or jump instructions)
- Expand the multiplexor mentioned above to include $\$ra$ register (31) as new input that is controlled by register destination section.
- add a multiplexor after data memory (again may already be assumed)
- Expand that multiplexor to include $PC + 4$ (address to be stored in $\$ra$) and the controlled operation is memory to register flag.

Control signals:

instr	reg dest	mem to reg	reg write	mem read	mem write	ALU op1	ALU op0	jump
jal	10	10	1	0	0	x	x	x

x : is a don't care

Mark break down:

3 marks for description

2 marks for signals table

Problem 2.

(4 marks) Determine the clock cycle at which each of the instructions in the sequence given below would be completed, assuming the 5-stage pipeline without forwarding, and numbering the clock cycle at which the first of the instructions is fetched as clock cycle 1. Assume that if one instruction reads a register during the same clock cycle as another instruction is writing it, the new value will be read. Do not reorder the instructions. Instructions are fetched and executed exactly in the order given below, with the pipeline stalling if necessary.

```
lw  $s1,0($s2)
lw  $t1,0($s1)
addi  $s3,$s1,4
addi  $s1,$t1,-1
add   $t0,$s3,$s1
```

Solution:

inst	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
lw	IF	ID	EX	M	WB										
stall		IF	ID	EX	M	WB									
stall			IF	ID	EX	M	WB								
lw				IF	ID	EX	M	WB							
addi					IF	ID	EX	M	WB						
stall						IF	ID	EX	M	WB					
addi							IF	ID	EX	M	WB				
stall								IF	ID	EX	M	WB			
stall									IF	ID	EX	M	WB		
add										IF	ID	EX	M	WB	

Break down: 3 marks for the stalls
1 marks for showing the instructions and getting 14 cycles

Problem 3.
(4 marks) Repeat problem 2 but now assume forwarding. **Solution:**

instruction	1	2	3	4	5	6	7	8	9	10	11
lw	IF	ID	EX	MEM	WB						
stall		IF	ID	EX	MEM	WB					
lw			IF	ID	EX	MEM	WB				
addi				IF	ID	EX	MEM	WB			
addi					IF	ID	EX	MEM	WB		
add						IF	ID	EX	MEM	WB	

Break down: 2 marks for having only 1 stall
2 marks for showing forwarding and/or getting 10 cycles

Problem 4.
(9 marks) Consider the following code fragments:

```
                li    $s1,1
                li    $s3,6
                add   $s4,$zero,$zero
outer_loop:     add   $s2,$zero,$zero
inner_loop:     addi  $s2,$s2,1
                mul   $t0,$s2,$s1
                add   $s4,$s4,St0
inner_test      bne   $s2,$s1,inner_loop
                addi  $s1,$s1,1
                bne   $s1,$s3,outer_loop
```

This code simple runs the inner loop $i+1$ times each time, with i starting at 1, going until 5, meaning the **inner_test** will be executed 1+2+3+4+5 = 15 times. Give the branch prediction accuracy for **inner_test** for the following schemes:

i Branch prediction of always **Not Taken**

ii 1-bit branch prediction of starting at **Not Taken**

iii 2-bit branch prediction of starting at **Strongly Not Taken**

Solution:

scheme	NT	T	NT	T	T	NT	T	T	T	NT	T	T	T	T	NT	accuracy
NT	H	M	H	M	H	M	M	H	M	M	M	H	M	M	M	33%
1-bit NT	H	M	M	M	H	M	M	H	H	M	M	H	H	H	M	46%
2-bit SNT	H	M	H	M	M	M	M	H	H	M	H	H	H	H	M	53%

Mark break down:
3 marks for each scheme
2 marks for correct Hit and Miss pattern or showing of work.
1 mark for correct accuracy

Problem 5.
(4 marks) Suppose that a program does read operations on the following memory addresses **96, 508**. Give the number of the memory block that each of these addresses belongs to, for each of the following memory block sizes. Remember the above addresses are byte addressed.

i block size of one word (4 bytes)

ii block size of four words (8 bytes)

Solution:

i

$$\begin{aligned} \text{block number} &= \frac{96}{4} \\ &= 24 \end{aligned}$$

$$\begin{aligned} \text{block number} &= \frac{508}{4} \\ &= 127 \end{aligned}$$

ii

$$\begin{aligned} \text{block number} &= \frac{96}{16} \\ &= 6 \end{aligned}$$

$$\begin{aligned} \text{block number} &= \frac{508}{16} \\ &= 31 \end{aligned}$$

2 marks for each question.
1 mark for work
1 mark for answer

Problem 6.
(8 marks) Give the position (or set) in the cache that would be checked on each of the read operations of the above question, for each of the following caches.

i Direct-mapped cache with total capacity of 16 one-word blocks

ii Direct-mapped cache with total capacity of 4 four-word blocks

iii 4-way set-associative cache with total capacity of 16 one-word blocks

iv 2-way set-associative cache with total capacity of 4 four-word blocks

Solution:

i

$$\begin{aligned}\text{block number} &= \frac{96}{4} \\ &= 24 \\ \text{cache position} &= 24 \mod 16 \\ &= 8 \\ \text{block number} &= \frac{508}{4} \\ &= 127 \\ \text{cache position} &= 127 \mod 16 \\ &= 15\end{aligned}$$

ii

$$\begin{aligned}\text{block number} &= \frac{96}{16} \\ &= 6 \\ \text{cache position} &= 6 \mod 4 \\ &= 2 \\ \text{block number} &= \frac{508}{16} \\ &= 31 \\ \text{cache position} &= 31 \mod 4 \\ &= 3\end{aligned}$$

Solution:

iii

$$\begin{aligned}
\text{block number} &= \frac{96}{4} \\
&= 24 \\
\text{number of sets} &= \frac{4}{16} \\
&= 4 \\
\text{set position} &= 24 \mod 4 \\
&= 0 \\
\text{block number} &= \frac{508}{4} \\
&= 127 \\
\text{set position} &= 127 \mod 4 \\
&= 3
\end{aligned}$$

iv

$$\begin{aligned}
\text{block number} &= \frac{96}{16} \\
&= 12 \\
\text{number of sets} &= \frac{2}{4} \\
&= 2 \\
\text{set position} &= 12 \mod 2 \\
&= 0 \\
\text{block number} &= \frac{508}{16} \\
&= 63 \\
\text{set position} &= 63 \mod 2 \\
&= 1
\end{aligned}$$

Mark break down:
2 marks per question 1 mark for work
1 mark for the solution

Problem 7.
(2 marks) Consider a computer system in which a physical page number is 24 bits, a virtual page number is 52 bits, and a virtual address is 64 bits. What is the maximum amount of physical memory, in GiB, that this system could have?

Solution:

$$\begin{aligned} \text{page size} &= 2^{(64-52)} \\ &= 2^{(12)} \\ \text{physical space} &= 2^{24} * 2^{12} \\ &= 2^{36} \\ &= 64GiB \end{aligned}$$

1 mark for the solution
1 mark for showing work

Bonus:

Problem 8.
(5 marks) Given two threads that share memory:

```
int a = 0;
int b = 4;
int c = 0;
int d = 0;
int z = 0
```

```
Thread 1:
 c = a+b;
 c = 0;
 a = d+b;

 end
```

```
Thread 0:
d = a+b;
z = a+d;
a = c+d;
```

What is the values of each variable at the end of the program? What is the technical term for what is going on? What are two ways to keep mutual exclusion?

Solution:

- If thread 1 before thread 1 then $a = 4$ If thread 2 before thread 1 then $a = 8$ 1 mark for listing each situation.
- race condition (concurrency for (0.5))
- locks, conditional variables, semaphores, mutexs (max 2 marks for listing at least two of the following)