Cache Simulations on Paper. The following table allows you to simulate the behavior of a cache on paper. The first 4 columns show you the contents of the cache at the time of a particular cache access. We are showing the **address** of each byte that lives in a particular cache block. A real cache would store a tag and data here, but for simulation purposes, the address itself is sufficient.

The **outcome** should say whether this access was a hit or a miss. If it was a miss, specify whether it was *cold, capacity, or conflict.* The next row should begin with the *new* contents of the cache as a result of the access on the previous line. Given that current state of the cache, determine the outcome of the next access. If the contents of a particular set does not change, feel free to leave that field empty on the next line down.

This cache is a direct-mapped, 8B cache with 4B blocks. This cache was filled via access to addresses in the order: 0000, 0100.

Cache contents (prior to access)		**Address of Cache Access**	**Outcome of Cache Access**
Set 0	**Set 1**		
0000 | 0001 | 0010 | 0011	**0100 | 0101 | 0110 | 0111**	1100	*Cold miss*
	1100 1101 1110 1111	1010	cold miss
1000 1001 1010 1011		1011	hit
		0011	capacity miss
0000 0001 0010 0011		0101	capacity miss
	0100 0101 0110 0111	1100	capacity miss
	1100 1101 1110 1111	1001	capacity miss

This cache is a 2-way set associative 8B cache with 2B blocks.
Use LRU replacement policy and assume that Way 1 of each set was most recently used.

Cache contents (prior to access)				Address of Cache Access	Outcome of Cache Access
Set0,Way0	**Set0,Way1**	**Set1,Way0**	**Set1,Way1**		
0000|0001	**0100|0101**	**0010|0011**	**0110|0111**	1100	*Cold miss*
1100 1101				1010	cold miss
		1010 1011		1011	hit
				0011	capacity miss
			0010 0011	0101	hit
				1100	hit
				1001	cold miss

This cache is a direct-mapped, 8B cache with 2B blocks. Addresses are 4 bits.
This cache was filled via access to addresses in the order: 0000, 0010, 0100, 0110.

Cache contents (prior to access)				address of cache access	outcome of cache access
Set 00	**Set 01**	**Set 10**	**Set 11**		
0000|0001	**0010|0011**	**0100|0101**	**0110|0111**	1100	cold miss
		1100 1101		1010	
	1010 1011			1011	
				0011	
	0010 0011			0101	
		0100 0101		1100	
		1100 1101		1001	