1. Name: Yiduo Ke. Collaboration: Jianan Li
2. True or False
   1. False
   2. False
   3. False
   4. False
   5. True
   6. False
3. Cache Performance
   1. D
   2. E
   3. A
4. Caches
   1. Temporal and spatial locality
   2. Bits:
      1. Direct mapped
         1. offset = 4 bits
         2. index = 3 bits
         3. tag = bits
      2. 2-way set associative
         1. Offset = 3 bits
         2. Index = 3 bits
         3. Tag =
      3. 4-way set associative
         1. Offset = 2 bits
         2. Index = 3 bits
         3. Tag =
      4. Fully associative
         1. Offset = bits
         2. Index = 0 bits
         3. Tag = bits
   3. M

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Address | Direct-mapped | 2-way set-ass (LRU) | 4-way set-ass (LRU) | Fully-ass (LRU) |
| 0x1000 | Cold miss | Cold miss | Cold miss | Cold miss |
| 0x1010 | Cold miss | Cold miss | Cold miss | Cold miss |
| 0x1008 | hit | Cold miss | Cold miss | hit |
| 0x2000 | Cold miss | Cold miss | Cold miss | Cold miss |
| 0x3000 | Cold miss | Cold miss | Cold miss | Cold miss |
| 0x4000 | Cold miss | Cold miss | Cold miss | Cold miss |
| 0x3004 | Conflict miss | hit | Cold miss | hit |
| 0x2001 | Conflict miss | Conflict miss | hit | hit |
| 0x0000 | Cold miss | Cold miss | Cold miss | Cold miss |
| 0x1004 | Conflict miss | Conflict miss | Cold miss | hit |
| 0x1011 | hit | hit | hit | hit |

* 1. D

1. TLB Performance Optimization
   1. bits
   2. Because the index bits for the cache lookup would not change during address translation. The last 8 bits would not change because they’re the page offset, and those 8 bits includes the 4 index bits.
   3. 1000 1000
   4. 0000 0000
   5. B and C
2. MMU and Virtual Memory
   1. bits; bits
   2. bits; bits
   3. entries; entries; this is a problem because that’s way too big; there’s no space for the computer to carry out actual tasks, it might as well not have a MMU
   4. Idk
   5. Idk
   6. Idk
   7. Idk
   8. Idk
   9. idk
3. Calling Conventions and Assembly code
   1. Using both caller- and callee-saved registers makes a program faster. Callee-saved registers are preserved across multiple function calls. Caller-saved registers are volatile and are used to do calculation when function calls execute.

PROLOGUE:

BODY:

BGE a1, a0, else

JAL x0, EPILOGUE

else:

add a0, x0, a1

EPILOGUE

jalr x0, ra, 0

1. Full System Layout – D, C, E, E, B, D
2. Linkers and Loaders
   1. E (none of the above)
   2. B (data)
   3. D (stack)
   4. E (none of the above)
   5. C (heap)
   6. It doesn’t even compile because requires . The compilation error:
3. main.c: In function ‘main’:
4. main.c:6:31: warning: implicit declaration of function ‘malloc’ [-Wimplicit-function-declaration]
5. int\* small\_array = (int\*) malloc(SMALL\_ARR\_SIZE \* sizeof(int));
6. ^~~~~~
7. main.c:6:31: warning: incompatible implicit declaration of built-in function ‘malloc’
8. main.c:6:31: note: include ‘’ or provide a declaration of ‘malloc’
9. main.c:11:5: error: expected ‘;’ before ‘printf’
10. printf("%d\n%d\n", big\_arr[0], small\_array[3]);
11. ^~~~~~

If I include , then and put the semicolon after the line, and correct big\_arr to big\_array, then it prints out:

12

16

done running

1. Exceptional Control Flow
   1. Asynchronous means that the event is not caused by execution of any instruction, but rather an asynchronous signal that an external IO device sends to the processor.
   2. D
   3. B
   4. C
2. meow