Collaborator: yc2454 (Yalu Cai)

The intuition behind this is sorting the inputs (putting all 1’s before all 0’s), and seeing if the

-th input after sorting is 1. If it is 1, then there is a majority of 1’s in the input, otherwise no. The type of sorting we will use is bubble sort, which we know to be time, which we will translate into a sized circuit.

There are “levels” the circuit (details later). We will implement bubble sort on the inputs as such: for the first level, we compare with , and if is 0 and is 1, then in the “next level”, will become 1 and will become 0; otherwise, they stay the same in the next level. through will stay the same in the next level. In the next level, we compare with and so on. After we’ve reached the comparison between and , we will have done comparisons, which is . Let’s call each sequence of comparisons from to a “line comparison”. Within line comparisons, the inputs will have been completely sorted (I hope I don’t have to prove this…). After the inputs are sorted, the answer to this MAJORITY problem is whether the -th bit is a 1. This whole thing is time.

The first detail we will implement is switching a “0 ,1” to a “1, 0” (not switching them otherwise). As CS 3410 taught me, we implement this by writing out the truth table for it first:

|  |  |  |  |
| --- | --- | --- | --- |
| -old | -old | -new | -new |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 |

We see that -new is only 1 when EITHER of the old values is 1, so

-new = (-old) (-old)

And that -new is only 1 when BOTH of the old values is 1, so

-new = (-old) (-old)

So, the lowest few levels look like this, where green node is input, blue node is OR gate, orange node is AND gate:



Level 3

Level 2

Level 1

Level 0



For each “line comparison”, there are levels (each level is comprised of a blue and orange node). In total (excluding the green level), there are levels to sort the inputs. The output is the -th bit of the sorted output, i.e. the -th blue node from the left of the last layers.

This circuit is in size because each level adds four wires/edges, and there’s levels, . QED.