Valued Customer,

I'd like to thank you for taking advantage of our USBCheck Design Review service. Here at Microchip, we feel it is very important to get involved with our customers' designs as soon as possible. We feel the sooner we start working with a customer and his design, the sooner we can identify any problems with that design. By doing this, we can get those problems fixed as quickly as possible. This should ensure you of having the fastest design cycle possible. I looked over your USB2244 design and for the most part, it was very good. I did have some minor comments; please review:

1. I checked your schematic shape for the USB2244 pin-by-pin and found no problems there.

2. You should incorporate a chassis (earth) ground plane in your system for X1. Typically, we pour a smaller, separate chassis plane up around the USB connector. We then mirror this plane on all four layers of the PCB. This new plane should be completely separate from your digital ground plane. You should take care in making sure that no other voltage plane, signal trace or component is within .250" of this chassis ground. This will ensure you of having the best possible isolation performance for your product. This prevents any high energy from entering the system and disturbing your other electrical components and devices.

3. You should connect the metal shield of the USB connector to this new chassis ground plane.

4. I'd also like to recommend one new component for your design. You should add a large surface mount footprint up around the USB connector. This footprint should be an SMD_1210 or larger footprint. This component should be connected between the new chassis ground plane and your existing digital ground plane. This component will allow you to configure these two planes in different manners. By leaving the footprint blank, the two planes are completely separated from each other. If you were to install a zero ohm resistor in the footprint, the two planes would be shorted together at a single point. Another option would be to AC couple the two planes together with a high voltage (2KV) capacitor. Another option would be to install a ferrite bead in the spot to connect the two planes together with some EMI impedance characteristics. This component will allow you to determine the best configuration for your product during EMC/FCC/CISPR testing. It will give you the flexibility you'll need at this stage of your development cycle.

5. Please verify that C7 in your design is a low ESR capacitor. The low ESR requirement is to ensure the proper stability of the +1.8V internal core regulator of the USB2244. We recommend a high quality, low ESR, ceramic type capacitor for this particular application. We recommend the ESR not be any higher than 1.0 ohms for frequency ranges from 10 KHz to 1 GHz.

6. Please verify that C6 in your design is a low ESR capacitor. The low ESR requirement is to ensure the proper stability of the second +1.8V internal regulator of the USB2244. Again, we recommend a high quality, low ESR, ceramic type capacitor for this particular application. We recommend the ESR not be any higher than 1.0 ohms for frequency ranges from 10 KHz to 1 GHz.

7. Microchip recommends one, single, large contiguous digital ground plane for all its USB products. We have found over the years that many customers have implemented split ground techniques incorrectly in their designs. If this technique (split grounds) is not implemented perfectly, EMC/signal integrity issues may be exacerbated. As a result, Microchip does not recommend having two grounds (analog ground & digital ground). I strongly recommend that all of the ground pins (VSS_A & GND_IO) be connected directly to the same solid, contiguous digital ground plane in your design.

8. As per item 7. above, you need to delete L2 from your design completely as this component is very incorrect in the schematic. You only want one solid digital ground plane throughout the entire design….

9. Please be sure to verify that you are using (9) power vias (thermal vias) in a 3x3 grid in the EDP (Exposed Die Paddle) pad underneath the USB2244 in order to connect the IC to your digital ground plane. The power via is slightly larger than regular vias used elsewhere in your design. This larger size helps to lower the inductance of the connection, increase the power capability of the connection and increase the thermal conductivity of the connection. Just as an example, using a typical via drill hole of 10 mil results in a Total Thermal Resistance of 3.43 K/W (Kelvins per Watt) in a 3x3 grid for our LAN8710 Phy. Increasing the via drill hole to 16 mil results in dropping the thermal resistance to a value of 2.11 K/W. Tenting or plugging the vias underneath the IC is recommended. The use of full contact vias is also recommended here. Please review the Amkor app note furnished with this review for more details on this subject.

10. Please verify the drive level of the crystal you have selected for use with the USB2244. The drive level must be between 300 uW and 500 uW; the higher, the better. In order to obtain the best performance from a crystal oscillator, it is necessary to ensure the crystal is driven at the correct level. If the drive level for the crystal is too high then the parasitic resonances of the crystal may be excited. The crystal oscillator may even run at an incorrect frequency. Additionally, if the drive level is too high then the phase noise performance of the crystal oscillator will be degraded. Also, the crystal can be damaged if the drive level is too high; in particular, the miniature types are susceptible to damage. Even if permanent damage is not caused, the high level of drive within the crystal oscillator increases the rate of ageing and can cause a frequency shift. It is therefore important to ensure the level of drive within the crystal oscillator circuit is approximately correct. In view of the need to ensure the correct operating conditions for the crystal oscillator itself, it is necessary to optimize the circuit for stability, gain and drive level.

11. Also on the crystal, please be sure of it's accuracy. The USB2244 requires a 24.000 MHz clock accuracy of better than +/- 350 PPM over the entire temperature range of your application.

12. In your crystal circuit, C13 & C14 seem a bit too low in value (10 pF). I think you will come to find that these values should be more in the neighborhood of 27 - 33 pF. These capacitors allow you to fine tune the 24.000 MHz frequency to the required tight tolerance as called for by the USB-IF. Please use the formula found in the USB2244 data sheet in order to determine the correct value for your crystal load capacitors.

13. **Design Note:** Customers should be aware that Microchip offers alternative solutions for their application's 24.000 MHz timing requirements. Our DSC1001/3/4 Low Power CMOS Oscillator is just one example of timing solutions the design engineer may consider for his project. For more information and the latest data sheets, please visit the Microchip website…

14. For recommended reset circuits for the USB2244, please review pages 11, 12 & 13 of the USB2244 schematic checklist furnished with this review. Be sure to select the circuit that best fits your application.

15. Please verify that the reset signal to the USB2244 is at least 1 uS long, as per the data sheet. Be sure to also review the data sheet for additional reset timing and voltage level requirements.

I'd like to thank you again for taking advantage of our USBCheck Design Review service. If you have any further questions or issues with any Microchip product, please do not hesitate to contact Microchip at any time. Your local Microchip FAE will be more than happy to answer any of your questions. I'd like to also invite you to visit the Microchip website to review our documentation on PCB design. You should find useful information on PCB component placement and PCB routing in the USB2244 application notes. They should prove to be very helpful in your PCB design effort. Thank you again, and have a good day.