Traffic-Light Control System

A project for hardware engineering lab

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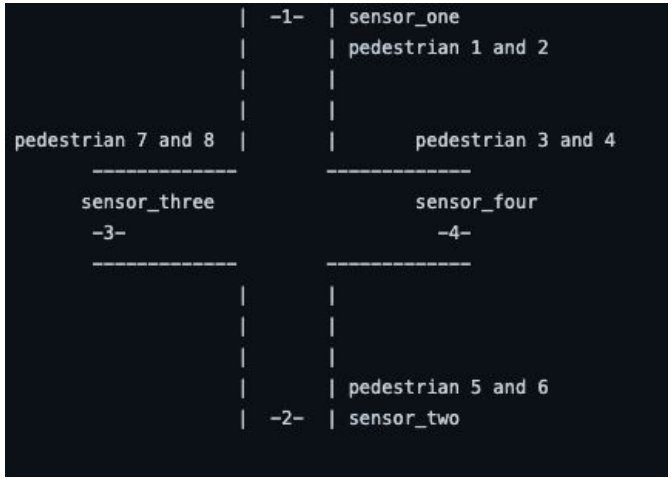
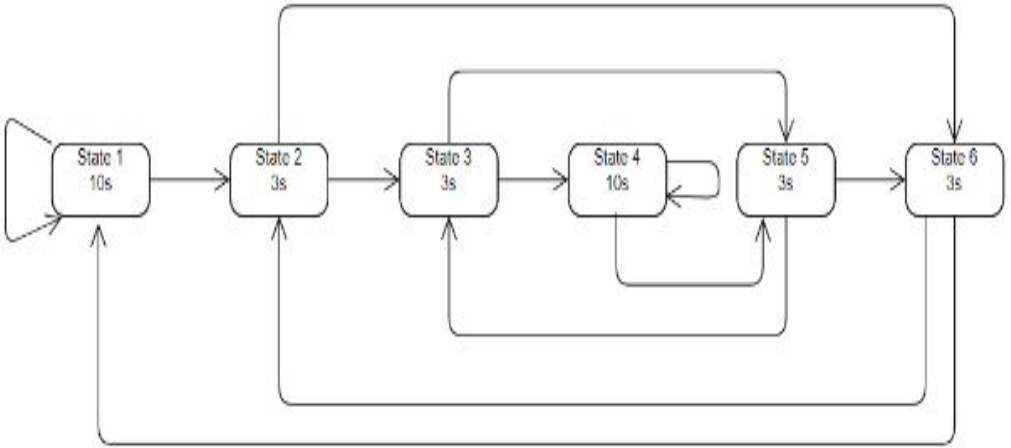
MOTIVATION

- Conventional Traffic Light Controller.
- 4-Way Junction for Oversaturated Traffic Conditions.
- Pedestrian Safety in Consideration.
- Design Approach for a Real-World Hardware.

Concept Description

FINITE STATE MACHINE DIAGRAM





VHDL SIMULATION WITH MODELSIM

PCB DESIGN

Conceptual model:

Sensors to detect vehicles/ pedestrians

Switches were used instead of sensors

- Complexity and cost of introducing sensors
- Limitation of time

Future development: Sensors implementation

Components

1 FPGA: Intel / Altera EP4CE22E22C8N

12 GREEN LED-GREEN0603

12 RED LED-RED0603

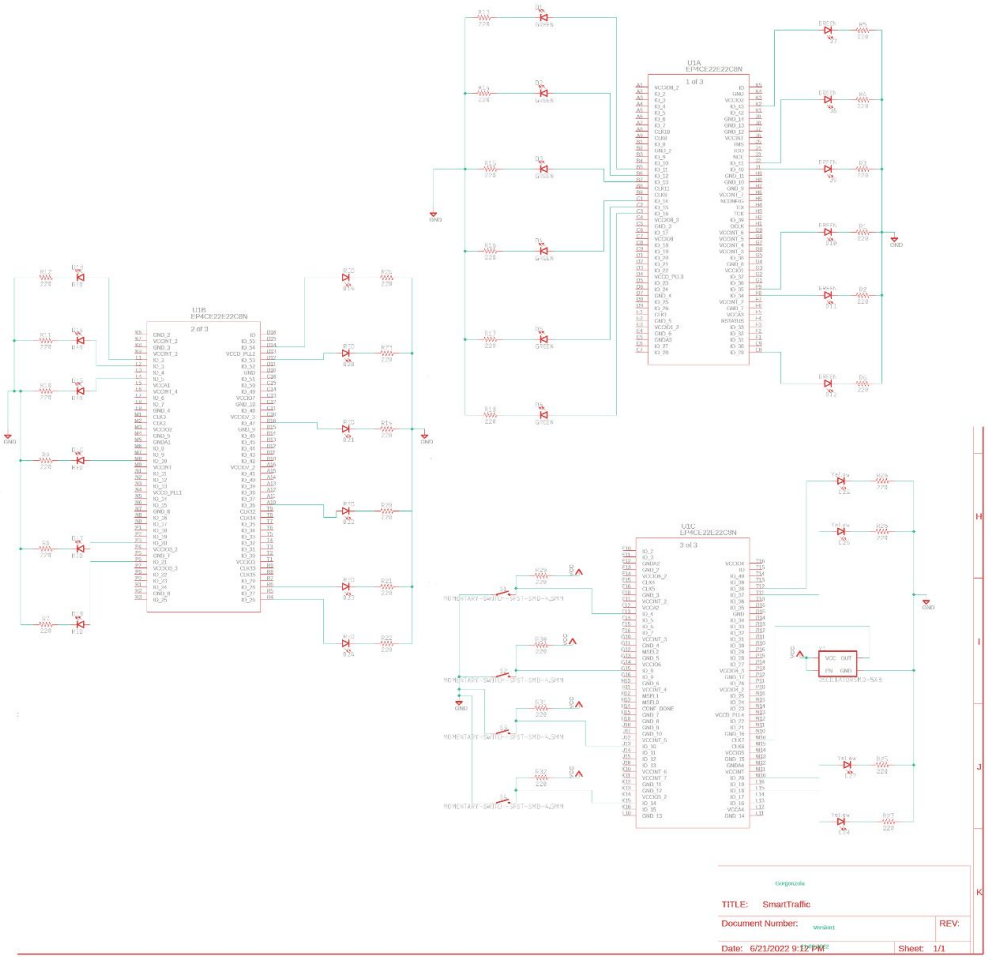
4 YELLOW LED-YELLOW0603

1 OSCILLATOR, Device: OSCILLATORSMD-5X3

4 MOMENTARY-SWITCH, Device: MOMENTARY-SWITCH-SPST-SMD-4.5MM

32 220 Ohm Resistor

SCHEMATIC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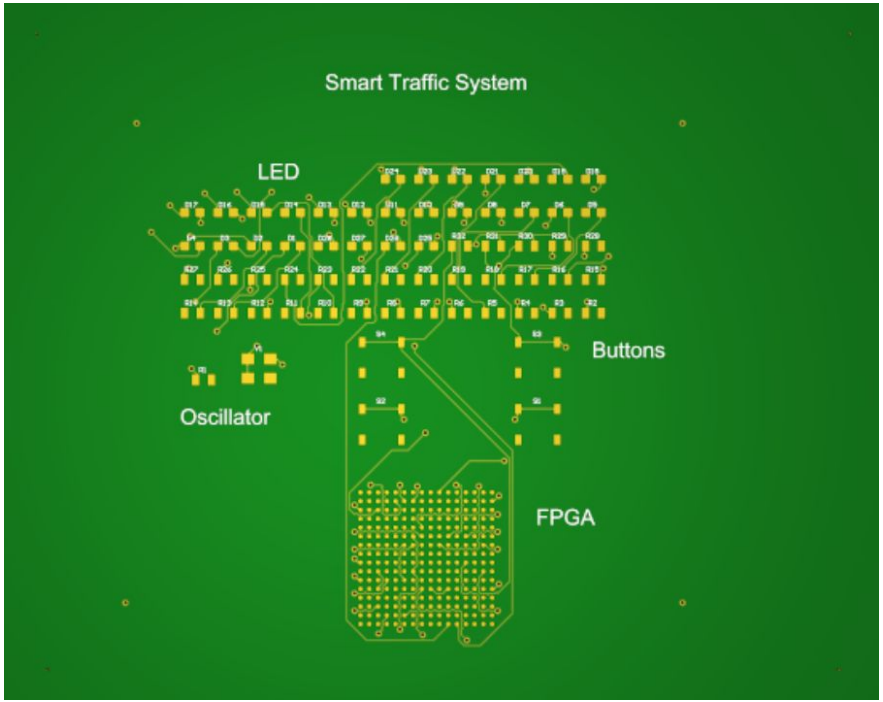
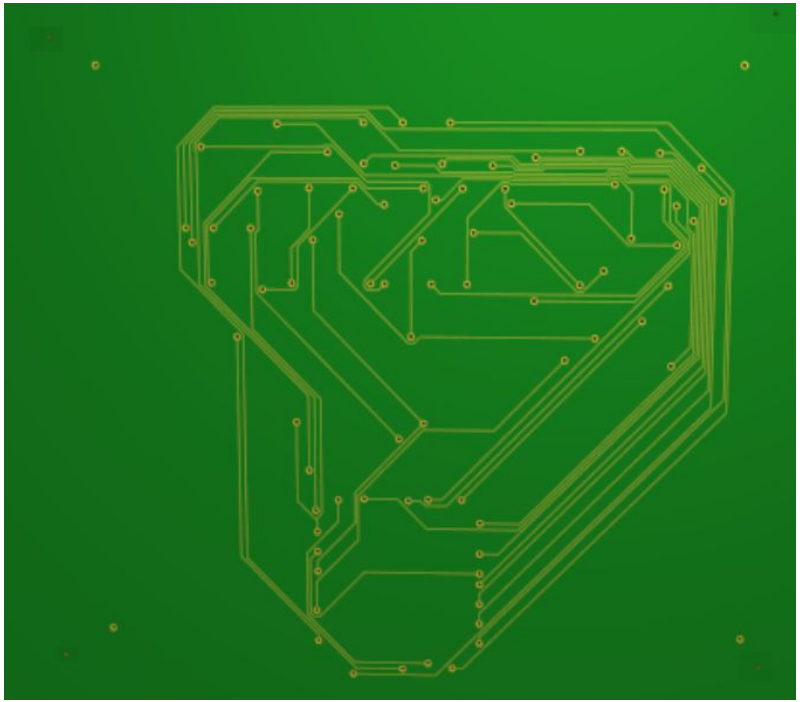
Date: 6/21/2022 9:12 PM
Sheet: 1/1

PCB Front view



PCB Rear view



Size: 100 × 80 millimeter

Cost:

FPGA: 75 €
Resistor: 32 × 0.25 € = 8 €
LED: 32 × 0.25 € = 8 €
Oscillator: 3 €
Switch: 4 × 1 € = 4 €

Total: 98 €

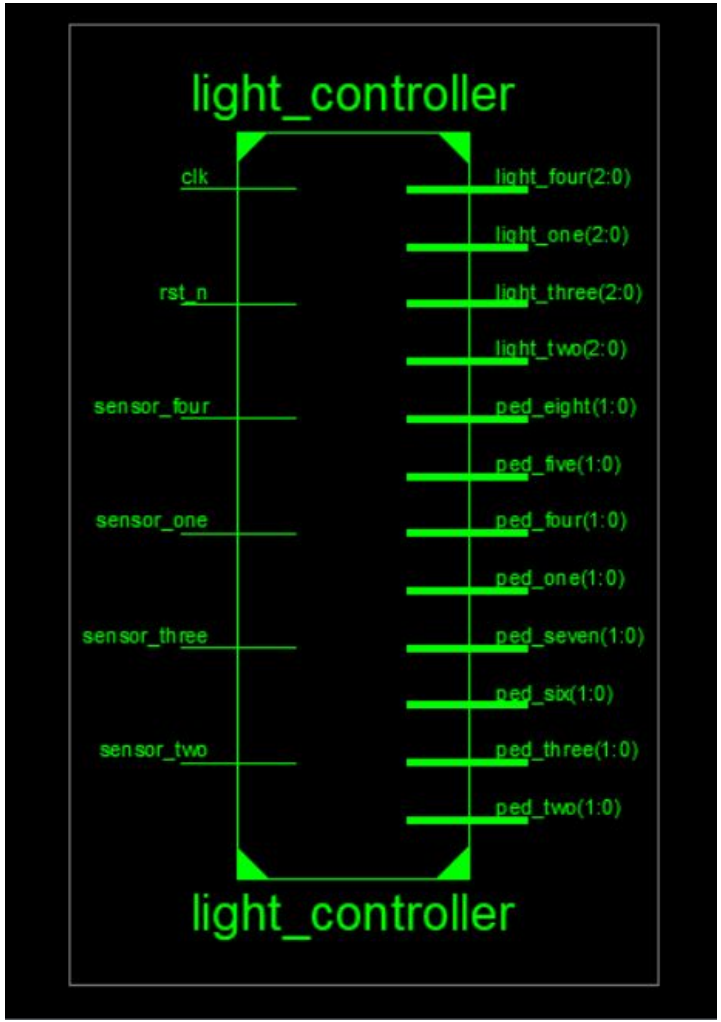
FPGA IMPLEMENTATION

The VHDL code developed during the project work was used

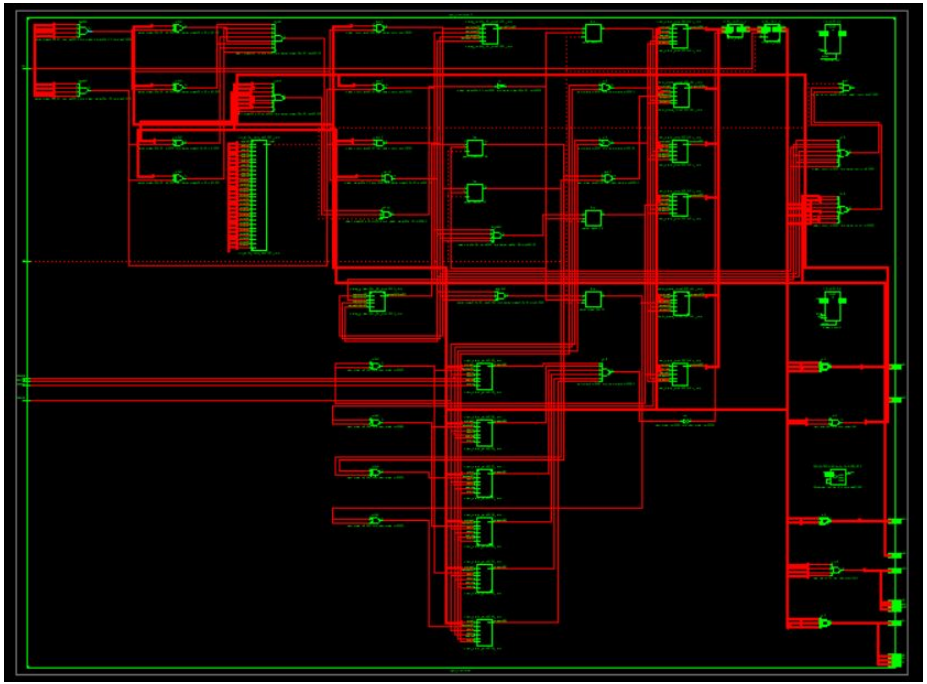
Software: ISE 14.7 Virtual Machine for Windows 10 software (Spartan3/ xc3s1000/ft256)

For reference, we have used the lecture slides

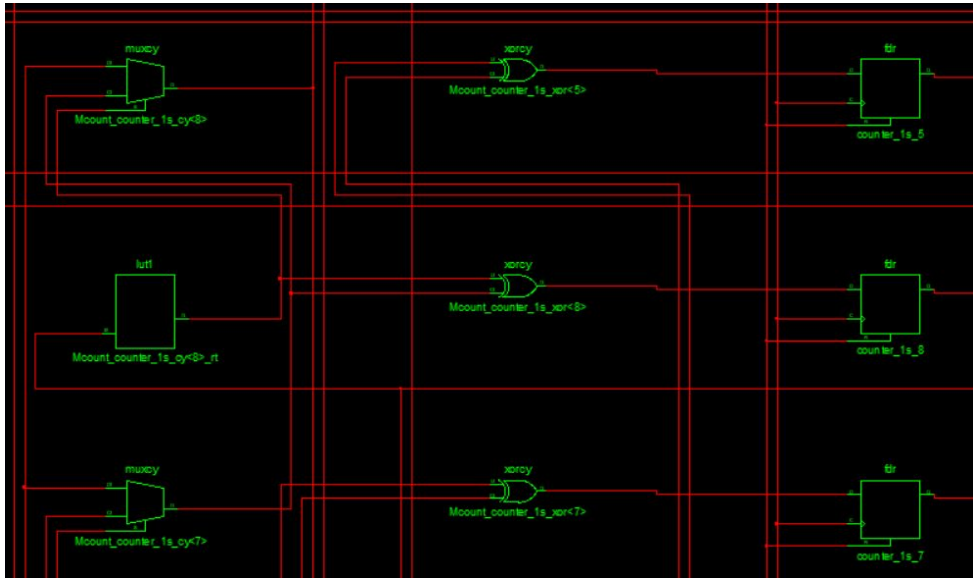
RTL



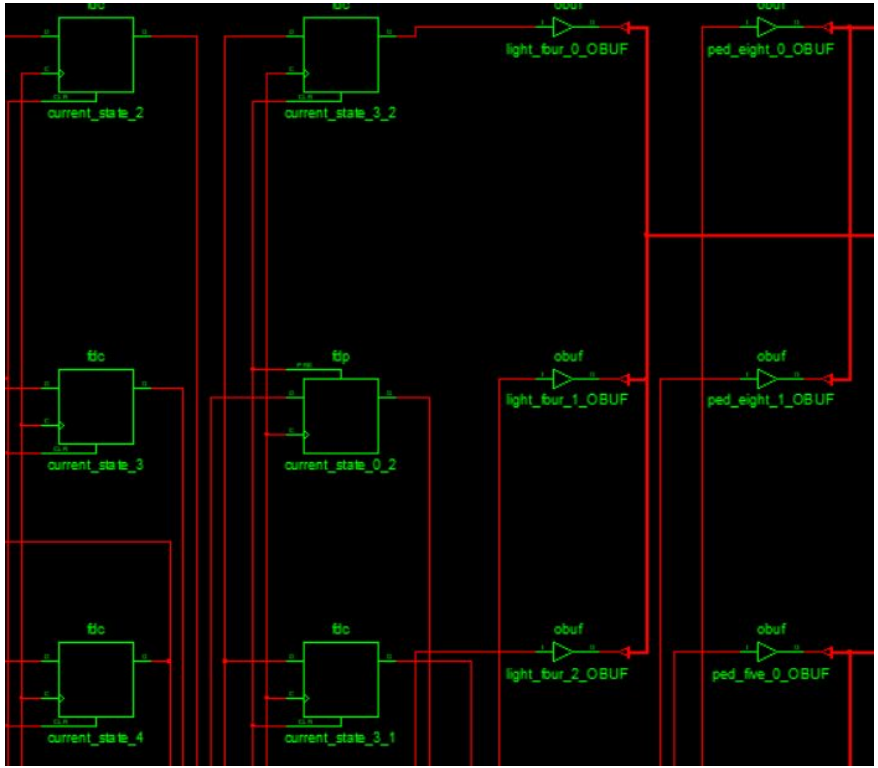
Technology Schematic



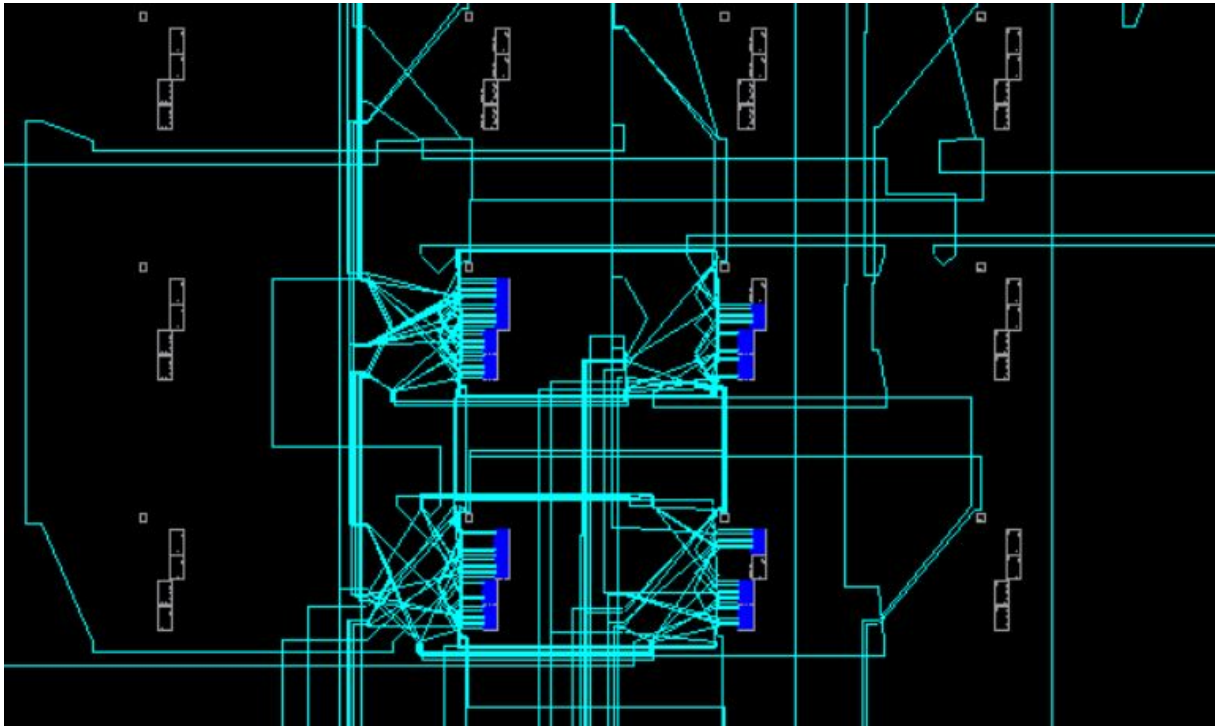
Technology Schematic FPGA component group 1



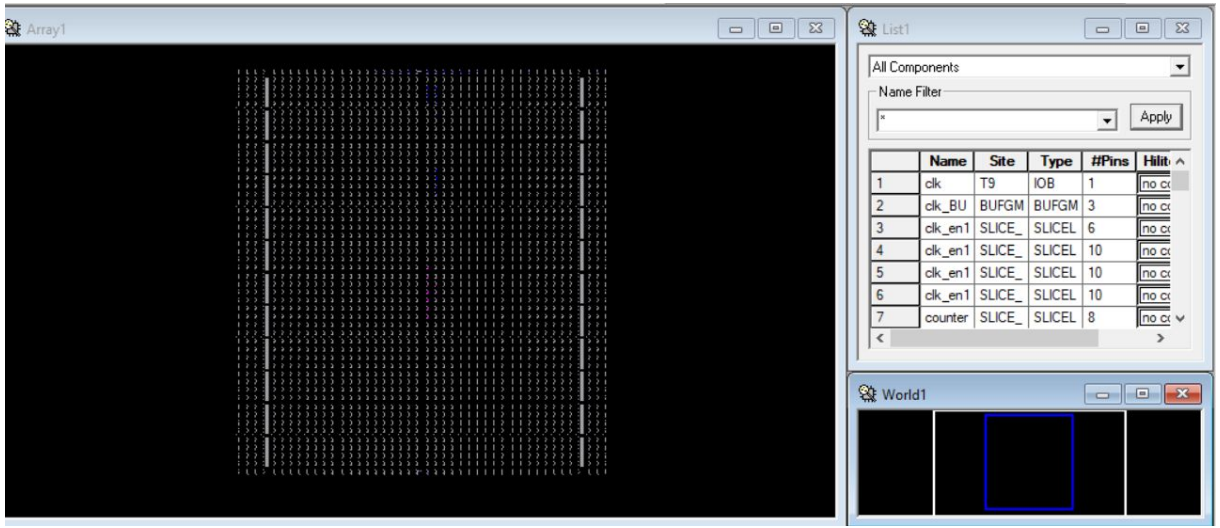
Technology Schematic FPGA component group 2



Routed Design for switches



Routed Design with partial components



Constraints:

- All pins are not mapped in ucf file, so the final bitstream file is not available

- Partial UCF file with limited components is generated (located: Github repository)

Design summary (Partial)

TST_BENCH Project Status (06/23/2022 - 18:36:07)			
Project File:	traffic_light_controller.xise	**Parser Errors:**	No Errors
Module Name:	light_controller	**Implementation State:**	Programming File Generated
Target Device:	xc3s1000-5ft256	**• Errors:**	No Errors
Product Version:	ISE 14.7	**• Warnings:**	13 Warnings (11 new)
Design Goal:	Balanced	**• Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	All Constraints Met
Environment:	System Settings	**• Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Total Number Slice Registers	49	15,360	1%	
Number used as Flip Flops	43			
Number used as Latches	6			
Number of 4 input LUTs	61	15,360	1%	
Number of occupied Slices	48	7,680	1%	
Number of Slices containing only related logic	48	48	100%	
Number of Slices containing unrelated logic	0	48	0%	
Total Number of 4 input LUTs	88	15,360	1%	
Number used as logic	61			
Number used as a route-thru	27			
Number of bonded IOBs	34	173	19%	
IOB Flip Flops	4			
Number of BUFGMUXs	1	8	12%	

THANK YOU !

FOR YOUR ATTENTION !