Homework-5 Solutions

1) Labelling the drain of M_2 or gate of M_3 as "X",

let's assume,

$V_{in} \uparrow$, $X \uparrow$, $V_{out} \uparrow$

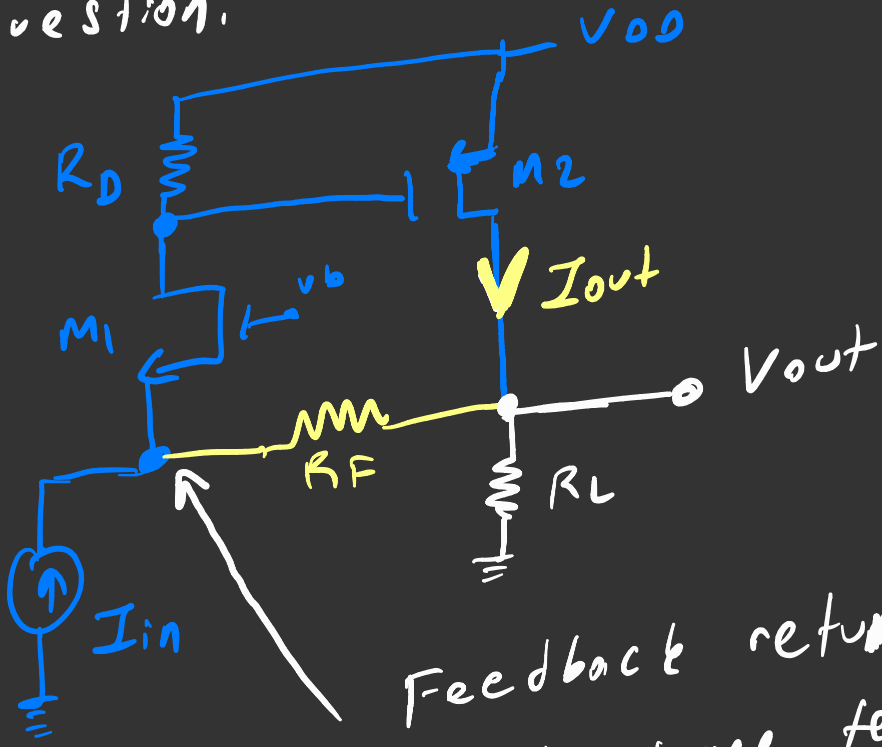
As a result of this, the difference between the input termnals of differential amplifier will decrease and the feedback will stabilize node X and Vout. The system has the "negative feedback".

2) Discussion about the feedback

→ It is relatively easy to find out which kind of feedback is employed at the input. If the feedback path returns to the same terminal with the input it is "parallel (shunt) input feedback". If the feedback returns to a different terminal it is "series input feedback".

However, for the output the kind of feedback depends on which signal we are processing.

Thus, output feedback depends on the application. Let's discuss our circuit in the question.



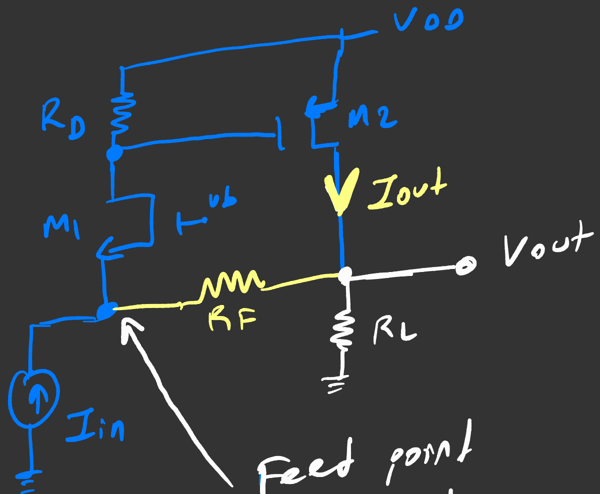
Feedback returns to the same terminal (source of M1). Input current signal also is applied at the same place.

The conclusion we have $\boxed{\text{shunt feedback}}$ at the input.

For the output we have two options. Iout or Vout. In the question, it is specifically expressed that collector current of Q2 will be processed. However, do not forget that we also could have selected Vout.

→ The output is current thus it is "series output feedback".

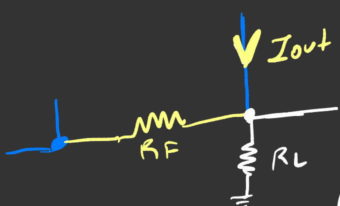
Overall, we have shunt-series (current-current) feedback



Feed point to the input

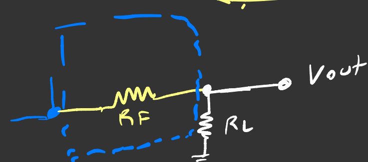
So, what does it change according to the output feedback. The feedback network will change.

Iout (our interest at the output)



Feedback network is current divider network RF, RL

Vout



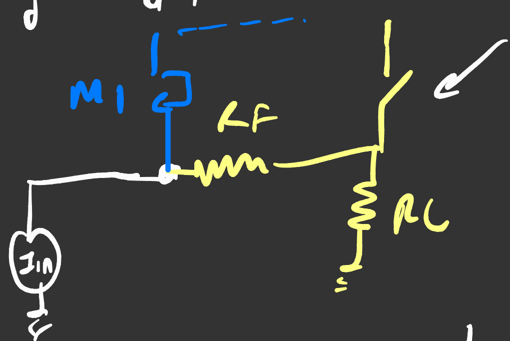
Feedback network only includes RF.

Let's go back to question.

My suggestion for feedback questions.

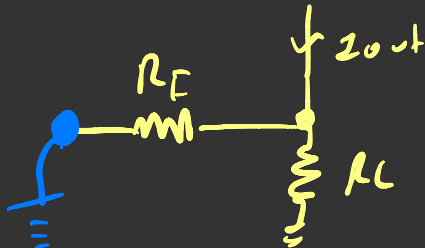
• Always determine the feedback (we have current-current or shunt-series feedback)

•• Solve the system for open loop. we need to find $\frac{I_{out}(OL)}{I_{in}}$. Include loading effects at the input and at the output.



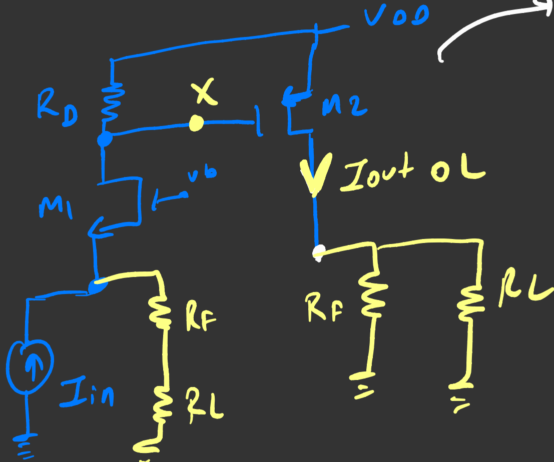
Since we have series feedback at the output, we need to set $\boxed{\text{open circuit}}$

(Input loading)



Since we have shunt feedback at the input we need to set short circuit.

As a rule apply short circuit for shunt feedback, apply open circuit for series feedback when you are dealing with loading effect.



The circuit for open loop gain calculations.

$$I_{in} \cdot \underbrace{\frac{R_F + R_L}{\frac{1}{g_{m1}} + R_F + R_L}}_{\text{current divider at input}} \cdot \underbrace{R_D \cdot}_{\text{converts } I_{in} \text{ to } V_X \text{ at } X} \underbrace{g_{m2}}_{\text{converts } V_X \text{ to } I_{out\,OL}} = I_{out_{OL}}$$

$$\boxed{\frac{I_{out\,OL}}{I_{in}} = A_{OL} = \frac{R_F + R_L}{\frac{1}{g_{m1}} + R_F + R_L} \cdot R_D \cdot g_{m2}}$$

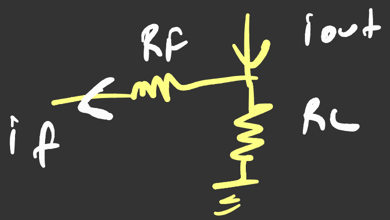
... Find open loop input - output resistances R_i and R_o.

$$\boxed{R_{in_{OL}} = \frac{1}{g_{m1}} \,//\, (R_F + R_L)}$$

$$\boxed{R_{o_{OL}} = \infty}$$

because $V_A = \infty$ for both transistor.

.... Find β factor from feedback network



$$\frac{i_f}{i_{out}} = \frac{R_L}{R_F + R_L}$$

current divider

..... Find loop gain $A\beta$

$$\frac{R_F + R_L}{\frac{1}{g_{m1}} + R_F + R_L} \cdot R_D \cdot g_{m2} \cdot \frac{R_L}{R_F + R_L} = A\beta$$

$$= \frac{g_{m2} R_D R_L}{\frac{1}{g_{m1}} + R_F + R_L}$$

Loop gain

. . . . . . Find closed loop parameters.

$$A_{CL} = \frac{I_{out}}{I_{in}} = \boxed{\frac{\frac{R_F + R_L}{\frac{1}{g_{m1}} + R_F + R_L} \cdot R_D \cdot g_{m2}}{1 + \frac{g_{m2} R_D R_L}{\frac{1}{g_{m1}} + R_F + R_L}}}$$

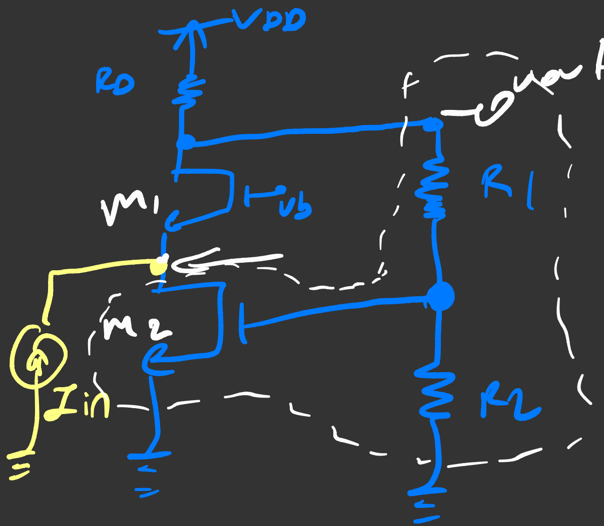
Comment

It goes to $\frac{R_F + R_L}{R_L}$ if $A\beta \gg 1$

$$\boxed{R_{in} = \frac{\frac{1}{g_{m1}} \parallel (R_F + R_L)}{1 + \frac{g_{m2} R_D R_L}{\frac{1}{g_{m1}} + R_F + R_L}}}$$

$$R_{out} = \infty$$

3) we will apply the steps in Question - 2.

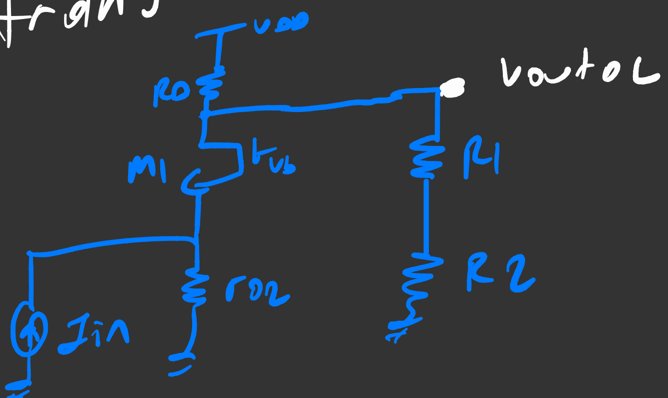


. Input feedback is parallel (shunt)

. Output is also parallel as we are processing vout.

. The feedback is shunt-shunt.

.. Calculation of open loop transresistance gain $\frac{V_{oc}}{I_{in}}$.



* In open-loop signal cannot travel through drain of M2 to gate of M2. This is why R1 and R2 do not load the input.

$$I_{in} \cdot \underbrace{\frac{r_{o2}}{r_{o2} + \frac{\cancel{R_x} + r_{o1}}{g_{m1} r_{o1}}}}_{\text{current divider at input}} \cdot \underbrace{\frac{r_{o2} g_{m1} r_{o1}}{R_x + r_{o2} g_{m1} r_{o1}}}_{\text{current divider at output } (\cancel{A} > 0)}$$

$$\cdot \underbrace{R_x}_{\text{convert } I_{outOL} \text{ to } V_{out\,OL}} = V_{out\,OL}$$

$$\boxed{R_x = R_o + R_1 // R_2}$$

$$R_{in\,OL} = r_{o2} // \frac{R_x + r_{o1}}{g_{m1} r_{o1}}$$

↳ open loop input res.

$R_{out\,OL} = R_x \,//\, r_{o2}\, g_{m1} r_{o1}$

$\hookrightarrow$ open loop output res.

Let's call $g_{m1} r_{o1} r_{o2} = R_y$

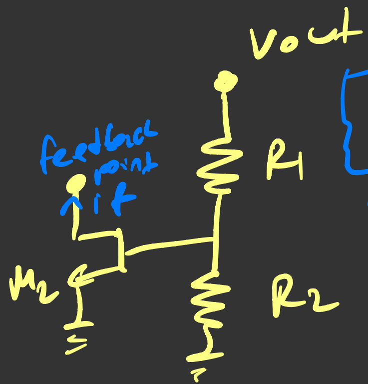
Summarize

$$A_{OL} = \frac{v_{out\,OL}}{I_{in}} = \frac{r_{o2}}{r_{o2} + \frac{R_x + r_{o1}}{g_{m1} r_{o1}}} \cdot \frac{R_y}{R_y + R_x} \cdot R_x$$

$$R_{in\,OL} = r_{o2} \,//\, \frac{R_x + r_{o1}}{g_{m1} r_{o1}}$$

$$R_{out\,OL} = R_x \,//\, g_{m1} r_{o1} r_{o2}$$

Let's zoom in to the feedback network.



$$\boxed{\beta = \frac{i_f}{v_{out}} = \frac{R_2}{R_1+R_2} \cdot g_{m2}}$$

↳ feedback factor.

→ Loop gain

$$\boxed{A\beta = \frac{r_{o2}}{r_{o2} + \frac{R_x + r_{o1}}{g_{m1} r_{o1}}} \cdot \frac{R_y}{R_y + R_x} \cdot R_x \cdot \frac{R_2}{R_1+R_2} \cdot g_{m2}}$$

→ Closed loop gain.

$$\underbrace{\frac{A}{1+A\beta}}_{A_{cl}} =$$ just put the expressions here :D I won't write to

$$R_{in} = \frac{R_{in\,OL}}{1+A\beta} \quad , \quad R_{out} = \frac{R_{OL}}{1+A\beta}$$

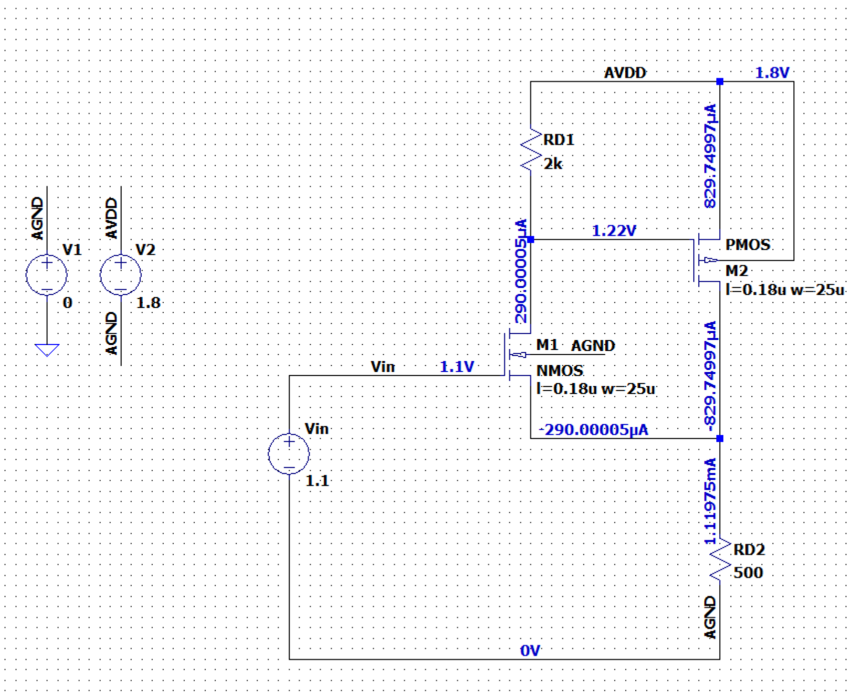
A when you apply shunt-shunt feedback both input and output resistances will decrease by $1+A\beta$

4) It is a series-shunt feedback circuit.

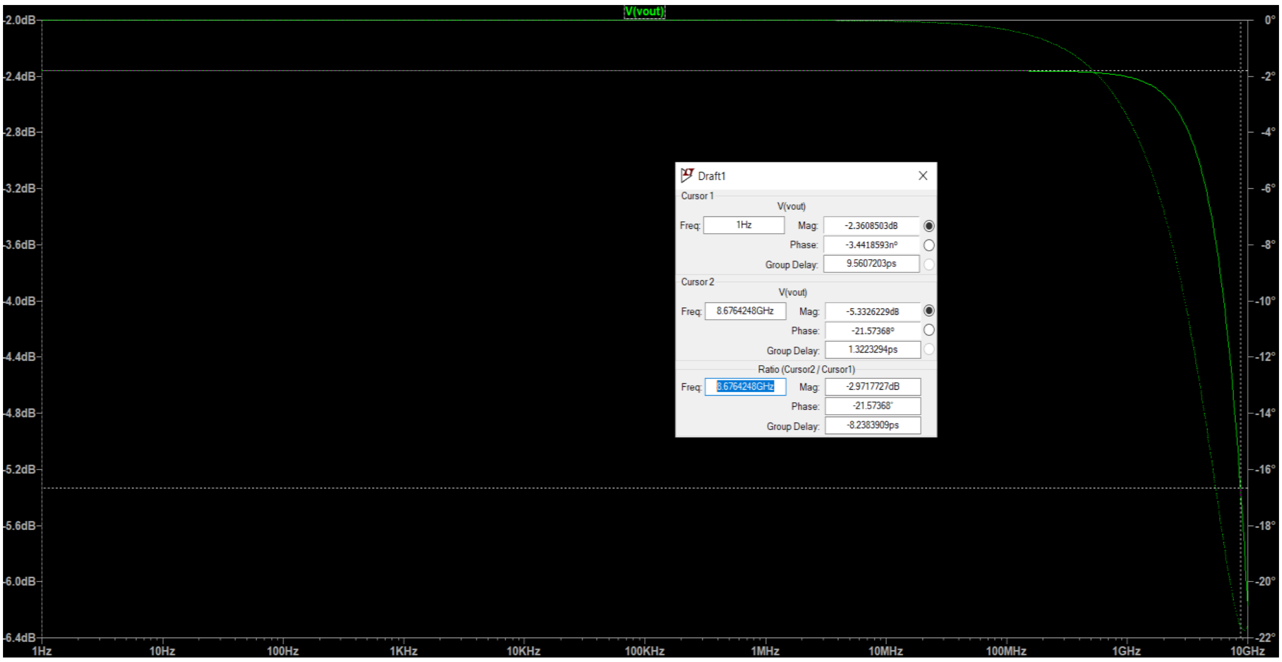
please see next-page for simulations.

QUESTION-4 (LTSPICE SOLUTIONS)

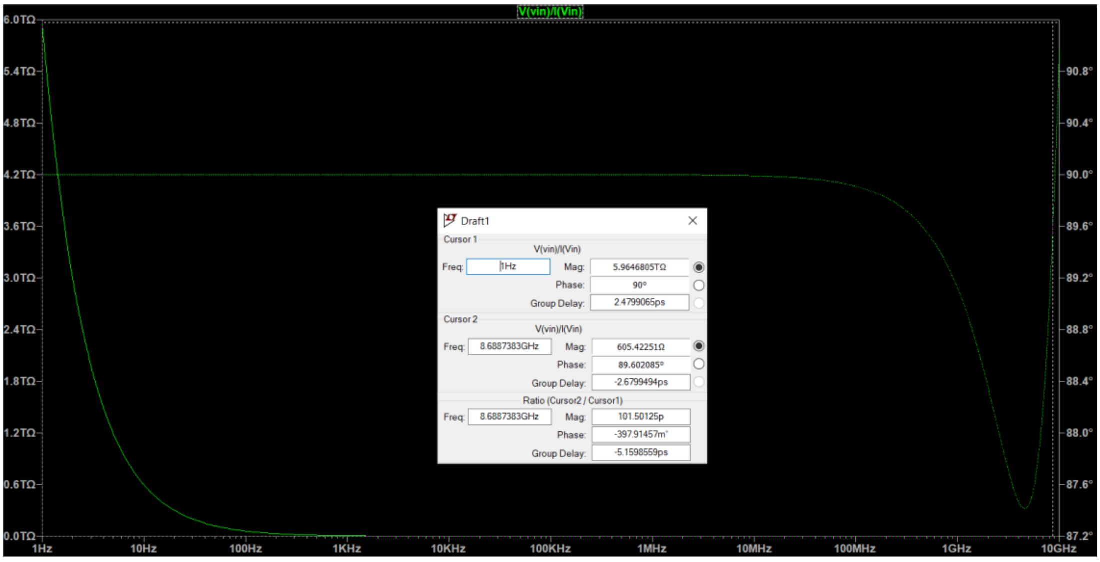
The circuit schematic and DC operating points can be seen below. **(5 pts)**



The feedback is unity. We expect a 0 dB closed loop gain, however the channel length is minimum and it will cause r_o transistors to be very small. It will decrease open loop voltage gain. So we may expect a smaller closed loop gain. You can see the AC response below. Please zoom to the cursor in the graph. The closed loop gain is -2.36 dB, and the bandwidth is around 8.7 GHz. **(5 pts)**



For input impedance you can directly plot for V_{in}/I_{in}. As we expected the input resistance is so high (close to infinity) for low frequencies. However around 3 dB frequency it decreases to 600 ohm as parasitic capacitance (C_{gs}) comes into the play. **(5 pts)**



For output impedance you should not put any AC in to the input voltage source. However you should not erase the 1.1V DC at the input as we must preserve the DC conditions. Then you can either apply test voltage or test current from the output. For the test voltage you can use a very high coupling capacitor to prevent short circuit to the test voltage. Thus, applying a test current much more easier as you do not need any external component. As you can see at low frequencies, it is around 30 ohm, for high frequencies arount the 3 Db frequency, it is around 107 ohm, as the feedback effect decreases and output resistance increases, which is a bad thing for a voltage output amplfier. **(10 pts)**