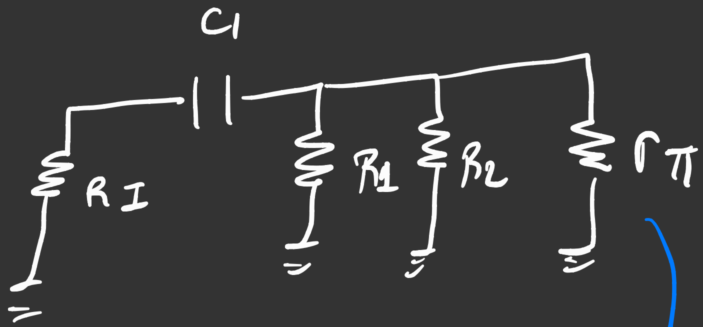
Homework 2 Solutions

1-a) Let's calculate all the time constants due to each capacitor.

$R_{C1} \rightarrow$

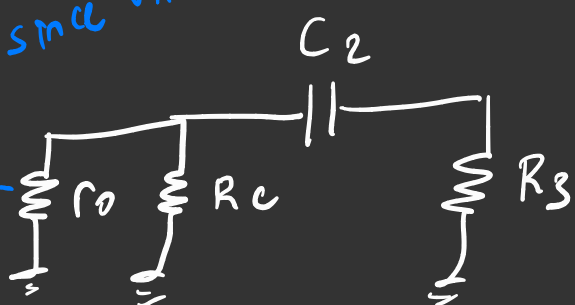


RE is not effective since C3 shorts.

$$\tau_{C1} = C_1 \left[R_I + (R_1 \,//\, R_2 \,//\, r_\pi) \right]$$

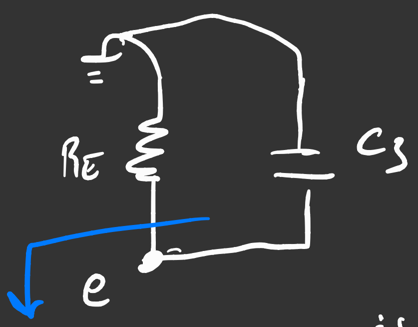
I did not neglect since VA < ∞

$R_{C2} \rightarrow$



$$\tau_{C2} = C_2 \cdot \left[(R_C \,//\, r_o) + R_3 \right]$$

C_3 is a little bit more tricky.



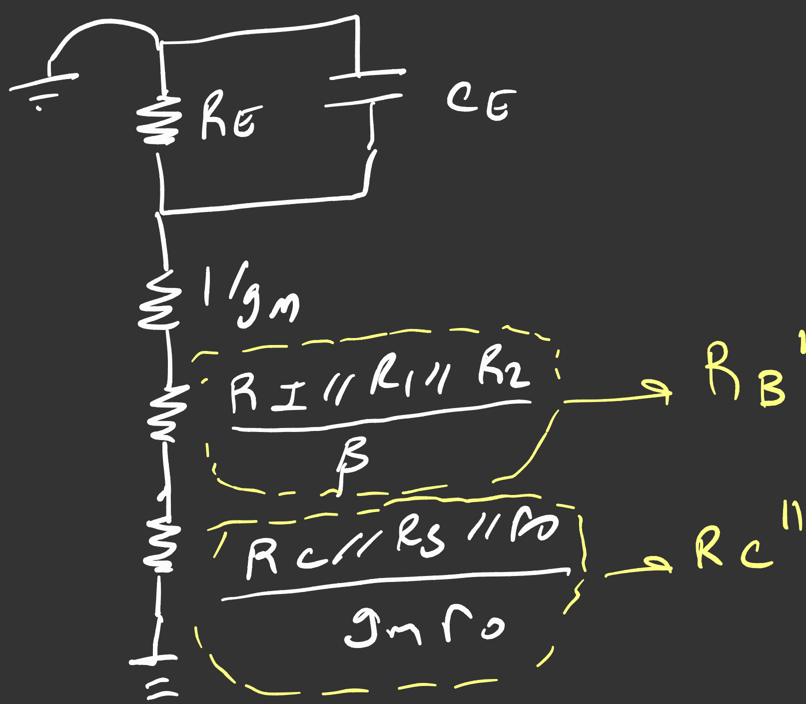
what is the resistance seen by the emitter side of the transistor. ~~A~~ we have resistance at base. Thus, we need to transfer this resistance to the emitter side. we also have $1/g_m$.

The resistance at base if you short C_1. $R_B = R_I \,//\, R_1 \,//\, R_2$

we can transfer it to the emitter by dividing it to β.

* we also have $V_A \to \infty$ so we can transfer collector resistance to the base by dividing it to $g_m r_o$. $R_C' = R_C // R_3 // r_o$ when we short R_3.

* Regarding this we have,



$$\tau_{c3} = C_3 \cdot [R_E \,//\, (\frac{1}{g_m} + R_B' + R_C')$$

You can write

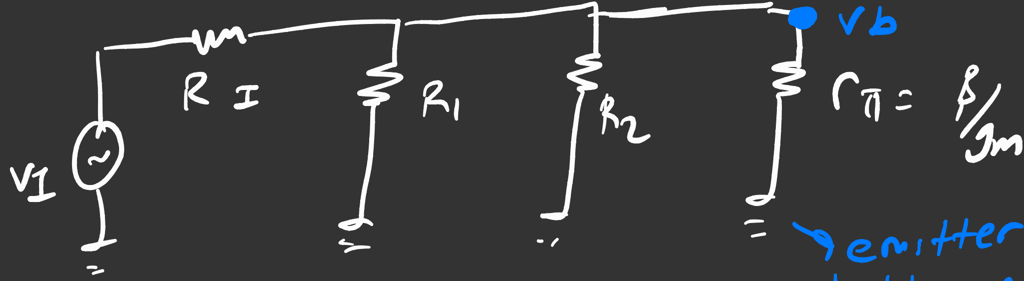
$$f_{3dBL} = \frac{1}{2\pi} \left[\frac{1}{\tau_{c1}} + \frac{1}{\tau_{c2}} + \frac{1}{\tau_{c3}} \right]$$

I did not write all the expression since it will be too long. The key is to find the time constants and equivalent resistances.

1-b) For the mid-band C_3 shorts R_E. R_E is not effective.

we have a voltage loss due to divider at the input.

↓

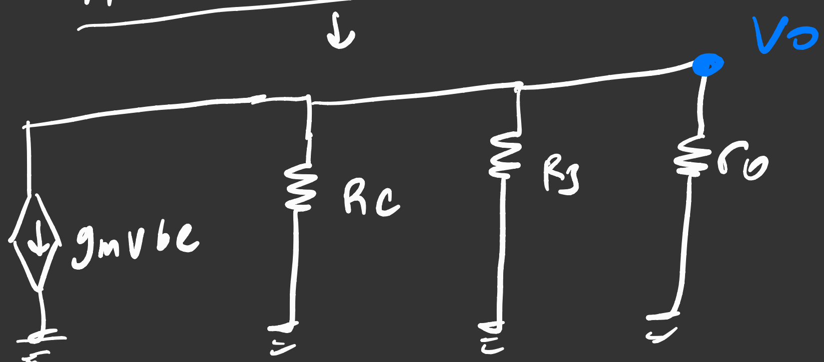


emitter at the ground due to C3!

$$R_1 // R_2 // \beta/g_m = R_{BB}$$

$$\frac{v_b}{v_I} = \frac{R_{BB}}{R_{BB} + R_I}, \quad v_b = v_{be}$$

<u>At the output</u>



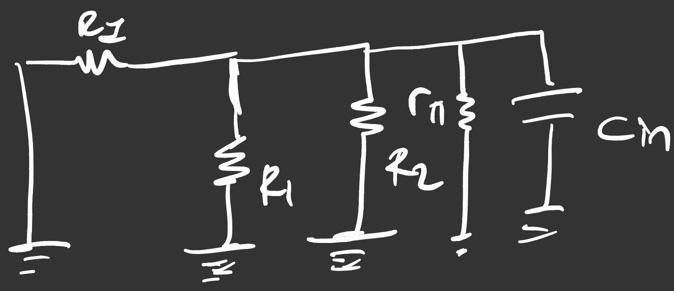
$$R_C // R_3 // r_o = R_L'$$

$$\frac{v_o}{v_b} = g_m R_L',$$

$$\boxed{\frac{v_o}{v_I} = g_m R_L' \left(\frac{R_{BB}}{R_{BB} + R_I} \right)}$$

Loss factor due to realistic source resistance.

1-c) At the input we have



$$C_{in} = C_\pi + (g_m R_L') C_\mu$$

↳ recall R_L' from 2-b

miller effect

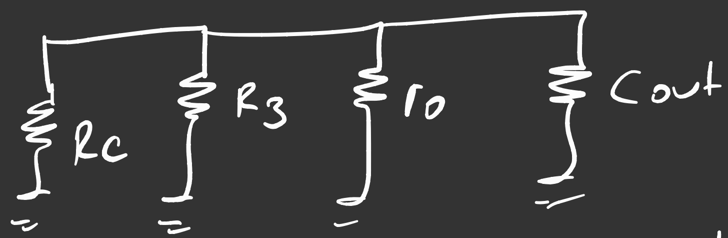
C_{in} sees the equivalent resistance

$$R_{cin} = R_I \,//\, R_2 \,//\, r_\pi$$

$$f_{p_1} = \frac{1}{2\pi (C_{in} R_{cin})}$$

- Again, the important part is to find resistance and capacitance.

At the output



- The miller capacitance reflect to the output with it's own value.

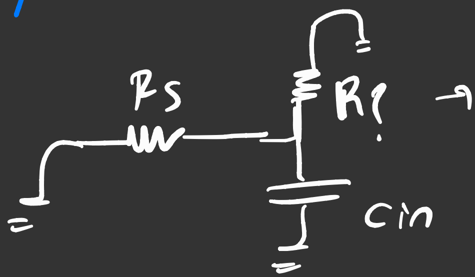
$$C_{out} = C_\mu$$

$$R_{cout} = R_C \parallel R_3 \parallel r_o$$

$$f_{P_2} = \frac{1}{2\pi\,(C_{out} R_{cout})}$$

- Note that we are shorting the bypass and coupling capacitor as their impedence goes to zero, while frequency is increased. $\rightarrow Z_C = \frac{1}{sC}$

2) At the input



→ if we can find this port, we can write input pole easily.

we have a common gate configuration.

The input resistance of it,

$\frac{1}{g_m} + \frac{R_D}{g_m r_o}$, if $\lambda > 0$ → input res. of CG

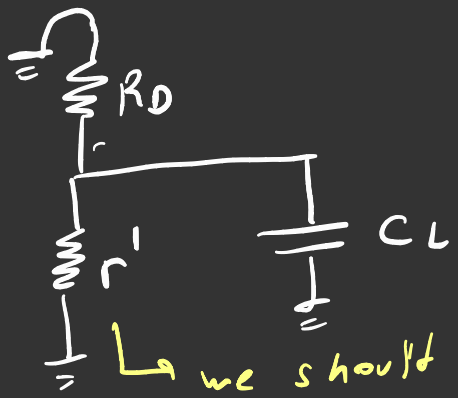
However, we also have R_P, thus

$$\boxed{R? = \frac{1}{g_m} + \frac{R_D}{g_m r_o} + R_P}$$

→ the important part of the question

$$f_{pin} = \frac{1}{2\pi \underbrace{(R_S // R?)\, C_{in}}_{\text{we know these variables}}}$$

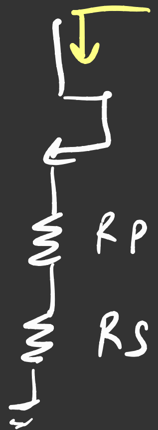
At the output



we should find this resistance

Essentially, when you look to the configuration from the drain, it's an amplifier with source degeneration.

what is the resistance?



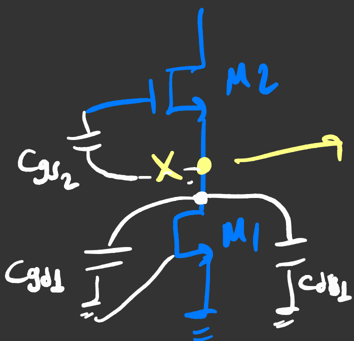
$$r' \cong (g_m r_o) \cdot (R_P + R_S)$$

$$f_{p_{out}} = \frac{1}{2\pi (R_D \| r') C_L}$$

the important part of the question

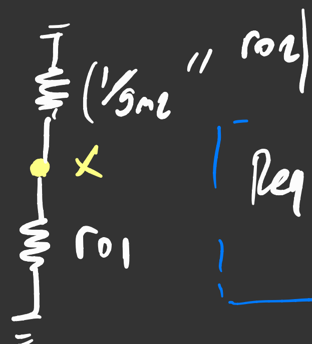
3) At the input we do not have any pole if we assume V_{in} is ideal, which means source resistance of the V_{in} source is equal to zero.

At the output



what is the equivalent resistance and capacitance at node X?

Gate is AC ground as V_b is a DC voltage.

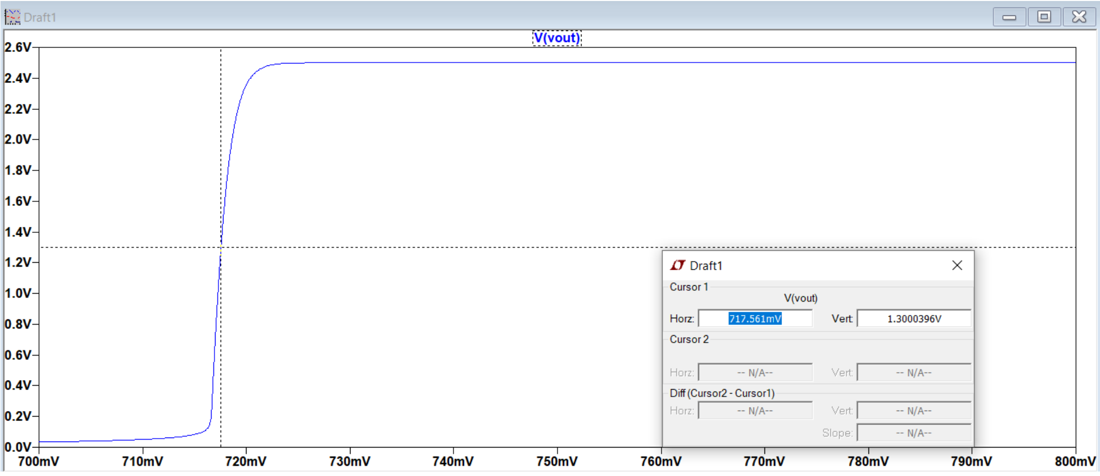


$$\boxed{R_{eq} = r_{o1} \,//\, r_{o2} \,//\, \frac{1}{g_{m2}}}$$

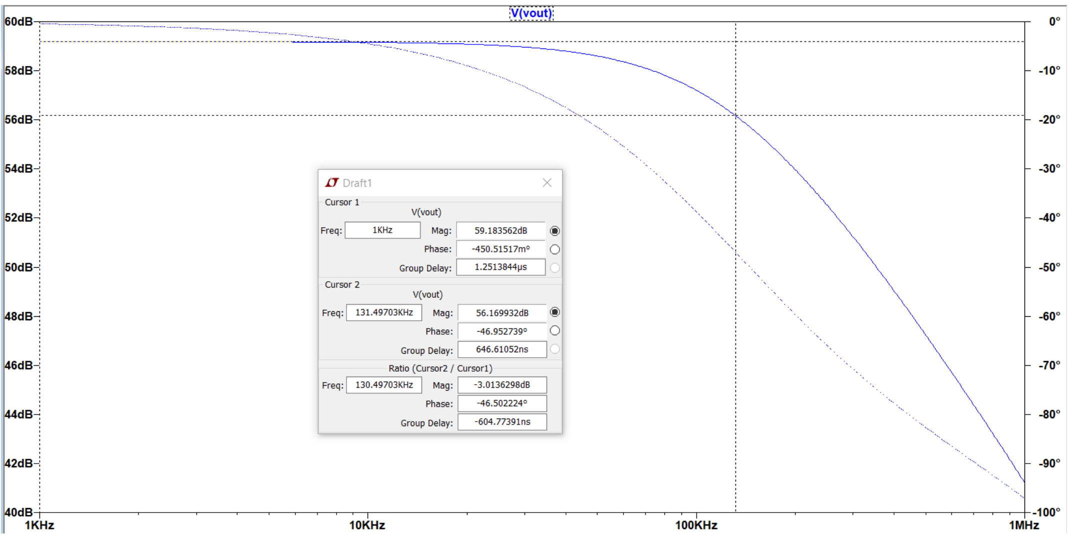
$$\boxed{C_{eq} = C_{gd1} + C_{db1} + C_{gs2}}$$

$$f_{3dB} = \frac{1}{2\pi (R_{eq})(C_{eq})}$$

4) a) To bring the output to the desire value 1.3V, the input source can be swept. You may need to increase the resolution of the sweep, since the circuit may have a large gain and the output would be very sensitive in this case. In figure below, you can see that, the required input DC level is 717.651 mV.



b) In the figure below, you can see the bode plot of the Vout/Vin. The gain is around 59 dB and the bandwidt is around 130 kHz. Also look at carefully to the phase in the cursor. It is around 45 degree, which is expected. You may not observe the effect of 200fF load capacitance as discrete transistors such as 2N2222 has really large parasitic capacitance.



As you observed, the biasing is really challenging in this way (VDCin=717.561mV, in real life supplies are not precise as much as in this question). The open loop amplifiers generally have this problem. In the negative feedback, we are going to see the feedback will also set the DC bias.