Homework-1 Solutions

1-a) The circuit is an active loaded cascode amplifier besides R_p. R_p is parallel to r_{o2}.

$$r_{o2}' = R_p // r_{o2} = \frac{R_p r_{o2}}{R_p + r_{o2}}$$

$$\text{Gain} = -g_{m1} R_{out}$$

$$R_{out} \cong (r_{o4} \cdot g_{m3} r_{o3}) // (r_{o1} g_{m2} r_{o2}')$$

$$= \frac{g_{m3} \cdot r_{o3} \cdot r_{o4} \cdot g_{m2} r_{o1} \frac{R_p r_{o2}}{R_p + r_{o2}}}{g_{m3} r_{o3} r_{o4} + g_{m2} r_{o1} \frac{R_p r_{o2}}{R_p + r_{o2}}}$$

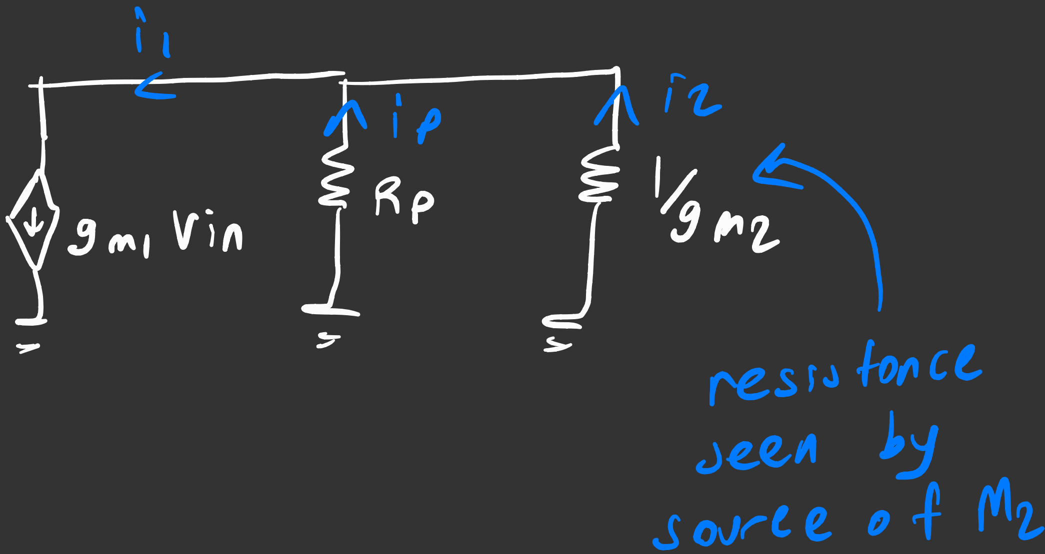
1-a (cnt)

$$= \frac{g_{m2} g_{m3} r_{o1} r_{o2} r_{o3} r_{o4} R_p}{g_{m3} r_{o3} r_{o4} (R_p + r_{o2}) + g_{m2} r_{o1} r_{o2} R_p}$$

$$\boxed{Gain = -g_{m1} \frac{g_{m2} g_{m3} r_{o1} r_{o2} r_{o3} r_{o4} R_p}{g_{m2} r_{o3} r_{o4} (R_p + r_{o2}) + g_{m2} r_{o1} r_{o2} R_p}}$$

- For this circuit $G_m = g_{m1}$
- Do not forget 180° phase!

1-b) In the circuit small signal current is created by M_1. However this current is shared by M_2 and R_p. Please see equivalent circuit.



M_2 is common gate amplifier, behaves as current buffer and buffers i_2 to i_{out}.

$$i_2 = \frac{V_{in}\, g_{m1}\, R_p}{\frac{1}{g_{m2}} + R_p}$$

$$= \frac{v_{in}\, g_{m1}\, g_{m2}\, R_p}{g_{m2} R_p + 1}$$

$i_{out} = i_2$ (current buffering)

$$G_m = \frac{i_{out}}{v_{in}}$$

$$G_m = \frac{g_{m1} g_{m2} R_p}{g_{m2} R_p + 1}$$

$$Gain = -G_m R_{out}$$

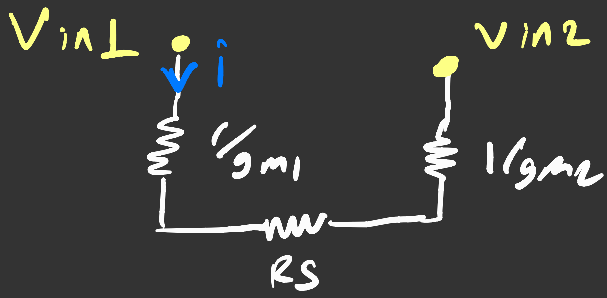
$$R_{out} = r_{o4} g_{m3} r_{o3}$$

→ we neglect the contribution of lower side of the circuit on output resistance as $\lambda_1 = \lambda_2 = 0$

$$\boxed{\text{Gain} = -\frac{g_{m1}\, g_{m2}\, g_{m3}\, r_{o3}\, r_{o4}\, R_p}{g_{m2} R_p + 1}}$$

- The differenca between 1-a and 1-b that Gms of the overall circuit are different. In 1-b Rp changes Gm!

2) Due to Rs, we need to calculate Gm of the circuit.



Assume $\frac{1}{g_{m1}} = \frac{1}{g_{m2}}$

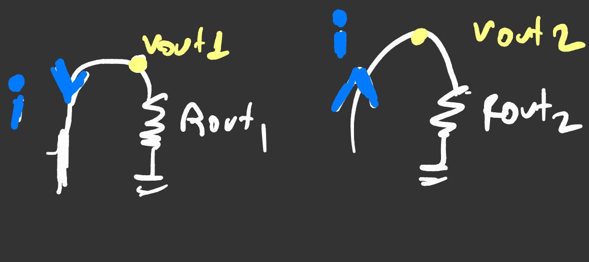
$$i = \frac{V_{in1} - V_{in2}}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}} + R_S}$$

- This current also flows throug $Q_3 - Q_4$ as they are current buffers. (Common-base config.)

$V_{in} - V_{in2} = V_{id}$ → differential input signal

$$i = \frac{v_{id}\, g_{m1,2}}{g_{m1,2} R_S + 2}$$

How about the output?



Let's assume that circuit is fully symmetrical so $R_{out1} = R_{out2}$

$$V_{out1} = -i \cdot R_{out1,2}$$

$$V_{out2} = i \cdot R_{out1,2}$$

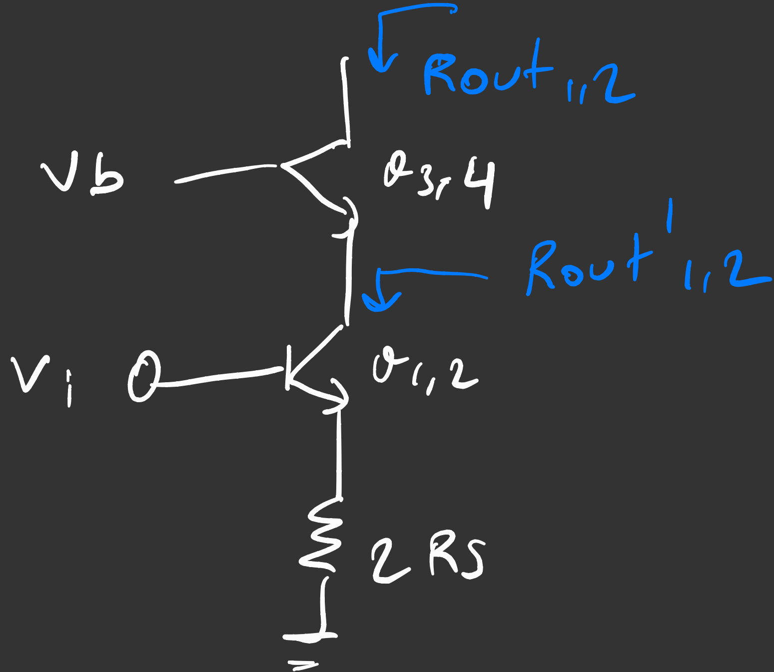
$$V_{out} = V_{out2} - V_{out1} = 2i\,R_{out1,2}$$

$$V_{out} = \frac{2V_{id}\,g_{m1,2}}{g_{m1,2}R_s + 2} \cdot R_{out1,2}$$

$$\frac{V_{out}}{V_{id}} = \text{Gain} = \underbrace{\frac{2g_{m1,2}}{g_{m1,2}R_s + 2}}_{G_m} \cdot \underbrace{R_{out1,2}}_{R_{out}}$$

So what about $R_{out1,2}$?

We can use half-equivalent circuit



$$R_{out}'{}_{1,2} = g_{m1} r_{o1} (2R_S // r_{\pi1})$$

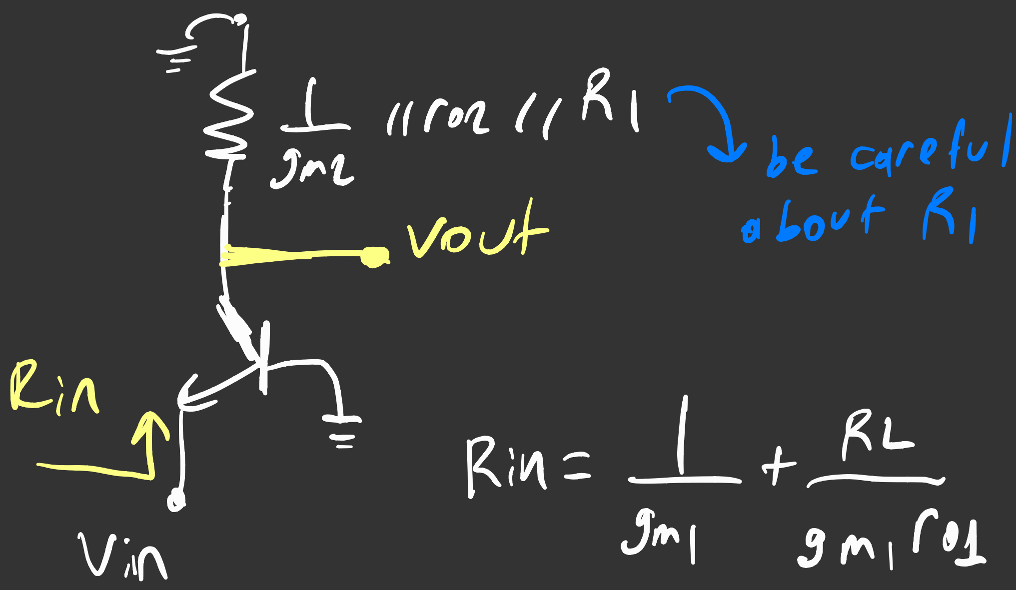
$$R_{out\,1,2} = (R_{out}'{}_{1,2} // r_{\pi3})\, g_{m3} r_{o3}$$

$$\boxed{R_{out\,1,2} = \left[\left(g_{m1} r_{o1} (2R_S // r_{\pi1}\right) // r_{\pi3}\right] g_{m3} r_{o3}}$$

Rout

3) C_B pulls base of Q_1 to ground and shorts R_2. (in AC)

Let's simplify the circuit for small signal.



$$R_{in} = \frac{1}{g_{m1}} + \frac{R_L}{g_{m1} r_{o1}}$$

where

$$R_L = \frac{1}{g_{m2}} \parallel r_{o2} \parallel R_1$$

$$\boxed{R_{in} = \frac{1}{g_{m1}} + \frac{\frac{1}{g_{m2}} \,//\, r_{o2} \,//\, R_1}{g_{m1} r_{o1}}}$$

$$Gain = G_m R_{out}$$

$$R_{out} = R_L \,//\, r_{o1}$$

$$G_m = g_{m1}$$

$$\boxed{Gain = g_{m1}\left(\frac{1}{g_{m2}} \,//\, r_{o1} \,//\, r_{o2} \,//\, R_1\right)}$$

☆ No phase inversion in common base amplifier!

4) Key points for the design.

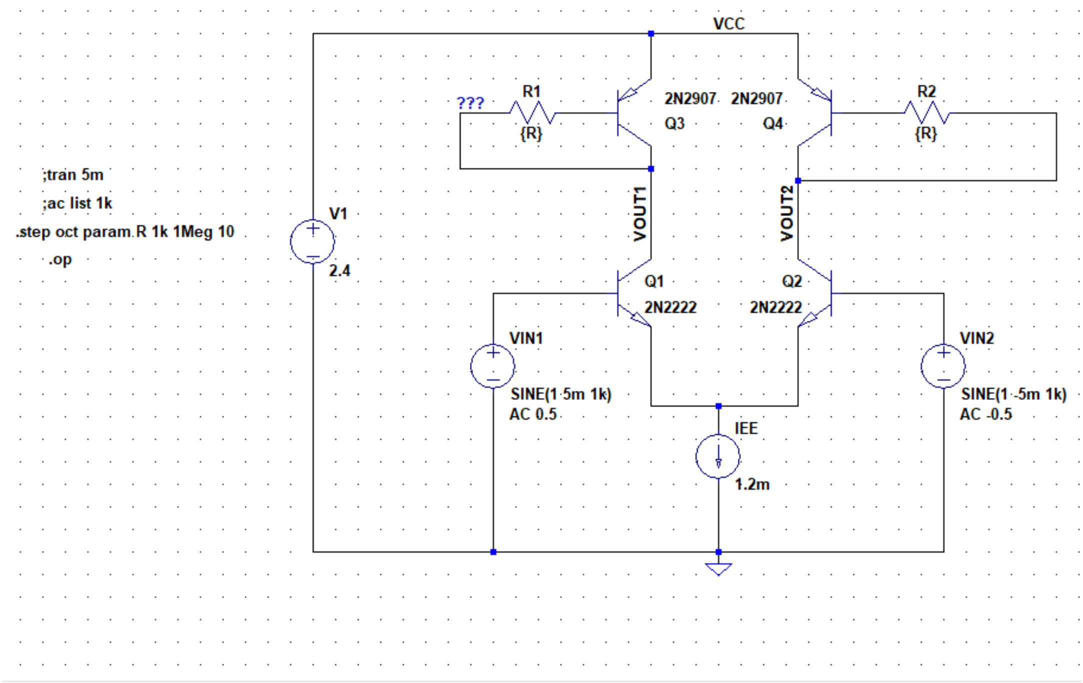
- Choose a proper common mode DC voltage otherwise the circuit won't amplify the signal.
- Since the circuit has perfect symmetry $R_1 = R_2$ and it is the only design parameter as V_{CC}, I_{EE} predefined. You cannot change the parameters of BJT

* How to maximize gain?

Since Gm of the circuit $gm_{1,2}$ you should maximize Rout. It's a spice question, so you can use spice as an optimizer tool!. For Ex. you can use single frequency with sweeping $R_{1,2}$ and you can choose the value.

Please see other page regarding this!

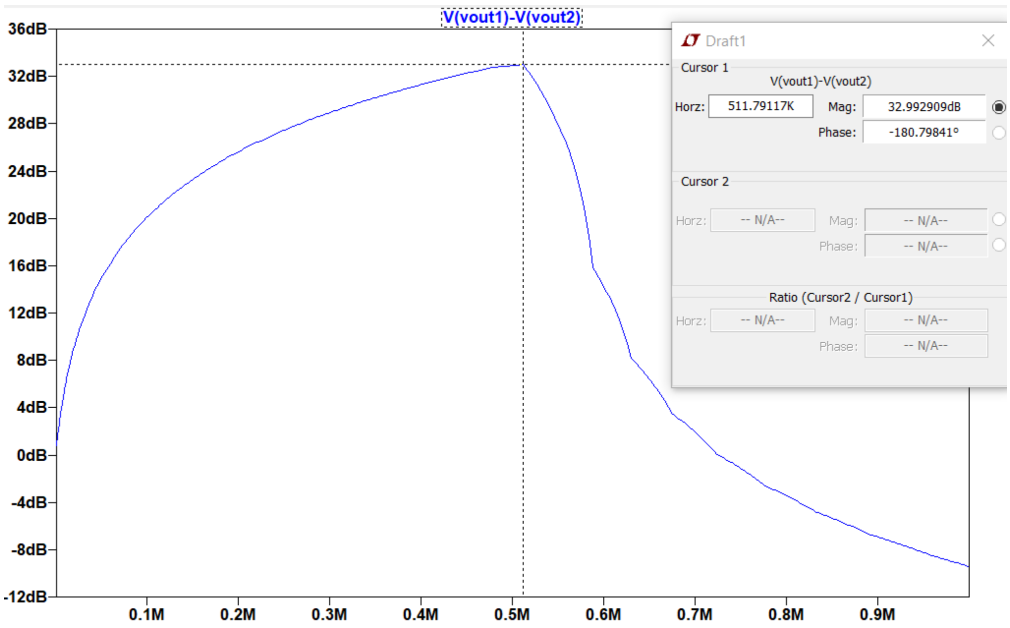
The schematic is given in below. I chose 1V common mode DC voltage. You can choose another reasonable value for common mode voltage.



Please analyze schematic,

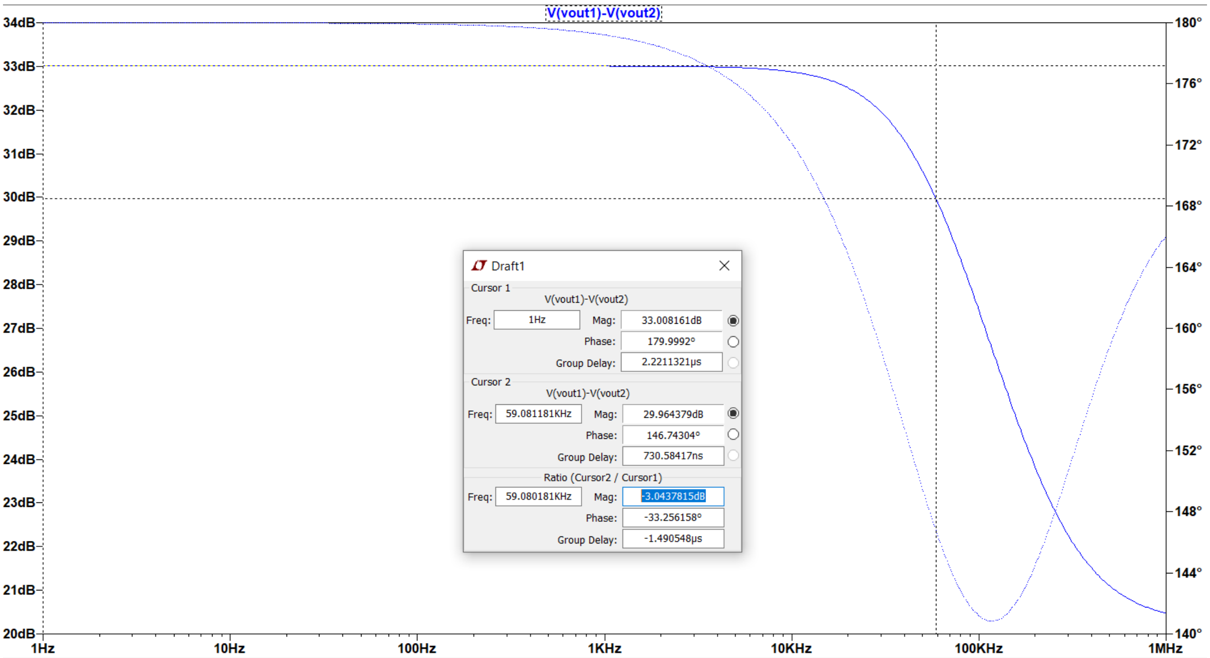
- ➔ We have sinusoidal sources with 1V offset (DC Common Mode), 10 mV differential signal @ 1kHz (for transient analysis) and 1V differential AC signal (for AC analysis)
- ➔ We defined a parameter {R} in order to sweep it to obtain maximum gain.
- ➔ We have "ac list 1k" command to choose single frequency. We are going to observe gain vs R1,2 @ 1kHz.
- ➔ ".step oct param R 1k 1Meg 10" command sweeps the design variable R, 1k to 1M.

The sweep result is given below.



The result shows us the optimal value of R is equal to 511 kΩ. After this point we can continue with this value.

The traditional AC simulation between 1 Hz and 1 MHz is given below. This is essentially a Bode plot. The gain is 33 dB and 3 dB frequency is around 60 kHz. Discuss why the circuit does not have any low frequency pole?



The transient analysis results are given below. Observe the DC common mode input-output voltages from these waveforms. Observe differential signals. For 10 mV differential input signal we have 360 mV differential output voltage. The gain is equal to 31V/V. It is not exactly the same as AC simulation results! (Why?)