

Homework \rightarrow Solution



1) Since both circuits have the same C_1 , we only need to provide series $L_1 - R_1$ to parallel $L_P - R_P$ conversion.

$$\begin{aligned} j\omega L_1 + R_1 &= \frac{j\omega L_P R_P}{j\omega L_P + R_P} \\ -\omega^2 L_1 L_P + j\omega L_1 R_P + j\omega R_1 L_P + R_1 R_P \\ j\omega L_P R_P &= \end{aligned}$$

$$\begin{aligned} R_1 R_P - \omega^2 L_1 L_P &= 0 \quad \textcircled{1} \\ R_1 L_P + R_P L_1 &= R_P L_P \quad \textcircled{2} \\ R_1 L_P + R_P L_1 &= R_P L_P \end{aligned}$$

In the schematic $L_1 = L_P$
is desired, using ①

$$R_P = \frac{\omega^2 L_1^2}{R_1}$$

Note: It is a question for
calculating complex impedances.
Although it seems pointless
now, you are going to see it
for impedance matching circuit
in RF electronics.

2)



Returned
vo/Huse

$$\text{Loop } b_{\text{ain}} = \frac{V_r}{V_n} = g_m \frac{z_L}{z_L + z_1 + z_2} \cdot z_2 \frac{V_r}{R_L}$$

LG

where

$$z_L = sL$$

$$z_1 = \frac{1}{sC_1}$$

$$z_2 = \frac{\frac{1}{sC_2} \cdot R_L}{\frac{1}{sC_2} + R_L} = \frac{R_L}{1 + sC_2 R_L}$$



$$L_6 = \frac{g_m \cdot sL}{sL + \frac{1}{sC_1} + \frac{R_L}{1+sC_2R_L}} \cdot \frac{R_L}{1+sC_2R_L}$$

$$= \frac{g_m R_L \cdot jwL}{jwL - w^2 R_L C_2 L - j \frac{R_L C_2}{C_1} + \frac{R_L C_2}{C_1} + R_L}$$

* we need to eliminate real part

$$-w^2 R_L C_2 L + R_L \frac{C_2}{C_1} + R_L = 0$$

$$w^2 C_2 L = \frac{C_2}{C_1} + 1$$

$$w = \sqrt{\frac{C_1 + C_2}{C_1 C_2 L}}$$

To provide oscillations

$$|L_6| \geq 1$$

L_6 at oscillation freq,

$$\frac{g_m R_L w L}{w L - \frac{1}{w C_1}} \geq 1$$

$$= \frac{g_m R_L L}{L - \frac{1}{\frac{(C_1 + C_2)}{LC_1 C_2} \cdot C_1}}$$

→ Let's finalize $|L6|$

$$|L6| \equiv \frac{g_m R_L}{1 - \frac{C_2}{C_1 + C_2}} \geq 1$$

$$\boxed{g_m R_L \geq \frac{C_1}{C_1 + C_2}}$$

* I may do a calculation error. But you got the point. For oscillation frequency cancel the real part. After that provide $|L6| \geq 1$ for oscillation

3) For this question, I won't analyse the circuit with details.
The short operation follows

→ V_o has two state for
or -10 v. V_o charges the
capacitor at negative terminal.

At the same time a resistive
divider network sets V^+ .
As soon as capacitor charged
and reaches an equal voltage
with V^+ , V_o goes to other
saturation voltage.

$$T = 2 R \times C \times \ln \left(\frac{1+\beta}{1-\beta} \right)$$

where β is the voltage divider factor

At point A and $T = 2 \text{ ms}$

$$\beta = \frac{R_1 + R_3}{R_1 + R_2 + R_3} = \frac{2}{3}$$

\downarrow
500 Hz

$$2 \text{ ms} = 2 \cdot R \times 10^{-8} F \cdot \ln \left(\frac{\frac{5}{3}}{\frac{1}{3}} \right)$$

$$R_X = \frac{2 \times 10^{-3}}{2 \times 10^{-8} \times 1.61} \approx 62 \text{ k}$$

At point B, β will change.

Corresponding $\frac{T}{T} = \frac{R_1}{R_1 + R_2 + R_3} = \frac{1}{3}$

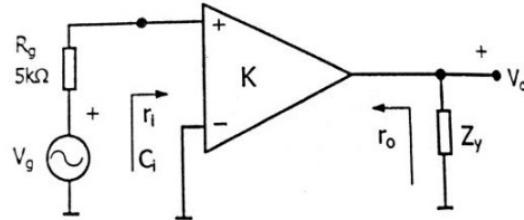
$$T = 2 \times 62 \times 10^3 \times 10^{-8} F \times \ln \left(\frac{\frac{4}{3}}{\frac{2}{3}} \right)$$

$\approx 0.86 \text{ ms}$

$f \approx 1.2 \text{ kHz}$

QUESTION-4 AND 5

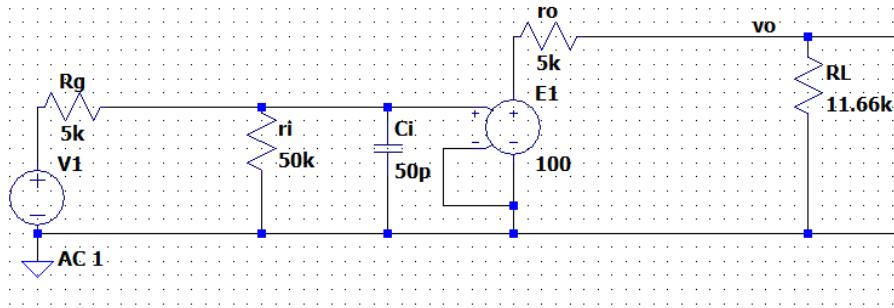
4) For this question, let's find the input pole first. We have the circuit below.



Here, r_i is equal to 50k, thus our pole at the input,

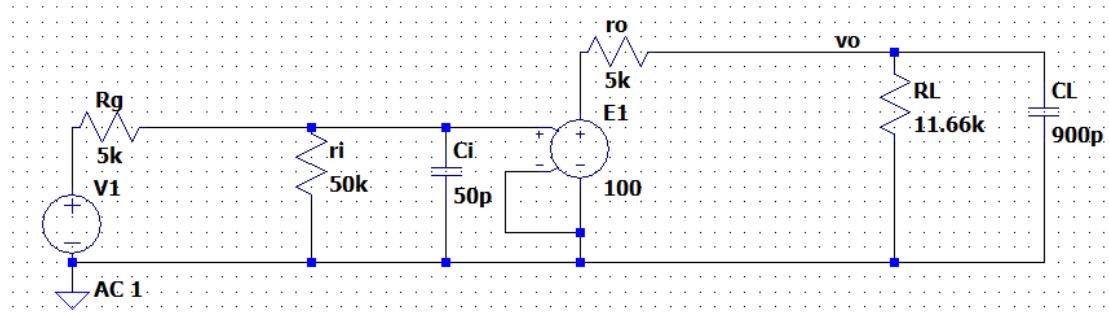
$$p_1 = 1/[2\pi(R_g/r_i)C_i] = 701 \text{ kHz}$$

At output our unloaded gain is 100V/V. It decreases 70V/V after adding a resistor. Thus we are adding a load 11.66k. The resistive divider network between 5k and 11.66k, decreases the gain to 70V/V. You can see the output network below. In the schematic 100 is the unloaded gain. You can see the output network and interface between R_L and r_o .



However the load is not completely true as -3 dB becomes 50 kHz. Thus we understand that the load includes a capacitance, which is called as p_2 .

$p_2 = 1/[2\pi(R_L/r_o)C_L] = 50 \text{ kHz}$, since we know all the values except C_L , we can calculate it. The resulting C_L is equal to 900 pF. See the updated schematic below.

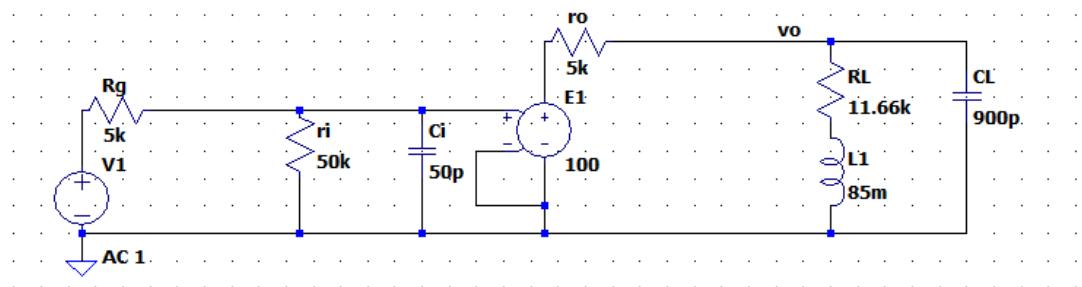


Now we have the whole circuit model. How can we provide bandwidth extension using L. If we add an L which is series to R_L , we can provide bandwidth extension, is called shunt peaking. L and R_L will bring a zero to the transfer function and will extend the bandwidth. Actually, there is no optimum value but we will define a factor m, which is given below. (**Note: I will grade your homeworks until this point. If you did not calculate an exact value it is not a problem, I will look for your comments.**)

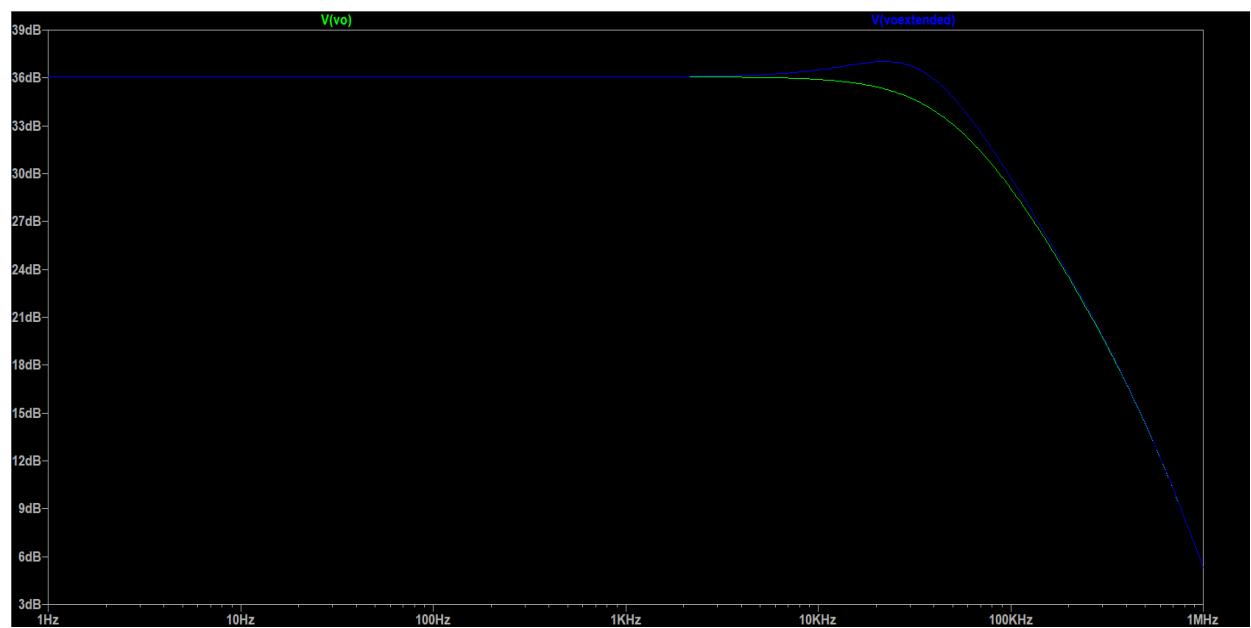
$$m = R_L^2 C_L / L$$

In this equation $m = \sqrt{2}$ results with optimum bandwidth but you will see a peaking in frequency response. See page 271,272,273 in “The Design of CMOS Radio Frequency Integrated Circuits” by Thomas H. Lee in second edition for further reading.

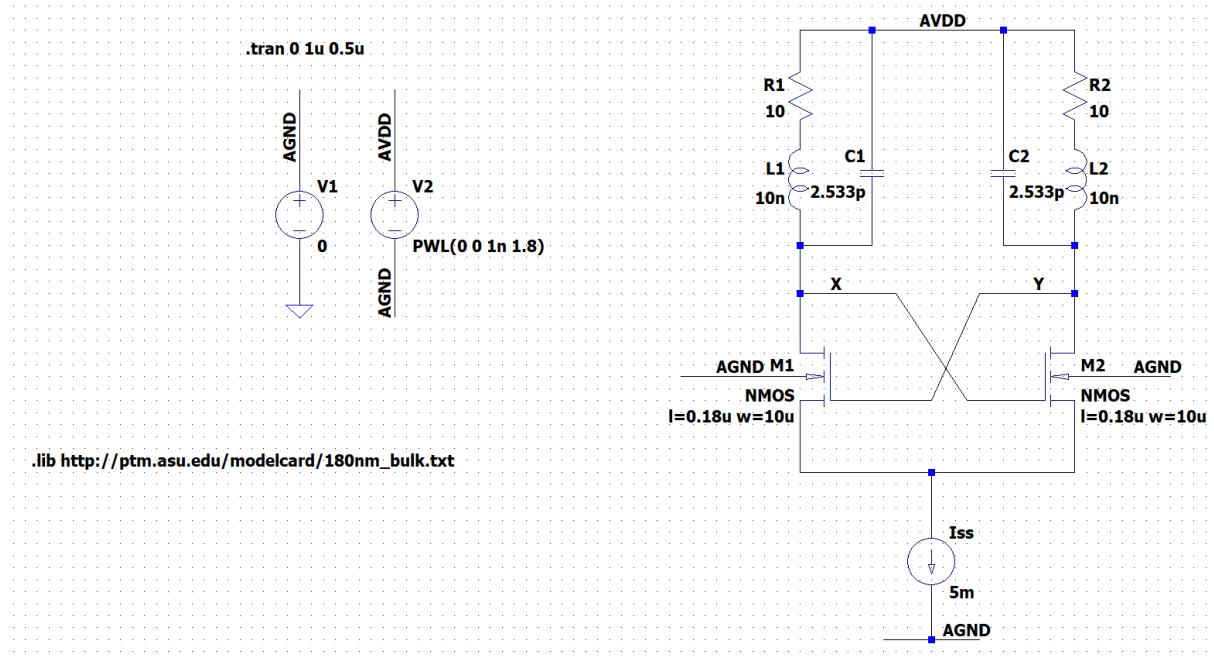
The resulting $L = 85 \text{ mH}$. The updated circuit model is given below.



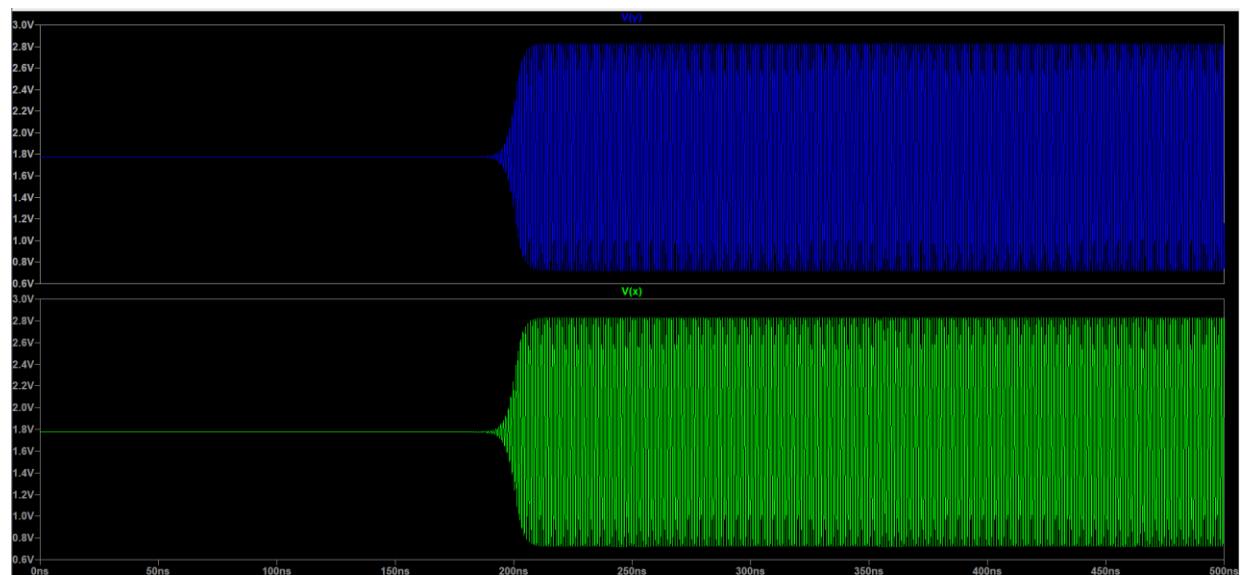
You can see the frequency response before and after using L in below. After using L bandwidth extends 50 kHz to 65 kHz.



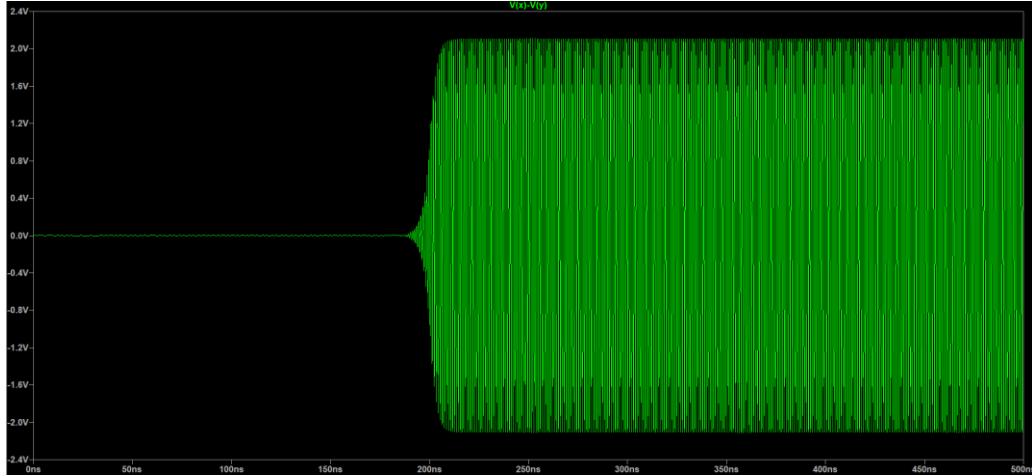
5) We can easily calculate the required capacitance from $w = \sqrt{1/LC}$. The corresponding C for 1 GHz is around 2.53 pF. The circuit schematic can be seen below.



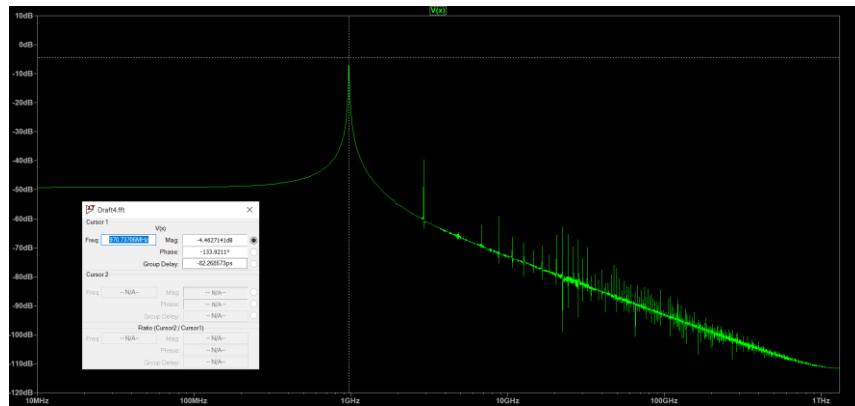
In real life, there are a lot of noise source from power supply etc. Thus the oscillation happens when Barkhausen criteria is met. However the simulator is an ideal environment. Thus we can apply a pw1 source from AVDD to give the switching effect of powering on which will inject a noise to the circuit. The oscillation at Vx and Vy can be seen below. After a while, the circuit starts oscillating.



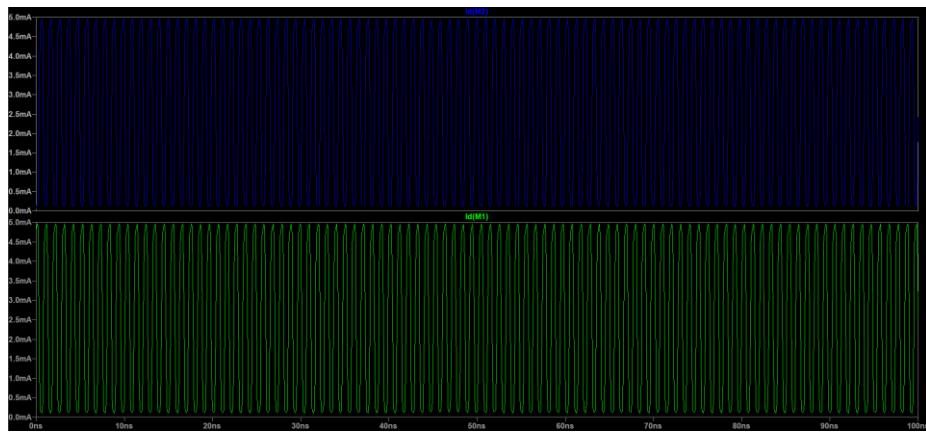
For the differential signal Vx-Vy, please see the waveform below.



You can see the Fast Fourier Transform of the signal to see the frequency. The oscillation frequency is around 970 MHz which is close to 1GHz but of course in practical it is very challenging to provide the exact frequency.



See drain currents of M1 and M2 below. As it is expected tail current limits the currents.



Note: After doing parametric or trial-error simulations I have found the minimum current as 1.5 mA for the oscillation to start.