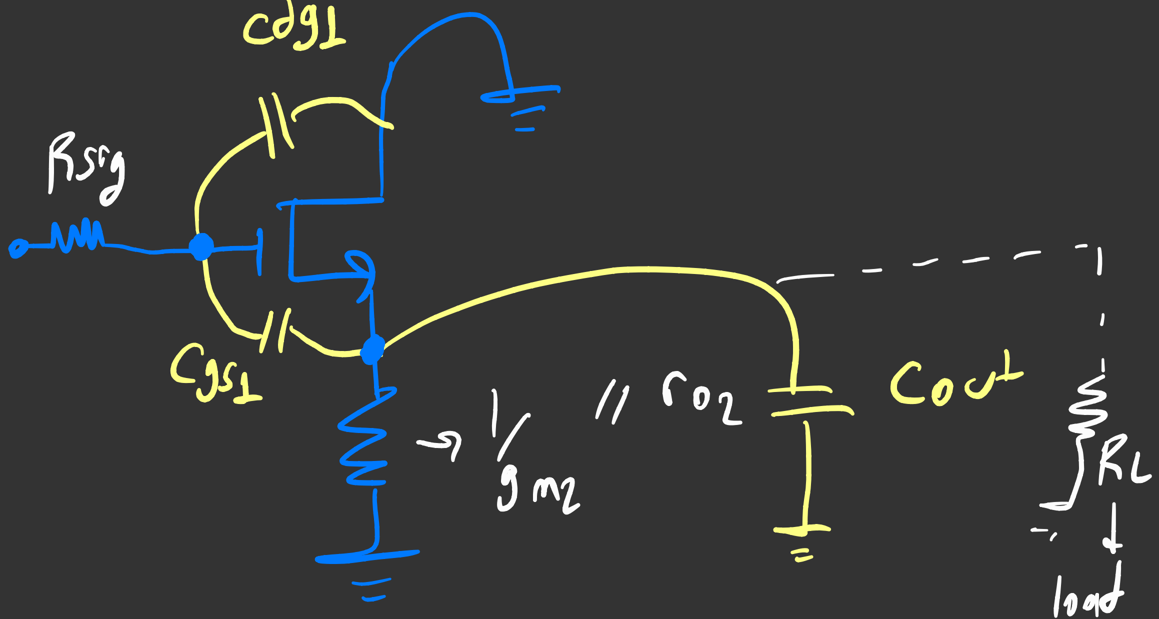
Homework-3 Solutions

1) Let's simplify the circuit and insert parasitic capacitances.



$$C_{out} = C_{sb1} + C_{gs2} + C_{db2}$$

* The rest of the parasitics are short. Due to AC ground.
(For ex. C_{db1} → drain at ground, bulk at ground)

• we need to calculate 3 different time constant.

For Cdg1

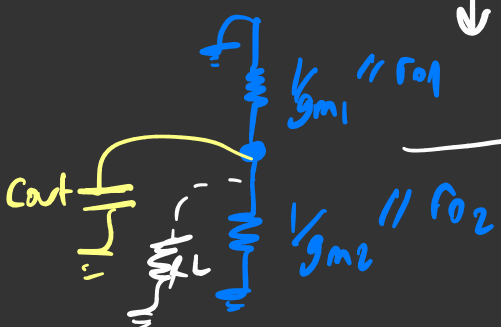
→ It is obvious. Cdg1 sees Rsig as the equivalent resistor

$$\boxed{\tau_1 = R_{sig} C_{gd1}}$$

For Cout

→ It is also easy. Cout sees total output resistance

↓

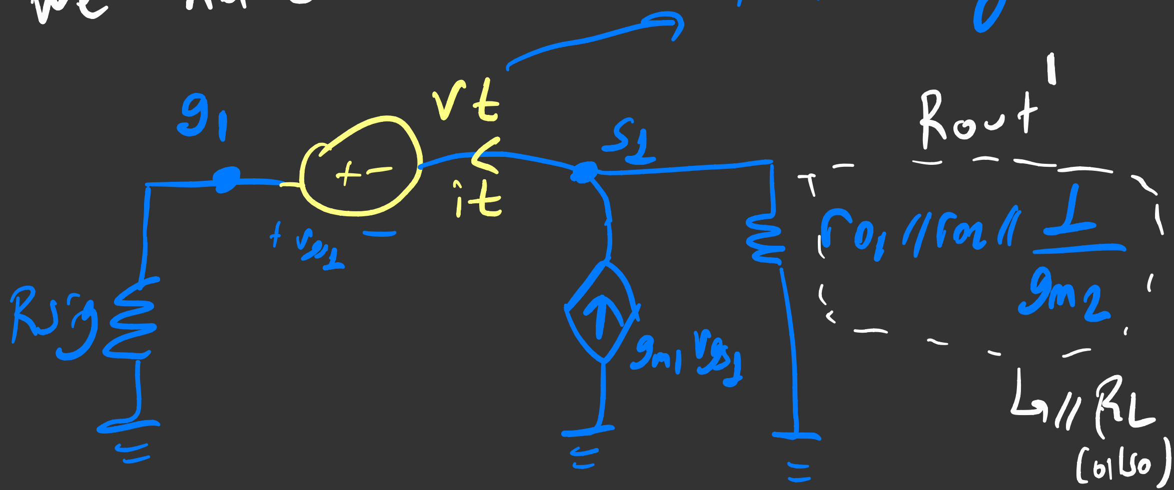


$$\boxed{\tau_2 = R_{out} C_{out}}$$

where

$$R_{out} = \frac{1}{g_{m1}} \parallel \frac{1}{g_{m2}} \parallel r_{o1} \parallel r_{o2} \parallel R_L$$

* C_{gs1} is the tricky part.
Remember in Hw-2 we neglected it as we assumed $R_{sig} = 0$, but in this case we have R_{sig}.



* Be careful while you are modelling. The transistor always converts v_{gs} to $g_m v_{gs}$ (voltage-current conversion).

we need KVL in here, but we are gonna discuss the results.

$$v_t = i_t R_{sig} + (i_t - g_{m1} v_{gs1}) R_{out}'$$

$$v_{gs1} = v_t$$

we have

$$R_{gs} = \frac{v_t}{i_t} = \frac{R_{sig} + R_{out}'}{1 + g_{m1} R_{out}'}$$

$$\boxed{\tau_3 = C_{gs1} \frac{R_{sig} + R_{out}'}{1 + g_{m1} R_{out}'}}$$

$$\boxed{f_{3dB} = \frac{1}{2\pi(\tau_1 + \tau_2 + \tau_3)}}$$

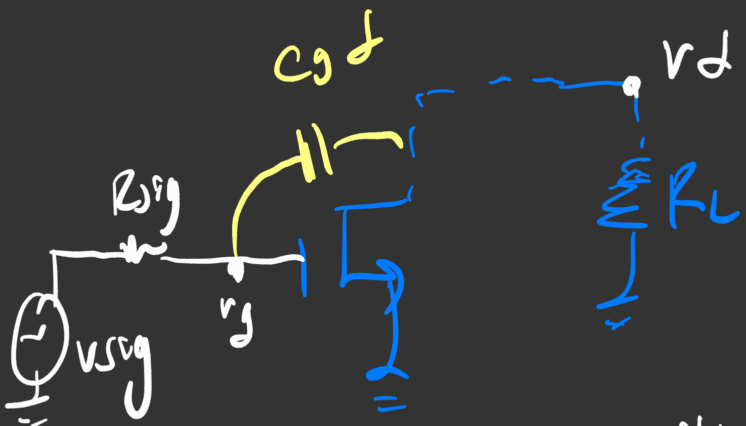
A discussion on the effect of C_{gs} to 3 dB frequency

(you can skip this part)

To understand the effect of C_{gs} in the source follower, we also need to understand the effect of Miller capacitance C_{gd} in common-source amplifiers.

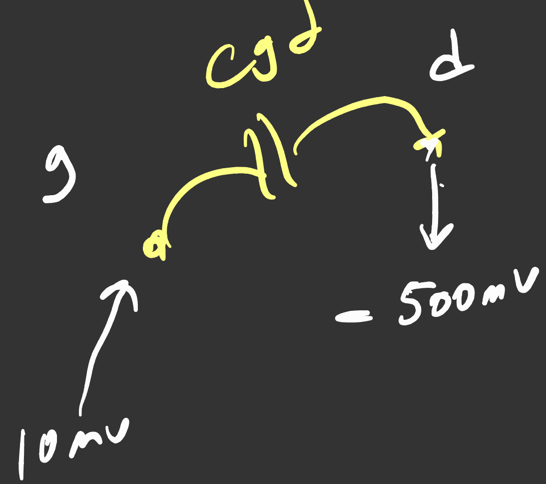
(P.S. → you can jump to page 26, this is extra)

So first of all think about Miller Effect. It will be an intuitive analysis that you cannot find in the textbooks.



- why we are multiplying cgd with the gain $\frac{vd}{vg}$?

- what are we charging at the input? (Beside cgs)



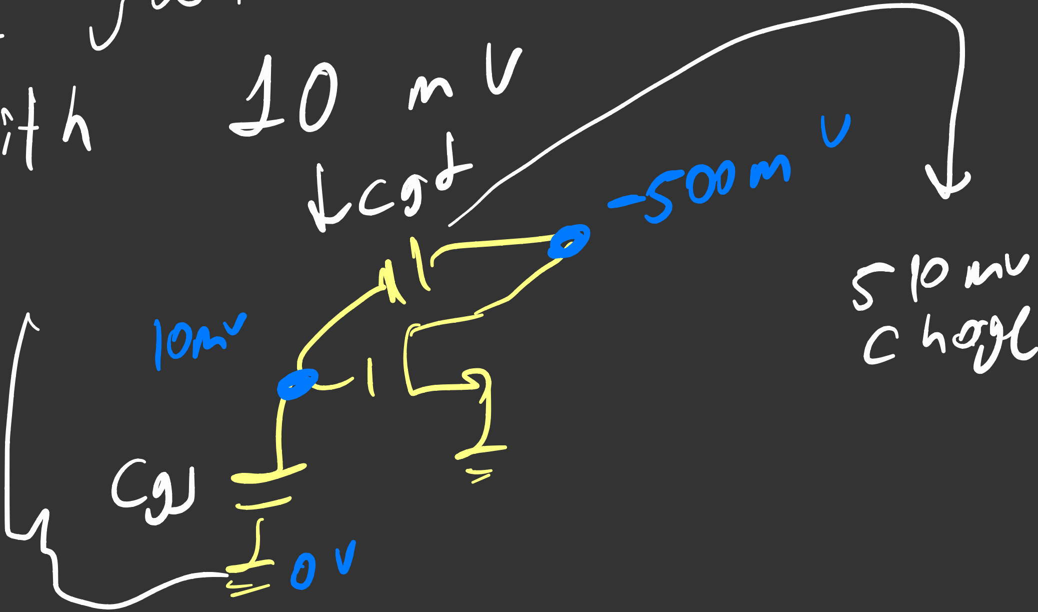
Assume our gain $\frac{V_d}{V_g} = -50 \frac{V}{V}$

Apply 10 mV input. Drain voltage → -500mV

The results

- we need to charge Cgd with $10\,mV - (-500\,mV) = 510\,mV$
- So we need more time, because instead of just 10mV we are charging Cgd with 510mV!

- On the other hand, for C_{gs} we just have to charge with 10 mV

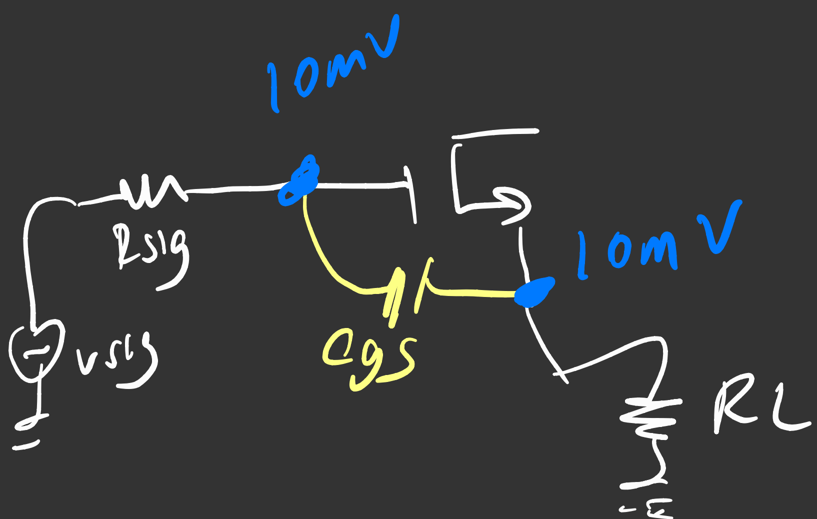


10mV charge

- This is why we are multiplying the C_{gd} with the gain. It is basically a capacitance multiplier.

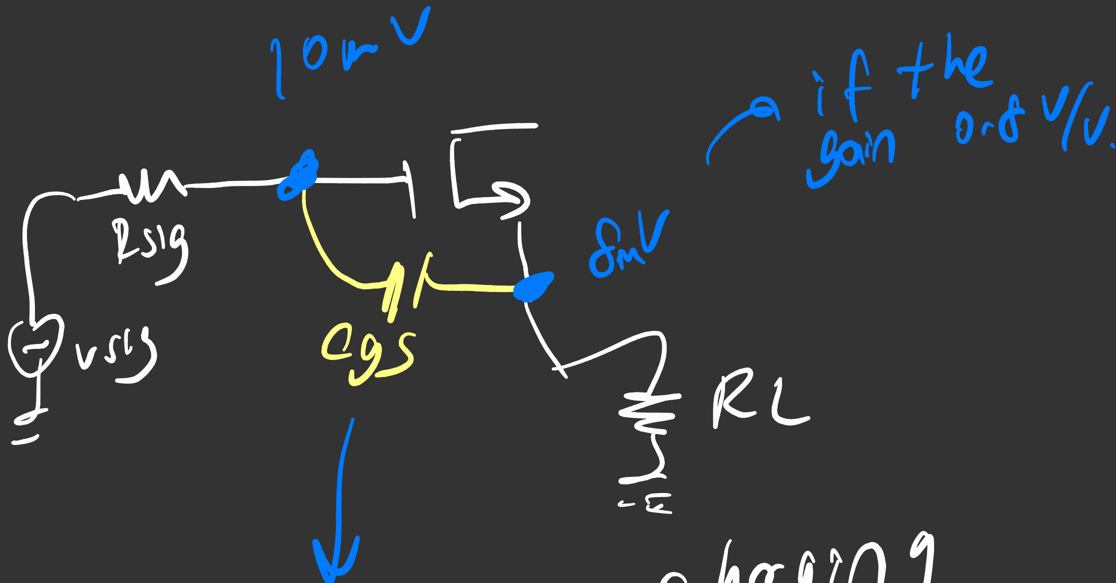
So what about Cgs for Source followers?

Apply small signal.



- what is the gain of Source followers? 1V/V
- So if we are talking about charging, we are not even charging Cgs in this case. ↓

- But, we know that, generally gain is 0.7, 0.8 V/V instead of 1 V/V due to non-idealities.



Still we are charging Cgs with 2mV instead of 10mV → Effective Cgs,

$$= Cgs/5$$

* It is like reverse miller effect!

Now, let's think about τ_3 in the question.

$$\tau_3 = C_{gs1} \frac{R_{sig} + R_{out}'}{1 + g_{m1} R_{out}'}$$

where $R_{out}' = \frac{1}{g_{m2}} \parallel r_{o1} \parallel r_{o2} \parallel R_L$

Assume $r_{o1}, r_{o2} \gg g_m$ and R_L (It should be in a good design)

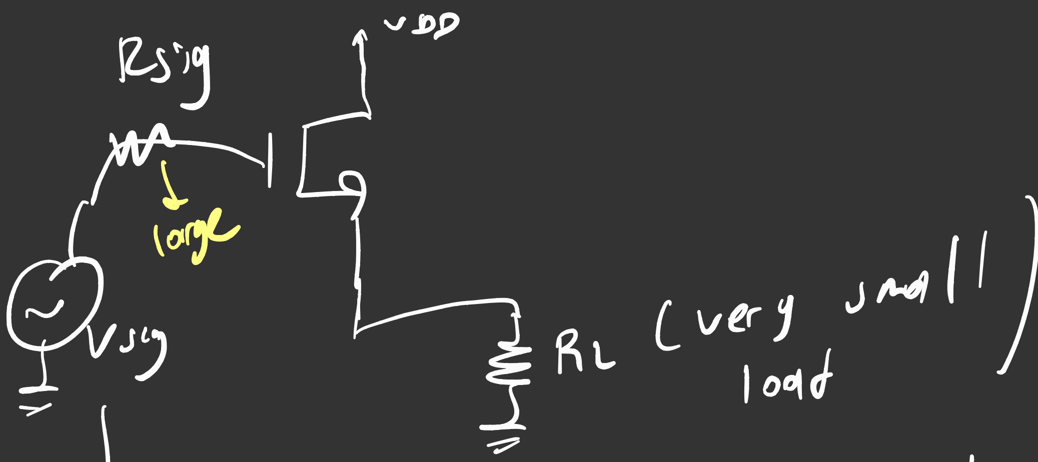
$$\tau_3 \cong C_{gs1} \frac{R_{sig} + \left(\frac{1}{g_{m2}} \parallel R_L\right)}{g_{m1}\left(\frac{1}{g_{m2}} \parallel R_L\right)}$$

$\downarrow$

→ why do we use source follower?

- voltage Buffer

↳ we need to drive very small resistance such as speaker (coil) in audio amplifiers.



Normally it comes from another stage.

In a good buffer

$$R_L \ll \frac{1}{g_m}$$

So let's recall τ_3 again.

$$\tau_3 \cong C_{gs1} \frac{R_{sig} + \left(\frac{1}{g_{m2}} // R_L\right)}{g_{m1}\left(\frac{1}{g_{m2}} // R_L\right)}$$

rearrange

$$R_{sig} >> \frac{1}{g_{m2}} >> R_L$$

$$\tau_3 \cong \frac{C_{gs1} R_{sig}}{g_{m1} R_L}$$

obvious part

division factor

↳ should be large in a good buffer!

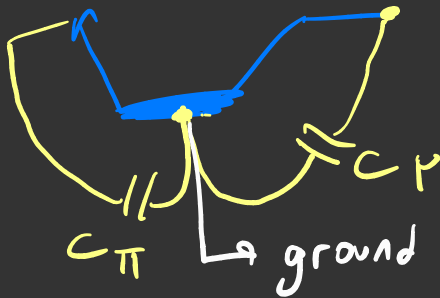
Conclusions

- For C_3 and C_{gs1} we have a reverse Miller effect, effective C_{gs}

$$C_{gs1,eff} = \frac{C_{gs1}}{g_{m1} R_L}$$

- In a good buffer design effect of C_{gs1} on 3dB bandwith would be negligible!

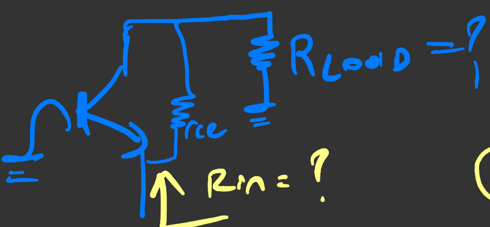
2) For this common-base configuration, we have parasitics



So, we have 2 time constant

$$\tau_1 = (R_{in} // R_E // R_I)\, C_\pi$$

what is R_{in} for common-base configuration



$R_{LOAD} = R_C // R_3$

so

$$R_{in} \simeq \frac{1}{g_m} + \frac{R_C // R_3}{g_m r_o}$$

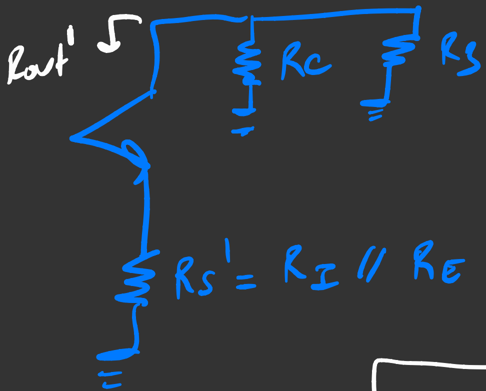
I assumed $\frac{R_L}{\beta} << r_o$ $\quad (r_o = r_{ce})$

$$\tau_2 = R_{out} C_P$$

what is R_{out}?

$$R_{out} = R_C \,//\, R_3 \,//\, R_{out}'$$

$$R_{out}' \cong g_m r_o \left(R_s' \,//\, \beta/g_m\right)$$



so

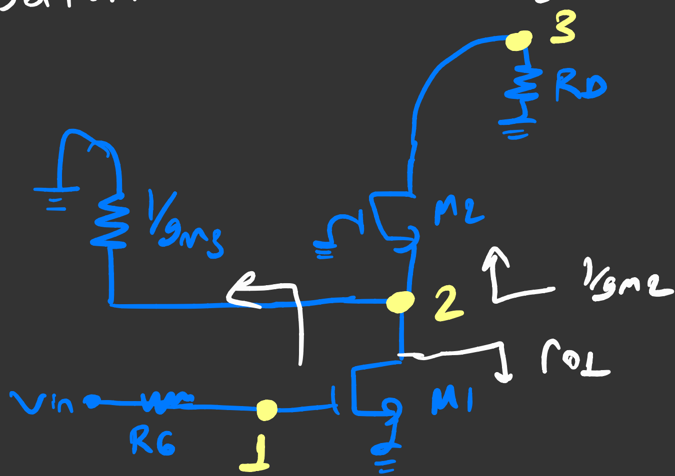
$$f_{3dB} = \frac{1}{2\pi(\tau_1 + \tau_2)}$$

* The important point is to find R_{in} and R_{out} in this question. In general you will see that

$R_{in} \cong 1/g_m$ $\quad R_{out} \cong R_C \,//\, R_3$

since other terms are negligible

3) We have 3 nodes in the signal path. Let's simplify the circuit.



$g_{m2} r_{o2} \ll 1$

The parasitic capacitances at node-1

$$C_1 = C_{gs1} + C_{gd1}\frac{V_2}{V_1} , \quad R_1 = R_G$$

$$\frac{V_2}{V_1} = g_{m1}\left(\frac{1}{g_{m2}} \parallel r_{o1} \parallel \frac{1}{g_{m3}}\right) \cong \frac{g_{m1}}{g_{m2}+g_{m3}}$$

So

$$\tau_1 = R_G\left(C_{gs1} + C_{gd}\frac{g_{m1}}{g_{m2}+g_{m3}}\right)$$

• I also assumed $\frac{1}{g_{m3}} \ll r_{o3}$

The parasitic capacitances at node-2

$$C_2 = C_{gd1} + C_{db1} + C_{gs3} + C_{sb2} + C_{gs2} + C_{sb2}$$

$$R_2 = 1/g_{m2} \,//\, r_{o1} \,//\, \frac{1}{g_{m3}} = \frac{1}{g_{m2}} \,//\, \frac{1}{g_{m3}}$$

$$\boxed{\tau_2 = \frac{1}{g_{m2}+g_{m3}} C_2}$$

The parasitic capacitances at node-3

$$C_3 = C_{gd2} + C_{db2}$$

$$R_3 = g_{m2} r_{o2} \left(\frac{1}{g_{m3}} \,//\, r_{o3} \,//\, r_{o1} \right)$$

↳ dominant

$$// \; R_D$$

$$R_3 \simeq g_{m2} r_{o2} \frac{1}{g_{m3}} \parallel R_D$$

$$\tau_3 = \left(\frac{g_{m2}}{g_{m3}} r_{o2} \parallel R_D\right)(C_{gd2} + C_{dB2})$$

Discussion about the circuit

(you can skip this part)

→ What is the gain of this circuit?

Let's assume $g_{m2} \gg g_{m3}$

Gain will be $g_{m1} R_D$

- Same as common source.

Why do we use cascode?

Recall τ_1

$$\tau_1 = R_G\left(C_{gs1} + C_{gd1}\frac{g_{m1}}{g_{m2}+g_{ms}}\right)$$

$$\tau_1 \simeq R_G\left(C_{gs1} + C_{gd1}\frac{g_{m1}}{g_{m2}}\right)$$

Assume $g_{m1} \simeq g_{m2}$

$$\tau_1 \simeq R_G\left(C_{gs1} + C_{gd1}\right)$$

No Miller Effect

τ_1 decreases

↳ better frequency response !!

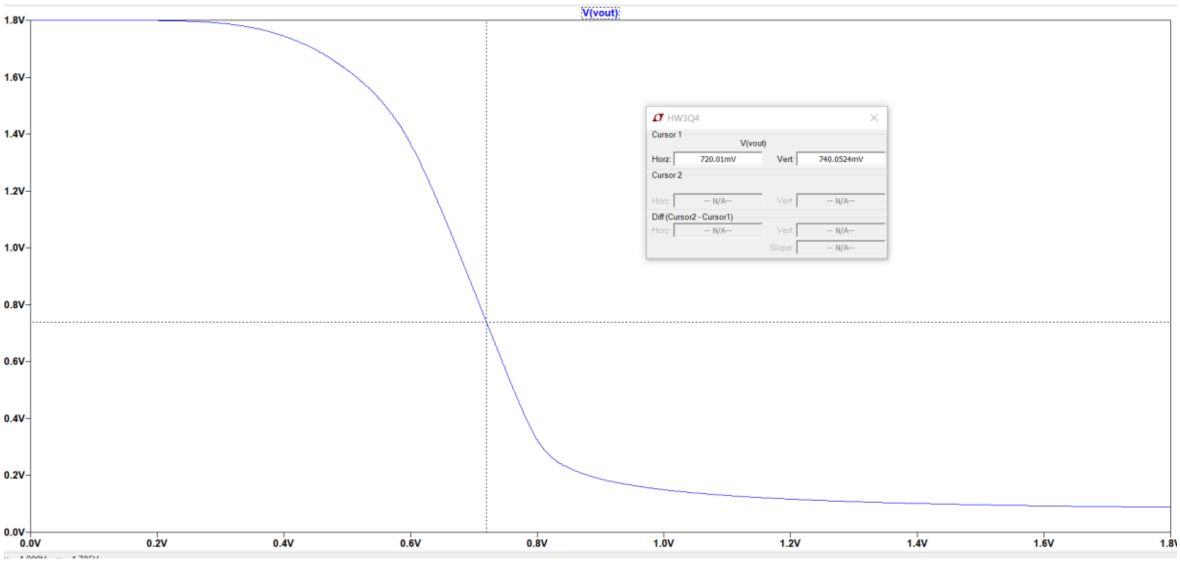
Q We use cascode structures for high frequency design, as it eliminates Miller Effect for RF Amps.

Q What are we trading off for this?

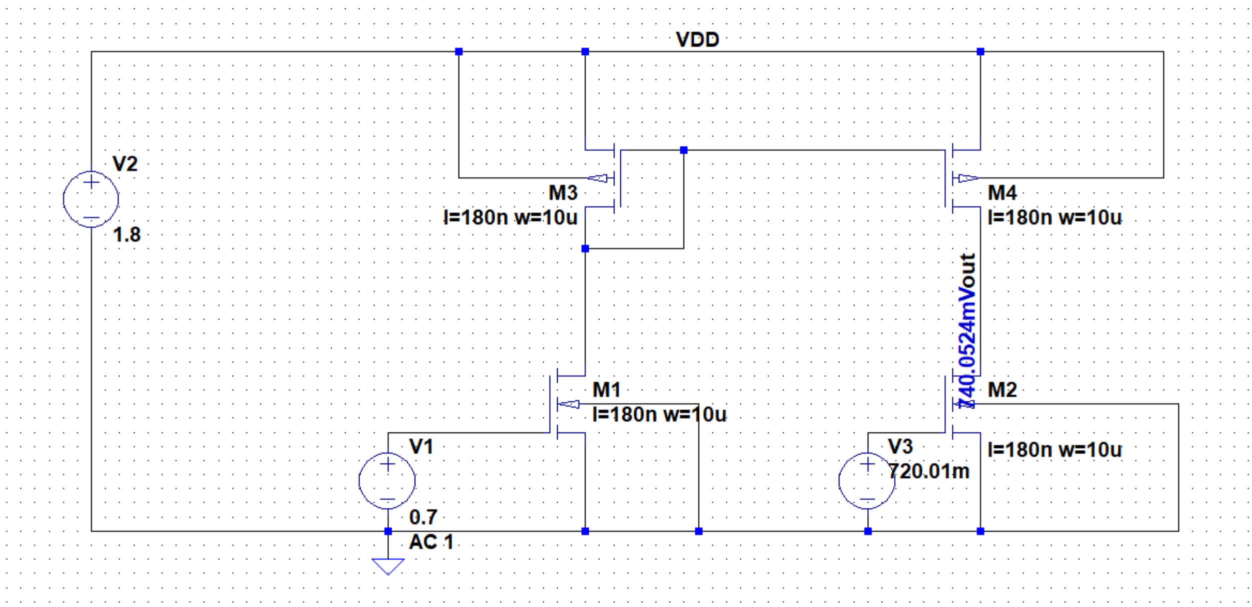
→ Extra transistor means that output voltage swing decreases. We can lower Vout to $V_{DS1on} + V_{DS2on}$

In common source it would be $V_{DS1on} \rightarrow (V_{GS1} - V_{TH})$

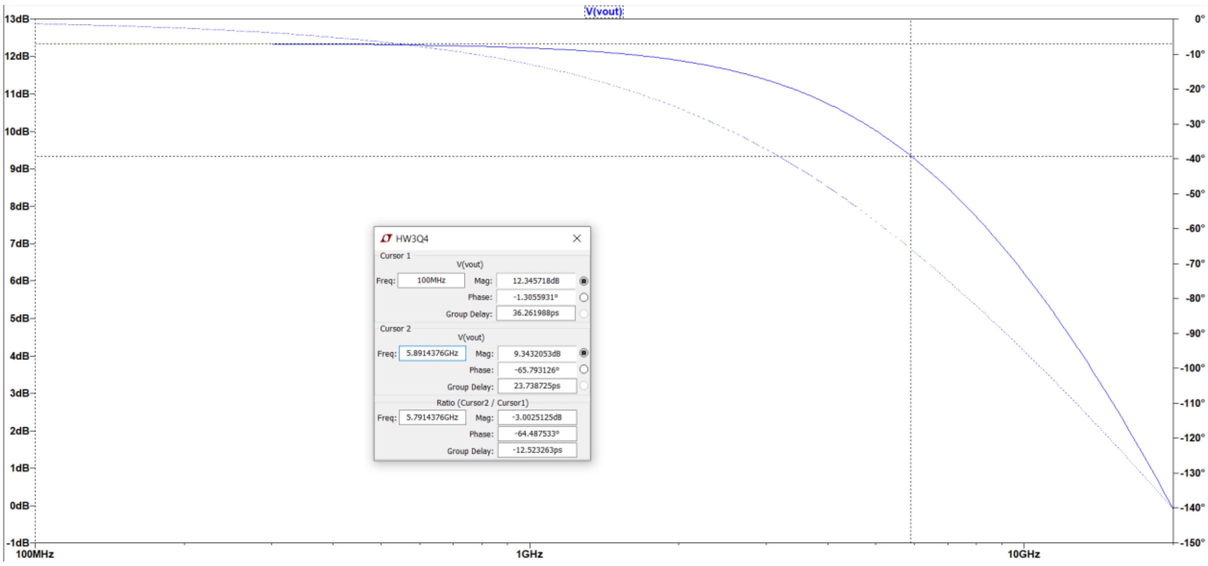
4) In the first part, we need to bias the circuit such that V_{OUT}=0.74V @ DC. Thus, we sweep the gate of M_{13}, with a DC voltage source to obtain this value.



The DC bias voltage value of V_{G13}=720.01 mV. After applying this bias voltage the DC operating point of the output can be seen below.



You can see the frequency response of the amplifier on the next page. The low frequency gain is equal to 12.34 dB and the 3 dB frequency is equal to 5.9 GHz. You can observe that the phase shift is equal to 65 degree. Normally, we would expect 45 degree for a single dominant pole but it is not the case for this amplifier.



Possible Mistakes

- Importing wrong models.
- Forgetting to enter the transistor geometry.
- Wrong DC biasing.
- Connecting bulk connections to the wrong nodes (It should be VDD for PMOS, ground for NMOS).
- Forgetting to apply AC signal from the input.
- Forgetting to apply power supply.

Notes

- For MOS the terminals drain and source do not matter. Remember that MOSFET is a symmetrical device.
- Transistor width and length are the design parameters for MOSFET. You should not include it to the model. It should be the designer's choice.
- The biasing method in the question is not a good choice. Biasing with the voltage sources are called as bad design. You are going to learn biasing with current sources in more advanced classes. It is always problem to bias single ended input circuits without using coupling capacitors.