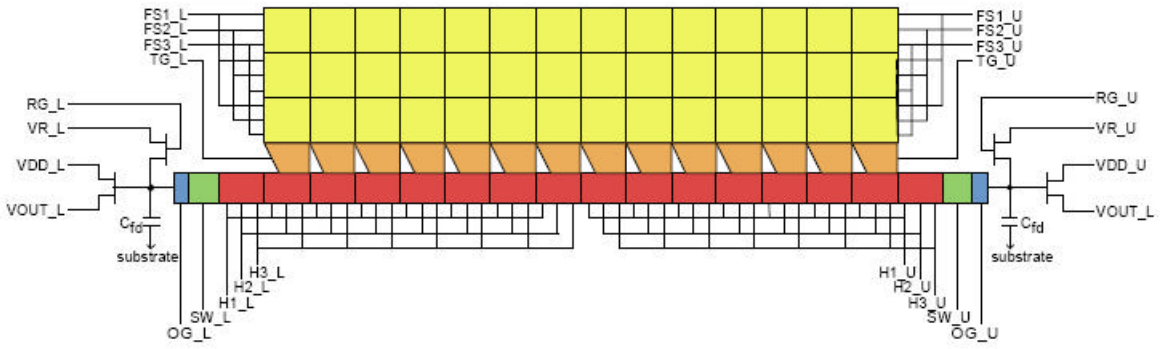

Figure 1. Segment of CCD showing the parallel register pixels (yellow), transfer gate (orange), the serial register pixels (red), summing well clock (green), sense capacitor with reset transistor and its gate clock, and the source follower output transistor.

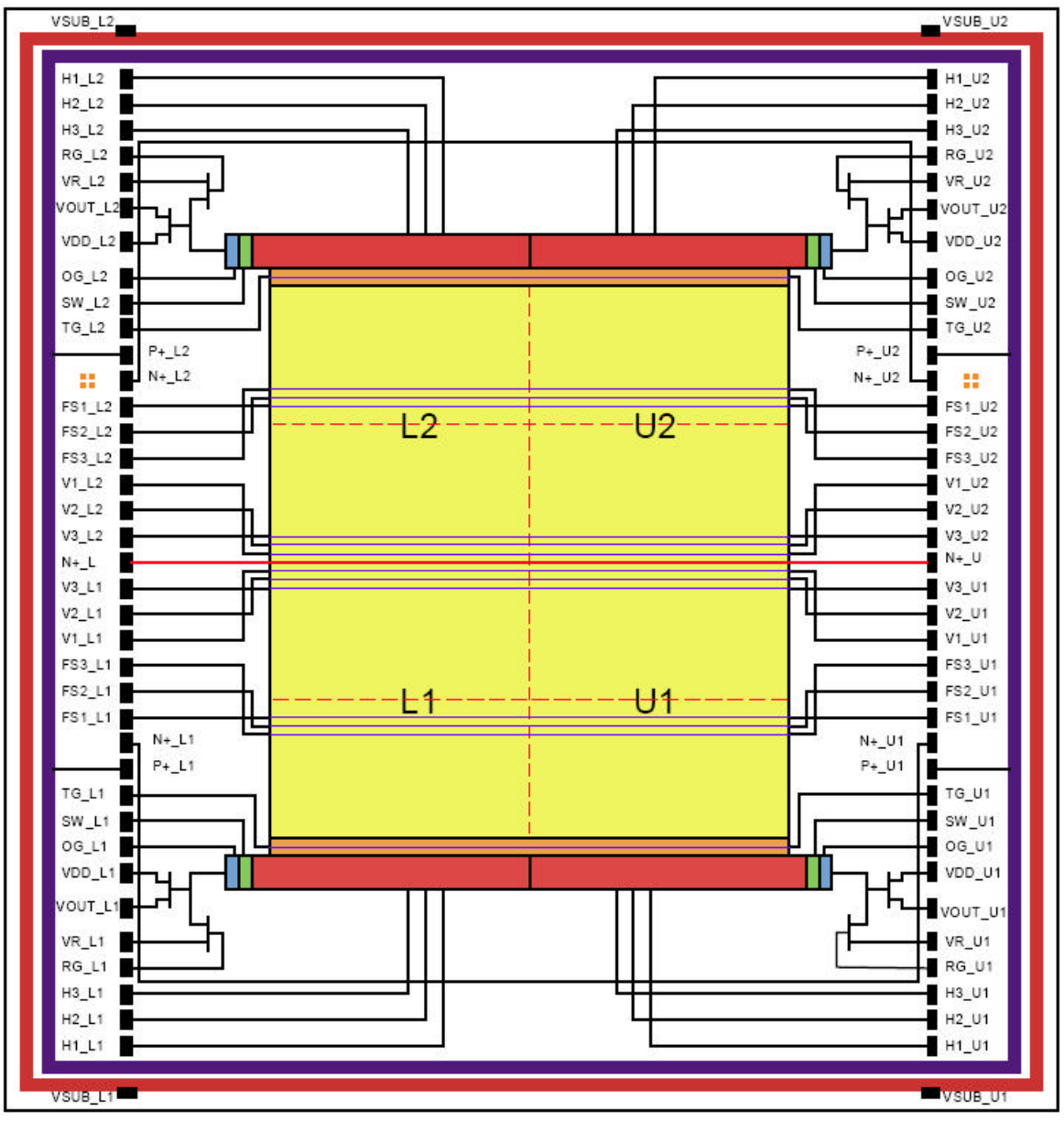

Table 1. SNAP imager CCD operating voltages and AC parameters.

Signal	# of copies	Type	Exposure VL	Exposure VH	Readout VL	Readout VH	Erase VL	Erase VH	Purge VL	Purge VH	Adj. Range VL	Adj. Range VH	t width (µsec)	Cap (pF)	I	max noise (uV)	worst freq (kHz)	max 20MHz noise (mV)
V1	2	ck	-3	5	-3	5	9	9	-9	-9	-5	15	50	30000		70	400	12
V2	2	ck	-3	5	-3	5	9	9	-9	-9	-5	15	50	30000		70	400	12
V3	2	ck	-3	5	-3	5	9	9	-9	-9	-5	15	50	30000		70	400	12
FS1	2	ck	-3	5	-3	5	9	9	-9	-9	-5	15	50	30000		70	400	9.5
FS2	2	ck	-3	5	-3	5	9	9	-9	-9	-5	15	50	30000		70	400	9.5
FS3	2	ck	-3	5	-3	5	9	9	-9	-9	-5	15	50	30000		70	400	9.5
TG	2	ck	-3	5	-3	5	-4	6	-4	6	-5	10	50	30		80	700	11
H1	4	ck	-4	6	-4	6	-4	6	-4	6	-5	10	0.5	50		200	100	13
H2	4	ck	-4	6	-4	6	-4	6	-4	6	-5	10	0.5	50		200	100	13
H3	4	ck	-4	6	-4	6	-4	6	-4	6	-5	10	0.5	50		200	100	13
SW	4	ck	-5	5	-5	5	-5	5	-5	5	-8	8	0.5	small		250	100	6.2
RG	4	ck	-6	0	-6	0	-6	0	-6	-6	-8	0	0.15	small		45	100	1.5
OG	4	dc	2.2		2.2		2.2		2.2		0	5				37	150	1.5
VR	4	dc	-12.5		-12.5		-12.5		-12.5		-15	0				420	150	1.5
VDD	4	dc	-22		-22		-22		-22		-25	0			<1 mA	12	150	2.4
VOUT	4	ac																
VSUB	1	dc	+80		+80		0		0		0	100			<1 µA	50	150	2.6
N+	3	float																
P+	1	dc	0		0		0		0		0							