BN54L-C15

MN54L-C15 evaluation Board

Datasheet Version 1.2

BLE Solution: Nordic NRF54L15

RF IC	Crystal	Chip antenna
Nordic NRF54L15/ Reversion 2	32MHz/20ppm Embedded	Embedded

Overview and Benefits

Overview

The MN54L-C15 from Aradconn is a highly flexible, ultra-low power, Bluetooth Low Energy module based on the nRF54L15 SoC from Nordic Semiconductor. With an Arm® Cortex®-M33 with FPU 32-bit processor, embedded 2.4GHz transceiver, and integrated chip antenna. Providing full use of the nRF54L15's capabilities and peripherals, which include I2C, SPI,QSPI, UART, I2S, ADC, GPIO, PWM, and NFC interfaces.

Benefits

- **Bluetooth qualification and Regulatory certification reduce the burden to enter the market.**
- **Complete RF solution with no additional RF design, allowing faster time to launch a new product, and providing long working distance.**

BN54L-C: Full test report please refer to Aradconn official website.

Test condition (Open space)	iPhone (0dBm)	NRF52840 Central (+8dBm)
1Mbps(BLE)	660m	1145m
125Kbps(BLE)	NA	2618m

- **Compact size:** (L) 60 x (W) 39mm

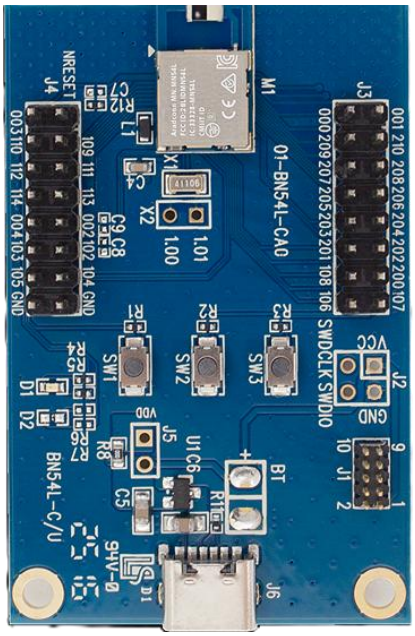
- **Provides flexibility in the OEM's application development choice with full support for using Nordic SDK and firmware tools.**

Contents

1. Packing information

A 2x5 /1.27mm debug cable for BN54L-C15 debugging

A BN54L-C15 board



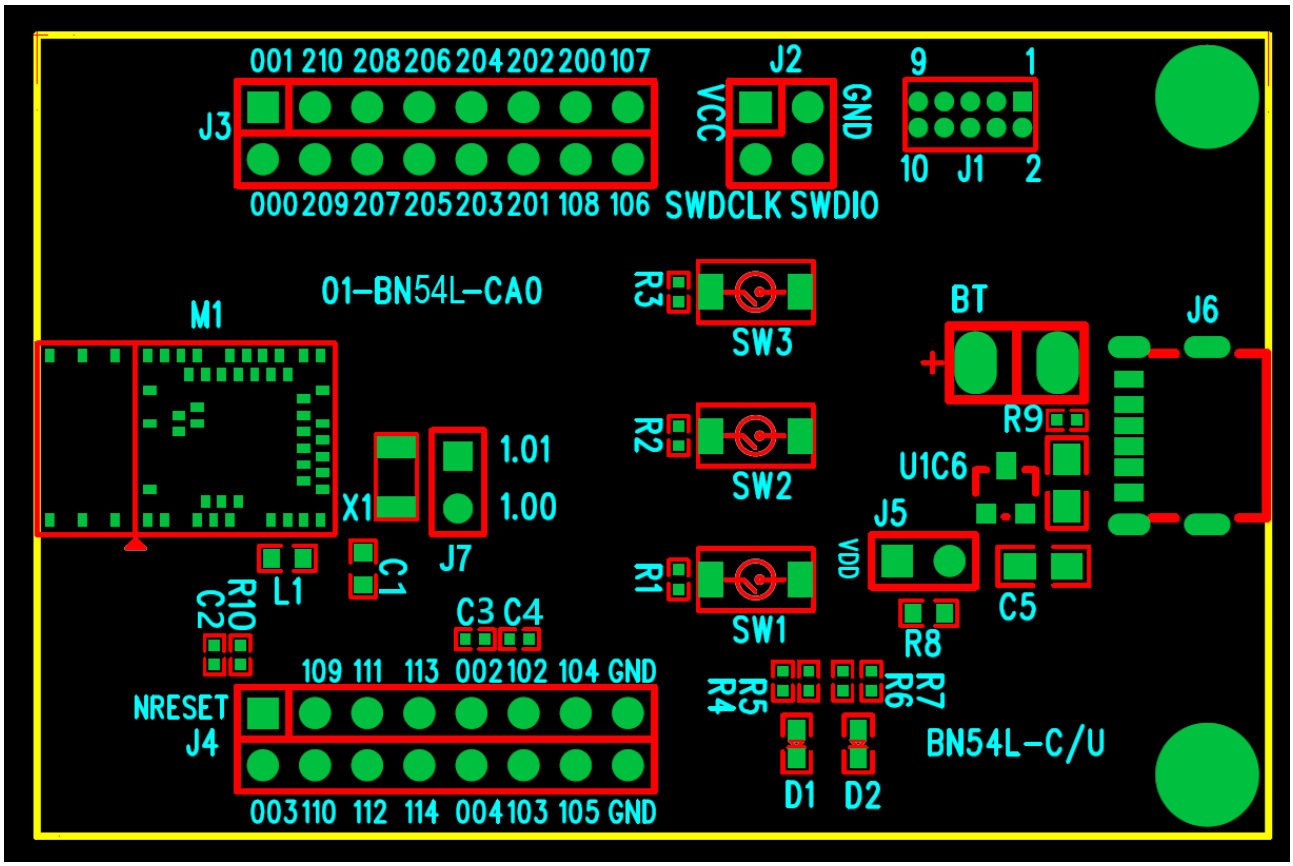
AN OUTER BOX (THE PART NUMBER WILL ALIGN WITH THE ACTUAL PRODUCT)

2. BN54L-C15 evaluation board

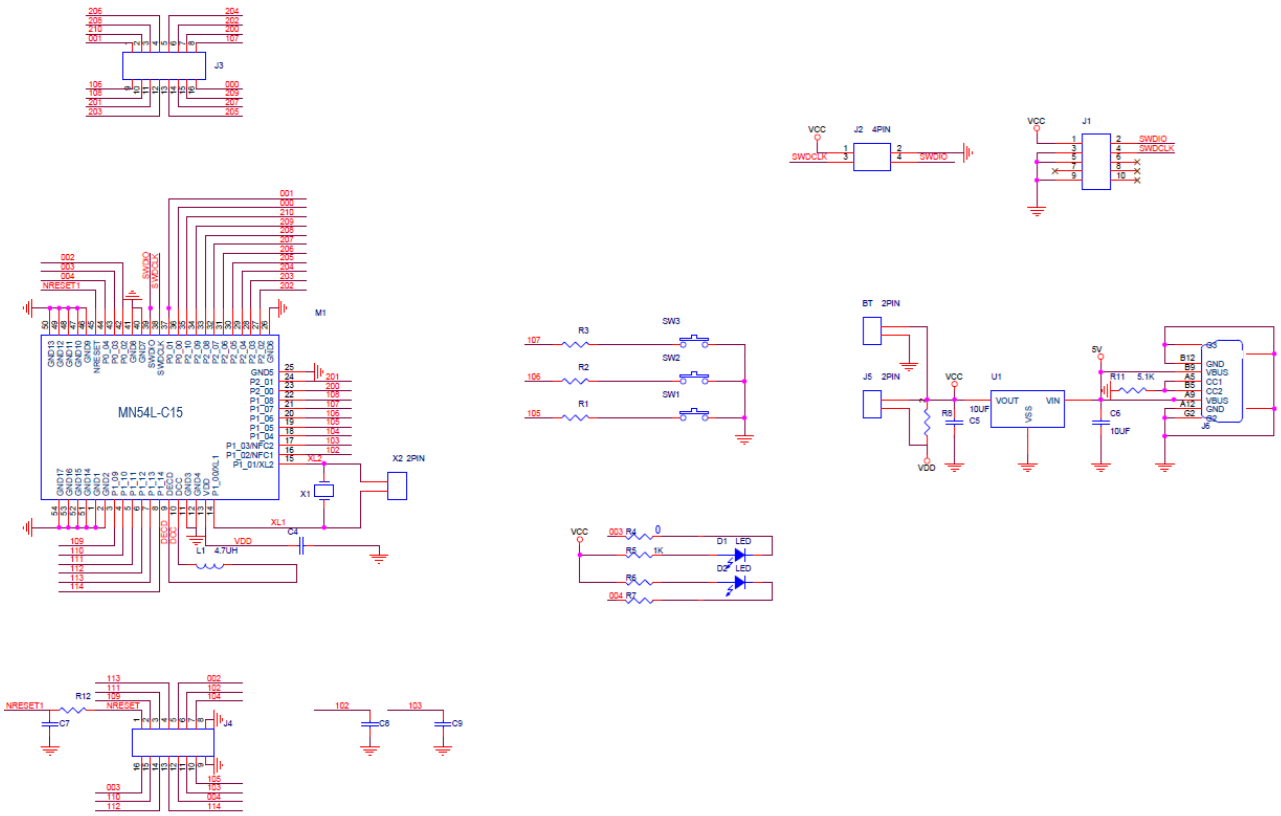
2.1 BN54L-C15 component placement

BN54L-C15 is a full-featured evaluation board for MN54L-C15 that supports:

M1:MN54L-C15 module
J6: Power over Type C-USB
J3/J4: Complete I/O pinout to headers
J1: On-board programming and debugging interface
X1:32.768 kHz crystal
D1: One user LED
SW1/SW2/SW3: Three user buttons
U1 : 3.3V LDO
J5 : A jumper uses for measuring current consumption (must remove R8 first)



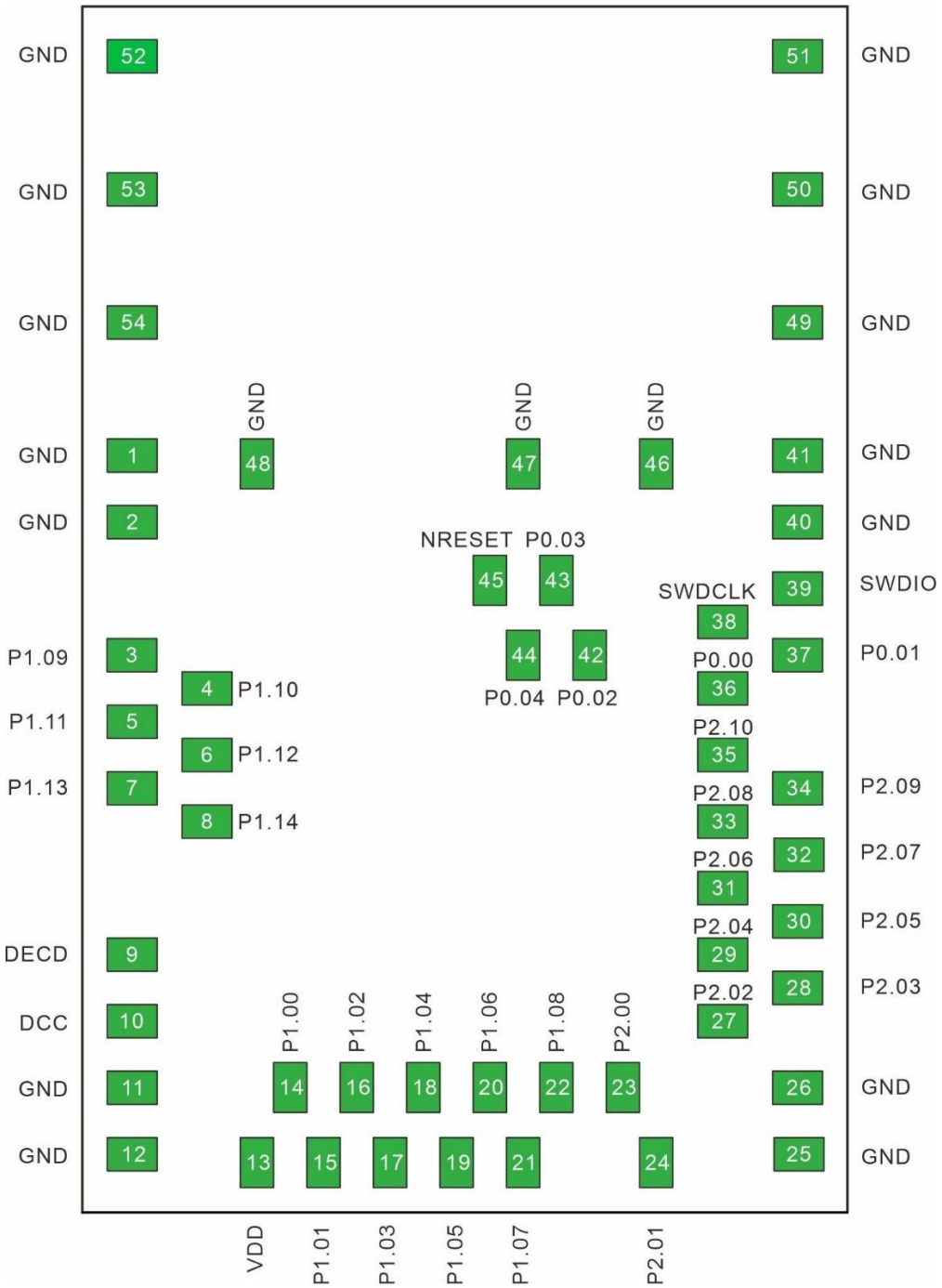
2.2 BN54L-C15 schematic



REMARK:

- **When using DC-DC mode, please add L1.**
- **When using internal 32.768kHz RC oscillator, please remove X1 and calibration performed at least every 8 seconds.**
- **NRESET pin radiated emissions are higher than expected .**
  Add a C7(3.9pF) direct connect to GND close to the module.
  Add a 1K Ω series resistance directly after the tracks close to the module.
  Keep PCB tracks as short as possible and in between ground layers if possible.
- **P1.09 radiated emissions are higher than expected.**
  It is recommended to leave P1.09 unused and unconnected.
  If P1.09 are used add a 330 Ω or larger series resistance directly after the tracks close to the module.
  Keep PCB tracks as short as possible and in between ground layers if possible.

2.3 MN54L-C15 PIN Assignment



Pin No.	Name	Pin function	Description
(1)	GND	Ground	The pad must be connected to a solid ground plane
(2)	GND	Ground	The pad must be connected to a solid ground plane
(3)	P1.09	Digital I/O	General-purpose I/O
	Radio 0	Digital I/O	DFEGPIO : Direction Finding Antenna select GPIO
(4)	P1.10	Digital I/O	General-purpose I/O
	Radio 1	Digital I/O	DFEGPIO : Direction Finding Antenna select GPIO
(5)	P1.11	Digital I/O	General-purpose I/O
	Radio 2	Digital I/O	DFEGPIO : Direction Finding Antenna select GPIO
	AIN4	Analog input	Analog input
		Clock pin	Can be set as TWI
(6)	P1.12	Digital I/O	General-purpose I/O
	Radio 3	Digital I/O	DFEGPIO : Direction Finding Antenna select GPIO
	AIN5	Analog input	Analog input
		Clock PIN	Can be set as TWI
(7)	P1.13	Digital I/O	General-purpose I/O
	Radio 4	Digital I/O	DFEGPIO : Direction Finding Antenna select GPIO
	AIN6	Analog input	Analog input
(8)	P1.14	Digital I/O	General-purpose I/O
	Radio 5	Digital I/O	DFEGPIO : Direction Finding Antenna select GPIO
	AIN7	Analog input	Analog input
(9)	DECD	Power	0.9 V regulator supply decoupling
(10)	DCC	Power	DC/DC regulator output
(11)	GND	Ground	The pad must be connected to a solid ground plane
(12)	GND	Ground	The pad must be connected to a solid ground plane
(13)	VDD	Power	Power supply
(14)	P1.00	Digital I/O	General-purpose I/O
	XL1	Analog input	Connection to 32.768kHz crystal (LFXO)
(15)	P1.01	Digital I/O	General-purpose I/O
	XL2	Analog input	Connection to 32.768kHz crystal (LFXO)
(16)	P1.02	Digital I/O	General-purpose I/O
	NFC1	NFC input	NFC antenna connection
(17)	P1.03	Digital I/O	General-purpose I/O
	NFC2	NFC input	NFC antenna connection
		Clock pin	Can be set as TWI when NFC is unused
(18)	P1.04	Digital I/O	General-purpose I/O
	AIN0	Analog input	Analog input
		Clock PIN	Can be set as TWI when NFC is unused
(19)	P1.05	Digital I/O	General-purpose I/O
	Radio 6	Digital I/O	DFEGPIO : Direction Finding Antenna select GPIO
	AIN1	Analog input	Analog input
(20)	P1.06	Digital I/O	General-purpose I/O
	AIN2	Analog input	Analog input
(21)	P1.07	Digital I/O	General-purpose I/O
	AIN3	Analog input	Analog input

Pin No.	Name	Pin function	Description
(22)	P1.08	Digital I/O	General-purpose I/O
	CLK16M	Clock PIN	GRTC HF clock output
	EXTREF	Analog input	External reference for SAADC
(23)	P2.00	Digital I/O	General-purpose I/O
		Digital I/O	SPIM DCX
		Digital I/O	UARTE RXD
		Digital I/O	QSPI D3
(24)	P2.01	Digital I/O	General-purpose I/O
		Clock PIN	SPIM SCK
		Clock PIN	SPIS SCK
		Clock PIN	QSPI SCK
(25)	GND	Ground	The pad must be connected to a solid ground plane
(26)	GND	Ground	The pad must be connected to a solid ground plane
(27)	P2.02	Digital I/O	General-purpose I/O
		Digital I/O	SPIM SDO
		Digital I/O	SPIS SDO
		Digital I/O	UARTE TXD
		Digital I/O	QSPI D0
(28)	P2.03	Digital I/O	General-purpose I/O
		Digital I/O	QSPI D2
(29)	P2.04	Digital I/O	General-purpose I/O
		Digital I/O	SPIM SDI
		Digital I/O	SPIS SDI
		Digital I/O	UARTE CTS
		Digital I/O	QSPI D1
(30)	P2.05	Digital I/O	General-purpose I/O
		Digital I/O	SPIM CS
		Digital I/O	UARTE RTS
		Digital I/O	QSPI CS
(31)	P2.06	Digital I/O	General-purpose I/O
		Clock PIN	SPIM SCK
		Clock PIN	SPIS SCK
(32)	P2.07	Digital I/O	General-purpose I/O
		Digital I/O	SPIM DCX
		Digital I/O	UART RXD
(33)	P2.08	Digital I/O	General-purpose I/O
		Digital I/O	SPIM SDO
		Digital I/O	SPIS SDO
		Digital I/O	UARTE TXD
(34)	P2.09	Digital I/O	General-purpose I/O
		Digital I/O	SPIM SDI
		Digital I/O	SPIS SDI
		Digital I/O	UART CTS

Pin No.	Name	Pin function	Description
(35)	P2.10	Digital I/O	General-purpose I/O
		Digital I/O	SPIM CS
		Digital I/O	UARTE RTS
(36)	P0.00	Digital I/O	General-purpose I/O
(37)	P0.01	Digital I/O	General-purpose I/O
(38)	SWDCLK	Debug	Serial wire clock. Input with onchip pull-up.
(39)	SWDIO	Debug	Serial wire data. Bidirectional with standard-drive and on-chip pull-down.
(40)	GND	Ground	The pad must be connected to a solid ground plane
(41)	GND	Ground	The pad must be connected to a solid ground plane
(42)	P0.02	Digital I/O	General-purpose I/O
(43)	P0.03	Digital I/O	General-purpose I/O
	GRTCPWM	Clock PIN	GRTC PWM output
(44)	P0.04	Digital I/O	General-purpose I/O
	GRTCLFCLKOUT	Clock PIN	GRTC LF clock output
(45)	nRESET	Reset	Pin reset with on-chip pull-up
(46)	GND	Ground	The pad must be connected to a solid ground plane
(47)	GND	Ground	The pad must be connected to a solid ground plane
(48)	GND	Ground	The pad must be connected to a solid ground plane
(49)	GND	Ground	The pad must be connected to a solid ground plane
(50)	GND	Ground	The pad must be connected to a solid ground plane
(51)	GND	Ground	The pad must be connected to a solid ground plane
(52)	GND	Ground	The pad must be connected to a solid ground plane
(53)	GND	Ground	The pad must be connected to a solid ground plane
(54)	GND	Ground	The pad must be connected to a solid ground plane

2.4 GPIO Recommended usage

Module PIN N0.	NRF54L15 GPIO	Recommended usage
QSPI		
23	P2.00	QSPI D3
24	P2.01	QSPI SCK
27	P2.02	QSPI D0
28	P2.03	QSPI D2
29	P2.04	QSPI D1
30	P2.05	QSPI CS
TWI	(Note: TWIM and TWIS must use clock pins for both SDA and SCL)	
5	P1.11	TWI
6	P1.12	TWI
17	P1.03	Can be set as TWI when NFC is unused
18	P1.04	Can be set as TWI when NFC is unused
43	P0.03	Can be set as TWI when PWM output is unused
44	P0.04	Can be set as TWI when LF Clock output is unused
UARTE 00/20		
23	P2.00	RXD
27	P2.02	TXD
29	P2.04	CTS
30	P2.05	RTS
UARTE 00/21		
32	P2.07	RXD
33	P2.08	TXD
34	P2.09	CTS
35	P2.10	RTS
SPI 00/20		
23	P2.00	SPIM DCX
24	P2.01	SPIM/SPIS SCK
27	P2.02	SPIM/SPIS SDO
29	P2.04	SPIM/SPIS SDI
30	P2.05	SPIM CS
SPI 00/21		
31	P2.06	SPIM/SPIS SCK
32	P2.07	SPIM DCX
33	P2.08	SPIM/SPIS SDO

34	P2.09	SPIM/SPIS SDI			
35	P2.10	SPIM CS			
NFC					
17	P1.02	NFC1			
18	P1.03	NFC2			
PWM					
	Port 1	PWM			
Clock Output					
22	P1.08	GRTC HF clock output(16MHZ)			
44	P0.04	GRTC LF clock output (32.768KHZ)			
Analog Input					
19	P1.05	AIN1			
20	P1.06	AIN2			
21	P1.07	AIN3			
22	P1.08	External reference for SAADC			
5	P1.11	AIN4			
6	P1.12	AIN5			
7	P1.13	AIN6			
8	P1.14	AIN7			
Radio (Direction Finding Antenna select GPIO)					
3	P1.09	Radio 0	P1.09 Radiated emissions are higher than expected. •It is recommended to leave P1.09 unused and unconnected. •If P1.09 are used add a 330 Ω or larger series resistance directly after the tracks close to the module. • Keep PCB tracks as short as possible and in between ground layers if possible.		
4	P1.10	Radio 1			
5	P1.11	Radio 2			
6	P1.12	Radio 3			
7	P1.13	Radio 4			
8	P1.14	Radio 5			
Port Special function and characteristics					
Port	Wakeup source	Extra high drive	Pin sense /detect	GPIOTE	Maximum speed(MHz)
P0	Yes	No	Yes	Yes	8
P1	Yes	No	Yes	Yes	8
P2	No	Yes	No	No	64

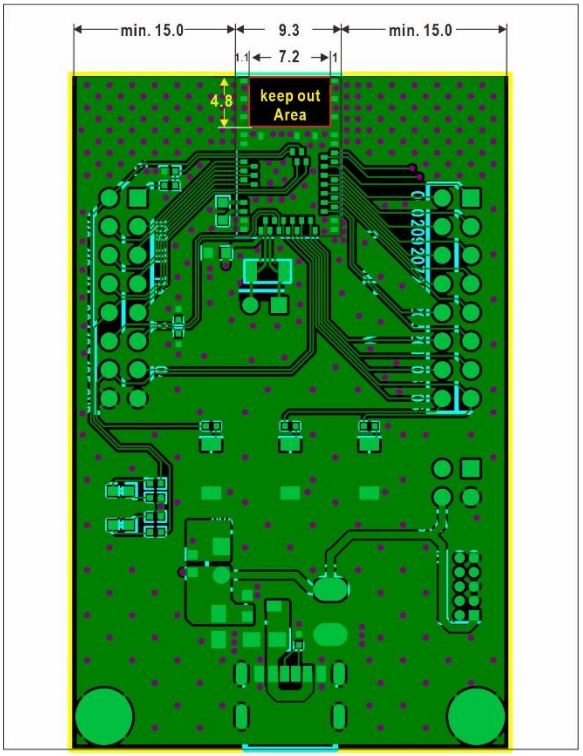
3. Layout design notes

3.1 Recommended RF layout and ground plane

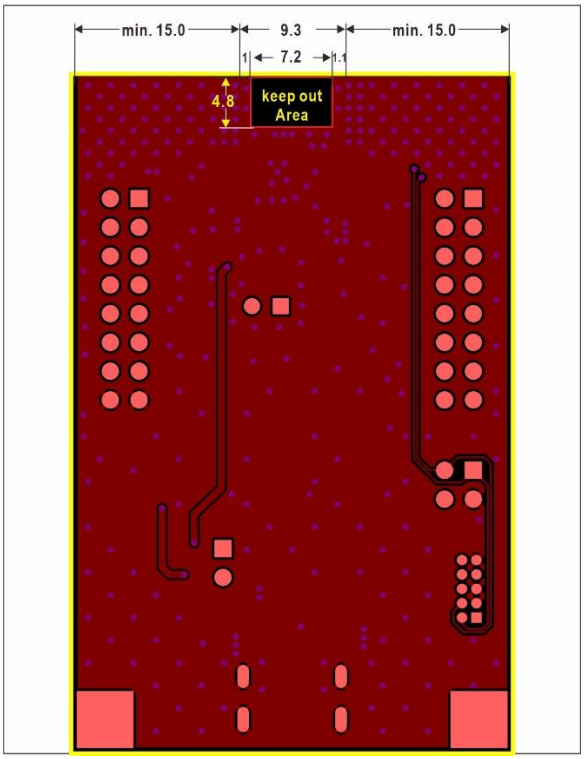
It is recommended to place the module:

- In the center (horizontal) of any mother PCB edge, with GND planes to the left and right
- Keep out Area should be included in the corresponding position of the antenna in each layer.
- Add via hole around GND pads on the mother PCB as many as you can, especially on the four corners and antenna area.

TOP VIEW

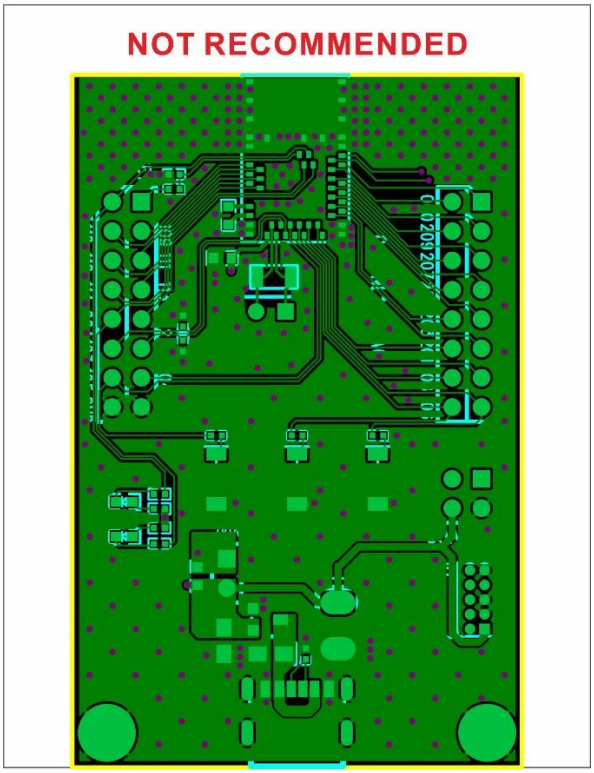


Bottom VIEW

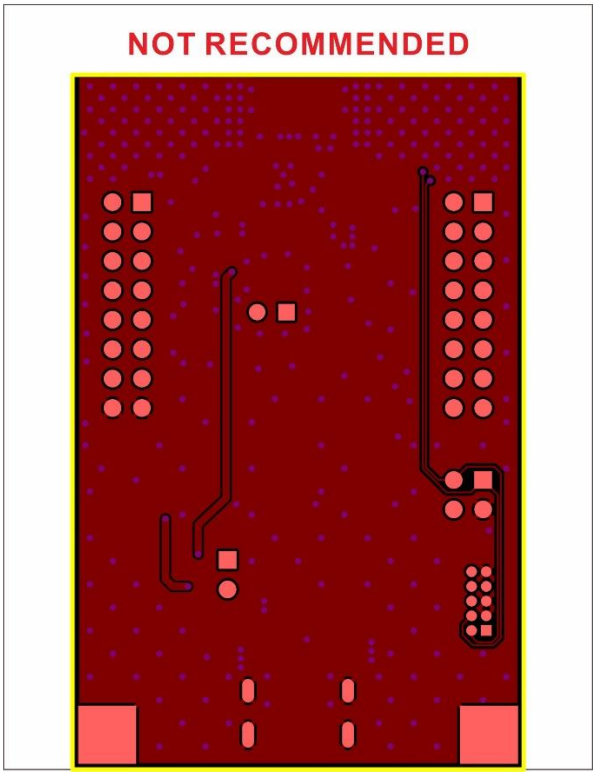


3.2 Not Recommended RF layout and ground plane

TOP VIEW



Bottom VIEW



3.3 Antenna keep out when proximity to Metal

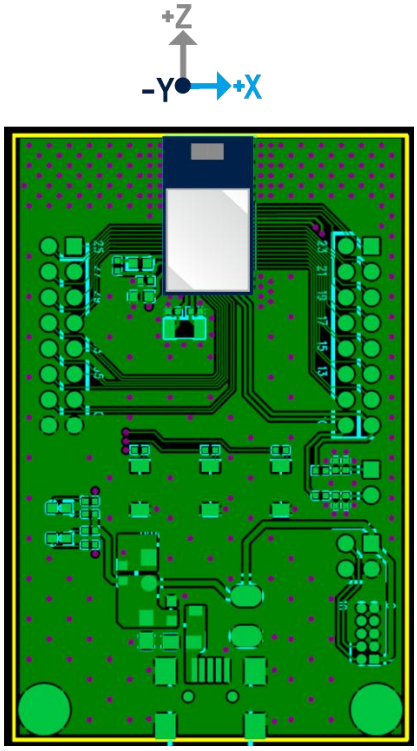
• The minimum safe distance for metals without seriously compromising the antenna tuning is 4cm (bottom, top, left, right).

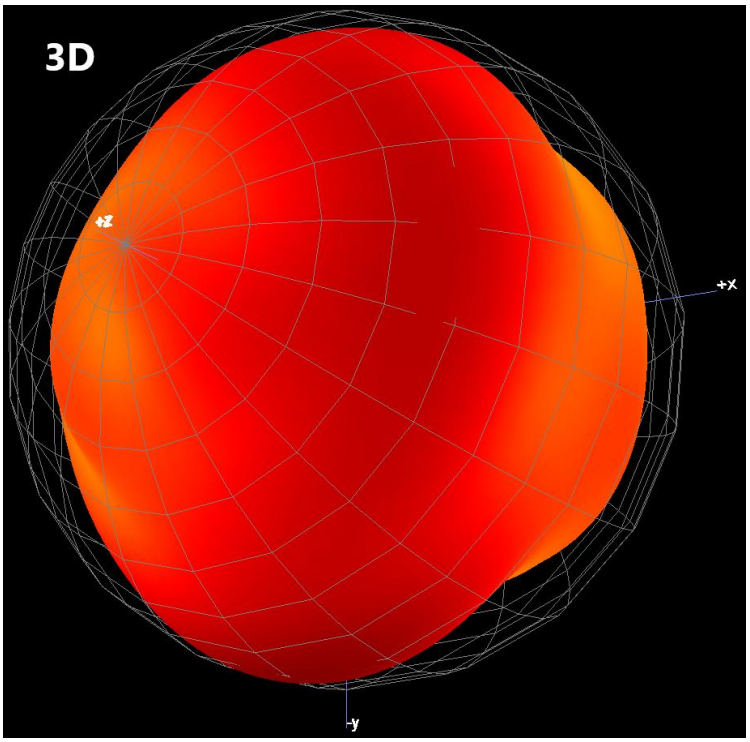
• Metal close to the antenna (bottom, top, left, right) will degrade RF performance. Any metal closer than 2 cm will significantly degrade RF performance.

4. Antenna information

Antenna test report is based on the BN54L-C15 with a ground plane size of 60 mm x 39 mm.

4.1 The orientation of Antenna

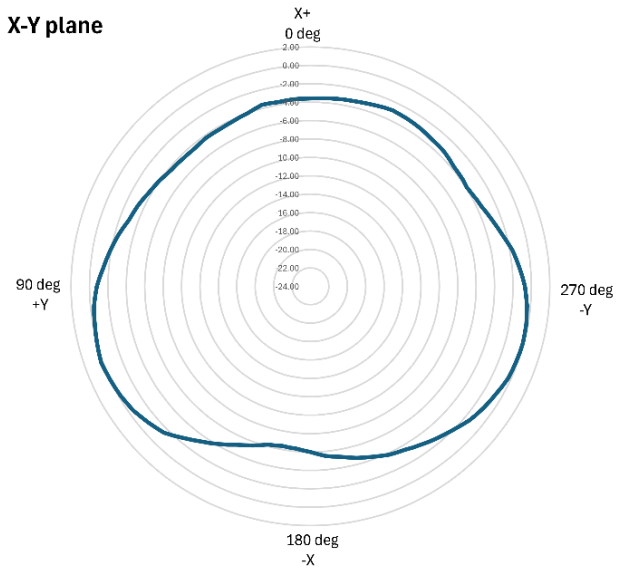


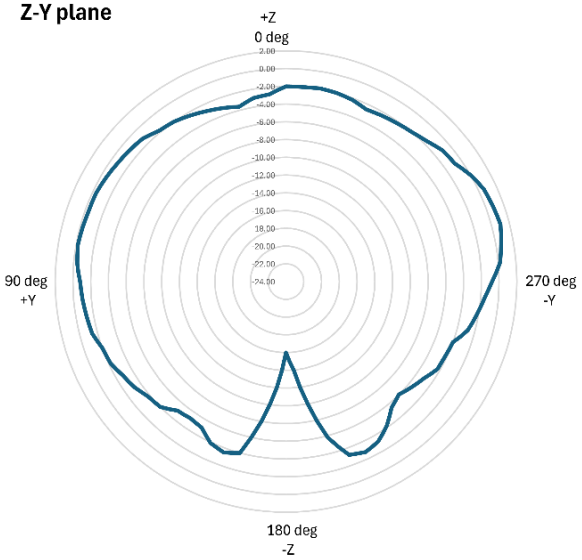


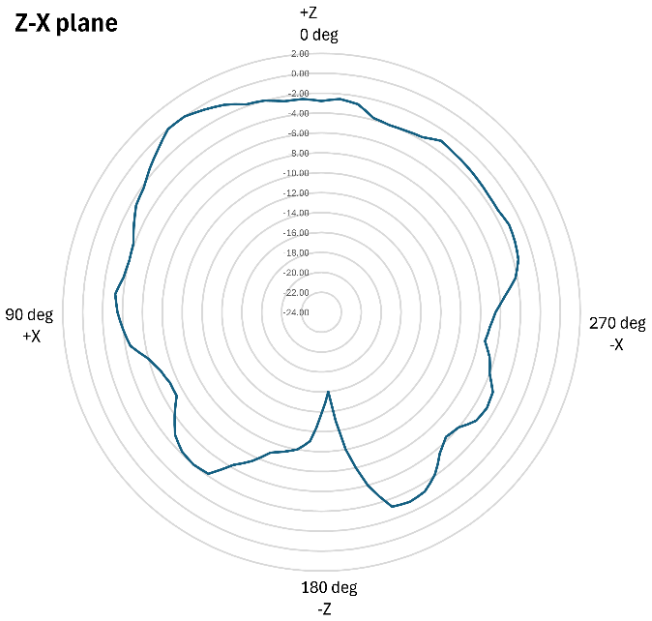
4.2 Antenna Gain and Efficiency

Frequency	Gain(dBi)	Efficiency
2400MHZ	-0.21	42
2410MHZ	0.22	45
2420MHZ	0.52	47
2430MHZ	0.92	50
2440MHZ	1.05	51
2450MHZ	0.87	50
2460MHZ	0.62	48
2470MHZ	0.43	44
2480MHZ	0.19	40
2490MHZ	-0.27	35

4.3 Antenna Pattern 2D







5. Electrical Specification

5.1 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the chip can be exposed for a limited amount of time without causing permanent damage. Prolonged exposure to absolute maximum ratings may affect the device's reliability.

Parameter	Min.	Max.	Unit
Supply voltage			
VDD	**-0.3**	**+3.6**	**V**
VSS		**0**	**V**
I/O pin voltage			
$V_{I/O}$, VDD ≤3.5 V	**-0.3**	**VDD+0.3**	**V**
$V_{I/O}$, VDD >3.5 V		**3.6**	**V**
Environmental			
Storage temperature	**-40**	**+105**	**°C**
MSL (moisture sensitivity level)		**2**	
ESD HBM (human body model)		**1**	**KV**
ESD CDM (charged device model)		**500**	**V**
Flash memory			
Endurance		**10000**	**Write/erase cycles**
Retention		**10 years at 85°C**	

5.2 Operation Conditions

Parameter	Min.	Nom.	Max.	Units
VDD (independent of DCDC)	**1.7**		**3.5**	**V**
VDD during power on reset	**1.75**			**V**
Operating temperature	**-40**	**25**	**85**	**°C**

Important: The on-chip power-on reset circuitry may not function properly if the rise times exceed the specified maximum.

5.3 Radio Specifications

Parameter	Description	Min.	Typ.	Max.	Unit
Operating frequencies	BLE	2402		2480	MHz
Channel spacing	BLE		2		MHz
Frequency deviation	BLE 1Mbps		±250		kHz
	BLE 2Mbps		±500		kHz
On-the-air data rate		125		4000	kHz
Transmitter					
TX power	Setting at +7dBm		+7		dBm
RF power control range	-8 ~+8dBm, in 1db step	-16		+7	dBm
TX current (TX only)	DCDC@3V/+7 dBm		9.1		mA
Receiver					
Receive Sensitivity	1Msps BLE ideal transmitter Packet <=37bytes BRE=0.1%		-96		dBm
	2Msps BLE ideal transmitter Packet <=37bytes BRE=0.1%		-94		dBm
	125ksps BLE ideal transmitter Packet <=37bytes BRE=0.1%		-104		dBm
RX current (RX only)	DCDC@3V/1Msps BLE		2.1		mA
	DCDC@3V/2Msps BLE		2.2		mA
RSSI	RSSI Accuracy Valid range	-90		-30	dBm
	RSSI resolution		1		dB
	Sample period		0.25		us
Antenna gain			1.05		dBi

5.4 System Clock

The MN54L-C15 requires two clocks, a high frequency clock and a low frequency clock.

- The high frequency clock (HFCLK)

HFCLK is provided on-module by a high-accuracy 32 MHz/±20 ppm crystal for radio and CPU operation.

- The low frequency clock (LFCLK)

LFCLK can be provided internally by an RC oscillator (±250 ppm) with calibration, or externally by a 32.768 kHz crystal.

Internal 32.768 kHz RC oscillator (LFRC)

Description	Min.	Typ.	Max.	Unit
Nominal frequency		32.768		kHz
Frequency tolerance for LFRC after calibration (calibration performed at least every 8 seconds)			±500	ppm
Run current for 32.768 kHz RC oscillator		0.7		uA
Startup time for 32.768 kHz RC oscillator		1000		us

External 32.768 kHz crystal oscillator (LFXO)

Parameter	Description	Min.	Typ.	Max.	Unit
	Crystal frequency		32.768		kHz
	Frequency tolerance requirement for BLE stack			±500	ppm
	Frequency tolerance requirement for ANT stack			±50	ppm
	Run current for 32.768 kHz crystal oscillator		0.23		uA
CL	Load capacitance	6		9	pF

An external crystal provides the lowest power consumption and greatest accuracy.

Using the internal RC oscillator with calibration provides acceptable performance for BLE stack at a reduced cost and slight increase in power consumption.

Important:

- The ANT protocol requires the use of an external crystal for high accuracy.
- Nordic SDK example program P1.00/P1.01 as external LFXO, you need an external crystal to work.
- Nordic SDK example program P1.00/P1.01 as external LFXO, if you would like to reduce material cost, save layout space or requires 2 more GPIO for application. you need program p0.00/p0.01 as internal LFRC.

6. Product information

Model	Description
BN54L-C15	**Model : BN54L-C15** **BN: Board/Nordic** **54L: NRF54L series** **C15: Chip antenna/nRF54L15**

BN54L Series

Model	IC/Version	Antenna	Quantity
BN54L-C15	NRF54L15/Revision 2	Chip	1
BN54L-C10	NRF54L10/Revision 2		1
BN54L-C05	NRF54L05/Revision 2		1
BN54L-P15	NRF54L15/Revision 2	PCB	1
BN54L-P10	NRF54L10/Revision 2		1
BN54L-P05	NRF54L05/Revision 2		1
BN54L-U15	NRF54L15/Revision 2	U.FL Connector	1

Revision history

Version	Date	Notes	Name
1.0	2025/06/19	Initial Release	
1.1	2025/09/25	Update section 2.4 /P1.09 description	
1.2	2025/11/25	Update page 2: test distance Update page 13: Port 1 for PWM	