Synthesis Report for 'yuv_filter'

General Information

Date: Mon Nov 1 16:56:38 2021
Version: 2021.1.1 (Build 3286242 on Wed Jul 28 13:10:47 MDT 2021)
Project: yuv_filter.prj
Solution: solution1 (Vivado IP Flow Target)
Product family: zynq
Target device: xc7z020-clg400-1

Performance Estimates

- **Timing**
  - **Summary**

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	6.651 ns	2.70 ns

- **Latency**
  - **Summary**

Latency (cycles)		Latency (absolute)		Interval (cycles)		Type
min	max	min	max	min	max	
721205	44248325	7.212 ms	0.442 sec	721206	44248326	no

  - **Detail**
    - **Instance**

Instance	Module	Latency (cycles)		Latency (absolute)		Interval (cycles)		Type
		min	max	min	max	min	max	
grp_rgb2yuv_1_fu_251	rgb2yuv_1	240401	14749441	2.404 ms	0.147 sec	240401	14749441	no
grp_yuv2rgb_1_fu_271	yuv2rgb_1	320401	19664641	3.204 ms	0.197 sec	320401	19664641	no

    - **Loop**

Loop Name	Latency (cycles)		Iteration Latency	Initiation Interval		Trip Count	Pipelined
	min	max		achieved	target		
- YUV_SCALE_LOOP_X	160400	9834240	802 ~ 5122	-	-	200 ~ 1920	no
+ YUV_SCALE_LOOP_Y	800	5120	4	-	-	200 ~ 1280	no

Utilization Estimates

- **Summary**

Name	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	130	-
FIFO	-	-	-	-	-
Instance	-	7	341	965	-
Memory	12288	-	0	0	0
Multiplexer	-	-	-	261	-
Register	-	-	214	-	-
Total	12288	7	555	1356	0
Available	280	220	106400	53200	0
Utilization (%)	4388	3	~0	2	0

- **Detail**
  - **Instance**

Instance	Module	BRAM_18K	DSP	FF	LUT	URAM
mul_8ns_8ns_15_1_1_U34	mul_8ns_8ns_15_1_1	0	0	0	41	0
mul_8ns_8ns_15_1_1_U35	mul_8ns_8ns_15_1_1	0	0	0	41	0
mul_8ns_8ns_15_1_1_U36	mul_8ns_8ns_15_1_1	0	0	0	41	0
grp_rgb2yuv_1_fu_251	rgb2yuv_1	0	3	181	492	0
grp_yuv2rgb_1_fu_271	yuv2rgb_1	0	4	160	350	0
Total	5	0	7	341	965	0

  - **DSP**

N/A

  - **Memory**

Memory	Module	BRAM_18K	FF	LUT	URAM	Words	Bits	Banks	W*Bits*Banks
p_yuv_channels_ch1_U	p_yuv_channels_ch1	2048	0	0	0	2457600	8	1	19660800
p_yuv_channels_ch2_U	p_yuv_channels_ch1	2048	0	0	0	2457600	8	1	19660800
p_yuv_channels_ch3_U	p_yuv_channels_ch1	2048	0	0	0	2457600	8	1	19660800
p_scale_channels_ch1_U	p_yuv_channels_ch1	2048	0	0	0	2457600	8	1	19660800
p_scale_channels_ch2_U	p_yuv_channels_ch1	2048	0	0	0	2457600	8	1	19660800
p_scale_channels_ch3_U	p_yuv_channels_ch1	2048	0	0	0	2457600	8	1	19660800
Total	6	12288	0	0	0	14745600	48	6	117964800

  - **FIFO**

N/A

  - **Expression**

Variable Name	Operation	DSP	FF	LUT	Bitwidth P0	Bitwidth P1
add_ln134_1_fu_370_p2	+	0	0	29	22	22
add_ln134_fu_349_p2	+	0	0	29	22	22
x_2_fu_319_p2	+	0	0	23	16	1
y_1_fu_360_p2	+	0	0	23	16	1
icmp_ln129_fu_314_p2	icmp	0	0	13	16	16
icmp_ln132_fu_355_p2	icmp	0	0	13	16	16
Total	6	0	0	130	108	78

  - **Multiplexer**

Name	LUT	Input Size	Bits	Total Bits
ap_NS_fsm	48	9	1	9
p_scale_channels_ch1_address0	14	3	22	66
p_scale_channels_ch1_ce0	14	3	1	3
p_scale_channels_ch2_address0	14	3	22	66
p_scale_channels_ch2_ce0	14	3	1	3
p_scale_channels_ch3_address0	14	3	22	66
p_scale_channels_ch3_ce0	14	3	1	3
p_yuv_channels_ch1_address0	14	3	22	66
p_yuv_channels_ch1_ce0	14	3	1	3
p_yuv_channels_ch1_we0	9	2	1	2
p_yuv_channels_ch2_address0	14	3	22	66
p_yuv_channels_ch2_ce0	14	3	1	3
p_yuv_channels_ch2_we0	9	2	1	2
p_yuv_channels_ch3_address0	14	3	22	66

p_yuv_channels_ch3_ce0	14	3	1	3
p_yuv_channels_ch3_we0	9	2	1	2
x_fu_96	9	2	16	32
y_reg_240	9	2	16	32
Total	261	55	174	493

- **Register**

Name	FF	LUT	Bits	Const Bits
U_reg_542	8	0	8	0
V_reg_547	8	0	8	0
Y_reg_537	8	0	8	0
add_ln134_reg_502	14	0	22	8
ap_CS_fsm	8	0	8	0
grp_rgb2yuv_1_fu_251_ap_start_reg	1	0	1	0
grp_yuv2rgb_1_fu_271_ap_start_reg	1	0	1	0
p_yuv_height_reg_473	16	0	16	0
p_yuv_width_reg_467	16	0	16	0
trunc_ln1_reg_557	8	0	8	0
trunc_ln2_reg_562	8	0	8	0
trunc_ln_reg_552	8	0	8	0
x_2_reg_497	16	0	16	0
x_fu_96	16	0	16	0
y_1_reg_510	16	0	16	0
y_reg_240	16	0	16	0
zext_ln134_1_reg_515	22	0	64	42
zext_ln137_reg_479	8	0	15	7
zext_ln138_reg_484	8	0	15	7
zext_ln139_reg_489	8	0	15	7
Total	214	0	285	71

Interface

- **Summary**

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
ap_clk	in	1	ap_ctrl_hs	yuv_filter	return value
ap_rst	in	1	ap_ctrl_hs	yuv_filter	return value
ap_start	in	1	ap_ctrl_hs	yuv_filter	return value
ap_done	out	1	ap_ctrl_hs	yuv_filter	return value
ap_idle	out	1	ap_ctrl_hs	yuv_filter	return value
ap_ready	out	1	ap_ctrl_hs	yuv_filter	return value
in_channels_ch1_address0	out	22	ap_memory	in_channels_ch1	array
in_channels_ch1_ce0	out	1	ap_memory	in_channels_ch1	array
in_channels_ch1_q0	in	8	ap_memory	in_channels_ch1	array
in_channels_ch2_address0	out	22	ap_memory	in_channels_ch2	array
in_channels_ch2_ce0	out	1	ap_memory	in_channels_ch2	array
in_channels_ch2_q0	in	8	ap_memory	in_channels_ch2	array
in_channels_ch3_address0	out	22	ap_memory	in_channels_ch3	array
in_channels_ch3_ce0	out	1	ap_memory	in_channels_ch3	array
in_channels_ch3_q0	in	8	ap_memory	in_channels_ch3	array
in_width	in	16	ap_none	in_width	pointer
in_height	in	16	ap_none	in_height	pointer
out_channels_ch1_address0	out	22	ap_memory	out_channels_ch1	array
out_channels_ch1_ce0	out	1	ap_memory	out_channels_ch1	array

out_channels_ch1_we0	out	1	ap_memory	out_channels_ch1	array
out_channels_ch1_d0	out	8	ap_memory	out_channels_ch1	array
out_channels_ch2_address0	out	22	ap_memory	out_channels_ch2	array
out_channels_ch2_ce0	out	1	ap_memory	out_channels_ch2	array
out_channels_ch2_we0	out	1	ap_memory	out_channels_ch2	array
out_channels_ch2_d0	out	8	ap_memory	out_channels_ch2	array
out_channels_ch3_address0	out	22	ap_memory	out_channels_ch3	array
out_channels_ch3_ce0	out	1	ap_memory	out_channels_ch3	array
out_channels_ch3_we0	out	1	ap_memory	out_channels_ch3	array
out_channels_ch3_d0	out	8	ap_memory	out_channels_ch3	array
out_width	out	16	ap_vld	out_width	pointer
out_width_ap_vld	out	1	ap_vld	out_width	pointer
out_height	out	16	ap_vld	out_height	pointer
out_height_ap_vld	out	1	ap_vld	out_height	pointer
Y_scale	in	8	ap_none	Y_scale	scalar
U_scale	in	8	ap_none	U_scale	scalar
V_scale	in	8	ap_none	V_scale	scalar