ECE4810J SoC Design

Fall 2021

Lab #0 – Reading Assignment

Due: 11:59pm Thursday Sept. 23th, 2021

Please Submit a PDF file on Canvas

The Arty Z7 is a ready-to-use development platform designed around the Zynq-7000™ All Programmable System-on-Chip (AP SoC) from Xilinx. It will be used as the main SoC platform for this course throughout the semester. In this assignment, you will be assigned to read several documents about this board and the SoC. Please answer the questions below and submit through canvas. Note that this is an **individual** lab assignment.

References:

1. Read about Arty Z7 reference manual
   https://digilent.com/reference/programmable-logic/arty-z7/start
2. Zynq datasheet (go to canvas > Files > Reading Materials > Zynq > ds187-XC7Z010-XC7Z020-Data-Sheet.pdf
   Or
   https://umjicanvas.com/courses/2347/files/folder/Reading%20Materials/Zynq?preview=567360)
3. The Zynq Book (go to canvas > Files > Reading Materials > Zynq > The_Zynq_Book_ebook_3.pdf
   Or
   http://www.zynqbook.com/)

Questions:

1. (10%)What are the benefits of having Programmable logic on Zynq?
2. (20%) How many cores does Zynq-7000 have? What are the names of those cores? How does the memory hierarchy look like? What is the main CPU frequency?
3. (15%) Please list the main interfaces of the Zynq-7000 AP SoC device.
4. (5%) How is the Arty Z7 board powered?
5. (10%) What is the Quad SPI Flash? What is the usage of it on this board?
6. (10%) What is DDR Memory? What is the usage of it?
7. (20%) What are the main custom IP blocks creation methods Xilinx provides?
8. (10%) What is High-Level Synthesis (HLS)? What are the motivations behind HLS?