Lab 1

Getting Started with Arty Z7 SoC development platform

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Group Assignment

Group 1	Group 2	Group 3
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Yiheng Xue	Siyuan Zhang	Chenfei Lou
Yutong Wu	Yihua Liu	Xiaotian Shi
	Yuchen Xu	

Lab Schedule

- https://umjicanvas.com/courses/2347/assignments/syllabus

Lab Schedule: (Note: Tentative and subject to adjustment.)

Week	Index	Date	Lab
2	1	9/20	Lab #0 Reading Assignment
	2	9/24	Lab #1
3	3	9/27	Lab #1
		10/1	No lab (National Holiday)
4		10/4	No lab (National Holiday)
	4	10/8	
5	5	10/11	
	6	10/15	
6	7	10/18	
	8	10/22	
7	9	10/25	
	10	10/29	

Logistics

- **16:00-17:40 (M) & 12:10-13:50 (F) week 2-13, 310 E**
- If you can’t make it, please justify your reasons and let the instructor/lab management know at least a week ahead!
- Lab deliverables include but are not limited to reports, codes, demos and beyond (mostly team based).
- Individual contributions will be mainly measured based on peer review (as specific as possible).
- Internet search is allowed, especially for bugs, interesting ideas, but not for direct copy and paste.
- Please read the documents (references) carefully before you ask the questions.

Lab logistics

- Try to understand why you do it before you do it.
- Debug should be a fun process instead of being an painful headache.
- Teamwork is very important, sharing what you learned with each other is valuable.
- Even you are not working on certain part, you should be able to know it.
- You will be plan how you divide the workload across your team, in the end, you need to submit the peer evaluation form.

Zynq-7000 architecture

- 650MHz dual-core Cortex-A9 processor
- DDR3 memory controller with 8 DMA channels and 4 High Performance AXI3 Slave ports
- High-bandwidth peripheral controllers: 1G Ethernet, USB 2.0, SDIO
- Low-bandwidth peripheral controller: SPI, UART, CAN, I2C
- Programmable from JTAG, Quad-SPI flash, and microSD card
- Programmable logic equivalent to Artix-7 FPGA

Zynq-7000 architecture

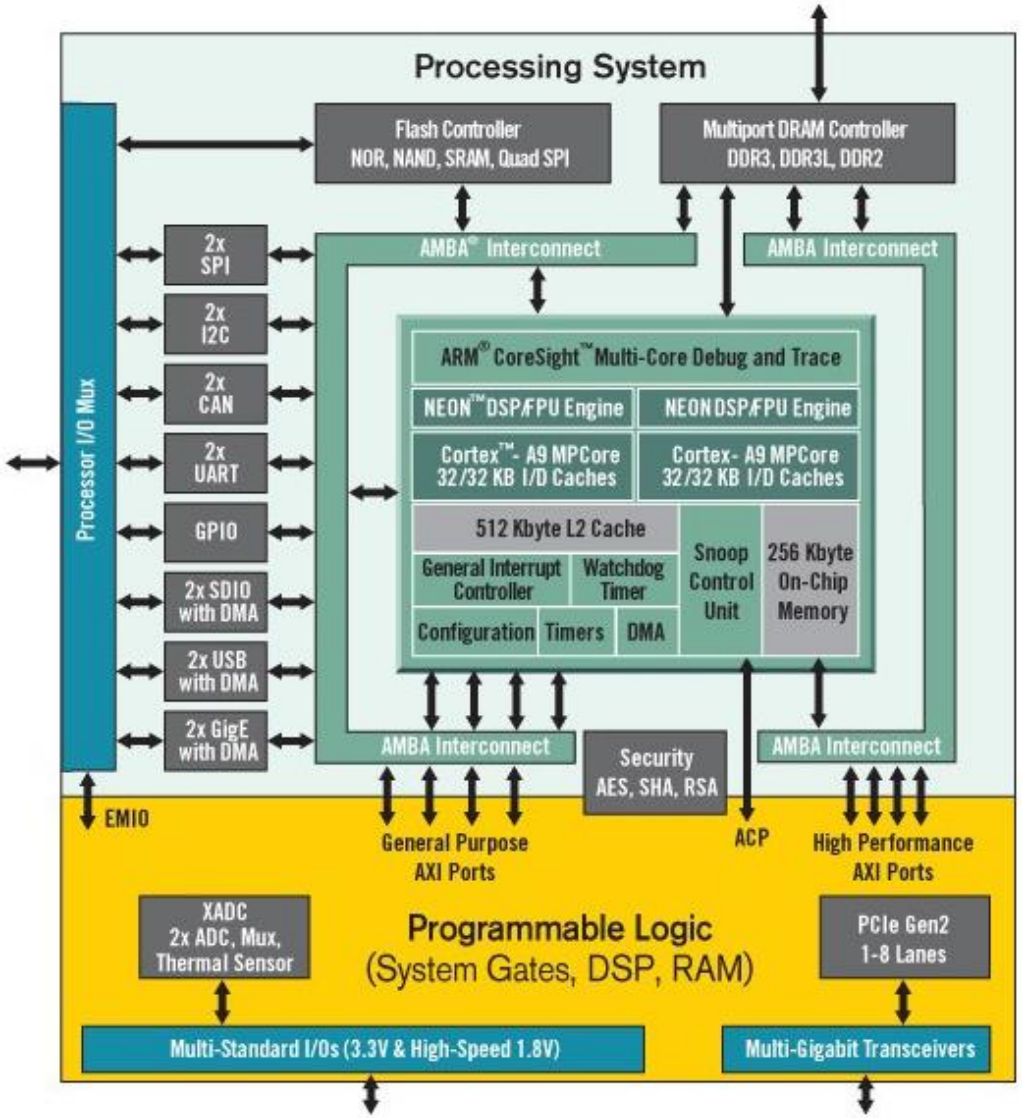


Image: Xilinx

Arty Z7

Product Variant	Arty Z7-10	Arty Z7-20
Zynq Part	XC7Z010-1CLG400C	XC7Z020-1CLG400C
1 MSPS On-chip ADC	Yes	Yes
Look-up Tables (LUTs)	17,600	53,200
Flip-Flops	35,200	106,400
Block RAM	270 KB	630 KB
Clock Management Tiles	2	4
Available Shield I/O	26	49

Arty Z7-20

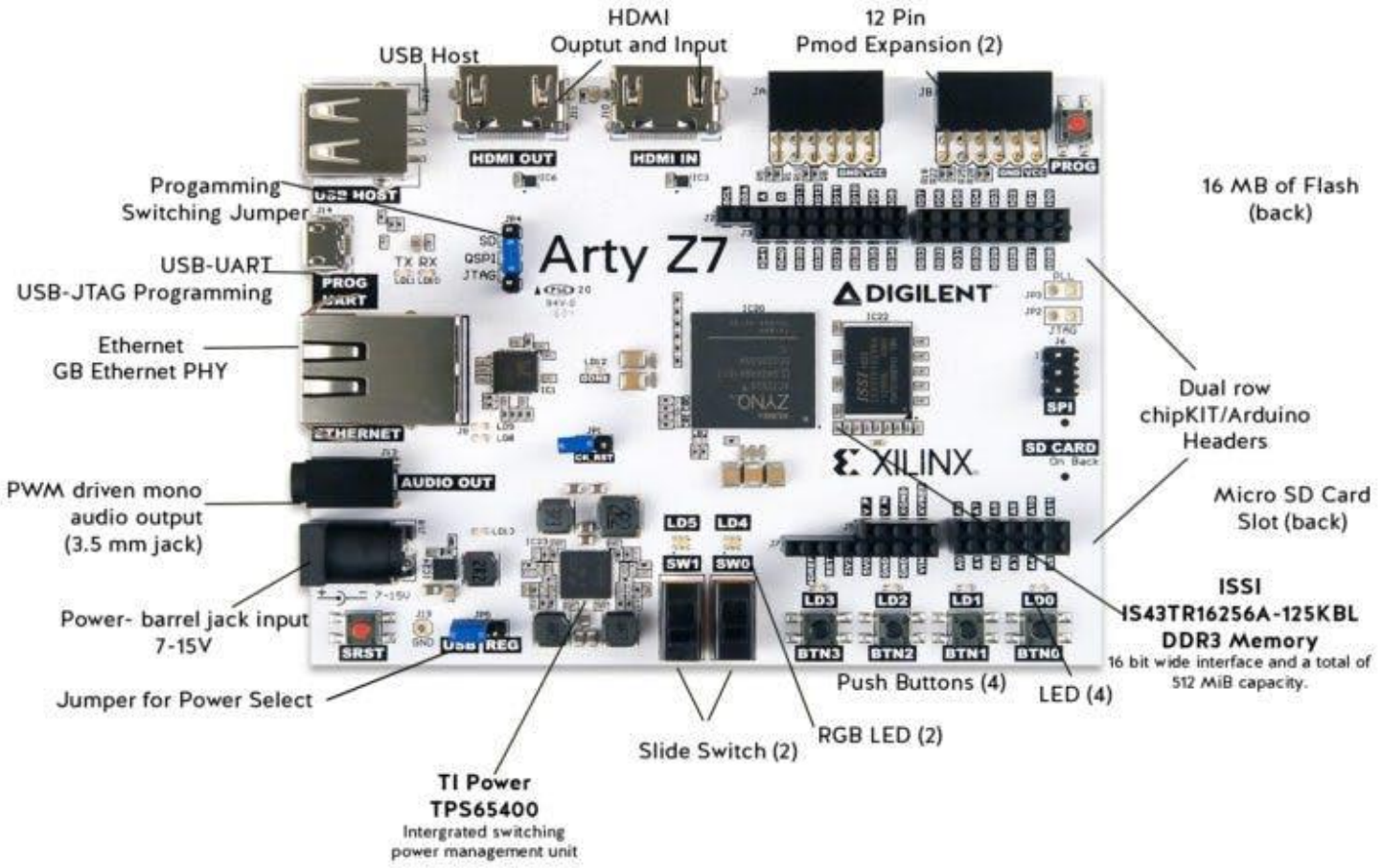


Image: Diligent

Arty Z7 Mechanical Drawing

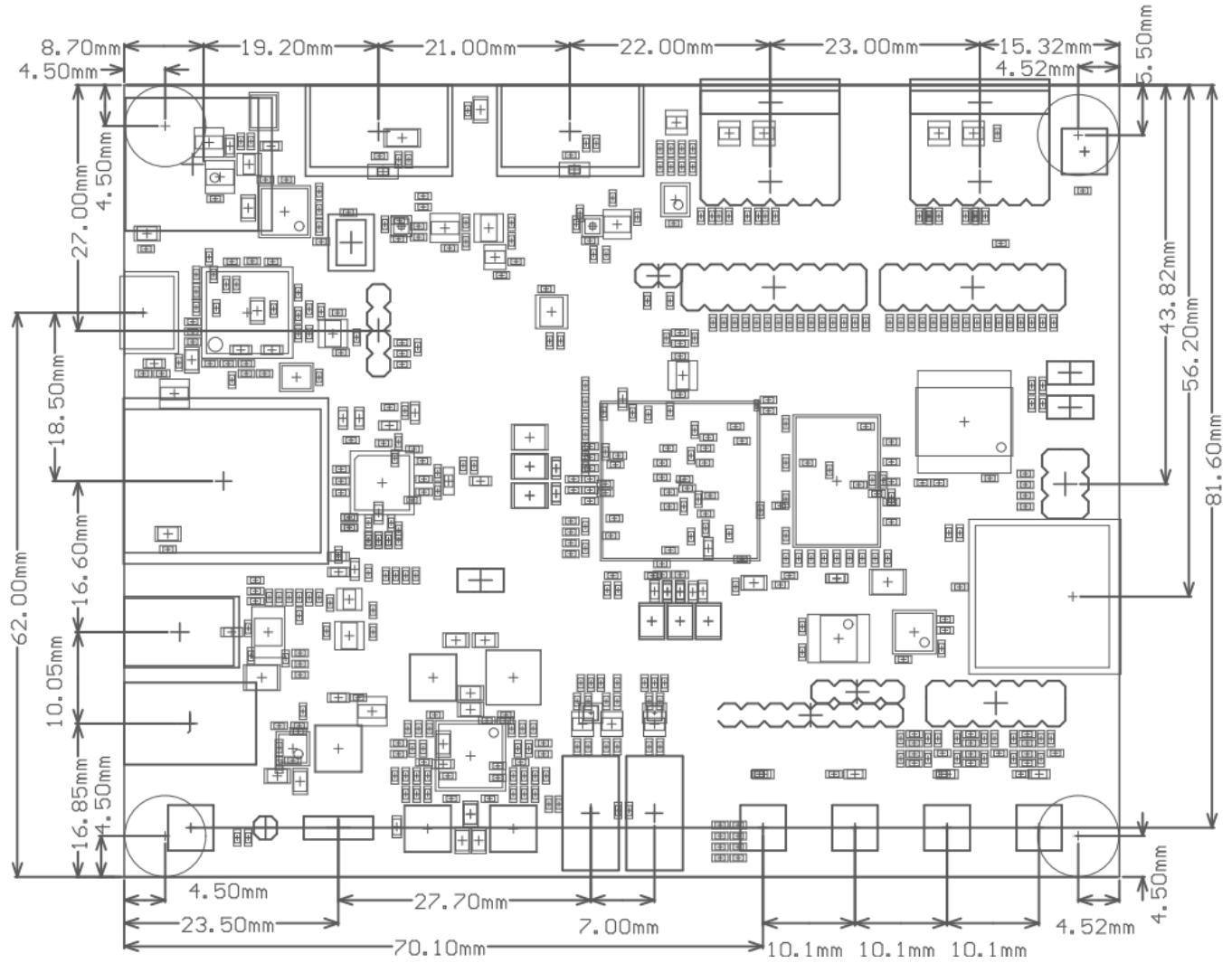


Image: Diligent

Arty Z7-20

- **Memory**
  - 512MB DDR3 with 16-bit bus @ 1050Mbps
  - 16MB Quad-SPI Flash with factory programmed 48-bit globally unique EUI-48/64™ compatible identifier
  - microSD slot
- **USB and Ethernet**
  - Gigabit Ethernet PHY
  - USB-JTAG Programming circuitry
  - USB-UART bridge
  - USB OTG PHY (supports host only)

Source: Diligent

Arty Z7-20

- **Audio and Video**
  - HDMI sink port (input)
  - HDMI source port (output)
  - PWM driven mono audio output with 3.5mm jack
- **Power**
  - Powered from USB or any 7V-15V external power source
- **Switches, Push-buttons, and LEDs**
  - 4 push-buttons
  - 2 slide switches
  - 4 LEDs
  - 2 RGB LEDs

Source: Diligent

Software Support

- Xilinx’s high-performance Vivado Design Suite.
  - You can also treat Zynq AP SoC as a standalone FPGA
- embedded Linux targets
  - e.g. using PYNQ-Z1 image

Boot Modes

- The Arty Z7 supports three different boot modes: microSD, Quad SPI Flash, and JTAG.

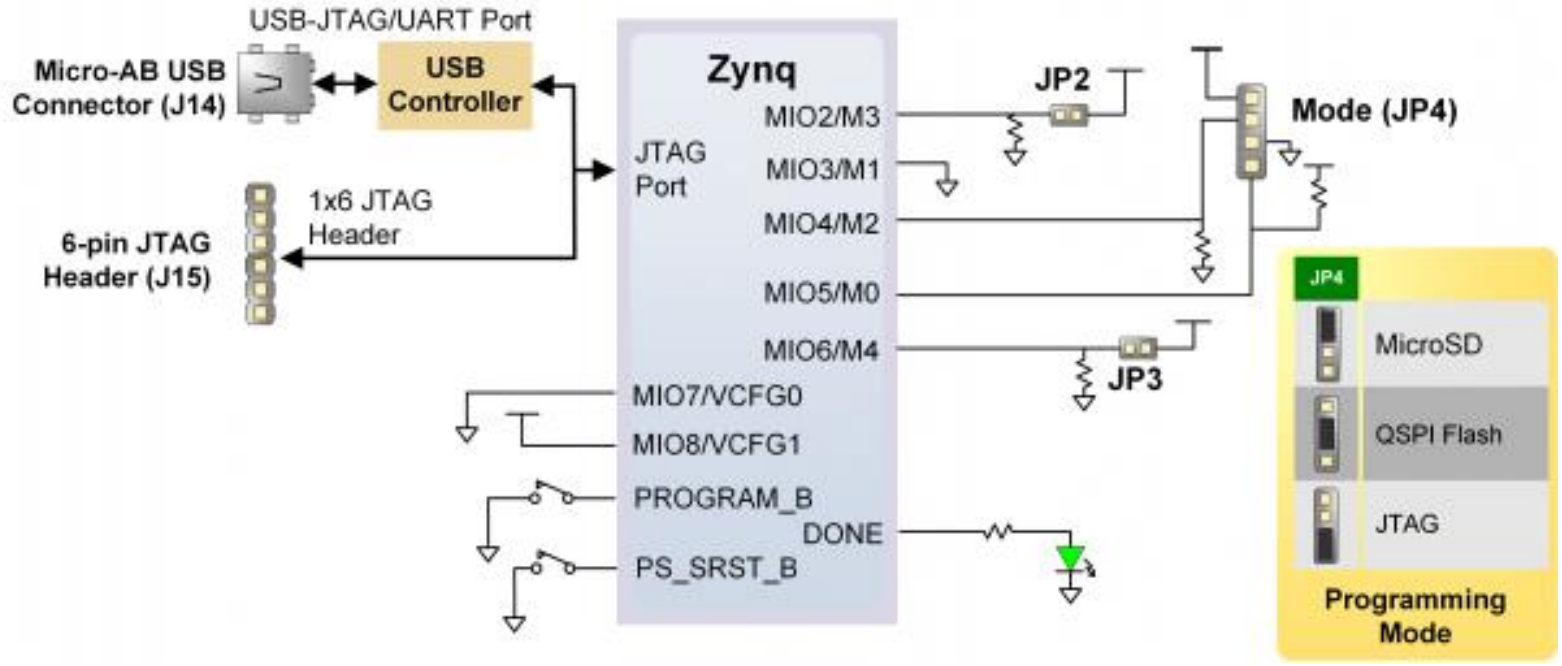
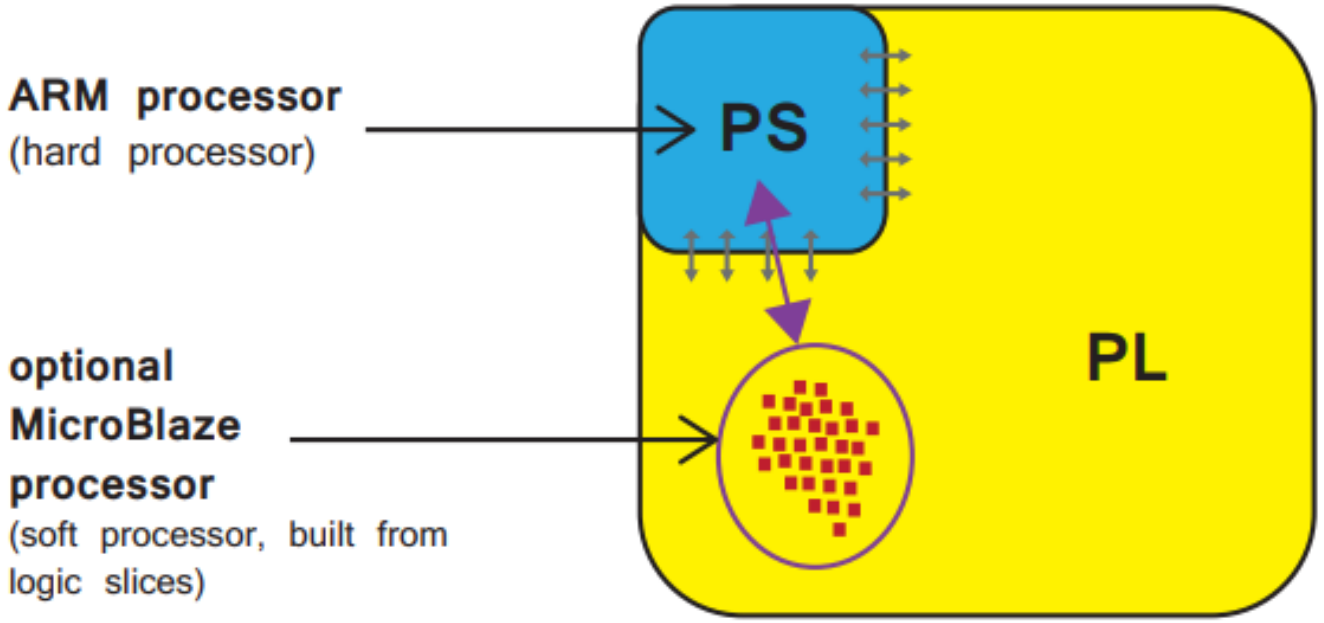
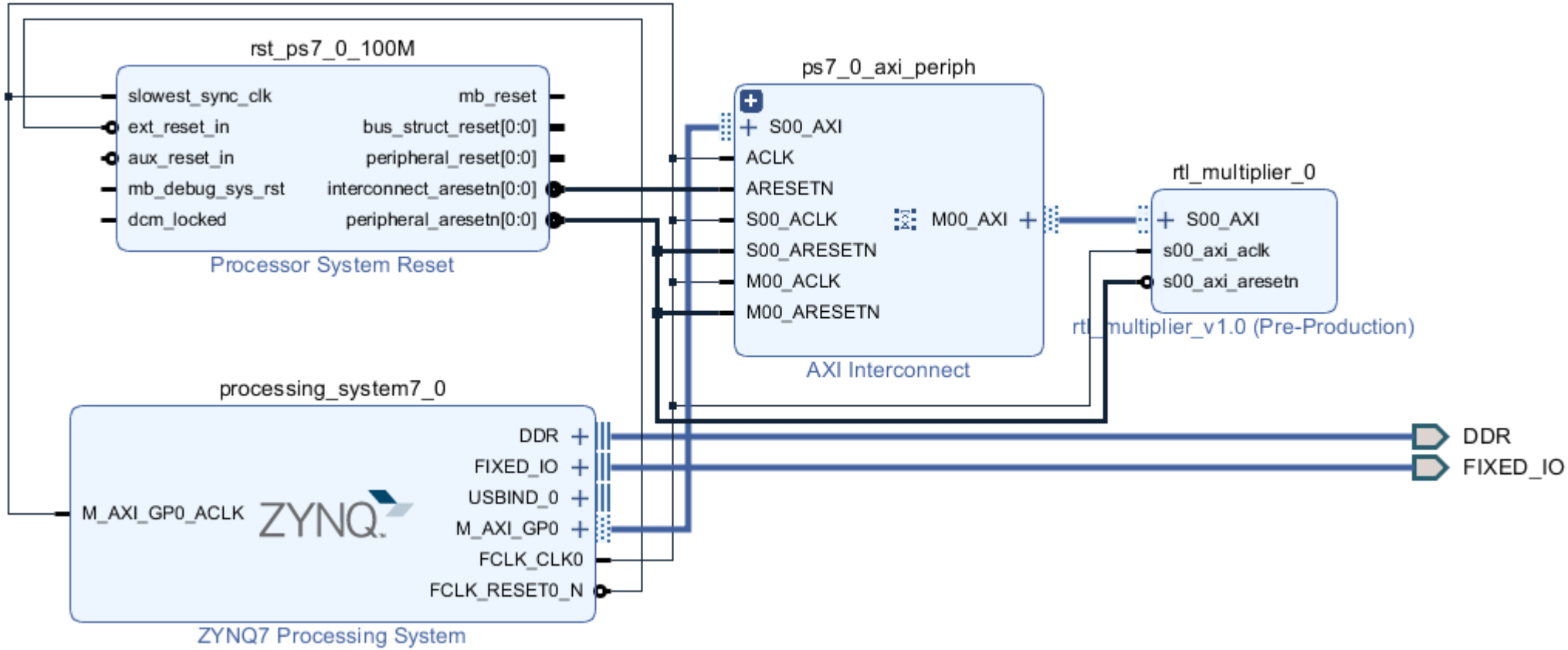


Image: Diligent

Hard vs. Soft Processor



AXI Interconnect



Lab #1

Goals

- Get familiar with the board
- Set up the environment correctly
- Be able to build a basic Zynq system on the board
- Be able to create a custom IP in Verilog
- Be able to use AXI bus to connect an IP block with the Zynq programing system

Deliverables

- Details are in the Lab #1 document
- Peer evaluation form (individual grade)