
UM–SJTU JOINT INSTITUTE
System-on-Chip Design (ECE4810J)

LABORATORY REPORT
Lab 3. PYNQ Overlays
Group 2

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1 Overview

In this lab, we will learn about PYNQ overlays. The goals of this lab are to:

- Load overlay, use overlay and create overlay.

2 Loading an overlay

All the available overlays for the Arty Z7 boards:

- Base Overlay
- Logictools Overlay

Under `/usr/local/lib/python3.6/dist-packages/pynq/overlays`, there are `base`, `__init__.py`, `logictools`, and `__pycache__`, so all the available overlays for the Arty Z7 boards are base overlay and logictools overlay [2].

Once we instantiate the base overlay, we use `help(base_overlay)` command to know IPs and methods available, which is:

```
| iop_pmoda : IOP
|   IO processor connected to the PMODA interface
| iop_pmodb : IOP
|   IO processor connected to the PMODB interface
| iop_arduino : IOP
|   IO processor connected to the Arduino/ChipKit interface
| trace_pmoda : pynq.logictools.TraceAnalyzer
|   Trace analyzer block on PMODA interface, controlled by PS.
| trace_arduino : pynq.logictools.TraceAnalyzer
|   Trace analyzer block on Arduino interface, controlled by PS.
| leds : AxiGPIO
|   4-bit output GPIO for interacting with the green LEDs LD0-3
| buttons : AxiGPIO
|   4-bit input GPIO for interacting with the buttons BTN0-3
| switches : AxiGPIO
|   2-bit input GPIO for interacting with the switches SW0 and SW1
| rgbleds : [pynq.board.RGBLED]
|   Wrapper for GPIO for LD4 and LD5 multicolour LEDs
| video : pynq.lib.video.HDMIWrapper
|   HDMI input and output interfaces
| audio : pynq.lib.audio.Audio
|   Headphone jack and on-board microphone
```

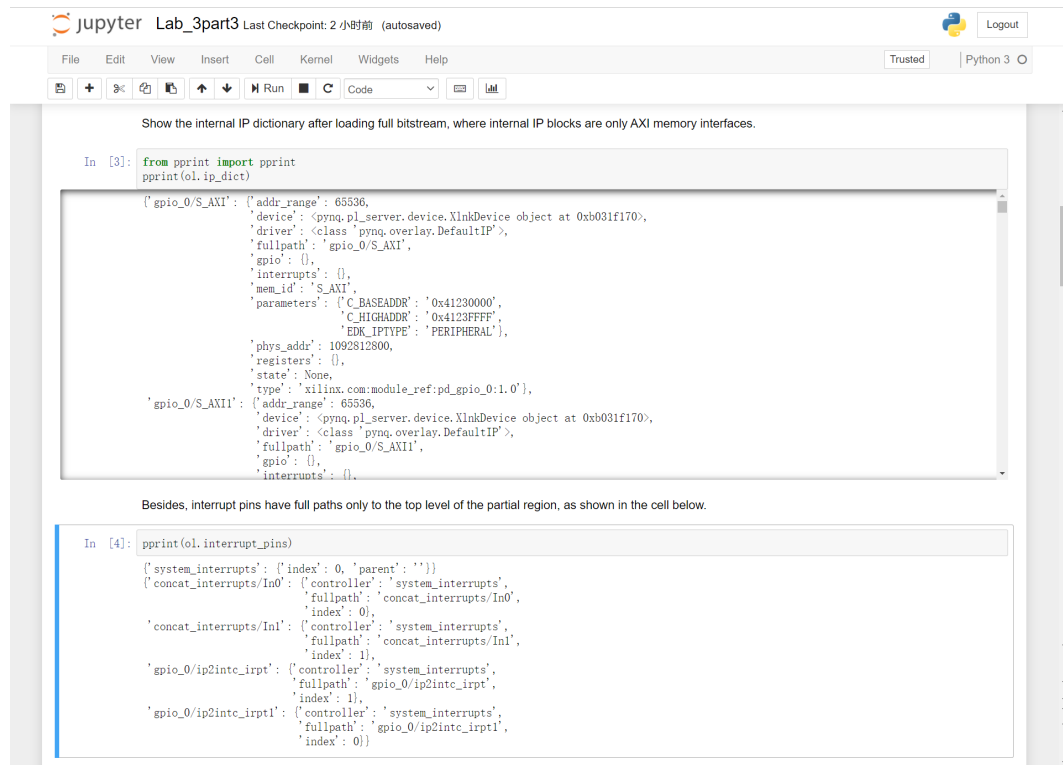
Figure 1. Screenshot of available IPs in base overlay

3 Partial Reconfiguration

3.1 Preparing the Files

In this section, we use the demo files provided by the professor, as included in this example [1].

3.2 Loading Full Bitstream



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File Edit View Insert Cell Kernel Widgets Help Trusted Python 3

Show the internal IP dictionary after loading full bitstream, where internal IP blocks are only AXI memory interfaces.

```
In [3]: from pprint import pprint
        pprint(ol.ip_dict)
```

```
{'gpio_0/S_AXI1': {'addr_range': 65536,
                  'device': <pyng.pl_server.device.XlnkDevice object at 0xb031f170>,
                  'driver': <class 'pyng.overlay.DefaultIP'>,
                  'fullpath': 'gpio_0/S_AXI1',
                  'gpio': {},
                  'interrupts': {},
                  'mem_id': 'S_AXI1',
                  'parameters': {'C_BASEADDR': '0x41230000',
                                'C_HIGHADDR': '0x4123FFFF',
                                'EDK_IPTYPE': 'PERIPHERAL'},
                  'phys_addr': 1092812800,
                  'registers': {},
                  'state': None,
                  'type': 'xilinx.com:module_ref:pd_gpio_0:1.0'},
 'gpio_0/S_AXI0': {'addr_range': 65536,
                  'device': <pyng.pl_server.device.XlnkDevice object at 0xb031f170>,
                  'driver': <class 'pyng.overlay.DefaultIP'>,
                  'fullpath': 'gpio_0/S_AXI0',
                  'gpio': {},
                  'interrupts': {}}}
```

Besides, interrupt pins have full paths only to the top level of the partial region, as shown in the cell below.

```
In [4]: pprint(ol.interrupt_pins)
```

```
{'system_interrupts': {'index': 0, 'parent': ''}}
{'concat_interrupts/In0': {'controller': 'system_interrupts',
                          'fullpath': 'concat_interrupts/In0',
                          'index': 0},
 'concat_interrupts/In1': {'controller': 'system_interrupts',
                          'fullpath': 'concat_interrupts/In1',
                          'index': 1},
 'gpio_0/ip2intc_irpt': {'controller': 'system_interrupts',
                       'fullpath': 'gpio_0/ip2intc_irpt',
                       'index': 1},
 'gpio_0/ip2intc_irpt1': {'controller': 'system_interrupts',
                        'fullpath': 'gpio_0/ip2intc_irpt1',
                        'index': 0}}
```

Figure 2. Screenshot that shows full bit stream is loaded.

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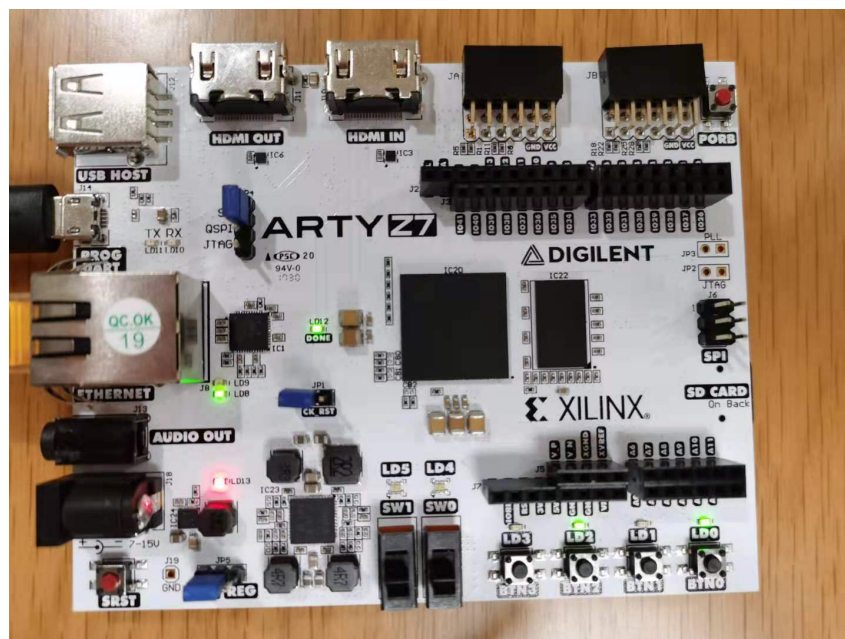
Python 3

In [7]:

pprint(ol.ip_dict)

```
'C_TRI_DEFAULT': '0xFFFFFFFF',  
  'C_TRI_DEFAULT_2': '0xFFFFFFFF',  
  'Component_Name': 'rm_led_5_btns_gpio_0',  
  'EDK_IP_TYPE': 'PERIPHERAL',  
  'GPIO_BOARD_INTERFACE': 'Custom',  
  'GPIO_BOARD_INTERFACE': 'Custom',  
  'USE_BOARD_FLOW': 'false'},  
  
  'phys_addr': 1092681728,  
  'registers': {},  
  'state': None,  
  'type': 'xilinx.com:ip:axi_gpio:2.0'),  
'gpio_0/leds_gpio': {'addr_range': 65536,  
  'device': <pynq_pl_server.device.XlnkDevice object at 0xb031f170>,  
  'driver': <class 'pynq.lib.axigpio.AxiGPIO'>,  
  'fullpath': 'gpio_0/leds_gpio',  
  'gpio': {},  
  'interrupts': {},  
  'mem_id': 'S_AXI',  
  'parameters': {'C_ALL_INPUTS': '0',  
    'C_ALL_INPUTS_2': '0',
```

After loading partial bitstream, we find that both internal IP block hierarchy and interrupt pins have been modified. Besides, after partial reconfiguration, the LEDs on Zynq board shows pattern of 0101:



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4 PYNQ-Helloworld

Resizer in Software

This reference design illustrates how to run a resize operation in **software** using Jupyter Notebooks and Python.

In this example, we will use the **Bilinear** interpolation.

The resize IP transforms the source image to the size of the destination image. Different types of interpolation techniques can be used in resize function, namely: Nearest neighbor, Bilinear, and Area interpolation. The type of interpolation can be passed as a parameter to the Python API. Reference: https://www.xilinx.com/support/documentation/ip_release/mxu-ultrascale017_1/ug1235-ultrascale-ip-core-user-guide.pdf

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Image resize using PIL library

PIL is the **Python Imaging Library**. This library provides extensive file format support, an efficient internal representation, and fairly powerful image processing capabilities.

The image module provides a class with the same name which is used to represent a PIL image. The module also provides a number of factory functions, including functions to load images from files, and to create new images.

Reference: <https://effbot.org/imagedata/pil-index.html#image-resize>

Import libraries

1. PIL library to load and resize the image
2. **numpy** to store the pixel array of the image
3. **matplotlib** to show the image in the notebook

```
In [1]: from PIL import Image
import numpy as np
import matplotlib.pyplot as plt
matplotlib inline
```

Create an Image object

We will load image from the SD card and create an Image object. Then we create a numpy array of the pixels.

Image by Akoskashadine - Own work, [CC-BY-SA-4.0 Link](https://commons.wikimedia.org/wiki/File:CC-BY-SA-4.0_Link)

```
In [2]: image_path = "images/i031_fig.jpg"
original_image = Image.open(image_path)
```

Display the image to be resized

Let's also show the original image size. It may take a while to render a large picture. For better visual effect, we double the size of the canvas. The following code only changes the display size, not the picture itself:

```
canvas = plt.get_fignums()[0].get_canvas()
size = canvas.get_size_inches()
canvas.set_size_inches(size*2)
```

```
In [3]: canvas = plt.get_fignums()[0].get_canvas()
size = canvas.get_size_inches()
canvas.set_size_inches(size*2)
old_width, old_height = original_image.size
print("Image size: [%d] pixels" % (old_width, old_height))
img = plt.imshow(original_image)
```

Image size: 3840x2160 pixels.

Resizing

We will set image resize dimensions.

```
In [4]: resize_factor = 2
new_width = int(old_width*resize_factor)
new_height = int(old_height*resize_factor)
```

We will use `resize()` method from the PIL library. We map multiple input pixels to a single output pixel to downscale the image. The Python Imaging Library provides different resampling filters. We will just choose the bilinear filter in our example. Pick one nearest pixel from the input image, ignore all other input pixels.

```
In [5]: resized_image = original_image.resize((new_width, new_height), Image.BILINEAR)
```

Display resized image

```
In [6]: print("Image size: [%d] pixels" % (new_width, new_height))
img = plt.imshow(resized_image)
```

Image size: 1476x864 pixels.

We can time the resize in software operation.

```
In [7]: %timeit
resized_image = original_image.resize((new_width, new_height), Image.BILINEAR)
1 loop, best of 3: 787 ms per loop
```

References

- <https://effbot.org/imagedata/pil-index.html>
- https://github.com/Xilinx/Vitis/blob/master/docs/source/python_advanced_tutorial
- https://github.com/Xilinx/Vitis/blob/master/docs/source/jupyter_notebooks.ipynb
- https://github.com/Xilinx/Vitis/blob/master/docs/source/jupyter_notebooks_advanced_tutorial.ipynb
- <https://effbot.org/imagedata/pil-index.html#image-resize>

Figure 5. A screen shot of the software accelerated resizing.

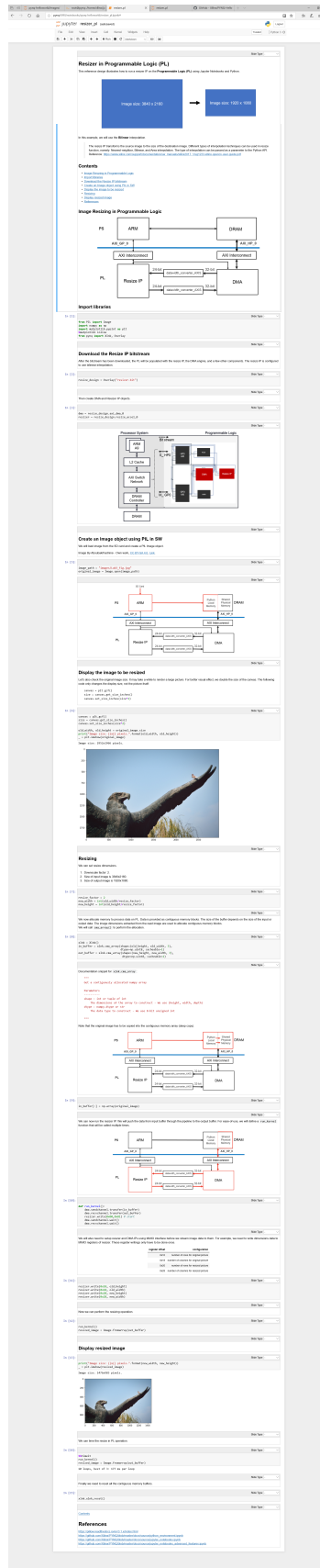
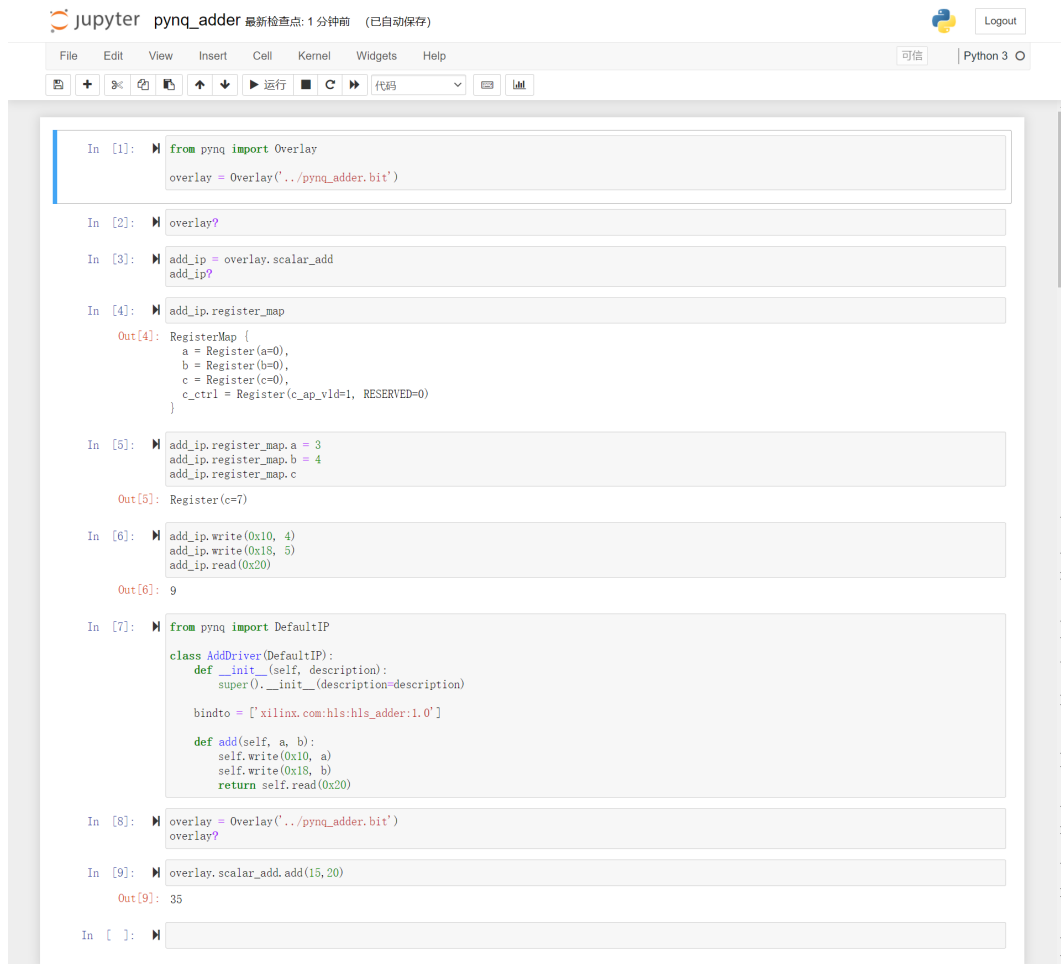


Figure 6. A screen shot of the hardware accelerated resizing.

As we can see in the figures above, the best loop in software is 3.707 ms while the beat loop in hardware acceleration is 3.177 ms.

5 Creating Overlays

The whole overlay package that we created: <https://github.com/yihuajack/PYNQ-Adder>. This Github repository includes our code for part 5.



```
In [1]: from pynq import Overlay
overlay = Overlay('../pynq_adder.bit')

In [2]: overlay?

In [3]: add_ip = overlay.scalar_add
add_ip?

In [4]: add_ip.register_map

Out[4]: RegisterMap {
  a = Register(a=0),
  b = Register(b=0),
  c = Register(c=0),
  c_ctrl = Register(c_ap_vld=1, RESERVED=0)
}

In [5]: add_ip.register_map.a = 3
add_ip.register_map.b = 4
add_ip.register_map.c

Out[5]: Register(c=7)

In [6]: add_ip.write(0x10, 4)
add_ip.write(0x18, 5)
add_ip.read(0x20)

Out[6]: 9

In [7]: from pynq import DefaultIP
class AddDriver(DefaultIP):
    def __init__(self, description):
        super().__init__(description=description)
        bindto = ['xilinx.com:hls:hls_adder:1.0']

    def add(self, a, b):
        self.write(0x10, a)
        self.write(0x18, b)
        return self.read(0x20)

In [8]: overlay = Overlay('../pynq_adder.bit')
overlay?

In [9]: overlay.scalar_add.add(15, 20)

Out[9]: 35

In [ ]:
```

Figure 7. Screenshot that shows your overlay works.

6 Questions

1. Please list out any advantages of using overlay.
Overlay can be regarded as hardware package. By using it, software engineers can simply use different overlays to handle known problems. It is easy to use without the knowledge of hardware designs.
2. In general, when you choose software approach vs. hardware acceleration approach, what are the considerations? Any tradeoffs?
Software is a simpler one by just import the corresponding Python module or other software resources. Hardware acceleration needs a designed ip programmed in the programmable logic and use boards like Arty-7z to finish the task. Hardware acceleration is faster if there is a certain deigned overlay. However, it is not always the case. In

contrast, the software acceleration adapts more task requirements and it do not need any external device.

References

- [1] PartialReconfig. *Partial reconfiguration example*. URL: https://github.com/yunqu/partial_reconfig_example/tree/master/boards/Pynq-Z1/gpio_pr/notebooks/partial_reconfig.
- [2] Xilinx. *Python productivity for Zynq (Pynq)*. Version v2.5.1. Feb. 20, 2020. URL: <https://pynq.readthedocs.io/en/v2.5.1/index.html>.