Synthesis Report for 'rgb2yuv_1'

General Information

Date: Mon Nov 1 17:17:30 2021
Version: 2021.1.1 (Build 3286242 on Wed Jul 28 13:10:47 MDT 2021)
Project: yuv_filter.prj
Solution: solution1 (Vivado IP Flow Target)
Product family: zynq
Target device: xc7z020-clg400-1

Performance Estimates

- **Timing**
  - **Summary**

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	6.270 ns	2.70 ns

- **Latency**
  - **Summary**

Latency (cycles)		Latency (absolute)		Interval (cycles)		Type
min	max	min	max	min	max	
240401	14749441	2.404 ms	0.147 sec	240401	14749441	no

  - **Detail**
    - **Instance**

N/A

    - **Loop**

Loop Name	Latency (cycles)		Iteration Latency	Initiation Interval		Trip Count	Pipelined
	min	max		achieved	target		
- RGB2YUV_LOOP_X	240400	14749440	1202 ~ 7682	-	-	200 ~ 1920	no
+ RGB2YUV_LOOP_Y	1200	7680	6	-	-	200 ~ 1280	no

Utilization Estimates

- **Summary**

Name	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	3	-	-	-
Expression	-	-	0	344	-
FIFO	-	-	-	-	-
Instance	-	0	0	82	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	66	-
Register	-	-	181	-	-
Total	0	3	181	492	0
Available	280	220	106400	53200	0
Utilization (%)	0	1	~0	~0	0

- **Detail**
  - **Instance**

Instance	Module	BRAM_18K	DSP	FF	LUT	URAM
mul_8ns_8s_16_1_1_U1	mul_8ns_8s_16_1_1	0	0	0	41	0
mul_8ns_8s_16_1_1_U2	mul_8ns_8s_16_1_1	0	0	0	41	0
Total	2	0	0	0	82	0

- **DSP**

Instance	Module	Expression
mac_muladd_8ns_5ns_9ns_13_4_1_U3	mac_muladd_8ns_5ns_9ns_13_4_1	i0 + i1 * i2
mac_muladd_8ns_7ns_16ns_16_4_1_U5	mac_muladd_8ns_7ns_16ns_16_4_1	i0 * i1 + i2
mac_muladd_8ns_7s_16s_16_4_1_U4	mac_muladd_8ns_7s_16s_16_4_1	i0 * i1 + i2

- **Memory**

N/A

- **FIFO**

N/A

- **Expression**

Variable Name	Operation	DSP	FF	LUT	Bitwidth P0	Bitwidth P1
add_ln54_1_fu_287_p2	+	0	0	29	22	22
add_ln54_fu_256_p2	+	0	0	29	22	22
add_ln57_1_fu_442_p2	+	0	0	14	16	16
add_ln57_2_fu_451_p2	+	0	0	14	16	16
add_ln57_3_fu_316_p2	+	0	0	14	9	8
add_ln57_fu_436_p2	+	0	0	23	16	16
add_ln58_1_fu_467_p2	+	0	0	14	16	8
add_ln58_2_fu_472_p2	+	0	0	14	16	16
add_ln59_1_fu_397_p2	+	0	0	14	14	8
add_ln59_2_fu_490_p2	+	0	0	23	16	16
out_channels_ch1_d0	+	0	0	15	8	5
x_6_fu_226_p2	+	0	0	23	16	1
y_fu_277_p2	+	0	0	23	16	1
sub_ln58_fu_358_p2	-	0	0	23	16	16
sub_ln59_1_fu_391_p2	-	0	0	14	14	14
sub_ln59_fu_370_p2	-	0	0	14	1	13
icmp_ln49_fu_221_p2	icmp	0	0	13	16	16
icmp_ln52_fu_272_p2	icmp	0	0	13	16	16
out_channels_ch2_d0	xor	0	0	9	8	9
out_channels_ch3_d0	xor	0	0	9	8	9
Total	20	0	0	344	282	248

- **Multiplexer**

Name	LUT	Input Size	Bits	Total Bits
ap_NS_fsm	48	9	1	9
x_fu_108	9	2	16	32
y_02_reg_202	9	2	16	32
Total	66	13	33	73

- **Register**

Name	FF	LUT	Bits	Const Bits
B_reg_619	8	0	8	0
G_reg_637	8	0	8	0

R_reg_613	8	0	8	0
add_ln54_reg_577	14	0	22	8
add_ln59_1_reg_664	13	0	14	1
ap_CS_fsm	8	0	8	0
sub_ln58_reg_654	12	0	16	4
trunc_ln5_reg_674	8	0	8	0
trunc_ln6_reg_679	8	0	8	0
trunc_ln_reg_669	8	0	8	0
x_6_reg_572	16	0	16	0
x_fu_108	16	0	16	0
y_02_reg_202	16	0	16	0
y_reg_585	16	0	16	0
zext_ln54_1_reg_590	22	0	64	42
Total	181	0	236	55

Interface

- **Summary**

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
ap_clk	in	1	ap_ctrl_hs	rgb2yuv.1	return value
ap_rst	in	1	ap_ctrl_hs	rgb2yuv.1	return value
ap_start	in	1	ap_ctrl_hs	rgb2yuv.1	return value
ap_done	out	1	ap_ctrl_hs	rgb2yuv.1	return value
ap_idle	out	1	ap_ctrl_hs	rgb2yuv.1	return value
ap_ready	out	1	ap_ctrl_hs	rgb2yuv.1	return value
ap_return_0	out	16	ap_ctrl_hs	rgb2yuv.1	return value
ap_return_1	out	16	ap_ctrl_hs	rgb2yuv.1	return value
in_channels_ch1_address0	out	22	ap_memory	in_channels_ch1	array
in_channels_ch1_ce0	out	1	ap_memory	in_channels_ch1	array
in_channels_ch1_q0	in	8	ap_memory	in_channels_ch1	array
in_channels_ch2_address0	out	22	ap_memory	in_channels_ch2	array
in_channels_ch2_ce0	out	1	ap_memory	in_channels_ch2	array
in_channels_ch2_q0	in	8	ap_memory	in_channels_ch2	array
in_channels_ch3_address0	out	22	ap_memory	in_channels_ch3	array
in_channels_ch3_ce0	out	1	ap_memory	in_channels_ch3	array
in_channels_ch3_q0	in	8	ap_memory	in_channels_ch3	array
p_read	in	16	ap_none	p_read	scalar
p_read1	in	16	ap_none	p_read1	scalar
out_channels_ch1_address0	out	22	ap_memory	out_channels_ch1	array
out_channels_ch1_ce0	out	1	ap_memory	out_channels_ch1	array
out_channels_ch1_we0	out	1	ap_memory	out_channels_ch1	array
out_channels_ch1_d0	out	8	ap_memory	out_channels_ch1	array
out_channels_ch2_address0	out	22	ap_memory	out_channels_ch2	array
out_channels_ch2_ce0	out	1	ap_memory	out_channels_ch2	array
out_channels_ch2_we0	out	1	ap_memory	out_channels_ch2	array
out_channels_ch2_d0	out	8	ap_memory	out_channels_ch2	array
out_channels_ch3_address0	out	22	ap_memory	out_channels_ch3	array
out_channels_ch3_ce0	out	1	ap_memory	out_channels_ch3	array
out_channels_ch3_we0	out	1	ap_memory	out_channels_ch3	array
out_channels_ch3_d0	out	8	ap_memory	out_channels_ch3	array