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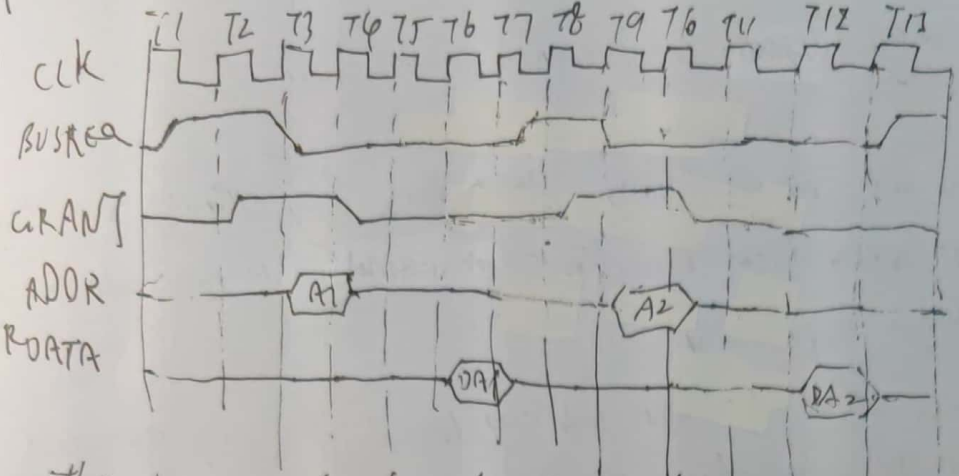
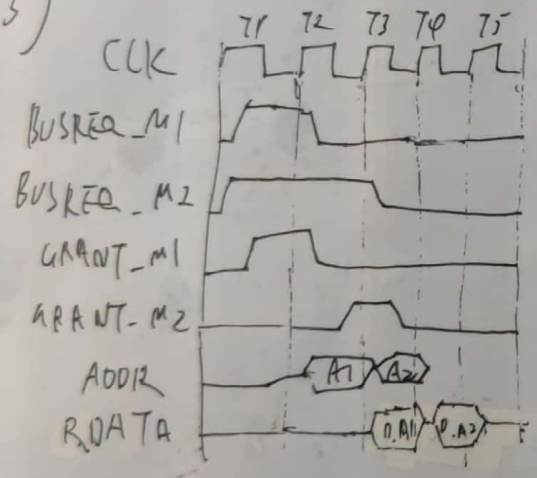
Q.1

1) 

The total number of cycles required for reading two data is 13.
(If the last a little is not counted, answer is 12)

2) 4 cycles can be saved for reading two data

It will take 15 cycles in total for reading two data.
(If last little bit not counted, answer is 14)

3) 

5 cycles (If last little bit is not counted, answer is 4)

4) Burst transfer can send multiple data items with only one single arbitration for the entire transaction. It saves time spent requesting for arbitration.

The total number of cycles it will take for reading two data is 8.

(If last little bit not counted, answer is 7)

Q2 I would choose

1) point-to-point bus, because it can connect every two IPs by a bus, which significantly expands data transfer throughput.

2) Hierarchical bus can reduce blocking. Single bus only allows two IP pairs on the bus, but hierarchical bus allows two IP pairs on the two sides of the bridge separately.

3) Point-to-point bus offers the best scability because it is easy to add buses between IPs in this bus topology.

Q3

Solution 1. b. The width of the bus doubles.

throughput-bus' = 2width-bus * clock_frequency_bus = 6,400 mB/s

Solution 2. a. Length of metal lines halves.

throughput-bus = width-bus * $\frac{\text{clock\_frequency}}{2}$ = 6,400 mB/s

Solution 3. c. Bus topology changes from single bus to point-to-point bus for more than 4 IPs.

Q4

By address and control mux, the arbiter selects slaves' HRDATA to use which master's HADDR

Read: By read data mux (demux), the arbiter use a decoder to decode HRDATA and decides which slave's HRDATA to transfer to the master.

Write: By write data mux, the arbiter selects which master's HWDATA to transfer to HWDATA.

The decoder is used to decode the destination slave address, selece the appropriate slave to receive the data transfer request.

Master first request for access to bus from arbiter, and arbiter will grant the access by address and control mux, and master will sends over the address in the next cycle.

Q5

① NoC's performance does not downgrade with network scaling, while for buses, longer connections lead to higher parasitic capacitance.

② NoCs arbitration and routing are distributed, so that arbitration won't become a bottleneck as it grows.

③ The network size of an NoC scales aggregated bandwidth, so bandwidth is easy to extend.

Q6 The major difference between circuit switching and packet switching:

circuit switching is a buffer-less -flow control, while

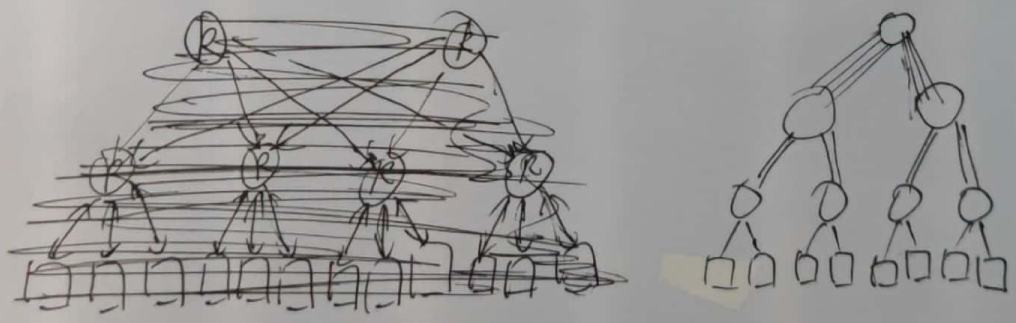
packet switching is a buffered flow control

which means circuit switching sends messages entirely from sender to receiver while packet switching sends different packets along different routes.

A circuit is a (physical) path between the source and the destination.

Q7 1) This NoC topology is Butterfly network that has 2-ary 4-fly.

Tree representation:



2)

2D Mesh — regular — a.

Clos Network (3, 4, 2) — regular — b.

Octagon — regular — c.

irregular — d.

Because it increase available bandwidth and reduce distance between nodes

customized