ECE4810J SoC Design

Fall 2021

HW #4

Due: 11:59pm November 18th, 2021

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Power:

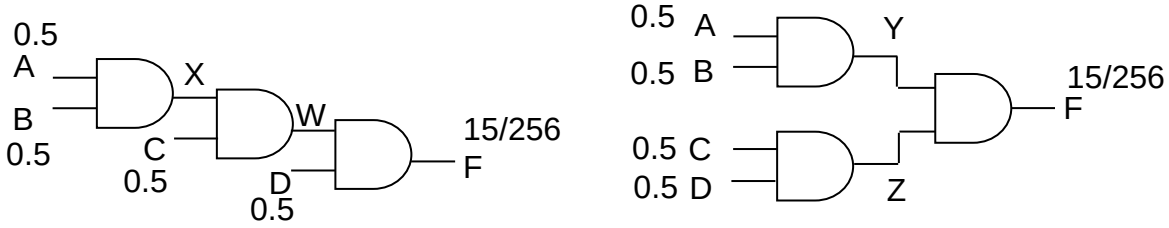
Q1 (20%): Calculate energy dissipated in circuit during 2ms period if

1) Its switching probability is 0.3, operating frequency 500MHz, load capacitance 10fF and supply voltage 1.2V
2) Its switching probability is 0.5, operating frequency 250MHz, load capacitance 12fF and supply voltage 1.0V

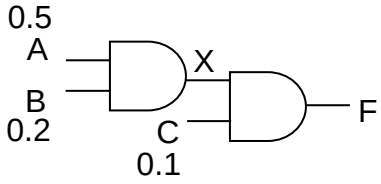
Q2 (20%): Calculate energy dissipated in circuit during 2ms period:

1) Take data from Q1 and assume that circuit powered down during 0.5ms (dynamic energy=0)
2) Take data from Q1 and assume that circuit powered down during 1.2ms (dynamic energy=0)

Q3 (10%): Show which circuit has lower switching activity (ignore glitching effects).



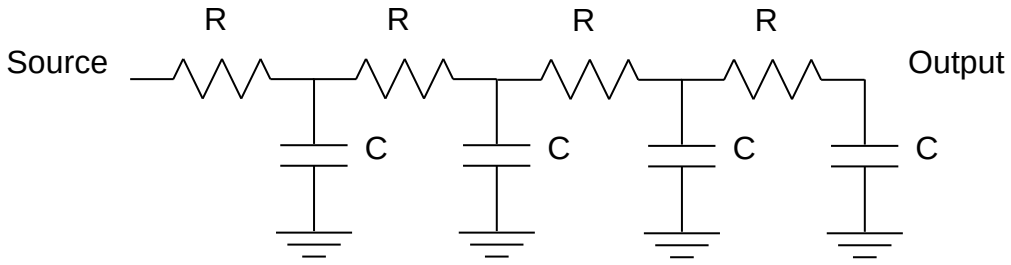
Q4 (10%): Show how input reordering can decrease switching activity.



Q5 (10%): Explain how MTCMOS (Multi Threshold CMOS) circuits work, and how they decrease leakage current.

Interconnects:

Q6 (10%): For the following RC-chain calculate Elmore delay from node "source" to node "output".



Reliability:

Q7 (10%): Calculate the parity of a byte with the value 17_{ten} and show the pattern stored to memory. Assume the parity bit is on the right. Suppose the second most significant bit was inverted in memory, and then you read it back. Did you detect the error? What happens if the two most significant bits are inverted?

Q8 (10%): Assume one byte data value is 11010010_{two}. First show the Hamming ECC code for that byte, and then invert 9^{th} bit and show that the ECC code finds and corrects the single bit error.