ECE4810J SoC Design

Fall 2021

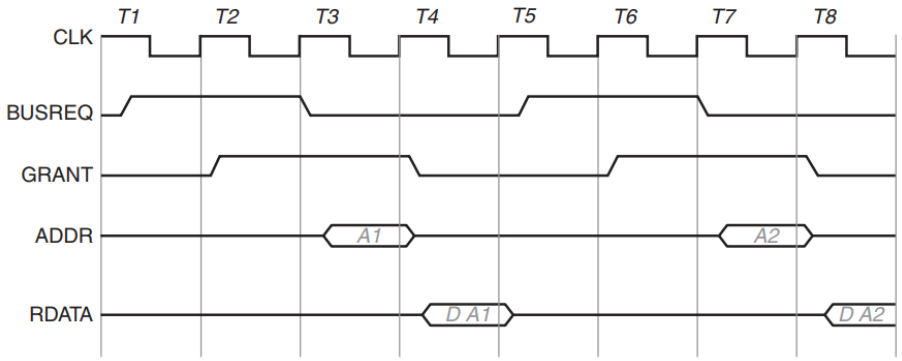
HW #2

Due: 11:59pm October 31st, 2021

Please Submit a PDF file on Canvas

Data Transfer Modes

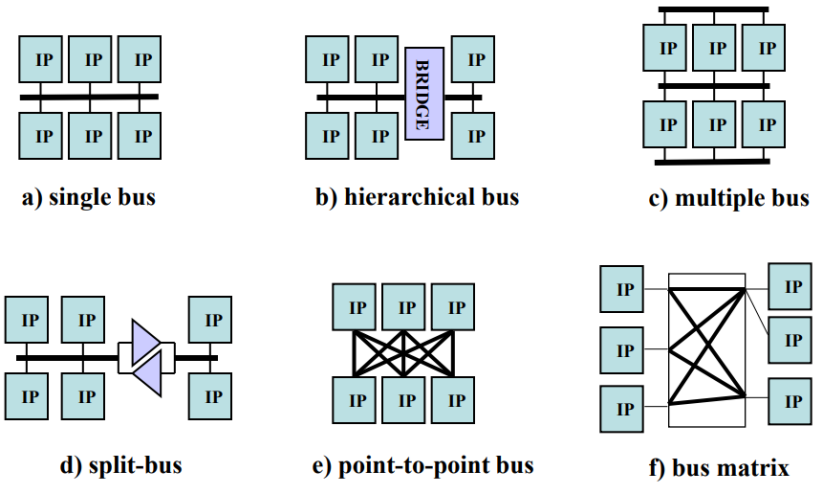
Q1 (35%): The simplest form of data transfer on a bus is the single non-pipelined data transfer mode. The master first requests access to the bus from the arbiter, and when it is granted access, sends out the address in the next cycle, and then writes data in the subsequent cycle (for a write data transfer) or waits for the slave to send the read data in the subsequent cycle(s). The following figure shows an example, where the slave takes only one cycle to return data.



1) (5%) If the slave takes three cycles instead of one in the above example, please draw the new timing diagram, and calculate the total number of cycles required for reading two data.
2) (10%) Given the above condition, if there is no arbitration, then how many cycles can be saved? What if the arbitration takes two cycles, and how many cycles it will take in total for reading two data?
3) (10%) This question is unrelated to the conditions in 1) and 2). Now if you are given an option to use pipeline transfer mode, please draw the new timing diagram and calculate the total number of cycles for reading two data.
4) (10%) What is the benefit of using burst transfer? If you are given an option of using burst transfer mode, and if the arbitration takes two cycles, what is the total number of cycles it will take for reading two data?

Bus Topology

Q2 (15%): Bus-based communication architectures can have several different types of bus arrangements or topology structures which affect the cost, complexity, power, and performance profiles of the communication architecture. The following figure shows several commonly used bus topology. Please answer the questions below.



1) (5%) For high performance systems that require extensive data transfer parallelism, which bus topology would you choose and why?
2) (5%) What is the benefit of using hierarchical bus (b) over single bus?
3) (5%) Based on your understandings, which bus offers the best scalability and why?

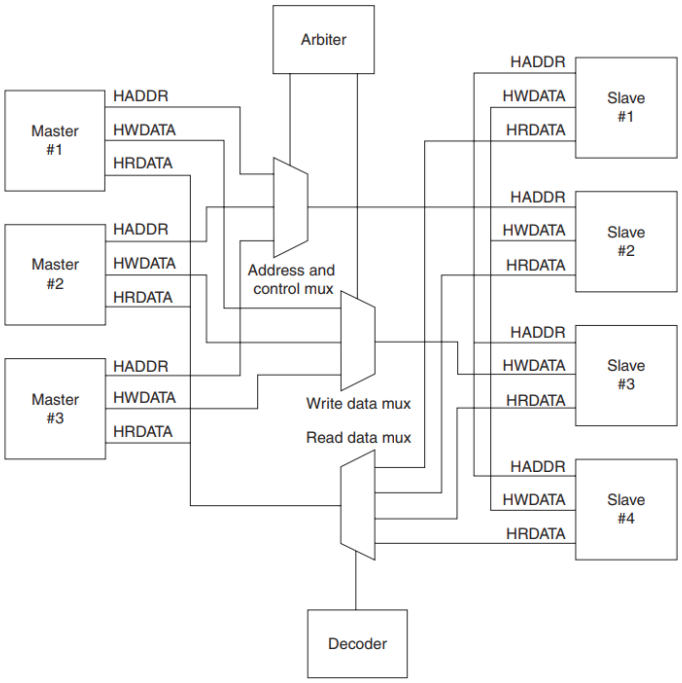
Q3 (10%) : Given that there is a 32-bit bus running at 100MHz, now you are assigned to improve the throughput of this bus by at least 2x. You have the following knobs to play with.

a. Length of metal lines
b. The width of the bus
c. Bus topology shown in Q2
d. The thickness of the metal lines

Please list at least two solutions, and show your calculations.

AMBA

Q4 (10%): The following figure shows the AHB multiplexer interconnection scheme. Please use your own words and describe how data transfer works (both read and write).



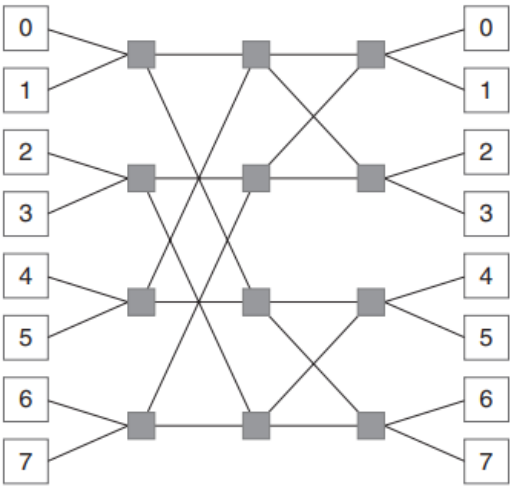
NOC

Q5 (10%): Please list at least 3 aspects where NoCs outperform buses.

Q6 (5%): What is the major difference between circuit switching vs. packet switching? What is a "circuit"?

Q7 (15%):

1) (5%) Which NoC topology is this (need to denote with full name that has number of ays or flys)? Please convert it into a tree representation.



2) (10%) What topologies do the following NoCs employ? Are they regular or irregular? If it is irregular, why do they need such topology?