OpenLane

An Open-Source Tape-Out-Hardened Flow

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Brief Background of OpenLane

OpenROAD

- Launched in June 2018 within the DARPA IDEA program, leaded by UCSD
- To enable no-humans, 24-hour design and catalyze open source EDA
- OpenLane released in 2020 as a project of OpenROAD

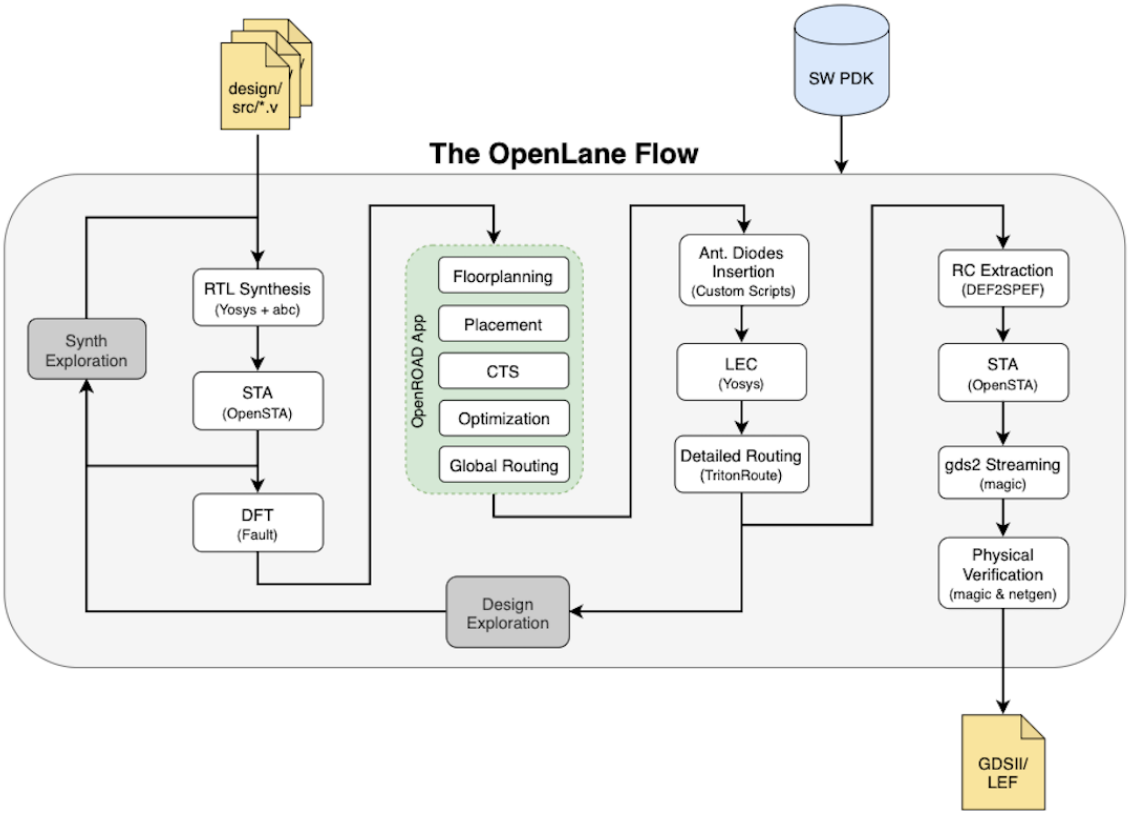
Main contributors of OpenLane

- Efabless
- Google
- OpenROAD

Main Objective of OpenLane

- Performs full ASIC implementation from RTL to GDSII with Sky130 pdks

OpenLane Architecture and Stages



Key Open Source Tools in OpenLane

- **OpenSTA**: Static timing analysis
- **Yosys**: RTL synthesis
- **abc**: Technology mapping
- **ioplacer**: Places marco input & output ports
- **pdn**: Power distribution network
- **RePlace**: Global Placement
- **TritonCTS**: Synthesizes the clock distribution network
- **FastRoute**: Global Routing
- **TritonRoute**: Detailed Routing
- **Magic & Klayout**: Final GDSII layout file and DRC checks

Sky130 PDKs

- Contributors:
  - Google
  - SkyWater Technology Foundry
- OpenLane flow is designed for using Sky130 standard cells from following released libraries:
  - sky130_fd_sc_hd
  - sky130_fd_sc_hs
  - sky130_fd_sc_ms
  - sky130_fd_sc_ls
  - sky130_fd_sc_hdll
  - sky130_fd_sc_hvl
  - sky130_fd_io

Thanks