Vitis HLS Report Comparison

All Compared Solutions

solution1: xc7z020-clg400-1
solution2: xc7z020-clg400-1

Performance Estimates

- **Timing**

Clock		solution1	solution2
ap_clk	Target	10.00 ns	10.00 ns
	Estimated	6.651 ns	6.960 ns

- **Latency**

		solution1	solution2
Latency (cycles)	min	721205	120038
	max	44248325	7372838
Latency (absolute)	min	7.212 ms	1.200 ms
	max	0.442 sec	73.728 ms
Interval (cycles)	min	721206	120039
	max	44248326	7372839

Utilization Estimates

	solution1	solution2
BRAM_18K	12288	12288
DSP	7	10
FF	555	1049
LUT	1356	1767
URAM	0	0

Resource Usage Implementation

	solution1	solution2
RTL	verilog	verilog
SLICE	-	-
LUT	-	-
FF	-	-
DSP	-	-
SRL	-	-
BRAM	-	-

Need to run vivado synthesis/implementation to populate the real data for "-"

Final Timing Implementation

	solution1	solution2
RTL	verilog	verilog
CP required	-	-
CP achieved post-synthesis	-	-
CP achieved post-implementation	-	-

Need to run vivado synthesis/implementation to populate the real data for "-"