Synthesis Report for 'yuv_filter'

General Information

Date: Mon Nov 1 19:24:14 2021
Version: 2021.1.1 (Build 3286242 on Wed Jul 28 13:10:47 MDT 2021)
Project: yuv_filter.prj
Solution: solution3 (Vivado IP Flow Target)
Product family: zynq
Target device: xc7z020-clg400-1

Performance Estimates

- **Timing**
  - **Summary**

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	7.271 ns	2.70 ns

- **Latency**
  - **Summary**

Latency (cycles)		Latency (absolute)		Interval (cycles)		Type
min	max	min	max	min	max	
120037	7372837	1.200 ms	73.728 ms	40013	2457613	dataflow

  - **Detail**
    - **Instance**

Instance	Module	Latency (cycles)		Latency (absolute)		Interval (cycles)		Type
		min	max	min	max	min	max	
entry_proc_U0	entry_proc	0	0	0 ns	0 ns	0	0	no
rgb2yuv_1_U0	rgb2yuv_1	40012	2457612	0.400 ms	24.576 ms	40012	2457612	no
yuv_scale_U0	yuv_scale	40011	2457611	0.400 ms	24.576 ms	40011	2457611	no
yuv2rgb_1_U0	yuv2rgb_1	40012	2457612	0.400 ms	24.576 ms	40012	2457612	no

    - **Loop**

N/A

Utilization Estimates

- **Summary**

Name	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	60	-
FIFO	-	-	693	476	-
Instance	-	11	1155	1692	-
Memory	24576	-	0	0	0
Multiplexer	-	-	-	108	-
Register	-	-	12	-	-
Total	24576	11	1860	2336	0
Available	280	220	106400	53200	0
Utilization (%)	8777	5	1	4	0

- **Detail**

- **Instance**

Instance	Module	BRAM_18K	DSP	FF	LUT	URAM
entry_proc_U0	entry_proc	0	0	2	38	0
rgb2yuv_1_U0	rgb2yuv_1	0	6	411	543	0
yuv2rgb_1_U0	yuv2rgb_1	0	4	373	613	0
yuv_scale_U0	yuv_scale	0	1	369	498	0
Total	4	0	11	1155	1692	0

- **DSP**

N/A

- **Memory**

Memory	Module	BRAM_18K	FF	LUT	URAM	Words	Bits	Banks	W*Bits*Banks
p_yuv_channels_ch1_U	p_yuv_channels_ch1	4096	0	0	0	2457600	8	1	19660800
p_yuv_channels_ch2_U	p_yuv_channels_ch1	4096	0	0	0	2457600	8	1	19660800
p_yuv_channels_ch3_U	p_yuv_channels_ch1	4096	0	0	0	2457600	8	1	19660800
p_scale_channels_ch1_U	p_yuv_channels_ch1	4096	0	0	0	2457600	8	1	19660800
p_scale_channels_ch2_U	p_yuv_channels_ch1	4096	0	0	0	2457600	8	1	19660800
p_scale_channels_ch3_U	p_yuv_channels_ch1	4096	0	0	0	2457600	8	1	19660800
Total	6	24576	0	0	0	14745600	48	6	117964800

- **FIFO**

Name	BRAM_18K	FF	LUT	URAM	Depth	Bits	Size:D*B
U_scale_c_U	0	99	0	-	3	8	24
V_scale_c_U	0	99	0	-	3	8	24
Y_scale_c_U	0	99	0	-	3	8	24
p_scale_height_U	0	99	0	-	2	16	32
p_scale_width_U	0	99	0	-	2	16	32
p_yuv_height_U	0	99	0	-	2	16	32
p_yuv_width_U	0	99	0	-	2	16	32
Total	0	693	0	0	17	88	200

- **Expression**

Variable Name	Operation	DSP	FF	LUT	Bitwidth P0	Bitwidth P1
ap_channel_done_p_scale_channels_ch1	and	0	0	2	1	1
ap_channel_done_p_scale_channels_ch2	and	0	0	2	1	1
ap_channel_done_p_scale_channels_ch3	and	0	0	2	1	1
ap_channel_done_p_scale_height	and	0	0	2	1	1
ap_channel_done_p_scale_width	and	0	0	2	1	1
ap_channel_done_p_yuv_channels_ch1	and	0	0	2	1	1
ap_channel_done_p_yuv_channels_ch2	and	0	0	2	1	1
ap_channel_done_p_yuv_channels_ch3	and	0	0	2	1	1
ap_channel_done_p_yuv_height	and	0	0	2	1	1
ap_channel_done_p_yuv_width	and	0	0	2	1	1
ap_idle	and	0	0	2	1	1
ap_sync_ready	and	0	0	2	1	1
entry_proc_U0_ap_start	and	0	0	2	1	1
rgb2yuv_1_U0_ap_continue	and	0	0	2	1	1
rgb2yuv_1_U0_ap_start	and	0	0	2	1	1
yuv2rgb_1_U0_ap_start	and	0	0	2	1	1
yuv_scale_U0_ap_continue	and	0	0	2	1	1
yuv_scale_U0_ap_start	and	0	0	2	1	1

ap_sync_channel_write_p_scale_channels_ch1	or	0	0	2	1	1
ap_sync_channel_write_p_scale_channels_ch2	or	0	0	2	1	1
ap_sync_channel_write_p_scale_channels_ch3	or	0	0	2	1	1
ap_sync_channel_write_p_scale_height	or	0	0	2	1	1
ap_sync_channel_write_p_scale_width	or	0	0	2	1	1
ap_sync_channel_write_p_yuv_channels_ch1	or	0	0	2	1	1
ap_sync_channel_write_p_yuv_channels_ch2	or	0	0	2	1	1
ap_sync_channel_write_p_yuv_channels_ch3	or	0	0	2	1	1
ap_sync_channel_write_p_yuv_height	or	0	0	2	1	1
ap_sync_channel_write_p_yuv_width	or	0	0	2	1	1
ap_sync_entry_proc_U0_ap_ready	or	0	0	2	1	1
ap_sync_rgb2yuv_1_U0_ap_ready	or	0	0	2	1	1
Total	30	0	0	60	30	30

- **Multiplexer**

Name	LUT	Input Size	Bits	Total Bits
ap_sync_reg_channel_write_p_scale_channels_ch1	9	2	1	2
ap_sync_reg_channel_write_p_scale_channels_ch2	9	2	1	2
ap_sync_reg_channel_write_p_scale_channels_ch3	9	2	1	2
ap_sync_reg_channel_write_p_scale_height	9	2	1	2
ap_sync_reg_channel_write_p_scale_width	9	2	1	2
ap_sync_reg_channel_write_p_yuv_channels_ch1	9	2	1	2
ap_sync_reg_channel_write_p_yuv_channels_ch2	9	2	1	2
ap_sync_reg_channel_write_p_yuv_channels_ch3	9	2	1	2
ap_sync_reg_channel_write_p_yuv_height	9	2	1	2
ap_sync_reg_channel_write_p_yuv_width	9	2	1	2
ap_sync_reg_entry_proc_U0_ap_ready	9	2	1	2
ap_sync_reg_rgb2yuv_1_U0_ap_ready	9	2	1	2
Total	108	24	12	24

- **Register**

Name	FF	LUT	Bits	Const Bits
ap_sync_reg_channel_write_p_scale_channels_ch1	1	0	1	0
ap_sync_reg_channel_write_p_scale_channels_ch2	1	0	1	0
ap_sync_reg_channel_write_p_scale_channels_ch3	1	0	1	0
ap_sync_reg_channel_write_p_scale_height	1	0	1	0
ap_sync_reg_channel_write_p_scale_width	1	0	1	0
ap_sync_reg_channel_write_p_yuv_channels_ch1	1	0	1	0
ap_sync_reg_channel_write_p_yuv_channels_ch2	1	0	1	0
ap_sync_reg_channel_write_p_yuv_channels_ch3	1	0	1	0
ap_sync_reg_channel_write_p_yuv_height	1	0	1	0
ap_sync_reg_channel_write_p_yuv_width	1	0	1	0
ap_sync_reg_entry_proc_U0_ap_ready	1	0	1	0
ap_sync_reg_rgb2yuv_1_U0_ap_ready	1	0	1	0
Total	12	0	12	0

Interface

- **Summary**

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
ap_clk	in	1	ap_ctrl_hs	yuv_filter	return value
ap_rst	in	1	ap_ctrl_hs	yuv_filter	return value
ap_start	in	1	ap_ctrl_hs	yuv_filter	return value
ap_done	out	1	ap_ctrl_hs	yuv_filter	return value

ap_ready	out	1	ap_ctrl_hs	yuv_filter	return value
ap_idle	out	1	ap_ctrl_hs	yuv_filter	return value
in_channels_ch1_address0	out	22	ap_memory	in_channels_ch1	array
in_channels_ch1_ce0	out	1	ap_memory	in_channels_ch1	array
in_channels_ch1_d0	out	8	ap_memory	in_channels_ch1	array
in_channels_ch1_q0	in	8	ap_memory	in_channels_ch1	array
in_channels_ch1_we0	out	1	ap_memory	in_channels_ch1	array
in_channels_ch1_address1	out	22	ap_memory	in_channels_ch1	array
in_channels_ch1_ce1	out	1	ap_memory	in_channels_ch1	array
in_channels_ch1_d1	out	8	ap_memory	in_channels_ch1	array
in_channels_ch1_q1	in	8	ap_memory	in_channels_ch1	array
in_channels_ch1_we1	out	1	ap_memory	in_channels_ch1	array
in_channels_ch2_address0	out	22	ap_memory	in_channels_ch2	array
in_channels_ch2_ce0	out	1	ap_memory	in_channels_ch2	array
in_channels_ch2_d0	out	8	ap_memory	in_channels_ch2	array
in_channels_ch2_q0	in	8	ap_memory	in_channels_ch2	array
in_channels_ch2_we0	out	1	ap_memory	in_channels_ch2	array
in_channels_ch2_address1	out	22	ap_memory	in_channels_ch2	array
in_channels_ch2_ce1	out	1	ap_memory	in_channels_ch2	array
in_channels_ch2_d1	out	8	ap_memory	in_channels_ch2	array
in_channels_ch2_q1	in	8	ap_memory	in_channels_ch2	array
in_channels_ch2_we1	out	1	ap_memory	in_channels_ch2	array
in_channels_ch3_address0	out	22	ap_memory	in_channels_ch3	array
in_channels_ch3_ce0	out	1	ap_memory	in_channels_ch3	array
in_channels_ch3_d0	out	8	ap_memory	in_channels_ch3	array
in_channels_ch3_q0	in	8	ap_memory	in_channels_ch3	array
in_channels_ch3_we0	out	1	ap_memory	in_channels_ch3	array
in_channels_ch3_address1	out	22	ap_memory	in_channels_ch3	array
in_channels_ch3_ce1	out	1	ap_memory	in_channels_ch3	array
in_channels_ch3_d1	out	8	ap_memory	in_channels_ch3	array
in_channels_ch3_q1	in	8	ap_memory	in_channels_ch3	array
in_channels_ch3_we1	out	1	ap_memory	in_channels_ch3	array
in_width	in	16	ap_none	in_width	pointer
in_height	in	16	ap_none	in_height	pointer
out_channels_ch1_address0	out	22	ap_memory	out_channels_ch1	array
out_channels_ch1_ce0	out	1	ap_memory	out_channels_ch1	array
out_channels_ch1_d0	out	8	ap_memory	out_channels_ch1	array
out_channels_ch1_q0	in	8	ap_memory	out_channels_ch1	array
out_channels_ch1_we0	out	1	ap_memory	out_channels_ch1	array
out_channels_ch1_address1	out	22	ap_memory	out_channels_ch1	array
out_channels_ch1_ce1	out	1	ap_memory	out_channels_ch1	array
out_channels_ch1_d1	out	8	ap_memory	out_channels_ch1	array
out_channels_ch1_q1	in	8	ap_memory	out_channels_ch1	array
out_channels_ch1_we1	out	1	ap_memory	out_channels_ch1	array
out_channels_ch2_address0	out	22	ap_memory	out_channels_ch2	array
out_channels_ch2_ce0	out	1	ap_memory	out_channels_ch2	array
out_channels_ch2_d0	out	8	ap_memory	out_channels_ch2	array
out_channels_ch2_q0	in	8	ap_memory	out_channels_ch2	array
out_channels_ch2_we0	out	1	ap_memory	out_channels_ch2	array
out_channels_ch2_address1	out	22	ap_memory	out_channels_ch2	array
out_channels_ch2_ce1	out	1	ap_memory	out_channels_ch2	array
out_channels_ch2_d1	out	8	ap_memory	out_channels_ch2	array
out_channels_ch2_q1	in	8	ap_memory	out_channels_ch2	array
out_channels_ch2_we1	out	1	ap_memory	out_channels_ch2	array

out_channels_ch3_address0	out	22	ap_memory	out_channels_ch3	array
out_channels_ch3_ce0	out	1	ap_memory	out_channels_ch3	array
out_channels_ch3_d0	out	8	ap_memory	out_channels_ch3	array
out_channels_ch3_q0	in	8	ap_memory	out_channels_ch3	array
out_channels_ch3_we0	out	1	ap_memory	out_channels_ch3	array
out_channels_ch3_address1	out	22	ap_memory	out_channels_ch3	array
out_channels_ch3_ce1	out	1	ap_memory	out_channels_ch3	array
out_channels_ch3_d1	out	8	ap_memory	out_channels_ch3	array
out_channels_ch3_q1	in	8	ap_memory	out_channels_ch3	array
out_channels_ch3_we1	out	1	ap_memory	out_channels_ch3	array
out_width	out	16	ap_vld	out_width	pointer
out_width_ap_vld	out	1	ap_vld	out_width	pointer
out_height	out	16	ap_vld	out_height	pointer
out_height_ap_vld	out	1	ap_vld	out_height	pointer
Y_scale	in	8	ap_none	Y_scale	scalar
U_scale	in	8	ap_none	U_scale	scalar
V_scale	in	8	ap_none	V_scale	scalar