Synthesis Report for 'yuv2rgb_1'

General Information

Date: Mon Nov 1 17:17:31 2021
Version: 2021.1.1 (Build 3286242 on Wed Jul 28 13:10:47 MDT 2021)
Project: yuv_filter.prj
Solution: solution1 (Vivado IP Flow Target)
Product family: zynq
Target device: xc7z020-clg400-1

Performance Estimates

- **Timing**
  - **Summary**

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	6.651 ns	2.70 ns

- **Latency**
  - **Summary**

Latency (cycles)		Latency (absolute)		Interval (cycles)		Type
min	max	min	max	min	max	
320401	19664641	3.204 ms	0.197 sec	320401	19664641	no

  - **Detail**
    - **Instance**

N/A

    - **Loop**

Loop Name	Latency (cycles)		Iteration Latency	Initiation Interval		Trip Count	Pipelined
	min	max		achieved	target		
- YUV2RGB_LOOP_X	320400	19664640	1602 ~ 10242	-	-	200 ~ 1920	no
+ YUV2RGB_LOOP_Y	1600	10240	8	-	-	200 ~ 1280	no

Utilization Estimates

- **Summary**

Name	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	4	-	-	-
Expression	-	-	0	273	-
FIFO	-	-	-	-	-
Instance	-	-	-	-	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	77	-
Register	-	-	160	-	-
Total	0	4	160	350	0
Available	280	220	106400	53200	0
Utilization (%)	0	1	~0	~0	0

- **Detail**
  - **Instance**

N/A

- **DSP**

Instance	Module	Expression
mac_muladd_8s_8s_18s_18_4_1_U21	mac_muladd_8s_8s_18s_18_4_1	i0 + i1 * i2
mac_muladd_8s_9ns_18s_18_4_1_U19	mac_muladd_8s_9ns_18s_18_4_1	i0 * i1 + i2
mac_muladd_8s_9s_18s_18_4_1_U20	mac_muladd_8s_9s_18s_18_4_1	i0 + i1 * i2
mac_muladd_9s_9ns_8ns_18_4_1_U18	mac_muladd_9s_9ns_8ns_18_4_1	i0 * i1 + i2

- **Memory**

N/A

- **FIFO**

N/A

- **Expression**

Variable Name	Operation	DSP	FF	LUT	Bitwidth P0	Bitwidth P1
C_fu_311_p2	+	0	0	14	9	6
add_ln102_1_fu_420_p2	+	0	0	25	18	18
add_ln102_fu_429_p2	+	0	0	26	19	19
add_ln94_1_fu_293_p2	+	0	0	29	22	22
add_ln94_fu_262_p2	+	0	0	29	22	22
x_4_fu_232_p2	+	0	0	23	16	1
y_2_fu_283_p2	+	0	0	23	16	1
icmp_ln100_fu_354_p2	icmp	0	0	8	2	1
icmp_ln101_fu_500_p2	icmp	0	0	8	2	1
icmp_ln102_fu_445_p2	icmp	0	0	8	3	1
icmp_ln89_fu_227_p2	icmp	0	0	13	16	16
icmp_ln92_fu_278_p2	icmp	0	0	13	16	16
or_ln100_fu_384_p2	or	0	0	2	1	1
or_ln101_fu_530_p2	or	0	0	2	1	1
or_ln102_fu_477_p2	or	0	0	2	1	1
B_fu_483_p3	select	0	0	8	1	8
G_fu_536_p3	select	0	0	8	1	8
R_fu_390_p3	select	0	0	8	1	8
select_ln100_fu_376_p3	select	0	0	2	1	2
select_ln101_fu_522_p3	select	0	0	2	1	2
select_ln102_fu_469_p3	select	0	0	2	1	2
D_fu_335_p2	xor	0	0	9	8	9
E_fu_321_p2	xor	0	0	9	8	9
Total		23	0	0	273	186	175

- **Multiplexer**

Name	LUT	Input Size	Bits	Total Bits
ap_NS_fsm	59	11	1	11
x_fu_114	9	2	16	32
y_reg_208	9	2	16	32
Total	77	15	33	75

- **Register**

Name	FF	LUT	Bits	Const Bits

B_reg_689	8	0	8	0
D_reg_661	8	0	8	0
G_reg_694	8	0	8	0
R_reg_679	8	0	8	0
add_ln100_reg_672	18	0	18	0
add_ln94_reg_609	14	0	22	8
ap_CS_fsm	10	0	10	0
x_4_reg_604	16	0	16	0
x_fu_114	16	0	16	0
y_2_reg_617	16	0	16	0
y_reg_208	16	0	16	0
zext_ln94_1_reg_622	22	0	64	42
Total	160	0	210	50

Interface

- **Summary**

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
ap_clk	in	1	ap_ctrl_hs	yuv2rgb.1	return value
ap_rst	in	1	ap_ctrl_hs	yuv2rgb.1	return value
ap_start	in	1	ap_ctrl_hs	yuv2rgb.1	return value
ap_done	out	1	ap_ctrl_hs	yuv2rgb.1	return value
ap_idle	out	1	ap_ctrl_hs	yuv2rgb.1	return value
ap_ready	out	1	ap_ctrl_hs	yuv2rgb.1	return value
ap_return_0	out	16	ap_ctrl_hs	yuv2rgb.1	return value
ap_return_1	out	16	ap_ctrl_hs	yuv2rgb.1	return value
in_channels_ch1_address0	out	22	ap_memory	in_channels_ch1	array
in_channels_ch1_ce0	out	1	ap_memory	in_channels_ch1	array
in_channels_ch1_q0	in	8	ap_memory	in_channels_ch1	array
in_channels_ch2_address0	out	22	ap_memory	in_channels_ch2	array
in_channels_ch2_ce0	out	1	ap_memory	in_channels_ch2	array
in_channels_ch2_q0	in	8	ap_memory	in_channels_ch2	array
in_channels_ch3_address0	out	22	ap_memory	in_channels_ch3	array
in_channels_ch3_ce0	out	1	ap_memory	in_channels_ch3	array
in_channels_ch3_q0	in	8	ap_memory	in_channels_ch3	array
p_read	in	16	ap_none	p_read	scalar
p_read1	in	16	ap_none	p_read1	scalar
out_channels_ch1_address0	out	22	ap_memory	out_channels_ch1	array
out_channels_ch1_ce0	out	1	ap_memory	out_channels_ch1	array
out_channels_ch1_we0	out	1	ap_memory	out_channels_ch1	array
out_channels_ch1_d0	out	8	ap_memory	out_channels_ch1	array
out_channels_ch2_address0	out	22	ap_memory	out_channels_ch2	array
out_channels_ch2_ce0	out	1	ap_memory	out_channels_ch2	array
out_channels_ch2_we0	out	1	ap_memory	out_channels_ch2	array
out_channels_ch2_d0	out	8	ap_memory	out_channels_ch2	array
out_channels_ch3_address0	out	22	ap_memory	out_channels_ch3	array
out_channels_ch3_ce0	out	1	ap_memory	out_channels_ch3	array
out_channels_ch3_we0	out	1	ap_memory	out_channels_ch3	array
out_channels_ch3_d0	out	8	ap_memory	out_channels_ch3	array