

ECE4810J SoC Design

Fall 2022

Lab #0 Getting to know Xilinx Arty Z7 & Vivado

Due: 11:59pm Sunday Sept. 18th, 2022

Please Submit a PDF file on Canvas

1 Xilinx Arty Z7 Platform

The Arty Z7 is a ready-to-use development platform designed around the Zynq-7000™ All Programmable System-on-Chip (AP SoC) from Xilinx. It will be used as the main SoC platform for this course throughout the semester. In this assignment, you will be assigned to read several documents about this board and the SoC. Please answer the questions below and submit through canvas. Note that this is an **individual** lab assignment.

References:

1. Read about Arty Z7 reference manual <https://digilent.com/reference/programmable-logic/arty-z7/start>
2. Zynq datasheet (go to Canvas > Files > Reading Materials > Zynq > ds187-XC7Z010-XC7Z020-Data-Sheet.pdf
or
<https://jicanvas.com/courses/43/files/594>
3. The Zynq Book (go to Canvas > Files > Reading Materials > Zynq > The_Zynq_Book_ebook_3.pdf
or
<http://www.zynqbook.com/>)

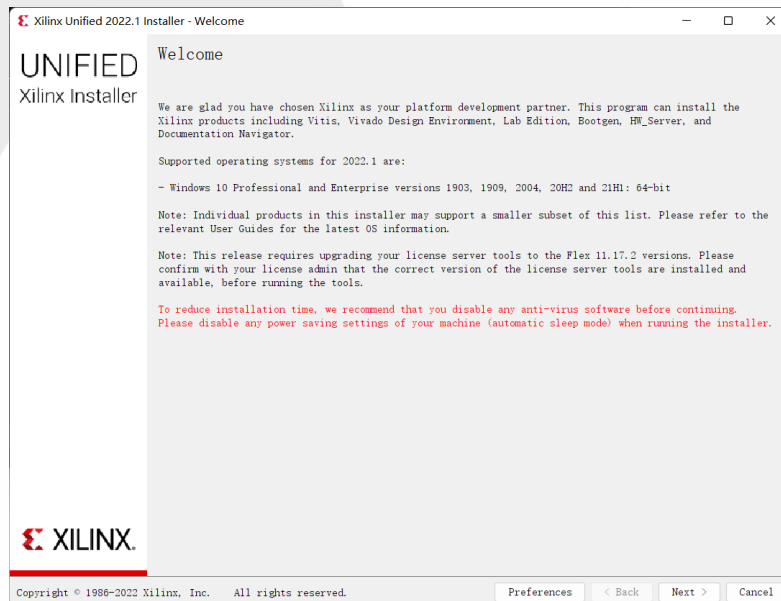
Questions:

1. (10%) What are the benefits of having Programmable logic on Zynq?
2. (20%) How many cores does Zynq-7000 have? What are the names of those cores? What does the memory hierarchy look like? What is the main CPU frequency?
3. (15%) Please list the main interfaces of the Zynq-7000 AP SoC device.
4. (5%) How is the Arty Z7 board powered?
5. (10%) What is the Quad SPI Flash? What is its usage on this board?
6. (10%) What is DDR Memory? What is its usage?
7. (20%) What are the main custom IP blocks creation methods Xilinx provides?
8. (10%) What is High-Level Synthesis (HLS)? What are the motivations behind HLS?

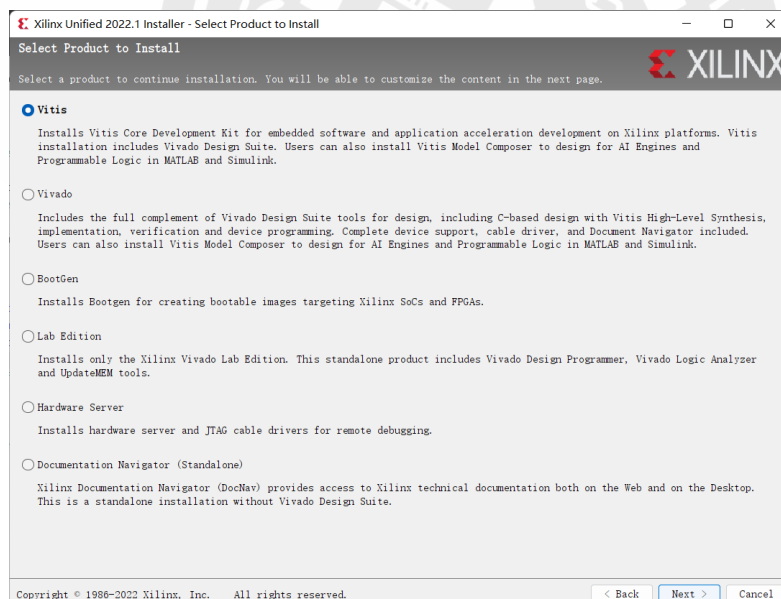
2 Installing Vivado Vitis for the first time

Xilinx Vitis Installation Guide: [Installing Vivado, Vitis, and Digilent Board Files](#)

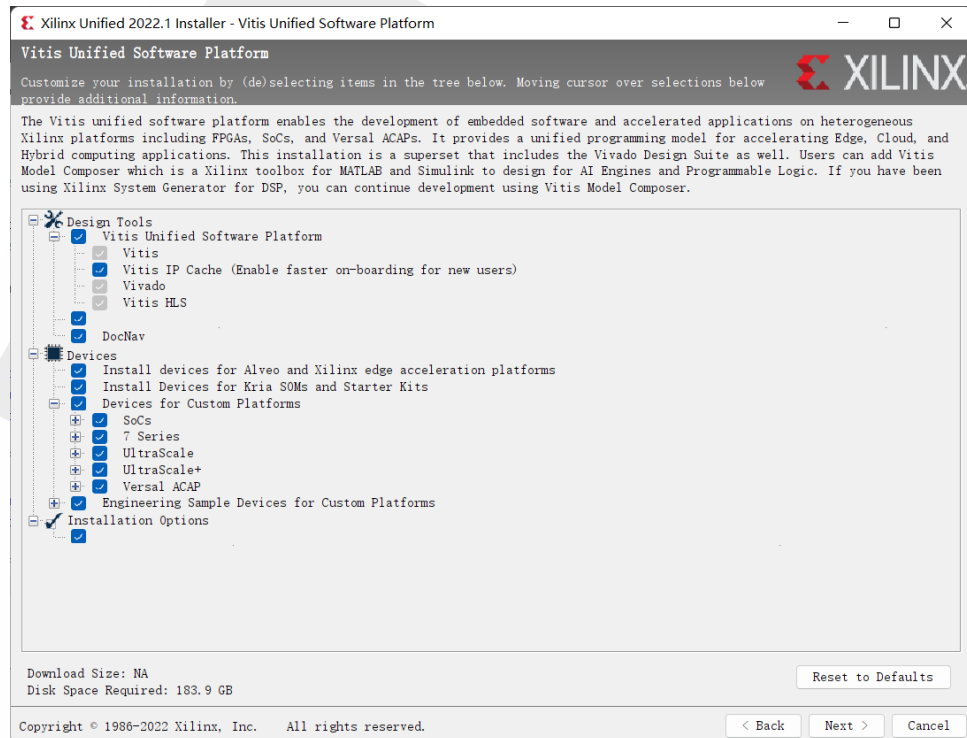
- Visit <https://china.xilinx.com/support/download/index.html/content/xilinx/zh/downloadNav/vitis.html>.
- Uninstall previous versions of Vitis or Vivado. Download Xilinx Unified Installer 2022.1 SFD (TAR/GZIP - 73.81 GB). Extract the zipped file.
- Under folder Xilinx_Unified_2022.1_0420_0327, run xsetup.exe:



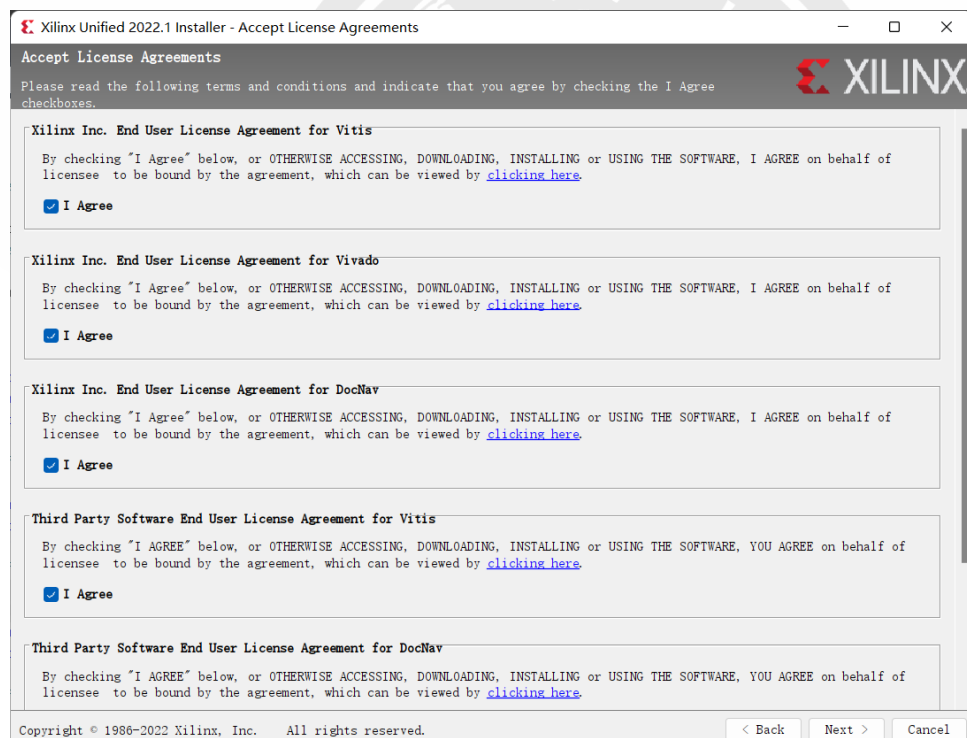
- Click Next:



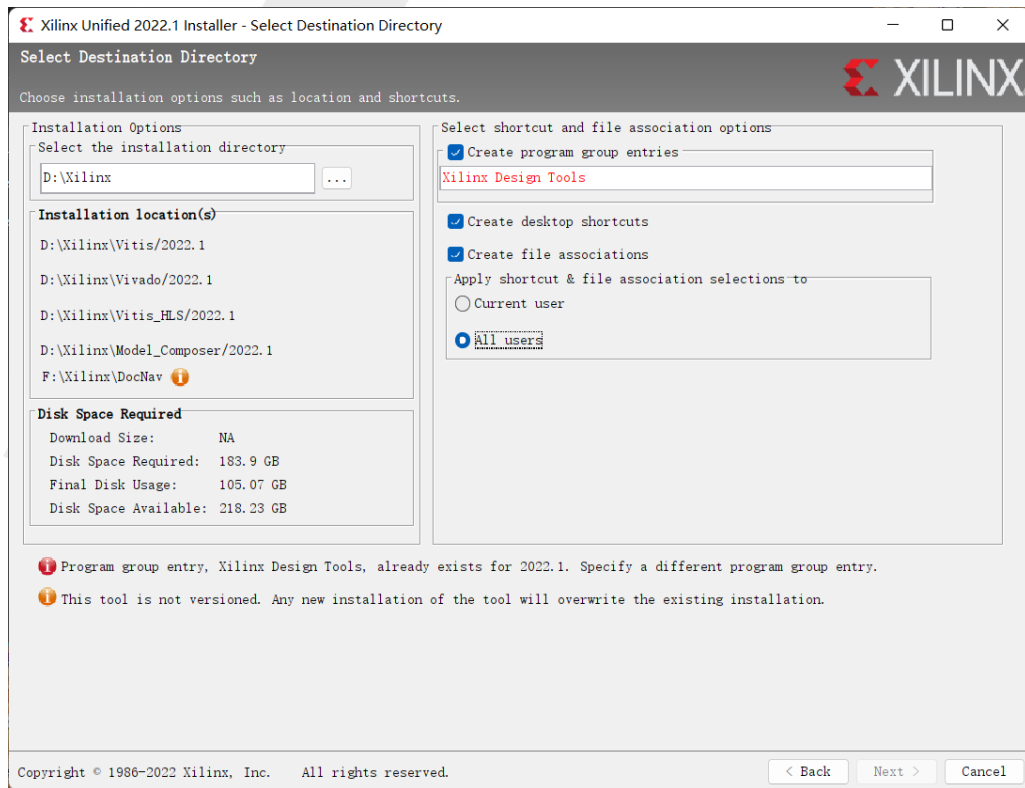
- Click Next. Select all (for Devices for Custom Platforms, at least select SoCs and UltraScale+):



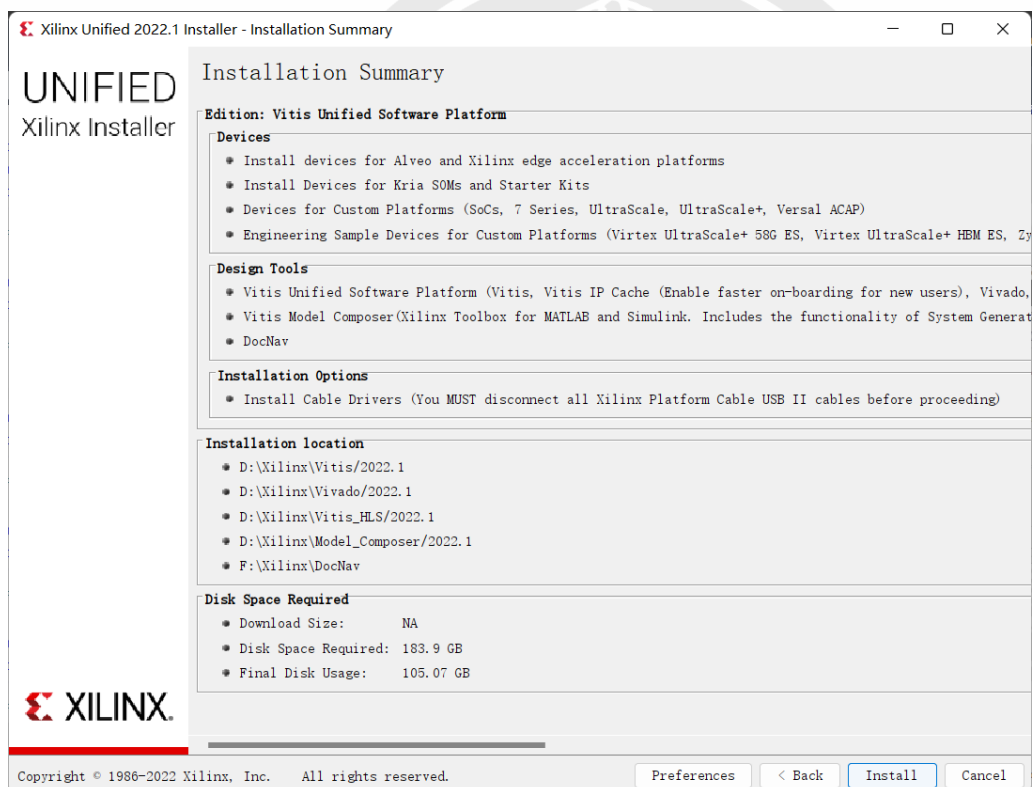
- Click Next. Check "I Agree" for all:



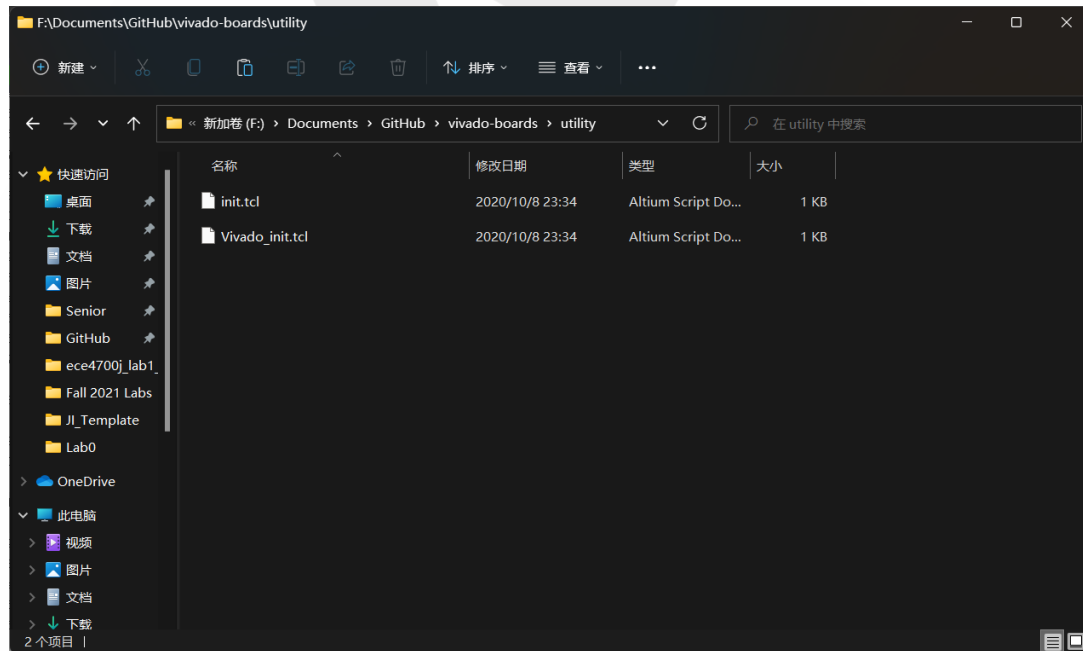
- Select the installation directory:



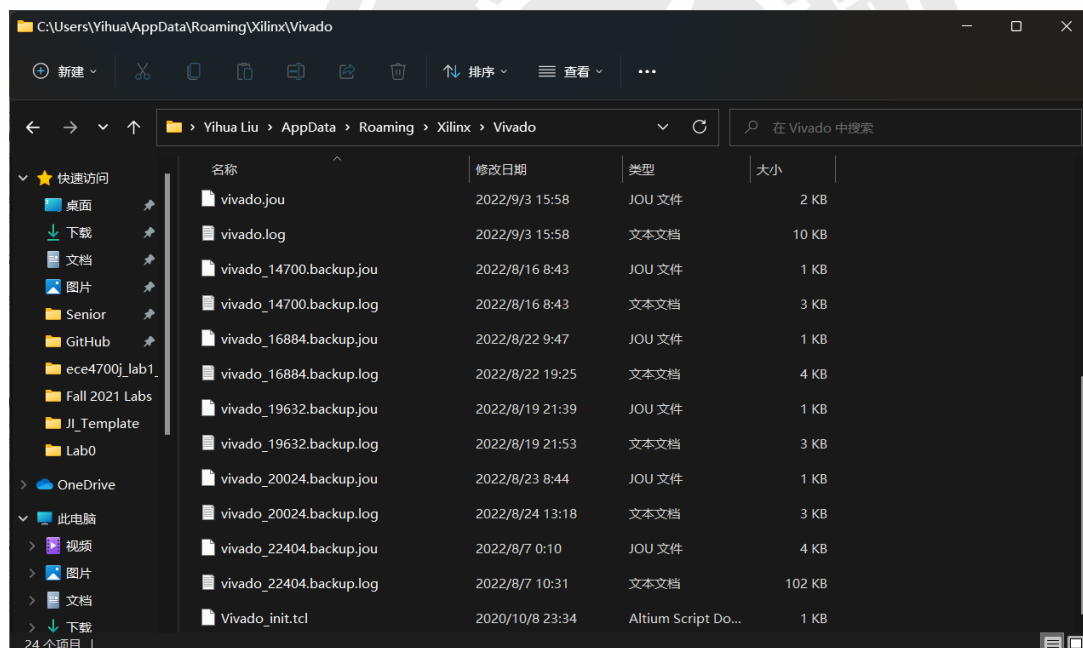
- Click Install:



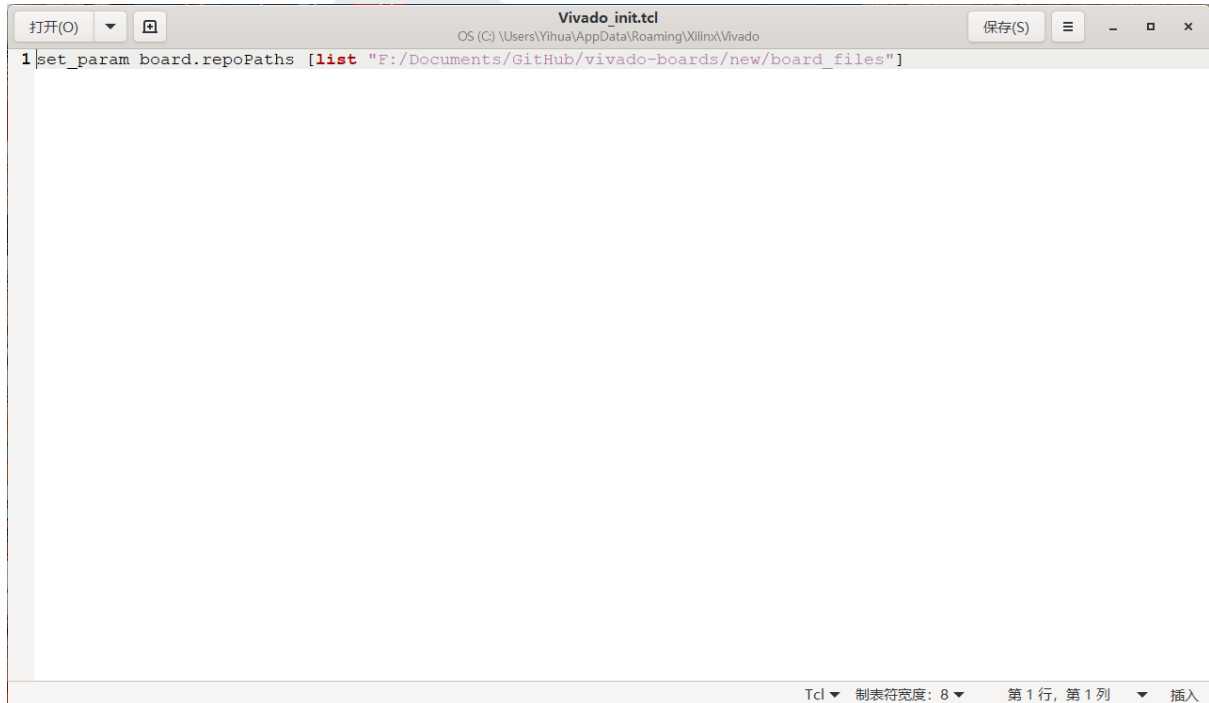
- Download Xilinx Unified 2022.1.2 : All OS installer Single-File Download (TAR/GZIP - 56.25 GB). Extract the zipped file.
- Under folder Xilinx_Vivado_Vitis_Update_2022.1.2_0806_0242, run xsetup.exe.
- Install the update.
- Clone the board files repository from [Digilent/vivado-boards](https://github.com/Digilent/vivado-boards).



- Copy vivado-boards/utility/Vivado_init.tcl and paste it into the %APPDATA%/Xilinx/Vivado/ directory.



- Open the copied init script in a text editor. Change the text <extracted path> in the script to the path to the extracted vivado-boards folder. Save and close the file.



- Check in Vivado:

