ECE4810J SoC Design

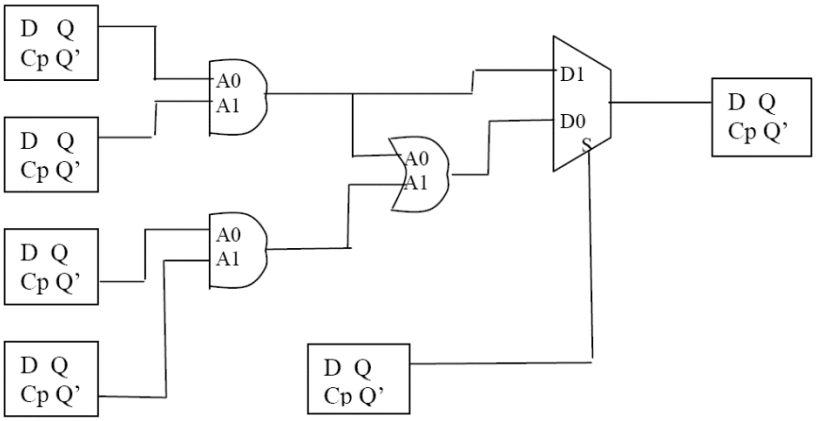
Fall 2022

HW #3

Due: 11:59pm November 25th, 2022

Please Submit a PDF file on Canvas

Q1 (20%): The purpose of this question is to give you some practice on timing calculations, as discussed in class. Consider the circuit shown below.



Answer the following questions, using the data given below:

- Clock skew = 750 ps
- T_clock_Q = (300 : 450 : 950) ps in (**min:typ:max**)
- AND delay = (70 : 120 : 210) ps
- OR delay = (50 : 110 : 200) ps
- Mux delay from D0 or D1 = (40 : 90 : 180) ps
- Mux delay from S = (30 : 80 : 170) ps
- T_setup = (100 : 200 : 300) ps
- T_hold = (200 : 300 : 400) ps

1) (10%) What is the fastest possible clock that allows worst-case circuits to work correctly without setup violations?

2) (10%) Is there potential for a hold violation? Show your work instead of just answering yes or no.

Q2 (20%): A processor die (1.4 cm × 1.4 cm) will be produced for five years. Over this period, defect densities are expected to drop linearly from 0.5 defects/cm^2 to 0.1 defects/cm^2. The cost of 20 cm wafer production will fall linearly from $5,000 to $3,000, and the cost of 30 cm wafer production will fall linearly from $10,000 to $6,000. Assume production of good devices is constant in each year. Which production process should be chosen and why?

Q3 (20%): In the class, we discussed about using rbe model as the basic measure to estimate area. Assume that we have an Xilinx Virtex XC2V6000 FPGA, which includes 33792 slices of logic. Each slice is around 700rbe. Each slice also has its associated logic element (LE), each of this LE is taking 1200rbe.

Unit	Relative Size
λ mask registration	
f minimum feature size	$f = 2\lambda$
rbe register bit equivalent	$rbe = 2700\lambda^2 = 675 f^2$
A functional unit area	$A = 10^6 f^2 = 1481$ rbe

1) (10%) If the feature size is 14nm, then what is the total area of this FPGA in mm^2?

2) (10%) If there is an 8x8 multiplier mapped on this FPGA and takes around 35 slices of logic. While if we build this multiplier with ASIC approach, one bit of the multiplier will contain a full-adder and an AND gate, which in total will be counted as 3840 transistors. Now please compare the area difference between the ASIC approach vs. the reconfigurable version of the 8x8 multiplier. Which one is more efficient in terms of area?

Q4 (20%): Let's assume we have the following baseline SoC area model. The total area budget is 5200A.

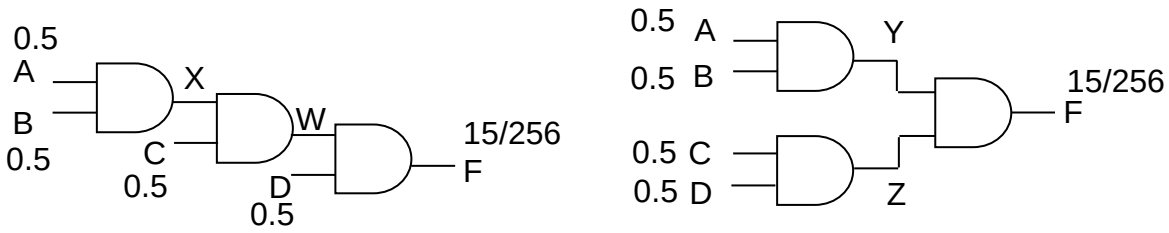
Unit	Area (*A*)
Core processor (32 b)	100
Core cache (24 KB)	96
Vector processor #1	200
Vector registers and cache #1	256 + 96
Vector processor #2	200
Vector registers and cache #2	352
Bus and bus control (50%)	650
Application memory (128 KB)	512

1) (10%) If we would like to use the remaining area for cache storage, and each bit is taking 1rbe. Then how big will be this cache in terms of byte?

2) (10%) If we consider to add more on chip storage with size of 3000A, this will blow out the area budget. In this case, you will have to increase the area budget. But there will be downsides too. Let's assume that this is a situation you (as a SoC designer) need to describe to your manager. Please list out at least 2 different pros and 3 cons regarding this area increase design decision.

Q5 (20%): Please answer the following two questions related to switching activity.

1) (10%) Show which circuit has lower switching activity (ignore glitching effects).



2) (10%) Show how input reordering can decrease switching activity.