ECE4810J SoC Design

Fall 2022

HW #1

Due: 11:59pm October 11th, 2022

Please Submit a PDF file on Canvas

Q1 (20%): For a chip product, the NRE cost and unit cost are the following for the four technologies:

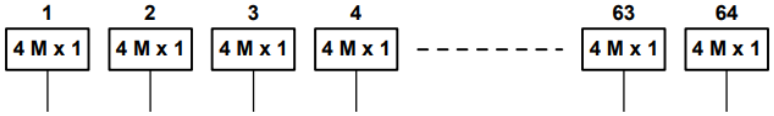
Technology	NRE Expense	Unit Cost
Semi-custom VLSI	$200,000	$5
ASIC	$50,000	$10
FPGA	$15,000	$20
Microcontroller	$10,000	$15

1) (5%) Calculate total per-unit cost for production volume of 100, 1k, 10k and 100k units.
2) (5%) Plot these data in a single graph and determine the best choice of technologies for these production volumes to achieve the lowest per-unit cost.
3) (5%) Determine the range of production volumes for which each of these technologies is financially optimal.

Q2 (15%): Assume that we have 4 different processors on a SoC, each does 25% of the application. If we improve two of the processors by 10 times, what would be the overall application speedup?

Q3 (15%): A SoC uses 4-Megabit memory chips and a 64-bit data bus. Draw a diagram and show the minimum number of memory chips we can use for each of the following chip configurations. What is the resulting minimum amount of memory (in bytes) we can use in a system for each chip configuration?
a. 4 Meg x 1
b. 1 Meg x 4
c. 256K x 16

Example diagram:



Q4 (15%): Hardware Acceleration, please answer the following questions based on your understandings.

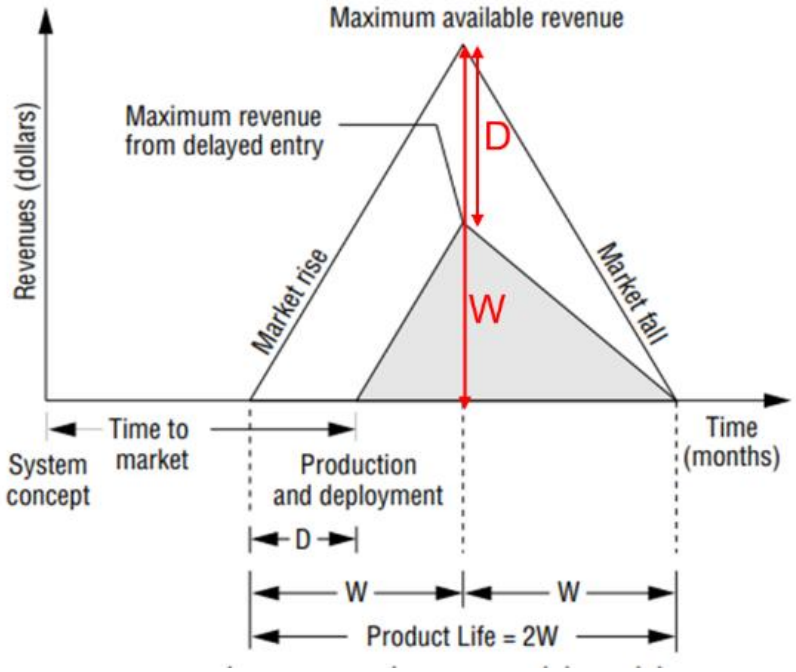
1) You are designing a SoC using an Intel Xeon processor (host). Does it make sense to add an accelerator to implement the function z = ax + by + c? Explain.

2) You are designing a SoC using a CPU core with no floating-point support. Does it make sense to add an accelerator to implement the floating-point function? Explain.

3) You are designing a SoC using a high-performance embedded processor with a floating point unit. Does it make sense to add an accelerator to implement the floating-point function? Explain.

Q5 (10%): Consider two approaches of doubling the number of transistors on a SoC: halving the size of a single transistor while maintaining constant die area (Moore's Law) versus maintaining the size of a single transistor while doubling the die area. List some reasons why the first approach is superior to the second approach.

Q6 (15%): In one of our lectures, we introduced the SoC profit model in the following. The lifetime of a SoC product is 2W. Assume 2W = 52 weeks. What will be the percentage revenue loss when the delay D is 4-week? How about delaying for 10 weeks? What conclusions can you draw from this study?



Q7 (10%): Based on readings, please list at least three downside or design challenges of reconfigurable technology.