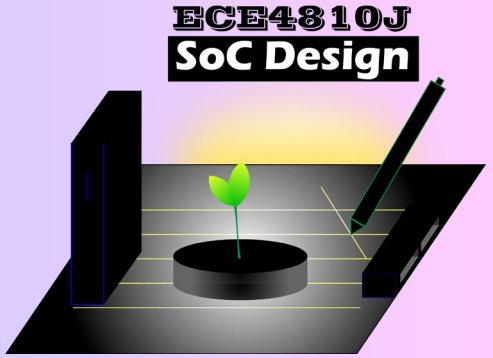
JOINT INSTITUTE
交大密西根学院

Final Project
FPGA Flow & ASIC Flow

ECE4810J System-on-Chip Design



Yihua Liu
UM-SJTU Joint Institute
ayka_tsuzuki@sjtu.edu.cn
Nov. 14, 2022

Overview

JOINT INSTITUTE
交大密西根学院

① Overview

② Schedule

③ Grading Policy

④ FPGA Flow

⑤ ASIC Flow

⑥ Reference

Schedule

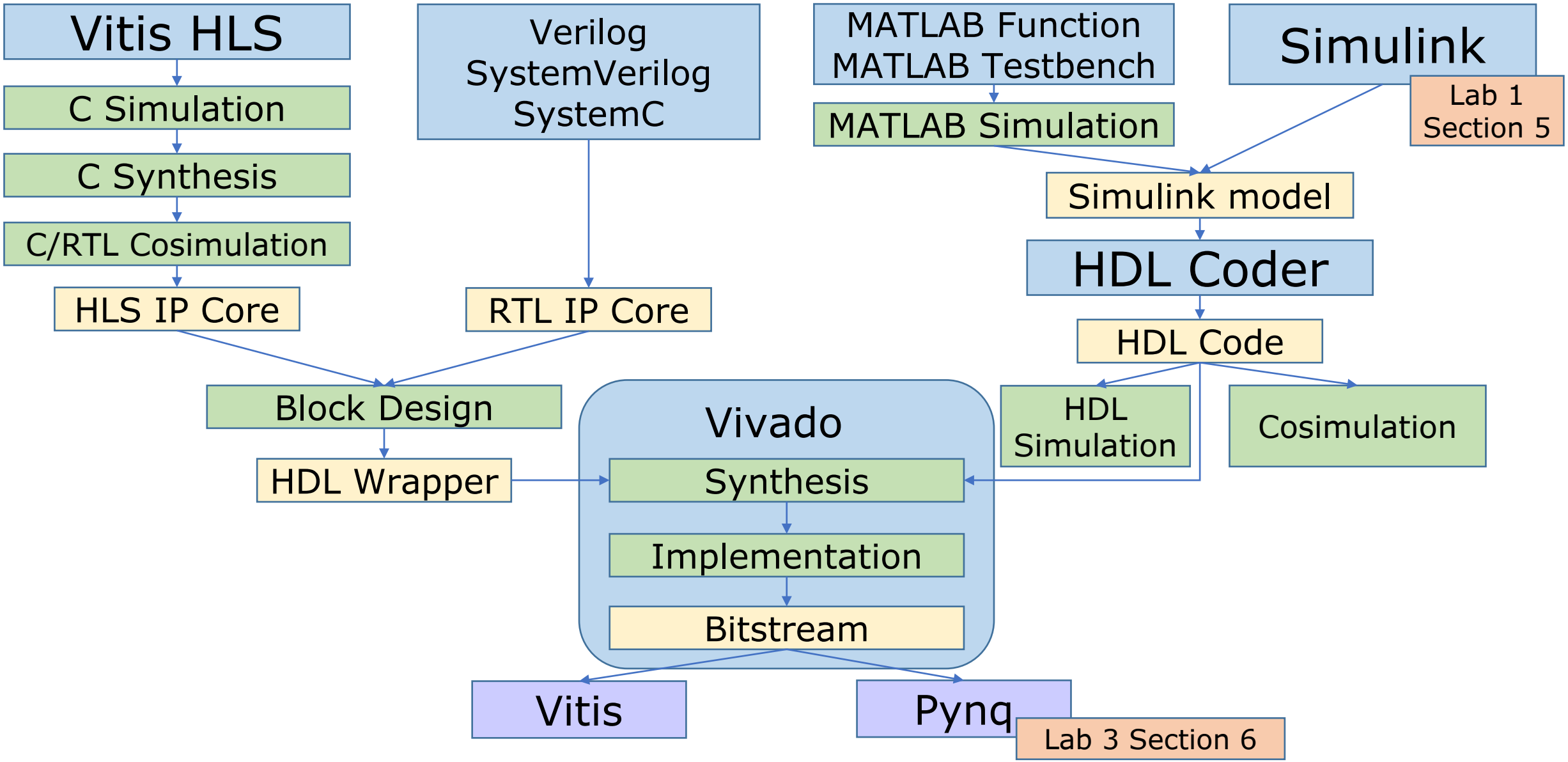
Date	Task
Nov. 14, 2022	Lab 6 continues (offline)
Nov. 15, 2022	Final Project Introduction (online)
Nov. 16, 2022	Final Project Topic Decision
Dec. 1, 2022	Milestone Check
Dec. 8, 2022	Presentation
Dec. 14, 2022	Report, Deliverables, and Slides

Grading Policy

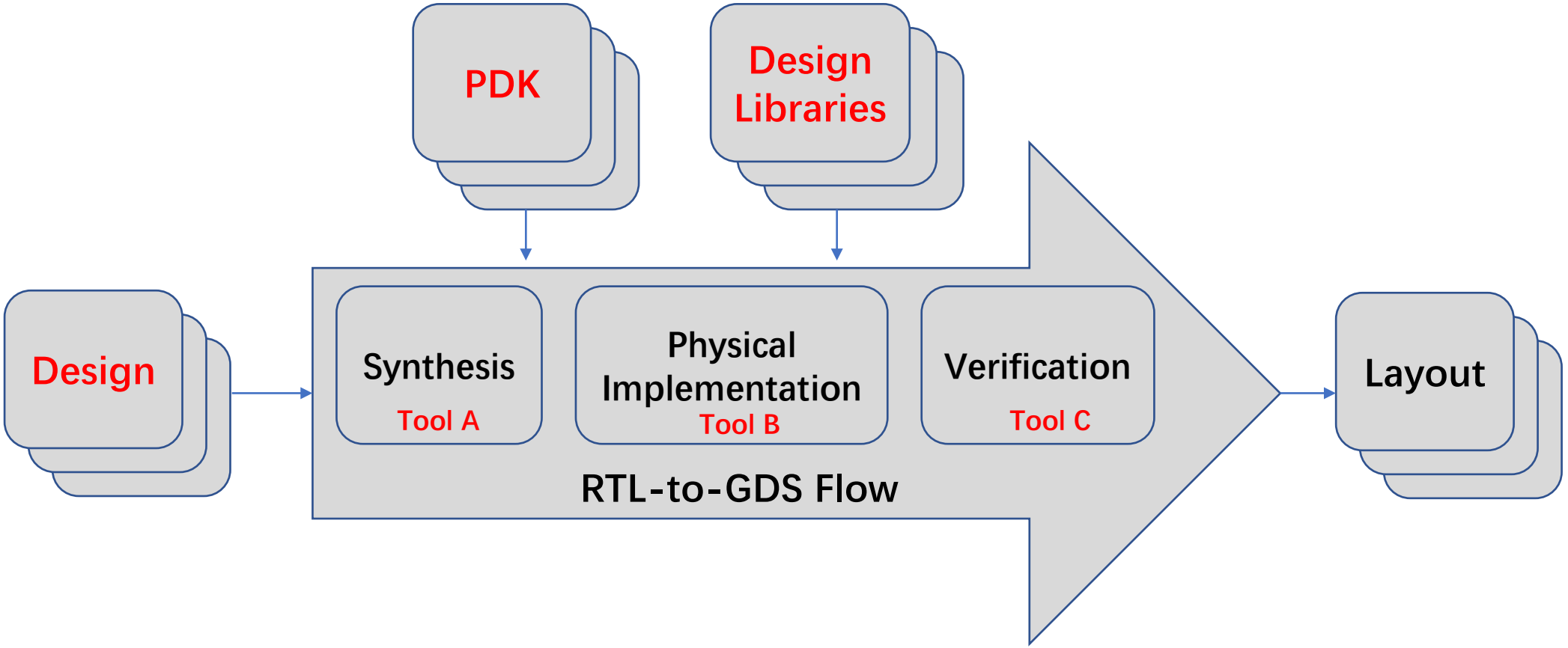
- Milestone Check
- Presentation & slides
- Report & documentation
- Implementation of base features
- Correctness and testing
- Performance optimization
- Analysis
- Additional features (upto 15% bonus)

Some seemingly easy topic can be difficult, vice versa

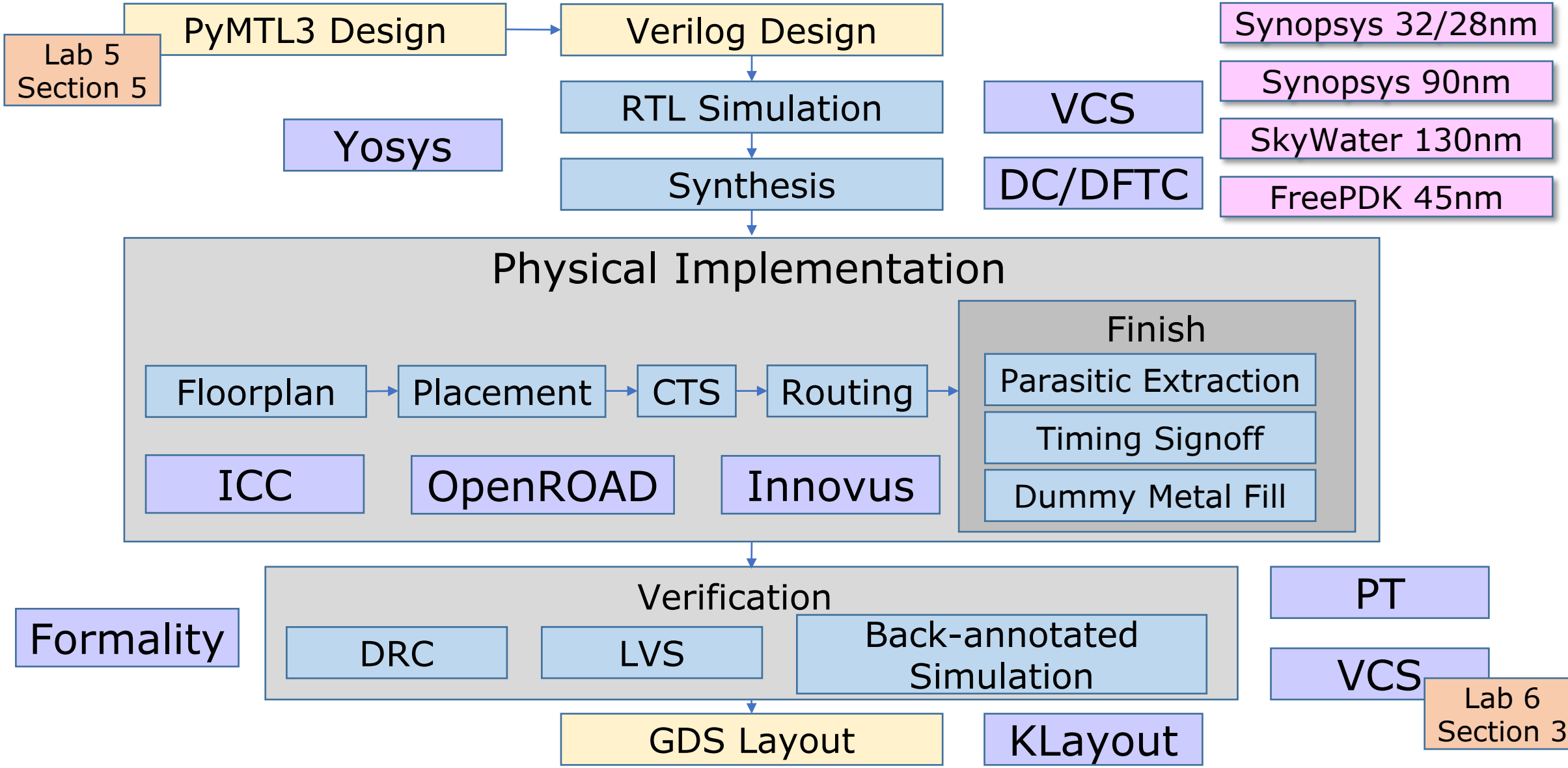
FPGA Flow


Vitis HLS
C Simulation
C Synthesis
C/RTL Cosimulation
HLS IP Core
Verilog
SystemVerilog
SystemC
RTL IP Core
MATLAB Function
MATLAB Testbench
MATLAB Simulation
Simulink
Lab 1
Section 5
Simulink model
HDL Coder
HDL Code
HDL
Simulation
Cosimulation
Block Design
HDL Wrapper
Vivado
Synthesis
Implementation
Bitstream
Vitis
Pynq
Lab 3 Section 6

ASIC Flow


PDK
Design Libraries
Design
Synthesis
Tool A
Physical Implementation
Tool B
Verification
Tool C
RTL-to-GDS Flow
Layout

ASIC Flow


PyMTL3 Design
Lab 5
Section 5
Verilog Design
RTL Simulation
Synthesis
Yosys
VCS
DC/DFTC
Synopsys 32/28nm
Synopsys 90nm
SkyWater 130nm
FreePDK 45nm
Physical Implementation
Floorplan
Placement
CTS
Routing
Finish
Parasitic Extraction
Timing Signoff
Dummy Metal Fill
ICC
OpenROAD
Innovus
Verification
DRC
LVS
Back-annotated
Simulation
Formality
PT
VCS
Lab 6
Section 3
GDS Layout
KLayout

Reference

① Austin Rovinski, Tutu Ajayi, and Christopher Batten. “OpenROAD Tutorial: Open-Source ASIC Design for Computer Architects”. Oct. 1, 2022.