
UM-SJTU Joint Institute

Introduction to Computer Organization (VE370)

VE370 Project 3 Simulation Results

Name	Yihua Liu	SID	518021910998
Name	Yiqi Sun	SID	518370910142
Name	Ruge Xu	SID	518370910165

Date: November 26, 2020

WinBox debugger interface showing a memory dump. The top panel displays assembly instructions: `read_r 0`, `add_0 200`, `int_1 000000ff`, `ht 0`, and `rea_0 8c159095`. The main panel shows a memory dump starting at address 0x00000000, with values 000, 200, 000, 200, and 200. The bottom panel shows a memory dump starting at address 0x8c159095, with values 47e808f3, 47e808ff, 8c159095, 47e808ff, 274f8004, and 8c159095. A yellow vertical line is positioned at the 50,000 ns mark on the timeline.

```
Tcl Console
```

```
Completed static elaboration
Starting simulation data flow analysis
Completed simulation data flow analysis
Time resolution for simulation is 1ps
Compiling module xil_defaultlib.Wesory
Compiling module xil_defaultlib.CacheA
Compiling module xil_defaultlib.sisla
Compiling module xil_defaultlib.glbl
Built simulation snapshot sisla_behav
INFO: [USF-XSia-09] 'elaborate' step finished in '3' seconds
INFO: [USF-XSia-4] XSia::Simulate design
INFO: [USF-XSia-01] Executing 'SIMULATE' step in 'D:/Documents/GitHub/VES70_FA2020/Project_3/1_a/1_a.sis/1_a/behav/xsia'
INFO: [USF-XSia-90] *** Running xsia
      with args "sisla_behav -key {Behavioral:sisla_1:Functional:sisla_1} -tclbatch {sisla.tcl} -log {simulate.log}"
INFO: [USF-XSia-0] Loading simulator feature
Vivado Simulator 2020.1.1
Time resolution is 1 ps
source sisla.tcl
# set curr_wave [current_wave_config]
# if { [string length $curr_wave] == 0 } {
#   # if { [llength [get_objects]] > 0 } {
#     add_wave /
#     set_property needs_save false [current_wave_config]
#   } else {
#     send_msg_id AddWave:: WARNING "No top level signals found. Simulator will start without a wave window. If you want to open a wave window go to 'File->New Waveform Configuration' or type 'create_wave_config' in the TCL console."
#   }
# }
# run 1000ns

=====
memory[0] = 0x47f808ff, memory[1] = 0xa20d2ffe, memory[2] = 0r9eee98c8, memory[3] = 0x7952f774
=====
memory[0] = 0x47f808ff, memory[1] = 0xa20d2ffe, memory[2] = 0r9eee98c8, memory[3] = 0x7952f774
=====
Stop called at time : 90 ns : File "D:/Documents/GitHub/VES70_FA2020_P3/sisla.v" Line 65
INFO: [USF-XSia-90] XSia completed. Design snapshot 'sisla_behav' loaded.
INFO: [USF-XSia-97] XSia simulation ran for 1000ms
launch_simulation: Time (s): cpu = 00:00:03 ; elapsed = 00:00:09 . Memory (MB): peak = 1094.310 ; gain = 0.000
```

1

```
Tcl Console
```

```
Completed static elaboration
Starting simulation data flow analysis
Completed simulation data flow analysis
Time resolution for simulation is 1ps
Compiling module xil_defaultlib.Wesory
Compiling module xil_defaultlib.Cacheb
Compiling module xil_defaultlib.siaib
Compiling module xil_defaultlib.glbl
Built simulation snapshot siaib_behav
INFO: [USF-XSia-69] 'elaborate' step finished in '4' seconds
INFO: [USF-XSia-4] XSia::Simulate design
INFO: [USF-XSia-61] Executing 'SIMULATE' step in 'D:/Documents/GitHub/VES70_FA2020/Project_3/1_b/1_b.sia/sia_1/behav/xsia'
INFO: [USF-XSia-90] *** Running xsia
      with args "siaib_behav -key {Behavioral:sia_1:Functional:siaib} -tclbatch {siaib.tcl} -log {simulate.log}"
INFO: [USF-XSia-8] Loading simulator feature
Vivado Simulator 2020.1.1
Time resolution is 1 ps
source siaib.tcl
# set curr_wave [current_wave_config]
# if { [string length $curr_wave] == 0 } {
#   # if { [llength [get_objects]] > 0 } {
#     add_wave /
#     set_property needs_save false [current_wave_config]
#   } else {
#     send_msg_id Add_Wave:: WARNING "No top level signals found. Simulator will start without a wave window. If you want to open a wave window go to 'File->New Waveform Configuration' or type 'create_wave_config' in the Tcl console."
#   }
# }
# run 1000ns

=====
memory[0] = 0x47f808ff, memory[1] = 0xa20d2ffe, memory[2] = 0r9ee99c8, memory[3] = 0x7952f774
=====
memory[0] = 0x47f808ff, memory[1] = 0xa20d2ffe, memory[2] = 0r9ee99c8, memory[3] = 0x7952f774
=====
Stop called at time : 90 ns : File "D:/Documents/GitHub/VES70_FA2020_P3/siaib.v" Line 58
INFO: [USF-XSia-96] XSia completed. Design snapshot "siaib_behav" loaded.
INFO: [USF-XSia-97] XSia simulation ran for 1000ms

launch_simulation: Time (s) : cpu = 00:00:04 ; elapsed = 00:00:11 . Memory (MB) : peak = 1094.310 ; gain = 0.000
|
```

2

3 Direct mapped write back

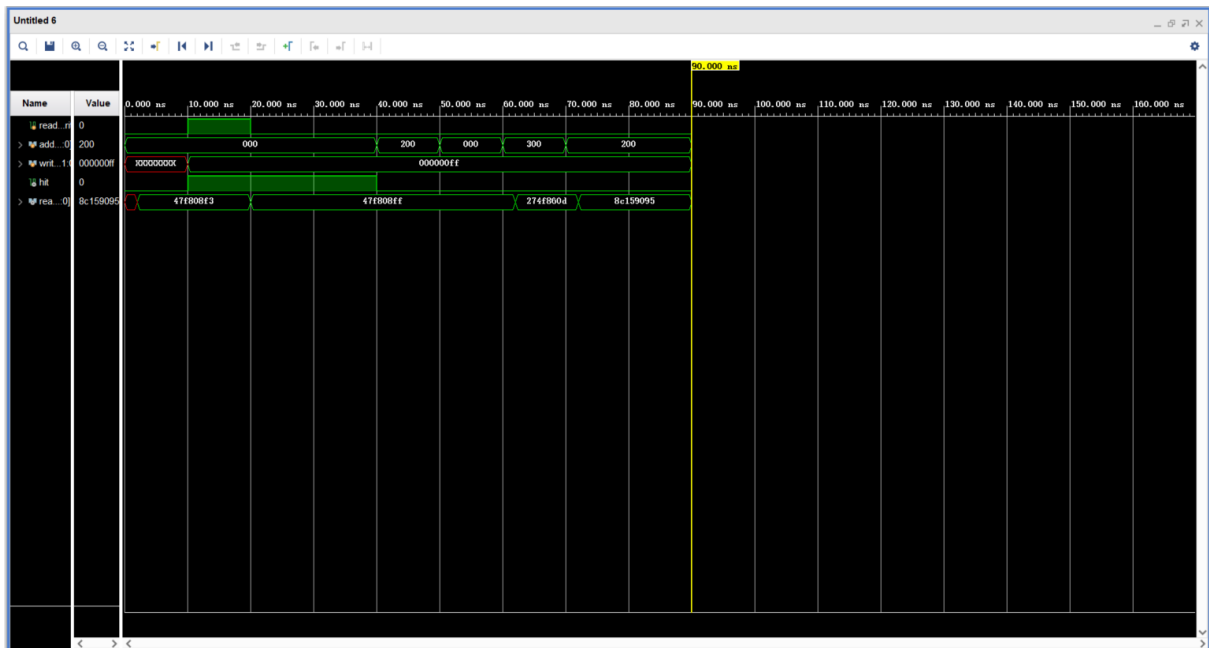


Figure 5. Graphical result.

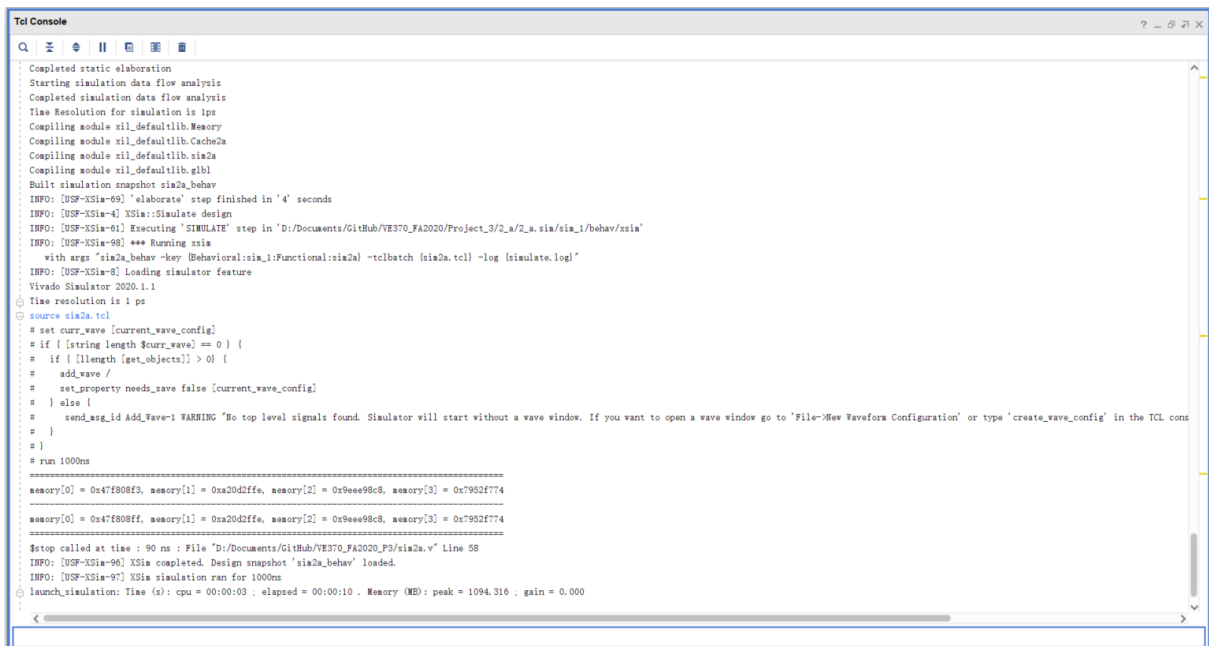


Figure 6. Textual result.

4 2-way associative write back

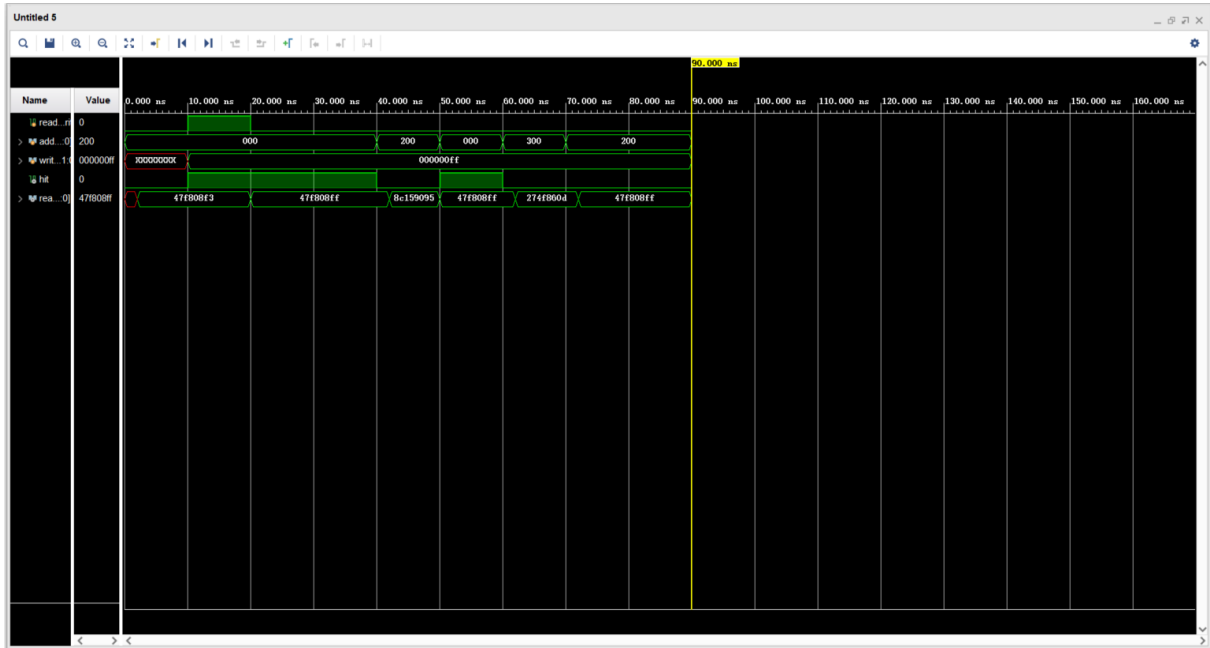


Figure 7. Graphical result.

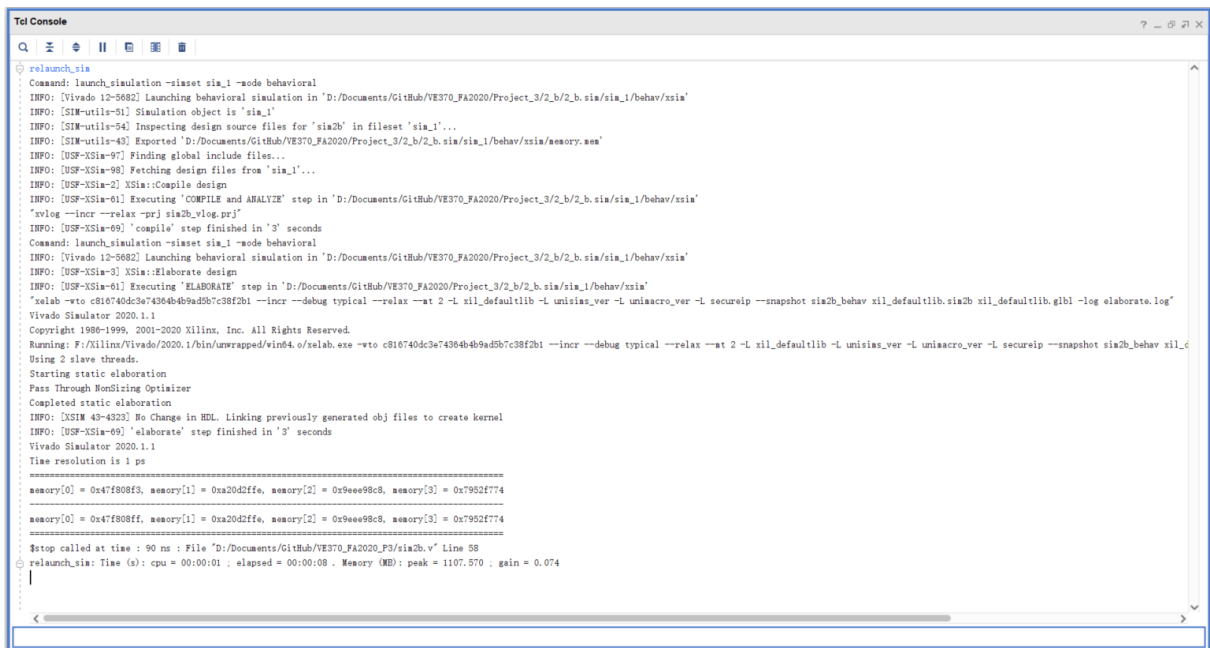


Figure 8. Textual result.