Yihua Liu

+86 15034078298 ayka_tsuzuki@sjtu.edu.cn GitHub CSDN Website

EDUCATION

Shanghai Jiao Tong University (SJTU), Shanghai, China **Sept. 2018 – Aug. 2022 (Expected)**
Bachelor of Science, Electrical and Computer Engineering
- Cumulative GPA: 3.2/4.0

Peter the Great St. Petersburg Polytechnic University (SPbPU), Saint Petersburg, Russia **Jan. 2020 – Feb. 2020**
International Polytechnic Winter School, Smart Manufacturing and Digital Future Project

RESEARCH EXPERIENCES

Design of Integrated Micro-robotic Fish, VE490 Undergraduate Research Program **Feb. 2021 – Apr. 2021**
Professor: Xuyang Lu, Assistant Professor at UM-SJTU Joint Institute
- Design and fabricate a microfluidic chip and channel
- Simulate and verify the performance of the chip by MATLAB and COMSOL Multiphysics

Optimization of Placement and Routing in VLSI, UM-SJTU JI Research Intern Program **May 2021 – Dec. 2021**
Professor: Xinfei Guo, Assistant Professor at UM-SJTU Joint Institute
- Pull request to DREAMPlace, deep learning toolkit-enabled VLSI placement

PROFESSIONAL HISTORY

Tongfang Co., Ltd., Beijing, China **Dec. 2019 – Jan. 2020**
Electrical Engineer Intern, Worked on the design of SCADA system of a thermal power company

SELECTED PROJECTS

MIPS Processor Design, VE370 Intro to Computer Organization **Nov. 2020**
- Project 2: Implement a five-stage pipeline with forwarding unit and hazard detection unit (Verilog & FPGA Demo)
- Project 3: Design caches both direct-mapped and 2-way-associative with write-through or write-back (Verilog)

VS Code Sidebar Multilingual Smart Reader Extension (vscode-covert-reader) **Dec. 2020 – Jan. 2021**

Gesture-Controlled Mantis Robot, VE373 Design of Microprocessor Based Systems **July 2021**
- Final Project: Build a gesture-controlled robot that can avoid obstacles using PIC32 MCU and Arduino

FIR Filter Implementation on FPGA, ECE4810J System-on-Chip Design **Nov. 2021 – Dec. 2021**
- Final Project: Simulation on MATLAB & Vivado, Verilog design, ZYNQ deployment on Arty Z7

Operating System Projects, VE482 Introduction to Operating Systems **Sept. 2021 – Dec. 2021**
- Project 1: mumsh shell, support redirection, pipes, quotes parsing, signals, background, error handling, etc.
- Project 2: lemondb multithreaded database
- Project 3: Minix 3.2.1 kernel lottery and EDF scheduling with keys and kernel params switching

Early-Exit Offloading for Embedded Question Answering Applications, ECE4730J Advanced Embedded System Capstone Design, leader & main contributor, repo: yihuajack/ECE4730J_FA2021 (github.com) **Oct. 2021 – Dec. 2021**
Entropy-based early-exit for PyTorch ALBERT model evaluated by SQuAD 2.0 on Jetson TX2 and VMware Bitfusion

HONORS & AWARDS

Best Technology Award of Project Design in the 2019 Summer Vg100 August 2019
2019-2020 The Excellent League Member of Shanghai Jiao Tong University May 2020
Student Development Scholarship of SJTU Joint Institute for 2019-2020 academic year June 2020
UM-SJTU Joint Institute 2020-2021 Undergraduate Excellent Scholarship November 2021

SKILLS & CERTIFICATION

English: TOEFL 97 (Reading: 30/Listening: 25/Speaking: 17/Writing: 25)
Languages: skilled in C/C++, LaTeX, MATLAB, Python; familiar with Linux Bash, Mathematica, MIPS assembly, TypeScript; basic knowledge of GNU Make/CMake, Lisp/Scheme, PostScript, SQL, TCL, etc.
Software: Capture CIS, COMSOL Multiphysics, KLayout, Multisim, Vitis, Vitis HLS, Vivado, Visio, etc.
Skills: Git, Linux, simple driver development, any editor/IDE (JetBrains, Vim, etc), usually using Windows/WSL/Ubuntu
Coursera: Python for Everybody, Machine Learning, Deep Learning, DeepLearning.AI TensorFlow Developer, GANs
Others: Opensource Contributions, Cppreference contributor, experiences in COMAP's Mathematical Contest in Modeling (MCM2019, MCM2020, MCM2021)