Chapter 24

Ethernet Media Access Controller (EMAC)

24.1 Overview

Features of Ethernet

By using the external Ethernet PHY (physical layer), ESP32 can send and receive data via Ethernet MAC (Media Access Controller) according to the IEEE 802.3 standard, as Figure 24.1-1 shows. Ethernet is currently the most commonly used network protocol that controls how data is transmitted over local- and wide-area networks, abbreviated as LAN and WAN, respectively.

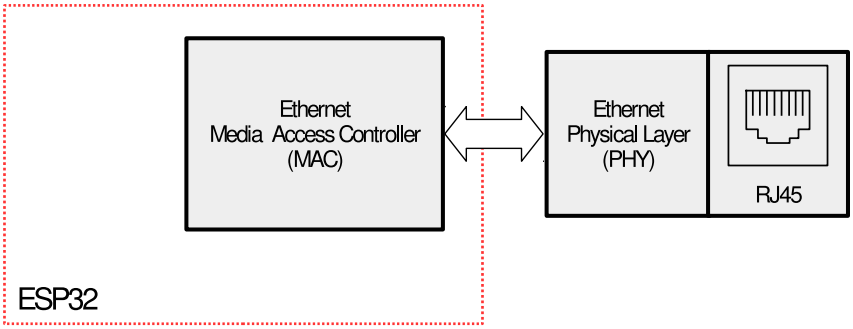

Figure 24.1-1. Ethernet MAC Functionality Overview

ESP32 MAC Ethernet complies with the following criteria:

- IEEE 802.3-2002 for Ethernet MAC
- Two industry-standard interfaces conforming with IEEE 802.3-2002: Media-Independent Interface (MII) and Reduced Media-Independent Interface (RMII).

Features of MAC Layer

- Support for a data transmission rate of 10 Mbit/s or 100 Mbit/s through an external PHY interface
- Communication with an external Fast Ethernet PHY through IEEE 802.3-compliant MII and RMII interfaces
- Support for:
  - Carrier Sense Multiple Access / Collision Detection (CSMA/CD) protocol in half-duplex mode
  - IEEE 802.3x flow control in full-duplex mode
  - operations in full-duplex mode, forwarding the received pause-control frame to the user application
  - backpressure flow control in half-duplex mode

  - If the flow control input signal disappears during a full-duplex operation, a pause frame with zero pause time value is automatically transmitted.

- The Preamble and the Start Frame Delimiter (SFD) are inserted in the Transmit path, and deleted in the Receive path.
- Cyclic Redundancy Check (CRC) and Pad can be controlled on a per-frame basis.
- The Pad is generated automatically, if data is below the minimum frame length.
- Programmable frame length supporting jumbo frames of up to 16 KB
- Programmable Inter-frame Gap (IFG) (40-96 bit times in steps of 8)
- Support for a variety of flexible address filtering modes:
  - Up to eight 48-bit perfect address filters to mask each byte
  - Up to eight 48-bit SA address comparison checks to mask each byte
  - All multicast address frames can be transmitted
  - All frames in mixed mode can be transmitted without being filtered for network monitoring
  - A status report is attached each time all incoming packets are transmitted and filtered
- Returning a 32-bit status for transmission and reception of packets respectively
- Separate transmission, reception, and control interfaces for the application
- Use of the Management Data Input/Output (MDIO) interface to configure and manage PHY devices
- Support for the offloading of received IPv4 and TCP packets encapsulated by an Ethernet frame in the reception function
- Support for checking IPv4 header checksums, as well as TCP, UDP, or ICMP (Internet Control Message Protocol) checksums encapsulated in IPv4/IPv6 packets in the enhanced reception function
- Two sets of FIFOs: one 2 KB Tx FIFO with programmable threshold and one 2 KB Rx FIFO with configurable threshold (64 bytes by default)
- When Rx FIFO stores multiple frames, the Receive Status Vector is inserted into the Rx FIFO after transmitting an EOF (end of frame), so that the Rx FIFO does not need to store the Receive Status of these frames.
- In store-and-forward mode, all error frames can be filtered during reception, but not forwarded to the application.
- Under-sized good frames can be forwarded.
- Support for data statistics by generating pulses for lost or corrupted frames in the Rx FIFO due to an overflow
- Support for store-and-forward mechanism when transmitting data to the MAC core
- Automatic re-transmission of collided frames during transmission (subject to certain conditions, see section 24.2.1.2)
- Discarding frames in cases of late collisions, excessive collisions, excessive deferrals, and under-run conditions

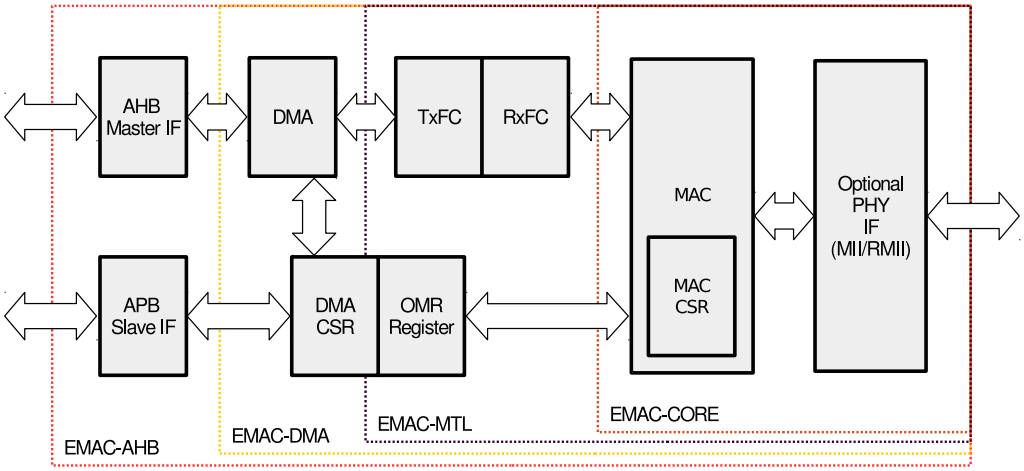

Figure 24.1-2. Ethernet Block Diagram

- The Tx FIFO is flushed by software control.
- Calculating the IPv4 header checksum, as well as the TCP, UDP, or ICMP checksum, and then inserting them into frames transmitted in store-and-forward mode.

Ethernet Block Diagram

Figure 24.1-2 shows the block diagram of the Ethernet.

Ethernet MAC consists of the MAC-layer configuration register module and three layers: EMAC_CORE (MAC Core Layer), EMAC_MTL (MAC Transition Layer), and EMAC_DMA (Direct Memory Access). Each of these three layers has two directions: Tx and Rx. They are connected to the system through the Advanced High-Performance Bus (AHB) and the Advanced Peripheral Bus (APB) on the chip. Off the chip, they communicate with the external PHY through the MII and RMII interfaces to establish an Ethernet connection.

24.2 EMAC_CORE

The MAC supports many interfaces with the PHY chip. The PHY interface can be selected only once after reset. The MAC communicates with the application side (DMA side), using the MAC Transmit Interface (MTI), MAC Receive Interface (MRI) and the MAC Control Interface (MCI).

24.2.1 Transmit Operation

A transmit operation is initiated when the MTL Application pushes in data at the time a response signal is asserted. When the SOF (start of frame) signal is detected, the MAC accepts the data and begins transmitting to the RMII or MII. The time required to transmit the frame data to the RMII or MII, after the application initiates transmission, varies, depending on delay factors like IFG delay, time to transmit Preamble or SFD (Start Frame Delimiter), and any back-off delays in half-duplex mode. Until then, the MAC does not accept the data received from MTL by de-asserting the ready signal.

After the EOF (end of frame) is transmitted to the MAC, the MAC completes the normal transmission and yields the Transmit Status to the MTL. If a normal collision (in half-duplex mode) occurs during transmission, the MAC makes valid the Transmit Status in the MTL. It then accepts and drops all further data until the next SOF is

received. The MTL block should retransmit the same frame from SOF upon observing a retry request (in the Status) from the MAC.

The MAC issues an underflow status if the MTL is not able to provide the data continuously during transmission. During the normal transmission of a frame from MTL, if the MAC receives an SOF without getting an EOF for the previous frame, it ignores the SOF and considers the new frame as a continuation of the previous one.

24.2.1.1 Transmit Flow Control

In full-duplex mode, when the Transmit Flow Control Enable bit (TFE bit in the Flow Control Register) is set to 1, the MAC will generate and send a pause frame, as needed. The pause frame is added and transmitted together with the calculated CRC. The generation of pause frames can be initiated in two ways.

When the application sets the Flow Control Busy bit (FCB bit in the Flow Control Register) to 1, or when the Rx FIFO is full, a pause frame is transmitted.

- If an application has requested flow control by setting the FCB bit in the Flow Control Register to 1, the MAC will generate and send a single pause frame. The pause time value in the generated frame is the pause time value programmed in the Flow Control Register. To extend or end the pause time before the time specified in the previously transmitted pause frame, the application program must configure the pause time value in the Flow Control Register to the appropriate value and, then, request another pause frame transmission.
- If the application has requested flow control when the Rx FIFO is full, the MAC will generate and transmit a pause frame. The value of the pause time of the generated frame is the pause time value programmed in the Flow Control Register. If the Rx FIFO remains full during the configurable interval, which is determined by the Pause Low Threshold bit (PLT) in the Flow Control Register before the pause time expires, a second pause frame will be transmitted. As long as the Rx FIFO remains full, the process repeats itself. If the FIFO is no longer full before the sample time, the MAC will send a pause frame with zero pause time, indicating to the remote end that the Rx buffer is ready to receive the new data frame.

24.2.1.2 Retransmission During a Collision

In half-duplex mode, a collision may occur on the MAC line interface when frames are transmitted to the MAC. The MAC may even give a status to indicate a retry before the end of the frame is received. The retransmission is then enabled and the frame is popped out from the FIFO. When more than 96 bytes are transmitted to the MAC core, the FIFO controller frees the space in the FIFO, allowing the DMA to push more data into FIFO. This means that data cannot be retransmitted after the threshold is exceeded or when the MAC core indicates that a late collision has occurred.

The MAC transmitter may abort the transmission of a frame because of collision, Tx FIFO underflow, loss of carrier, jabber timeout, no carrier, excessive deferral, and late collision. When frame transmission is aborted because of collision, the MAC requests retransmission of the frame.

24.2.2 Receive Operation

A receive operation is initiated when the MAC detects an SFD on the RMII or MII. The MAC strips the Preamble and SFD before processing the frame. The header fields are checked for the filtering and the FCS (Frame

Check Sequence) field used to verify the CRC for the frame. The received frame is stored in a shallow buffer until the address filtering is performed. The frame is dropped in the MAC if it fails the address filtering.

The frame received by the MAC will be pushed into the Rx FIFO. Once the FIFO status exceeds the Receive Threshold, configured by the Receive Threshold Control (RTC) bit in the Operation Mode register, the DMA can initiate a preconfigured burst transmission to the AHB interface.

In the default pass-through mode, when the FIFO receives a complete packet or 64 bytes configured by the RTC bit in the Operation Mode Register, the data pops up and its availability is notified to the DMA. After the DMA initiates the transmission to the AHB interface, the data transmission continues from the FIFO until the complete packet is transmitted. Upon completing transmitting the EOF, the status word will pop up and be transmitted to the DMA controller.

In the Rx FIFO Store-and-Forward mode (configured through the RSF or Receive Store and Forward bit in the Operation Mode Register), only the valid frames are read and forwarded to the application. In the passthrough mode, error frames are not discarded because the error status is received at the end of the frame. The start of frame will have been read from the FIFO at that point.

24.2.2.1 Reception Protocol

After the receive module receives the packets, the Preamble and SFD of the received frames are removed. When the SFD is detected, the MAC starts sending Ethernet frame data to the Rx FIFO, starting at the first byte (destination address) following the SFD.

If the received frame length/type is less than 0x600 and the automatic CRC/Pad removal option is programmed for the MAC, the MAC will send frame data to the Rx FIFO (the amount of data does not exceed the number specified in the length/type field). Then MAC begins discarding the remaining section, including the FCS field. If the frame length/type is greater than, or equal to, 0x600, the MAC will send all received Ethernet frame data to the Rx FIFO, regardless of the programmed value of the automatic CRC removal option. By default, the MAC watchdog timer is enabled, meaning that frames, including DA, SA, LT, data, pad and FCS, which exceed 2048 bytes, are cut off. This function can be disabled by programming the Watchdog Disable (WD) bit in the MAC Configuration Register. However, even if the watchdog timer is disabled, frames longer than 16 KB will be cut off and the watchdog timeout status will be given.

24.2.2.2 Receive Frame Controller

If the RA (Receive All) bit in the MAC Frame Filter Register is reset, the MAC will filter frames based on the destination and source addresses. If the application decides not to receive any bad frames, such as runt frames and CRC error frames, another level of filtering is needed. When a frame fails the filtering, the frame is discarded and is not transmitted to the application. When the filter parameters are changed dynamically, if a frame fails the DA and SA filterings, the remaining part of the frame is discarded and the Receive Status word is updated immediately and, therefore, the zero frame length bit, CRC error bit, and runt frame error bit are set to 1. This indicates that the frame has failed the filtering.

24.2.2.3 Receive Flow Control

The MAC will detect the received pause frame and pause transmission of frames for a specified delay within the received pause frame (in full-duplex mode only). The Pause Frame Detect Function can be enabled or disabled by the RFCE (Receive Flow Control Enable) bit in the Flow Control Register. When receive flow control is enabled, it starts monitoring whether the destination address of the received frame matches the

multicast address of the control frame (0x0180 C200 0001). If a match is detected (i.e. the destination address of the received frame matches the destination address of the reserved control frame), the MAC will determine whether to transmit the received control frame to the application, according to the PCF (Pass Control Frames) bit in the Frame Filter Register.

The MAC will also decode the type, the opcode, and the pause timer field of the Receive Control Frame. If the value of the status byte counter is 64 bits and there are no CRC errors, the MAC transmitter will halt the transmission of any data frame. The duration of the pause is the decoded pause time value multiplied by the interval (which is 64 bytes for both 10 Mbit/s and 100 Mb/s modes). At the same time, if another pause frame of zero pause time is detected, the MAC will reset the pause time to manage the new pause request.

If the type field (0x8808), the opcode (0x00001), and the byte length (64 bytes) of the received control frame are not 0x8808, 0x00001, and 64 bytes, respectively, or if there is a CRC error, the MAC will not generate a pause.

If a pause frame has a multicast destination address, the MAC filters the frame, according to the address matching.

For pause frames with a unicast destination address, the MAC checks whether the DA matches the content of the EMACADDR0 Register, and whether the Unicast Pause Frame Detect (UPFD) bit in the Flow Control Register is set to 1. The Pass Control Frames (PCF) bits in the Frame Filter Register [7:6] control the filtering of frames and addresses.

24.2.2.4 Reception of Multiple Frames

Since the status is available immediately after the data is received. Frames can be stored there, as long as the FIFO is not full.

24.2.2.5 Error Handling

If the Rx FIFO is full before receiving the EOF data from the MAC, an overflow will be generated and the entire frame will be discarded. In fact, status bit RDES0[11] will indicate that this frame is partial due to an overflow, and that it should be discarded.

If the function that corresponds to the Flush Transmit FIFO (FTF) bit and the Forward Undersized Good Frames (FUGF) bit in the Operation Mode Register is enabled, the Rx FIFO can filter error frames and runt frames. If the receive FIFO is configured to operate in store-and-forward mode, all error frames will be filtered and discarded.

In passthrough mode, if a frame's status and length are available when reading a SOF from the Rx FIFO, the entire error frame can be discarded. DMA can clear the error frame being read from the FIFO by enabling the Receive Frame Clear bit. The data transmission to the application (DMA) will then stop, and the remaining frames will be read internally and discarded. If FIFO is available, the transmission of the next frame will be initiated.

24.2.2.6 Receive Status Word

After receiving the Ethernet frames, the MAC outputs the receive status to the application. The detailed description of the receive status is the same as that which is configured by bit [31:0] in RDES0.

24.3 MAC Interrupt Controller

The MAC core can generate interrupts due to various events.

The interrupt register bits only indicate various interrupt events. To clear the interrupts, the corresponding status register and other registers must be read. An Interrupt Status Register describes the events that prompt the MAC core to generate interrupts. Each interrupt event can be prevented by setting the corresponding mask bit in the Interrupt Mask Register to 1. For example, if bit3 of the interrupt register is set high, it indicates that a magic packet or Wake-on-LAN frame has been received in Power-down mode. The PMT Control and Status register must be read to clear this interrupt event.

24.4 MAC Address Filtering

Address filtering will check the destination and source addresses of all received frames and report the address filtering status accordingly. For example, filtered frames can be identified either as multicast or broadcast.The address check, then, is based on the parameters selected by the application (Frame Filter Registers).

Physical (MAC) addresses are used for address checking during address filtering.

24.4.1 Unicast Destination Address Filtering

The MAC supports up to 8 MAC addresses for perfect filtering of unicast addresses. If a perfect filtering is selected (by resetting bit[1] in the Frame Filter Register), the MAC compares all 48 bits of the received unicast address with the programmed MAC address to determine if there is a match. By default, EMACADDR0 is always enabled, and the other addresses (EMACADDR0 ~ EMACADDR7) are selected by a separate enable bit. When the individual bytes of the other addresses (EMACADDR0 ~ EMACADDR7) are compared with the DA bytes received, the latter can be masked by setting the corresponding Mask Byte Control bit in the register to 1. This facilitates the DA group address filtering.

24.4.2 Multicast Destination Address Filtering

The MAC can be programmed to pass all multicast frames by setting the Pass All Multicast (PAM) bit in the Frame Filter Register to 1. If the PAM bit is reset, the MAC will filter multicast addresses, according to Bit[2] in the Frame Filter Register.

In perfect filtering mode, the multicast address is compared with the programmed MAC Destination Address Registers (EMACADDR0 ~ EMACADDR7). Group address filtering is also supported.

24.4.3 Broadcast Address Filtering

The MAC does not filter any broadcast frames in the default mode. However, if the MAC is programmed to reject all broadcast frames, which can happen by setting the Disable Broadcast Frames (DBF) bit in the Frame Filter Register to 1, all broadcast frames will be discarded.

24.4.4 Unicast Source Address Filtering

The MAC may also perform a perfect filtering based on the source address field of the received frame. By default, the Address Filtering Module (AFM) compares the Source Address (SA) field with the values

programmed in the SA register. By setting Bit[30] in the SA register to 1, the MAC Address Register (EMACADDR0 - EMACADDR7) can be configured to contain SA, instead of Destination Address (DA), for filtering. Group filtering with SA is also supported. If the Source Address Filter (SAF) enable bit in the Frame Filter Register is set to 1, the MAC discards frames that do not pass the SA filtering. Otherwise, the result of SA filtering is given as a status bit in the Receive Status word (Please refer to Table 24.8-5).

When the SAF enable bit is set to 1, the result of the SA filtering and DA filtering is AND'ed to determine whether or not to forward the frame. Any frame that fails to pass will be discarded. Frames need to pass both filterings in order to be forwarded to the application.

24.4.5 Inverse Filtering Operation

For both destination address (DA) and source address (SA) filtering, you can invert the results matched through the filtering at the final output. The inverse filtering of DA and SA are controlled by the DAIF and SAIF bits, respectively, in the Frame Filter Register. The DAIF bit applies to both unicast and multicast DA frames. When DAIF is set to 1, the result of unicast or multicast destination address filtering will be inverted. Similarly, when the SAIF bit is set to 1, the result of unicast SA filtering is reversed.

The following two tables summarize the destination address and source address filtering, based on the type of the frames received.

Table 24.4-1. Destination Address Filtering

Frame Type	PM	PF	DAIF	PAM	DB	DA Filter Result
Broadcast	1	X	X	X	X	Pass
	0	X	X	X	0	Pass
	0	X	X	X	1	Fail
Unicast	1	X	X	X	X	All frames pass.
	0	X	0	X	X	Pass when results of perfect/group filtering match.
	0	X	1	X	X	Fail when results of perfect/group filtering match.
	0	1	0	X	X	Pass when results of perfect/group filtering match.
	0	1	1	X	X	Fail when results of perfect/group filtering match.
Multicast	1	X	X	X	X	All frames pass.
	X	X	X	1	X	All frames pass.
	0	X	0	0	X	Pass when results of perfect/group filtering match and pause control frame is discarded, if PCF = 0x.
	0	1	0	0	X	Pass when results of perfect/group filtering match and pause control frame is discarded, if PCF = 0x.
	0	X	1	0	X	Fail when results of perfect/group filtering match and pause control frame is discarded, if PCF = 0x.
	0	1	1	0	X	Fail when results of perfect/group filtering match and pause control frame is discarded, if PCF = 0x.

The filtering parameters in the MAC Frame Filter Register described in Table 24.4-1 are as follows.

Parameter name:

PM: Pass All Multicast
PF: Perfect Filter
DAIF: Destination Address Inverse Filtering
PAM: Pass All Multicast
DB: Disable Broadcast Frames

Parameter setting:

1: Set
0: Cleared

Table 24.4-2. Source Address Filtering

Frame Type	PM	SAIF	SAF	Source Address Filter Operation
Unicast	1	X	X	Pass all frames
	0	0	0	Pass when results of perfect/group filtering match. Frames not passed are not discarded.
	0	1	0	Fail when results of perfect/group filtering match. Frames not passed are not discarded.
	0	0	1	Pass when results of perfect/group filtering match. Frames not passed are discarded.
	0	1	1	Fail when results of perfect/group filtering match. Frames not passed are discarded.

The filtering parameters in the MAC Frame Filter Register described in Table 24.4-2 are as follows.

Parameter name:

PM: Pass All Multicast
SAF: Source Address Filtering
SAIF: Source Address Inverse Filtering

Parameter setting:

1: Set
0: Cleared
X: Don't care

24.4.6 Good Transmitted Frames and Received Frames

A frame successfully transmitted is considered a "good frame". In other words, a transmitted frame is considered to be good, if the frame transmission is not aborted due to the following errors:

- Jabber timeout
- No carrier or loss of carrier
- Late collision
- Frame underflow
- Excessive deferral
- Excessive collision

The received frames are considered "good frames", if there are not any of the following errors:

- CRC error
- Runt frames (frames shorter than 64 bytes)
- Alignment error (in 10/100 Mbps modes only)
- Length error (non-type frames only)
- Frame size over the maximum size (for non-type frames over the maximum frame size only)

- MII_RXER input error

The maximum frame size depends on the frame type:

- The maximum size of untagged frames = 1518 bytes
- The maximum size of VLAN frames = 1522 bytes

24.5 EMAC_MTL (MAC Transaction Layer)

The MAC Transaction Layer provides FIFO memory to buffer and regulates the frames between the application system memory and the MAC. It also enables the data to be transmitted between the application clock domain and the MAC clock domains. The MTL layer has two data paths, namely the Transmit path and the Receive path. The data path for both directions is 32-bit wide and operates with a simple FIFO protocol.

24.6 PHY Interface

The DMA and the Host driver communicate through two data structures:

- Control and Status Registers (CSR)
- Descriptor lists and data buffers

For details please refer to Register Summary and Linked List Descriptors.

24.6.1 MII (Media Independent Interface)

Media Independent Interface (MII) defines the interconnection between MAC sublayers and PHYs at the data transmission rate of 10 Mbit/s and 100 Mbit/s.

24.6.1.1 Interface Signals Between MII and PHY

Interface signals between MII and PHY are shown in Figure 24.6-1.

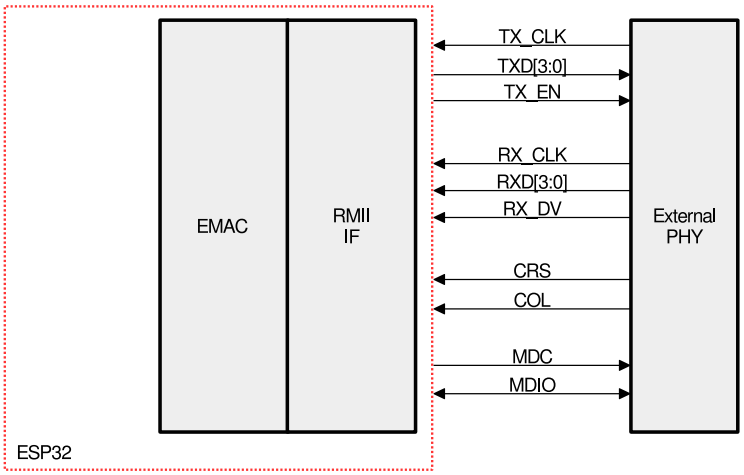

Figure 24.6-1. MII Interface

MII Interface Signal Description:

- MII_TX_CLK: TX clock signal. This signal provides the reference timing for TX data transmission. The frequencies are divided into two types: 2.5 MHz at a data transmission rate of 10 Mbit/s, and 25 MHz at 100 Mbit/s.
- MII_TXD[3:0]: Transmit data signal in groups of four, syn-driven by the MAC sub-layer, and valid only when the MII_TX_EN signal is valid. MII_TXD[0] is the lowest significant bit and MII_TXD[3] is the highest significant bit. When the signal MII_TX_EN is pulled low, sending data does not have any effect on the PHY.
- MII_TX_EN: Transmit data enable signal. This signal indicates that the MAC is currently sending nibbles (4 bits) for the MII. This signal must be synchronized with the first nibble of the header (MII_TX_CLK) and must be synchronized when all nibbles to be transmitted are sent to the MII.
- MII_RX_CLK: RX clock signal. This signal provides the reference timing for RX data transmission. The frequencies are divided into two types: 2.5 MHz at the data transmission rate of 10 Mbit/s, and 25 MHz at 100 Mbit/s.
- MII_RXD[3:0]: Receive data signal in groups of four, syn-driven by the PHY, and valid only when MII_RX_DV signal is valid. MII_RXD[0] is the lowest significant bit and MII_RXD[3] is the highest significant bit. When MII_RX_DV is disabled and MII_RX_ER is enabled, the specific MII_RXD[3:0] value represents specific information from the PHY.
- MII_RX_DV: Receive data valid signal. This signal indicates that the PHY is currently receiving the recovered and decoded nibble that will be transmitted to the MII. This signal must be synchronized with the first nibble of the recovered frame (MII_RX_CLK) and remain synchronized till the last nibble of the recovered frame. This signal must be disabled before the first clock cycle following the last nibble. In order to receive the frame correctly, the MII_RX_DV signal must cover the frame to be received over the time range, starting no later than when the SFD field appears.
- MII_CRS: Carrier sense signal. When the transmitting or receiving medium is in the non-idle state, the signal is enabled by the PHY. When the transmitting or receiving medium is in the idle state, the signal is disabled by the PHY. The PHY must ensure that the MII_CRS signal remains valid under conflicting conditions. This signal does not need to be synchronized with the TX and RX clocks. In full-duplex mode, this signal is insignificant.
- MII_COL: Collision detection signal. After a collision is detected on the medium, the PHY must immediately enable the collision detection signal, and the collision detection signal must remain active as long as a condition for collision exists. This signal does not need to be synchronized with the TX and RX clocks. In full-duplex mode, this signal is meaningless.
- MII_RX_ER: Receive error signal. The signal must remain for one or more cycles (MII_RX_CLK) to indicate to the MAC sublayer that an error has been detected somewhere in the frame.
- MDIO and MDC: Management Data Input/Output and Management Data Clock. The two signals constitute a serial bus defined for the Ethernet family of IEEE 802.3 standards, used to transfer control and data information to the PHY, see section Station Management Agent (SMA) Interface.

24.6.1.2 MII Clock

In MII mode, there are two directions of clock, Tx and Rx clocks in the interface between MII and the PHY. MII_TX_CLK is used to synchronize the TX data, and MII_RX_CLK is used to synchronize the RX data. The MII_RX_CLK clock is provided by the PHY. The MII_TX_CLK is provided by the chip's internal PLL or external

crystal oscillator. For details regarding Figure 24.6-2, please refer to the clock-related registers in Register Summary.

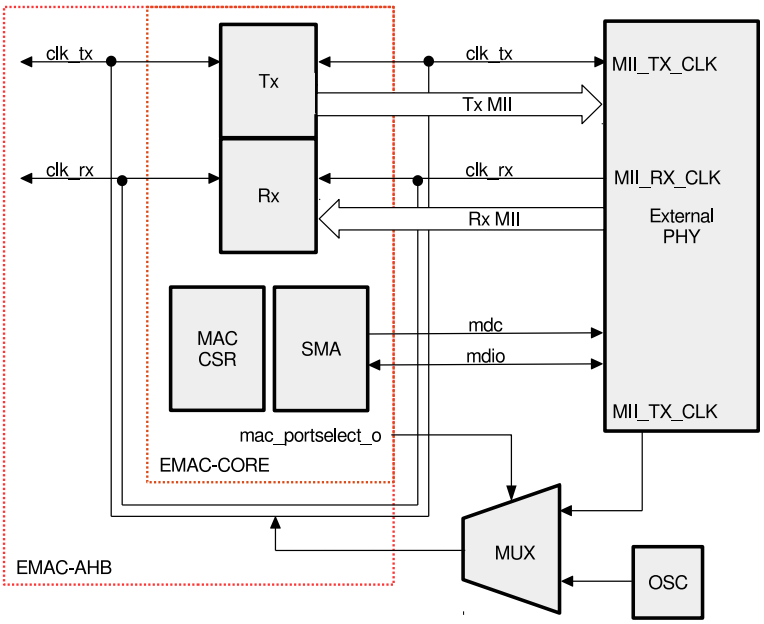

Figure 24.6-2. MII Clock

24.6.2 RMII (Reduced Media-Independent Interface)

RMII interface signals are shown in figure 24.6-3.

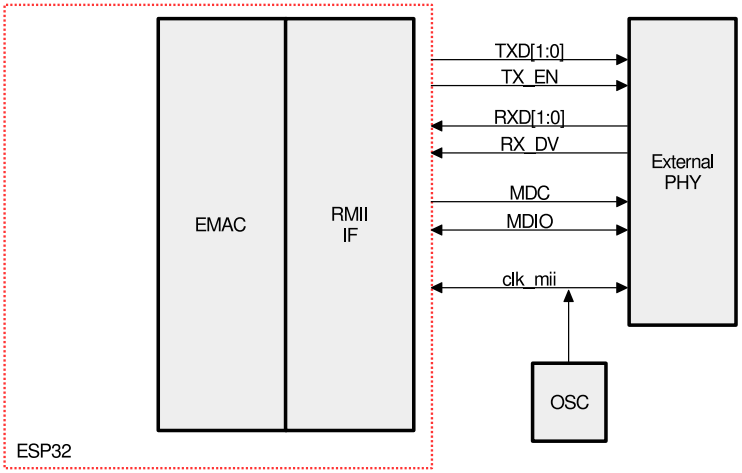

Figure 24.6-3. RMII Interface

24.6.2.1 RMII Interface Signal Description

The Reduced Media-Independent Interface (RMII) specification reduces the number of pins between the microcontroller's external peripherals and the external PHY at a data transmission rate of 10 Mbit/s or 100 Mbit/s. According to the IEEE 802.3u standard, MII includes 16 pins that contain data and control signals. The RMII specification reduces 62.5% of the pins to the number of seven.

RMII has the following features:

- Support for an operating rate of 10 Mbit/s or 100 Mbit/s
- The reference clock frequency must be 50 MHz.
- The same reference clock must be provided to the MAC and the external Ethernet PHY. The PHY provides independent 2-bit-wide TX and RX data paths.
- **Note:** If Wi-Fi and Ethernet are used simultaneously, the RMII clock cannot be generated by the internal APLL clock, as it would result in clock instability. In this case, please use an external PHY or external clock source to provide the reference clock.

24.6.2.2 RMII Clock

The configuration of the RMII clock is as figure 24.6-4 shows.

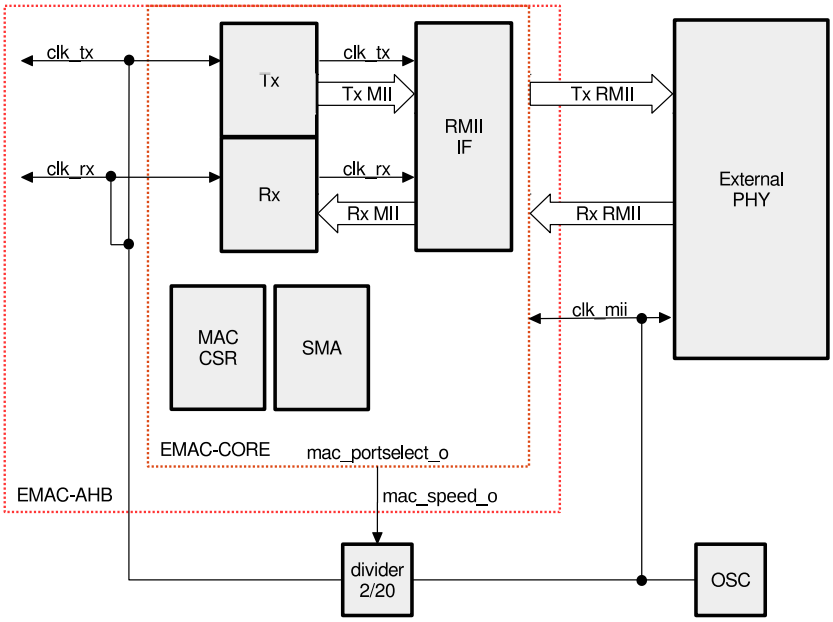

Figure 24.6-4. RMII Clock

24.6.3 Station Management Agent (SMA) Interface

As Figure 24.6-2 shows, the MAC uses MDC and MDIO signals to transfer control and data information to the PHY. The maximum clock frequency is 2.5 MHz. The clock is generated from the application clock by a clock divider. The PHY transmits register data during a write/read operation through the MDIO. This signal is driven synchronously to the MDC clock.

Please refer to Register Summary for details about the EMII Address Register and the EMII Data Register.

24.6.4 RMII Timing

This section describes the RMII timing specifications.

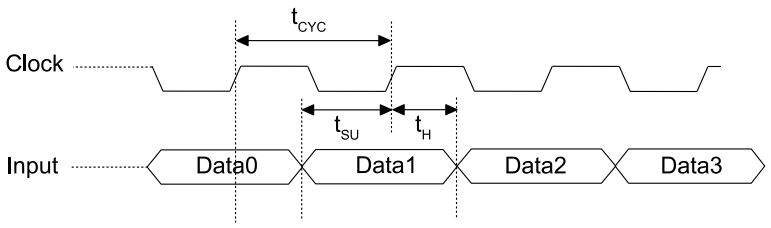

Figure 24.6-5. RMII Timing - Receiving Data

Table 24.6-1. Timing Parameters - Receiving Data

Timing Parameters	Description	Min	Typ	Max	Unit
t_{CYC}	Clock cycle	20	20	20	ns
t_{SU}	Setup time	4	–	–	ns
t_{H}	Hold time	1	–	–	ns
t_{ID}	Input delay	3	5	8	ns

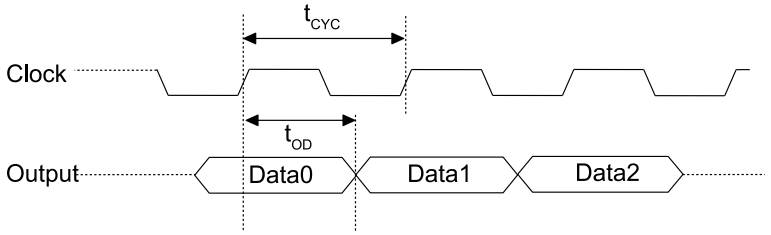

Figure 24.6-6. RMII Timing – Transmitting Data

Table 24.6-2. Timing Parameters – Transmitting Data

Timing Parameters	Description	Min	Typ	Max	Unit
t_{CYC}	Clock cycle	20	20	20	ns
t_{SU}	Setup time	4	–	–	ns
t_{H}	Hold time	1	–	–	ns
t_{OD}	Output delay	6	9	12	ns

24.7 Ethernet DMA Features

The DMA has independent Transmit and Receive engines, and a CSR (Control and Status Registers) space. The Transmit engine transfers data from the system memory to the device port (MTL), while the Receive engine transmits data from the device port to the system memory. The controller uses descriptors to efficiently move data from source to destination with minimal Host CPU intervention. The DMA is designed for packet-oriented data transmission, such as frames in Ethernet. The controller can be programmed to interrupt the Host CPU for normal situations, such as the completion of frame transmission or reception, or when errors occur.

24.8 Linked List Descriptors

This section shows the structure of the linked lists and the descriptors. Every linked list consists of eight words.

24.8.1 Transmit Descriptors

The structure of the transmitter linked lists is shown in Figure 24.8-1. Table 24.8-1 to Table 24.8-4 show the description of the linked lists.

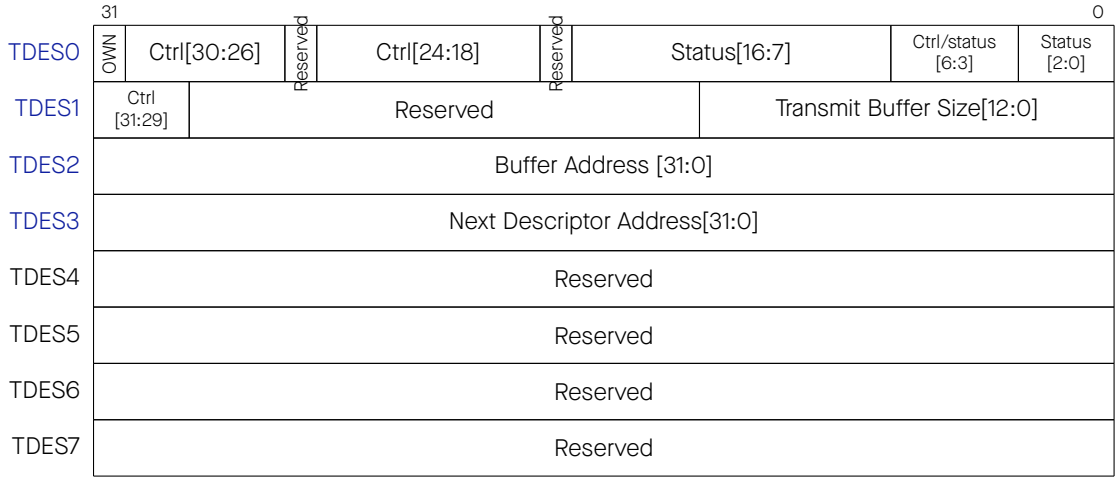

Figure 24.8-1. Transmit Descriptor

Table 24.8-1. Transmit Descriptor 0 (TDES0)

Bits	Name	Description
[31]	OWN: Own Bit	When set, this bit indicates that the descriptor is owned by the DMA. When this bit is reset, it indicates that the descriptor is owned by the Host. The DMA clears this bit, either when it completes the frame transmission or when the buffers allocated to the descriptor are empty. The ownership bit of the First Descriptor of the frame should be set after all subsequent descriptors belonging to the same frame have been set. This avoids a possible race condition between fetching a descriptor and the driver setting an ownership bit.
[30]	IC: Interrupt on Completion	When set, this bit sets the Transmit Interrupt (Register 5[0]) after the present frame has been transmitted. This bit is valid only when the last segment bit (TDES0[29]) is set.
[29]	LS: Last Segment	When set, this bit indicates that the buffer contains the last segment of the frame. When this bit is set, the TBS1 or TBS2 field in TDES1 should have a non-zero value.
[28]	FS: First Segment	When set, this bit indicates that the buffer contains the first segment of a frame.

Bits	Name	Description
[27]	DC: Disable CRC	When this bit is set, the MAC does not append a cyclic redundancy check (CRC) to the end of the transmitted frame. This is valid only when the first segment (TDES0[28]) is set.
[26]	DP: Disable Pad	When set, the MAC does not automatically add padding to a frame shorter than 64 bytes. When this bit is reset, the DMA automatically adds padding and CRC to a frame shorter than 64 bytes, and the CRC field is added despite the state of the DC (TDES0[27]) bit. This is valid only when the first segment (TDES0[28]) is set.
[25]	Reserved	Reserved
[24]	CRCR: CRC Replacement Control	When set, the MAC replaces the last four bytes of the transmitted packet with recalculated CRC bytes. The host should ensure that the CRC bytes are present in the frame being transmitted from the Transmit Buffer. This bit is valid when the First Segment control bit (TDES0[28]) is set. In addition, CRC replacement is done only when Bit TDES0[27] is set to 1.
[23:22]	CIC: Checksum Insertion Control	These bits control the checksum calculation and insertion. The following list describes the bit encoding: • 2'b00: Checksum insertion is disabled. • 2'b01: Only IP header checksum calculation and insertion are enabled. • 2'b10: IP header checksum and payload checksum calculation and insertion are enabled, but pseudo-header checksum is not calculated in hardware. • 2'b11: IP Header checksum and payload checksum calculation and insertion are enabled, and pseudo-header checksum is calculated in hardware. This field is valid when the First Segment control bit (TDES0[28]) is set.
[21]	TER: Transmit End of Ring	When set, this bit indicates that the descriptor list reached its final descriptor. The DMA returns to the base address of the list, creating a Descriptor Ring.
[20]	TCH: Second Address Chained	When set, this bit indicates that the second address in the descriptor is the Next Descriptor address, rather than the second buffer address. When TDES0[20] is set, TBS2 (TDES1[28:16]) is a "don't care" value. TDES0[21] takes precedence over TDES0[20]. This bit should be set to 1.

Bits	Name	Description
[19:18]	VLIC: VLAN Insertion Control	When set, these bits request the MAC to perform VLAN tagging or untagging before transmitting the frames. If the frame is modified for VLAN tags, the MAC automatically recalculates and replaces the CRC bytes. The following list describes the values of these bits: • 2'b00: Do not add a VLAN tag. • 2'b01: Remove the VLAN tag from the frames before transmission. This option should be used only with the VLAN frames. • 2'b10: Insert a VLAN tag with the tag value programmed in VLAN Tag Inclusion or Replacement Register. • 2'b1: Replace the VLAN tag in frames with the Tag value programmed in VLAN Tag Inclusion or Replacement Register. This option should be used only with the VLAN frames.
[17]	Reserved	Reserved
[16]	IHE: IP Header Error	When set, this bit indicates that the MAC transmitter detected an error in the IP datagram header. The transmitter checks the header length in the IPv4 packet against the number of header bytes received from the application, and indicates an error status if there is a mismatch. For IPv6 frames, a header error is reported if the main header length is not 40 bytes. Furthermore, the Ethernet Length/Type field value for an IPv4 or IPv6 frame must match the IP header version received with the packet. For IPv4 frames, an error status is also indicated if the Header Length field has a value less than 0x5.
[15]	ES: Error Summary	Indicates the logical OR of the following bits: • TDES0[14]: Jabber Timeout • TDES0[13]: Frame Flush • TDES0[11]: Loss of Carrier • TDES0[10]: No Carrier • TDES0[9]: Late Collision • TDES0[8]: Excessive Collision • TDES0[2]: Excessive Deferral • TDES0[1]: Underflow Error • TDES0[16]: IP Header Error • TDES0[12]: IP Payload Error
[14]	JT: Jabber Timeout	When set, this bit indicates the MAC transmitter has experienced a jabber timeout. This bit is only set when EMACCONFIG_REG's bit EMACJABBER is not set.
[13]	FF: Frame Flushed	When set, this bit indicates that the DMA or MTL flushed the frame because of a software Flush command given by the CPU.

Bits	Name	Description
[12]	IPE: IP Payload Error	When set, this bit indicates that MAC transmitter detected an error in the TCP, UDP, or ICMP IP datagram payload. The transmitter checks the payload length received in the IPv4 or IPv6 header against the actual number of TCP, UDP, or ICMP packet bytes received from the application, and issues an error status in case of a mismatch.
[11]	LOC: Loss of Carrier	When set, this bit indicates that a loss of carrier occurred during frame transmission (that is, the MII_CRS signal was inactive for one or more transmit clock periods during frame transmission). This is valid only for the frames transmitted without collision when the MAC operates in the half-duplex mode.
[10]	NC: No Carrier	When set, this bit indicates that the Carrier Sense signal from the PHY was not asserted during transmission.
[9]	LC: Late Collision	When set, this bit indicates that frame transmission is aborted because of a collision occurring after the collision window (64 byte-times including Preamble in MII mode, and 512 byte-times including Preamble and Carrier Extension). This bit is not valid if the Underflow Error bit is set.
[8]	EC: Excessive Collision	When set, this bit indicates that the transmission was aborted after 16 successive collisions while attempting to transmit the current frame. If bit EMACRETRY of EMACCONFIG_REG is set, this bit is set after the first collision, and the transmission of the frame is aborted.
[7]	VF: VLAN Frame	When set, this bit indicates that the transmitted frame is a VLAN-type frame.
[6:3]	Ctrl/status	These status bits indicate the number of collisions that occurred before the frame was transmitted. This count is not valid when the Excessive Collisions bit (TDES0[8]) is set. The core updates this status field only in the half-duplex mode.
[2]	ED: Excessive Deferral	When set, this bit indicates that the transmission has ended because of excessive deferral of over 24,288 bit times (if Jumbo Frame is enabled) if bit EMACDEFERRAL of EMACCONFIG_REG is set high.
[1]	UF: Underflow Error	When set, this bit indicates that the MAC aborted the frame because the data arrived late from the Host memory. Underflow Error indicates that the DMA encountered an empty transmit buffer while transmitting the frame. The transmission process enters the Suspended state and sets both Bit[5] in Transmit Underflow Register (Status Register) and Bit[0] in Transmit Interrupt Register (Status Register).
[0]	DB: Deferred Bit	When set, this bit indicates that the MAC defers before transmission because of the presence of a carrier. This bit is valid only in the half-duplex mode.

Table 24.8-2. Transmit Descriptor 1 (TDES1)

Bits	Name	Description
[31:29]	SAIC: SA Insertion Control	These bits request the MAC to add or replace the Source Address field in the Ethernet frame with the value given in the MAC Address 0 register. If the Source Address field is modified in a frame, the MAC automatically recalculates and replaces the CRC bytes. The Bit[31] specifies the MAC Address Register value (1 or 0) that is used for Source Address insertion or replacement. The following list describes the values of Bits[30:29]: • 2'b00: Do not include the source address. • 2'b01: Include or insert the source address. For reliable transmission, the application must provide frames without source addresses. • 2'b10: Replace the source address. For reliable transmission, the application must provide frames with source addresses. • 2'b11: Reserved These bits are valid when the First Segment control bit (TDES0[28]) is set.
[28:16]	Reserved	Reserved
[15:13]	Reserved	Reserved
[12:0]	TBS1: Transmit Buffer 1 Size	These bits indicate the data buffer byte size in bytes. If this field is 0, the DMA ignores this buffer and uses Buffer 2 or the next descriptor.

Table 24.8-3. Transmit Descriptor 2 (TDES2)

Bits	Name	Description
[31:0]	Buffer 1 Address Pointer	These bits indicate the physical address of Buffer 1.

Table 24.8-4. Transmit Descriptor 3 (TDES3)

Bits	Name	Description
[31:0]	Next Descriptor Address	This address contains the pointer to the physical memory where the Next Descriptor is present.

24.8.2 Receive Descriptors

The structure of the receiver linked lists is shown in Figure 24.8-2. Table 24.8-5 to Table 24.8-9 provide the description of the linked lists.

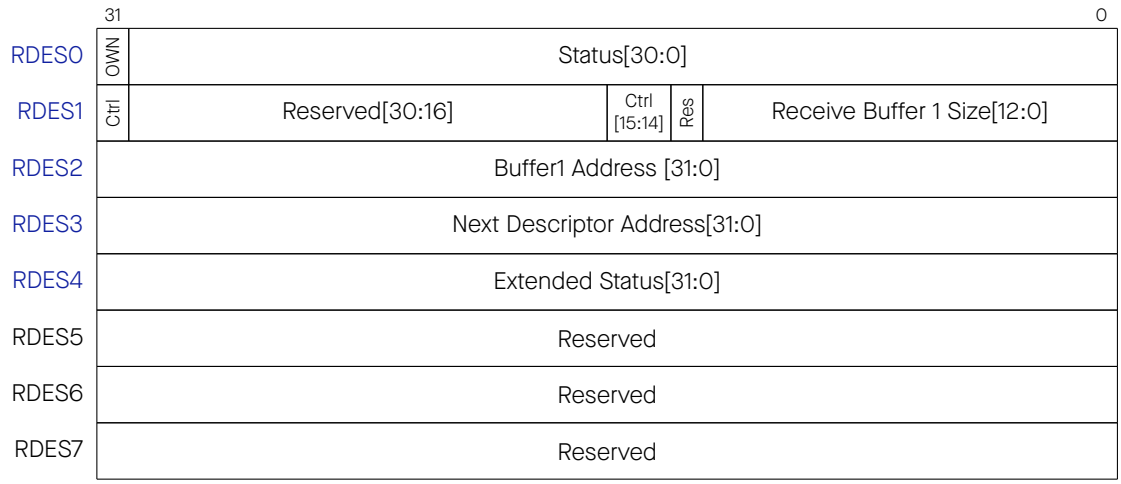

Figure 24.8-2. Receive Descriptor

Table 24.8-5. Receive Descriptor 0 (RDES0)

Bits	Name	Description
[31]	OWN: Own Bit	When set, this bit indicates that the descriptor is owned by the DMA of the DWC_gmac. When this bit is reset, it indicates that the descriptor is owned by the Host. The DMA clears this bit either when it completes the frame reception or when the buffers that are associated with this descriptor are full.
[30]	AFM: Destination Address Filter Fail	When set, this bit indicates a frame that failed in the DA Filter in the MAC.
[29:16]	FL: Frame Length	These bits indicate the byte length of the received frame that was transmitted to host memory. This field is valid when Last Descriptor (RDES0[8]) is set and either the Descriptor Error (RDES0[14]) or Overflow Error bits is reset. The frame length also includes the two bytes appended to the Ethernet frame when IP checksum calculation (Type 1) is enabled and the received frame is not a MAC control frame.
[15]	ES: Error Summary	Indicates the logical OR of the following bits: • RDES0[1]: CRC Error • RDES0[3]: Receive Error • RDES0[4]: Watchdog Timeout • RDES0[6]: Late Collision • RDES0[7]: Giant Frame • RDES4[4:3]: IP Header or Payload Error • RDES0[11]: Overflow Error • RDES0[14]: Descriptor Error This field is valid only when the Last Descriptor (RDES0[8]) is set.
[14]	DE: Descriptor Error	When set, this bit indicates a frame truncation caused by a frame that does not fit within the current descriptor buffers, and that the DMA does not own the Next Descriptor. The frame is truncated. This field is valid only when the Last Descriptor (RDES0[8]) is set.

Bits	Name	Description
[13]	SAF: Source Address Filter Fail	When set, this bit indicates that the SA field of frame failed the SA Filter in the MAC.
[12]	LE: Length Error	When set, this bit indicates that the actual length of the frame received and that the Length/Type field does not match. This bit is valid only when the Frame Type (RDES0[5]) bit is reset.
[11]	OE: Overflow Error	When set, this bit indicates that the received frame was damaged because of buffer overflow in MTL.
[10]	VLAN: VLAN Tag	When set, this bit indicates that the frame to which this descriptor is pointing is a VLAN frame tagged by the MAC. The VLAN tagging depends on checking the VLAN fields of the received frame based on the Register (VLAN Tag Register) settings.
[9]	FS: First Descriptor	When set, this bit indicates that this descriptor contains the first buffer of the frame. If the size of the first buffer is 0, the second buffer contains the beginning of the frame. If the size of the second buffer is also 0, the next Descriptor contains the beginning of the frame.
[8]	LS: Last Descriptor	When set, this bit indicates that the buffers pointed to by this descriptor are the last buffers of the frame.
[7]	IP Checksum Error (Type1), or Giant Frame	When IP Checksum Engine (Type 1) is selected, this bit, if set, indicates one of the following: • The 16-bit IPv4 header checksum calculated by the core did not match the received checksum bytes. • The header checksum checking is bypassed for non-IPv4 frames. Otherwise, this bit, when set, indicates the Giant Frame Status. Giant frames are larger than 1,518 bytes (or 1,522 bytes for VLAN or 2,000 bytes when Bit[27] of the MAC Configuration register is set), normal frames and larger-than-9,018-byte (9,022-byte for VLAN) frames when Jumbo Frame processing is enabled.
[6]	LC: Late Collision	When set, this bit indicates that a late collision has occurred while receiving the frame in the half-duplex mode.
[5]	FT: Frame Type	When set, this bit indicates that the Receive Frame is an Ethernet-type frame (the LT field is greater than, or equal to, 1,536). When this bit is reset, it indicates that the received frame is an IEEE 802.3 frame. This bit is not valid for Runt frames which are less than 14 bytes.
[4]	RWT: Receive Watchdog Timeout	When set, this bit indicates that the Receive Watchdog Timer has expired while receiving the current frame and the current frame is truncated after the Watchdog Timeout.
[3]	RE: Receive Error	When set, this bit indicates that the MII_RXER signal is asserted while MII_RXDV is asserted during frame reception.
[2]	DE: Dribble Bit Error	When set, this bit indicates that the received frame has a non-integer multiple of bytes (odd nibbles). This bit is valid only in the MII Mode.

Bits	Name	Description
[1]	CE: CRC Error	When set, this bit indicates that a Cyclic Redundancy Check (CRC) Error occurred on the received frame. This field is valid only when the Last Descriptor (RDES0[8]) is set.
[0]	Extended Status Available/ Rx MAC Address	When the IP Checksum Offload (Type 2) is present, this bit, when set, indicates that the extended status is available in descriptor word 4 (RDES4). This is valid only when the Last Descriptor bit (RDES0[8]) is set. This bit is invalid when Bit 30 is set. When IP Checksum Offload (Type 2) is present, this bit is set even when the IP Checksum Offload engine bypasses the processing of the received frame. The bypassing may be because of a non-IP frame or an IP frame with a non-TCP/UDP/ICMP payload. When the IPC Full Offload is not selected, this bit indicates an Rx MAC Address status. When set, this bit indicates that the Rx MAC Address registers value (1 to 15) matched the frame's DA field. When reset, this bit indicates that the Rx MAC Address Register 0 value matched the DA field.

Table 24.8-6. Receive Descriptor 1 (RDES1)

Bits	Name	Description
[31]	Ctrl	When set, this bit prevents setting the Status Register's RI bit (CSR5[6]) for the received frame that ends in the buffer indicated by this descriptor. This, in turn, disables the assertion of the interrupt to Host because of the RI for that frame.
[30:29]	Reserved	Reserved
[28:16]	Reserved	Reserved
[15]	RER: Receive End of Ring	When set, this bit indicates that the descriptor list reached its final descriptor. The DMA returns to the base address of the list, creating a Descriptor Ring.
[14]	RCH: Second Address Chained	When set, this bit indicates that the second address in the descriptor is the Next Descriptor address rather than the second buffer address. When this bit is set, RBS2 (RDES1[28:16]) is a "don't care" value. RDES1[15] takes precedence over RDES1[14].
[13]	Reserved	Reserved
[12:0]	RBS1: Receive Buffer 1 Size	Indicates the first data buffer size in bytes. The buffer size must be a multiple of 4, even if the value of RDES2 (buffer1 address pointer) is not aligned to bus width. When the buffer size is not a multiple of 4, the resulting behavior is undefined. If this field is 0, the DMA ignores this buffer and uses Buffer 2 or the next descriptor depending on the value of RCH (Bit[14]).

Table 24.8-7. Receive Descriptor 2 (RDES2)

Bits	Name	Description
[31:0]	Buffer 1 Address Pointer	These bits indicate the physical address of Buffer 1.

Table 24.8-8. Receive Descriptor 3 (RDES3)

Bits	Name	Description
[31:0]	Next Descriptor Address	This address contains the pointer to the physical memory where the Next Descriptor is present.

Table 24.8-9. Receive Descriptor 4 (RDES4)

Bits	Name	Description
[31:28]	Reserved	Reserved
[27:26]	Reserved	Reserved
[25]	Reserved	Reserved
[24]	Reserved	Reserved
[23:21]	Reserved	Reserved
[20:18]	Reserved	Reserved
[17]	Reserved	Reserved
[16]	Reserved	Reserved
[15]	Reserved	Reserved
[14]	Reserved	Reserved
[13]	Reserved	Reserved
[12]	Reserved	Reserved
[11:8]	Message Type	These bits are encoded to give the type of the message received. • 3'b0000: Reserved • 3'b0001: SYNC (all clock types) • 3'b0010: Follow_Up (all clock types) • 3'b0011: Delay_Req (all clock types) • 3'b0100: Delay_Resp (all clock types) • 3'b0101: Pdelay_Req (in peer-to-peer transparent clock) • 3'b0110: Pdelay_Resp (in peer-to-peer transparent clock) • 3'b0111: Pdelay_Resp_Follow_Up (in peer-to-peer transparent clock) • 3'b1000: Announce • 3'b1001: Management • 3'b1010: Signaling • 3'b1011-3'b1110: Reserved • 3'b1111: Reserved
[7]	IPv6 Packet Received	When set, this bit indicates that the received packet is an IPv6 packet. This bit is updated only when Bit[10] (IPC) of Register (MAC Configuration Register) is set.

Bits	Name	Description
[6]	IPv4 Packet Received	When set, this bit indicates that the received packet is an IPv4 packet. This bit is updated only when Bit[10] (IPC) of Register (MAC Configuration Register) is set.
[5]	IP Checksum Bypassed	When set, this bit indicates that the checksum offload engine is bypassed.
[4]	IP Payload Error	When set, this bit indicates that the 16-bit IP payload checksum (that is, the TCP, UDP, or ICMP checksum) that the core calculated does not match the corresponding checksum field in the received segment. It is also set when the TCP, UDP, or ICMP segment length does not match the payload length value in the IP Header field. This bit is valid when either Bit 7 or Bit 6 is set.
[3]	IP Header Error	When set, this bit indicates that either the 16-bit IPv4 header checksum calculated by the core does not match the received checksum bytes, or the IP datagram version is not consistent with the Ethernet Type value. This bit is valid when either Bit[7] or Bit[6] is set.
[2:0]	IP Payload Type	These bits indicate the type of payload encapsulated in the IP datagram processed by the Receive Checksum Offload Engine (COE). The COE also sets these bits to 2'b00 if it does not process the IP datagram's payload due to an IP header error or fragmented IP. • 3'b000: Unknown or did not process IP payload • 3'b001: UDP • 3'b010: TCP • 3'b011: ICMP • 3'b1xx: Reserved This bit is valid when either Bit[7] or Bit[6] is set.

24.9 Register Summary

Note that specific fields or bits of a given register may have different access attributes. Below is the list of all attributes together with the abbreviations used in register descriptions.

- Read Only (RO)
- Write Only (WO)
- Read and Write (R/W)
- Read, Write, and Self Clear (R/W/SC)
- Read, Self Set, and Write Clear (R/SS/WC)
- Read, Write Set, and Self Clear (R/WS/SC)
- Read, Self Set, and Self Clear or Write Clear (R/SS/SC/WC)
- Read Only and Write Trigger (RO/WT)

- Read, Self Set, and Read Clear (R/SS/RC)
- Read, Write, and Self Update (R/W/SU)
- Latched-low (LL)
- Latched-high (LH)

Name	Description	Address	Access
DMA configuration and control registers			
DMABUSMODE_REG	Bus mode configuration	0x3FF69000	R/WS/SC
DMATXPOLLDEMAND_REG	Pull demand for data transmit	0x3FF69004	RO/WT
DMARXPOLLDEMAND_REG	Pull demand for data receive	0x3FF69008	RO/WT
DMARXBASEADDR_REG	Base address of the first receive descriptor	0x3FF6900C	R/W
DMATXBASEADDR_REG	Base address of the first transmit descriptor	0x3FF69010	R/W
DMASTATUS_REG	State of interrupts, errors and other events	0x3FF69014	R/SS/WC
DMAOPERATION_MODE_REG	Receive and Transmit operating modes and command	0x3FF69018	R/SS/WC
DMAIN_EN_REG	Enable / disable interrupts	0x3FF6901C	R/W
DMAMISSEDFR_REG	Missed Frame and Buffer Overflow Counter Register	0x3FF69020	R/W
DMARINTWDTIMER_REG	Watchdog timer count on receive	0x3FF69024	R/W
DMATXCURRDESC_REG	Pointer to current transmit descriptor	0x3FF69048	RO
DMARXCURRDESC_REG	Pointer to current receive descriptor	0x3FF6904C	RO
DMATXCURRADDR_BUF_REG	Pointer to current transmit buffer	0x3FF69050	RO
DMARXCURRADDR_BUF_REG	Pointer to current receive buffer	0x3FF69054	RO
MAC configuration and control registers			
EMACCONFIG_REG	MAC configuration	0x3FF6A000	R/W
EMACFF_REG	Frame filter settings	0x3FF6A004	R/W
EMACGMIIADDR_REG	PHY configuration access	0x3FF6A010	R/WS/SC
EMACMIIDATA_REG	PHY data read write	0x3FF6A014	R/W
EMACFC_REG	frame flow control	0x3FF6A018	R/WS/SC(FCB) R/W(BPA)
EMACDEBUG_REG	Status debugging bits	0x3FF6A024	RO
PMT_RWUFFR_REG	Remote Wake-Up Frame Filter	0x3FF6A028	RO
PMT_CSR_REG	PMT Control and Status	0x3FF6A02C	RO
EMACLPI_CSR_REG	LPI Control and Status	0x3FF6A030	RO
EMACLPITIMERSCONTROL_REG	LPI Timers Control	0x3FF6A034	RO
EMACINTS_REG	Interrupt status	0x3FF6A038	RO
EMACINTMASK_REG	Interrupt mask	0x3FF6A03C	R/W
EMACADDROHIGH_REG	Upper 16 bits of the first 6-byte MAC address	0x3FF6A040	R/W
EMACADDROLOW_REG	Lower 32 bits of the first 6-byte MAC address	0x3FF6A044	R/W

Name	Description	Address	Access
EMACADDR1HIGH_REG	MAC address filtering and upper 16 bits of the second 6-byte MAC address	0x3FF6A048	R/W
EMACADDR1LOW_REG	Lower 32 bits of the second 6-byte MAC address	0x3FF6A04C	R/W
EMACADDR2HIGH_REG	MAC address filtering and upper 16 bits of the third 6-byte MAC address	0x3FF6A050	R/W
EMACADDR2LOW_REG	Lower 32 bits of the third 6-byte MAC address	0x3FF6A054	R/W
EMACADDR3HIGH_REG	MAC address filtering and upper 16 bits of the fourth 6-byte MAC address	0x3FF6A058	R/W
EMACADDR3LOW_REG	Lower 32 bits of the fourth 6-byte MAC address	0x3FF6A05C	R/W
EMACADDR4HIGH_REG	MAC address filtering and upper 16 bits of the fifth 6-byte MAC address	0x3FF6A060	R/W
EMACADDR4LOW_REG	Lower 32 bits of the fifth 6-byte MAC address	0x3FF6A064	R/W
EMACADDR5HIGH_REG	MAC address filtering and upper 16 bits of the sixth 6-byte MAC address	0x3FF6A068	R/W
EMACADDR5LOW_REG	Lower 32 bits of the sixth 6-byte MAC address	0x3FF6A06C	R/W
EMACADDR6HIGH_REG	MAC address filtering and upper 16 bits of the seventh 6-byte MAC address	0x3FF6A070	R/W
EMACADDR6LOW_REG	Lower 32 bits of the seventh 6-byte MAC address	0x3FF6A074	R/W
EMACADDR7HIGH_REG	MAC address filtering and upper 16 bits of the eighth 6-byte MAC address	0x3FF6A078	R/W
EMACADDR7LOW_REG	Lower 32 bits of the eighth 6-byte MAC address	0x3FF6A07C	R/W
EMACWDOGTO_REG	Watchdog timeout control	0x3FF6A0DC	R/W
Clock configuration registers			
EMAC_EX_CLKOUT_CONF_REG	RMII clock divider setting	0x3FF69800	R/W
EMAC_EX_OSCCLK_CONF_REG	RMII clock half and whole divider settings	0x3FF69804	R/W
EMAC_EX_CLK_CTRL_REG	Clock enable and external / internal clock selection	0x3FF69808	R/W
PHY type and SRAM configuration registers			
EMAC_EX_PHYINF_CONF_REG	Selection of MII / RMII phy	0x3FF6980C	R/W
EMAC_PD_SEL_REG	Ethernet RAM power-down enable	0x3FF69810	R/W

24.10 Registers

The addresses in this section are relative to the EMAC base address provided in Table 3.3-6 in Chapter 3 *System and Memory*. The absolute register addresses are listed in Section 24.9 *Register Summary*.