Yi-Min Tsai

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Email: yimintsai@gmail.com
Website: http://yimintsai.github.io/mysite

Summary

I am Yi-Min Tsai, a passionate and enthusiastic engineer! My interests are computer vision algorithms and image/video signal processing. I am also an IC designer. My current missions include developing advanced vision algorithms and building system prototypes for future products.

Experience

Senior Engineering Specialist, Quanta Computer Inc.

Algorithm Team Leader
October 2013 – Present

I am an algorithm and hardware engineer in Quanta Computer Inc, Taiwan. The job responsibilities include development of advanced image/video processing and intelligent vision/video analysis for IP cameras, mobile cameras and car cameras. I am also responsible for SoC architecture design of the corresponding device chips.

Education

Graduate Institute of Electronics Engineering, National Taiwan University (NTU-GIEE)

Ph.D. — 2007 – 2013

My proficient subjects include digital image and video signal processing, object recognition, machine learning, computer vision, and compressive sensing. I also majors in VLSI architecture design, digital circuit design, and cell-based design flow.

GPA: 4.28 / 4.3

Visiting Scholar, School of Engineering and Applied Sciences (SEAS), Harvard University

July 2011 – September 2011, July 2012 – September 2012

Dept. of Electrical Engineering, National Taiwan University (NTUEE)

B.S. — 2003 – 2007

GPA: 3.84 / 4.3, Grade: 85.81 / 100

Kaohsiung Senior High School (KSHS)

High School — 2000 – 2003

Honors

NTU-GIEE Research Award

Graduate Institute of Electronics Engineering, National Taiwan University

- Outstanding Research Award, 2013
- Outstanding Research Award, 2012

YM

National Taiwan University Innovation Contest
National Taiwan University

- First Prize Team, 2011
- Third Place Team, 2010
- Second Place Team, 2009
- Second Place Team, 2008

Yulon-Nissan Innovative Design Contest
Nissan Company, Inc.

- First Place Team, 2007

IEEE Custom Integrated Circuits Conference (CICC) Paper Award
IEEE

- Best Paper Award, Co-author, 2010

Taiwan Ministry of Education IC Design Contest
Taiwan Ministry of Education

- Third Place Team, 2009

MXIC Golden Silicon IC Design Contest
Macronix International Co., Ltd.

- Excellent Award Team, 2013
- Excellent Award Team, 2008
- First Prize Team, 2007
- Best Innovation Award Team, 2007

Phoenix IC Design Contest
Himax Technologies, Inc.

- First Prize Team, 2007
- Best Innovation Award Team, 2007

Skills

Software Programming
- C/C++
- Python
- JavaScript/jQuery
- Matlab

Hardware Design
- Verilog
- NC-Sim
- nLint
- Verdi
- Prime Power
- Design Vision
- SoC Encounter
- IC Compiler
- Calibre DRC/LVS
- Virtuoso

Web Design
- HTML5
- CSS3

Publications

Conference

1. **Yi-Min Tsai**, Tien-Ju Yang, and Liang-Gee Chen, “A 401GFlops/W 16-Cores Signal Reconstruction Platform with a 4G Entries/s Matrix Generation Engine for Compressed Sensing and Sparse Representation”, in Symposium on VLSI Circuits (VLSIC), 2013

2. **Yi-Min Tsai**, Keng-Yen Huang, H. T. Kung, Dario Vlah, Youngjune L. Gwon, and Liang-Gee Chen, “A Chip Architecture for Compressive Sensing Based Detection of IC Trojans”, in IEEE Workshop on Signal Processing Systems (SiPS), 2012

3. I-Kuei Chen, **Yi-Min Tsai**, Jyh-Jing Hwang, and Liang-Gee Chen , “Real-time Multi-user Face Unlock System via Fast Sparse Coding Approximation”, in IEEE International Conference on Consumer Electronics – Berlin (ICCE-Berlin), 2012

4. Chieh-Han Wu, Chung-Yu Chi, **Yi-Min Tsai**, and Liang-Gee Chen, “Compressive Sensing Based Client-Cloud System for 3D Depth Reconstruction”, in IEEE International Conference on Consumer Electronics – Berlin (ICCE-Berlin), 2012

5. Tien-Ju Yang, **Yi-Min Tsai**, Chung-Te Li, and Liang-Gee Chen, “WarmL1: A Warm-start Homotopy-based Reconstruction Algorithm for Sparse Signals”, in IEEE International Symposium on Information Theory (ISIT), 2012

6. **Yi-Min Tsai**, Tien-Ju Yang, Chih-Chung Tsai, Keng-Yen Huang and Liang-Gee Chen, “A 69mW 140-meter/60fps and 60-meter/300fps Intelligent Vision SoC for Versatile Automotive Applications”, in Symposium on VLSI Circuits (VLSIC), 2012

7. Keng-Yen Huang, **Yi-Min Tsai**, Tien-Ju Yang, and Liang-Gee Chen, “A High Speed Feature Matching Architecture for Real-time Video Stabilization” , in IEEE International Symposium on Circuits and Systems (ISCAS), 2012

8. Youngjune Gwon, H. T. Kung, Dario Vlah, Keng-Yen Huang, **Yi-Min Tsai**, “Statistical Screening for IC Trojan Detection”, in IEEE International Symposium on Circuits and Systems (ISCAS), 2012

9. Wei-Kai Chan, Yu-Hsiang Tseng, Pei-Kuei Tsung, Tzu-Der Chuang, **Yi-Min Tsai**, Wei-Yin Chen, Liang-Gee Chen, and Shao-Yi Chien, “ReSSP: A 5.877 TOPS/W Reconfigurable Smart-camera Stream Processor”, in IEEE Custom Integrated Circuits Conference (CICC), 2011

10. Yu-Chi Su, Keng-Yen Huang, Tse-Wei Chen, **Yi-Min Tsai**, Shao-Yi Chien and Liang-Gee Chen, “A 52mW Full HD 80-Degree Viewpoint Recognition SoC with Visual Vocabulary Processor for Wearable Vision Applications”, in IEEE International Symposium on VLSI Circuits (VLSIC), 2011

11. **Yi-Min Tsai**, Chih-Chung Tsai, Keng-Yen Huang, and Liang-Gee Chen, “Algorithm and Architecture Design of a Knowledge-based Vehicle Tracking for Intelligent Cruise Control”, in IEEE International Conference on Multimedia and Expo (ICME), 2011

12. Tien-Ju Yang, **Yi-Min Tsai**, and Liang-Gee Chen, “Smart Display: A Mobile Self-adaptive Projector-camera System”, in IEEE International Conference on Multimedia and Expo (ICME), 2011

13. Yun-Yu Chen, **Yi-Min Tsai**, and Liang-Gee Chen, “Algorithm and Implementation of Multi-channel Spike Sorting Using GPU in a Home-care Surveillance System”, in IEEE International Conference on Multimedia and Expo (ICME), 2011

14. **Yi-Min Tsai**, Chih-Chung Tsai, Keng-Yen Huang, and Liang-Gee Chen, “An Intelligent Vision-based Vehicle Detection and Tracking System for Automotive Applications”, in IEEE International Conference on Consumer Electronics (ICCE), 2011

15. **Yi-Min Tsai**, Keng-Yen Huang, Chih-Chung Tsai, and Liang-Gee Chen, “An Exploration of On-road Vehicle Detection Using Hierarchical Scaling Schemes”, in IEEE International Conference on Image Processing (ICIP), 2010

16. Keng-Yen Huang, **Yi-Min Tsai**, Chih-Chung Tsai, and Liang-Gee Chen, “Video Stabilization for Vehicular Applications Using Surf-like Descriptor and KD-tree”, in IEEE International Conference on Image Processing (ICIP), 2010

17. Chih-Chi Cheng, **Yi-Min Tsai**, Liang-Gee Chen and Anantha P. Chandrakasan, “A 0.077 to 0.168 nJ/bit/iteration Scalable 3GPP LTE Turbo Decoder with an Adaptive Sub-Block Parallel Scheme and an Embedded DVFS Engine”, in IEEE Custom Integrated Circuits Conference (CICC), 2010 (Best Paper Award)

18. **Yi-Min Tsai**, Keng-Yen Huang, Chih-Chung Tsai, and Liang-Gee Chen, “Learning-based Vehicle Detection Using Up-scaling Schemes and Predictive Frame Pipeline Structures”, in IEEE International Conference on Pattern Recognition (ICPR), 2010

19. Keng-Yen Huang, **Yi-Min Tsai**, Chih-Chung Tsai, and Liang-Gee Chen, “Feature-based Video Stabilization for Vehicular Applications”, in IEEE International Symposium on Consumer Electronics (ISCE), 2010

20. Chao-Chung Cheng, Chung-Te Li, Po-Sen Huang, Tsung-Kai Lin, **Yi-Min Tsai**, and Liang-Gee Chen, “A Block-based 2D-to-3D Conversion System with Bilateral Filter”, in IEEE International Conference on Consumer Electronics (ICCE), 2009

21. Chao-Chung Cheng, Chung-Te Li, **Yi-Min Tsai**, Liang-Gee Chen, “Hybrid Depth Cueing for 2D-to-3D Conversion System”, in Proceedings of SPIE-IS&T Electronic Imaging, 2009

22. Chao-Chung Cheng, Chung-Te Li, **Yi-Min Tsai**, Liang-Gee Chen, “A Quality-scalable Depth-aware Video”, in Society For Information Display (SID), 2009

23. Chung-Te Li, Chao-Chung Cheng, **Yi-Min Tsai** and Liang-Gee Chen, “Depth-aware Achromatic Image/Video Enhancement”, International Display Manufacturing Conference / 3D Systems and Applications / Asia Display (3DSA), 2009

24. Yu-Lin Chang, **Yi-Min Tsai**, Liang-Gee Chen, “A Real-time Augmented View Synthesis System for Transparent Car Pillars”, in IEEE International Conference on Image Processing (ICIP), 2008

25. Yu-Lin Chang, Wei-Yin Chen, Jing-Ying Chang, **Yi-Min Tsai**, Chia-Lin Lee, and Liang-Gee Chen, “Priority Depth Fusion for the 2D to 3D Conversion System”, in Proceedings of SPIE-IS&T Electronic Imaging, 2008

26. **Yi-Min Tsai**, Yu-Lin Chang, Liang-Gee Chen, “Symmetric Trinocular Dense Disparity Estimation for Car Surrounding Camera Array”, in Proceedings of SPIE-IS&T Electronic Imaging, 2007

27. **Yi-Min Tsai**, Yu-Lin Chang, Liang-Gee Chen, “Block-based Vanishing Line and Vanishing Point Detection for 3D Scene Reconstruction”, in IEEE International

Symposium on Intelligent Signal Processing and Communication Systems (ISPACS), 2006

Journal

1. Yu-Chi Su, Keng-Yen Huang, Tse-Wei Chen, **Yi-Min Tsai**, Shao-Yi Chien and Liang-Gee Chen, "A 52mW Full HD 80-Degree Viewpoint Recognition SoC with Visual Vocabulary Processor for Wearable Vision Applications", in IEEE Journal of Solid State Circuit (JSSC), 2012

2. Tse-Wei Chen, Yu-Chi Su, Keng-Yen Huang, **Yi-Min Tsai**, Shao-Yi Chien and Liang-Gee Chen, "Visual Vocabulary Processor Based on Binary Tree Architecture for Full-HD Object Recognition", in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012

Patent

1. "3D Depth Generation by Vanishing Line Detection", Liang-Gee Chen, Chao-Chung Cheng , **Yi-Min Tsai**, and Ling-Hsiu Huang, US 2010-0079453-A1

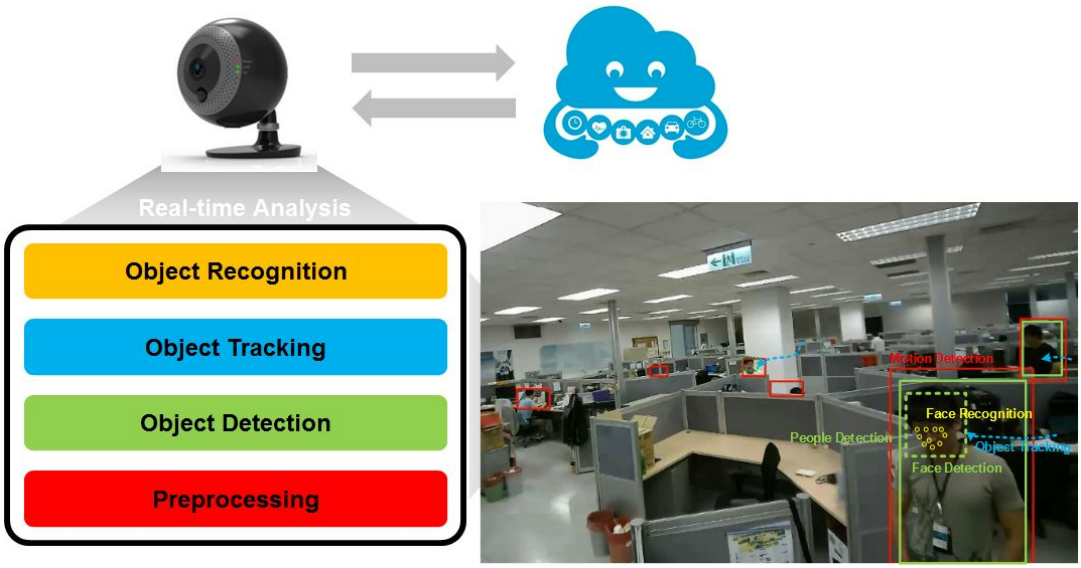
2. "Driving Support System with Plural Dimension Processing Units", Liang-Gee Chen, Yu-Lin Chang, **Yi-Min Tsai**, and Chao-Chung Cheng, US-2010-0054541-A1

3. "System and Method for Automatically Adjusting Visual Setting of Display Device", Liang-Gee Chen, Jing-Ying Chang, and **Yi-Min Tsai**, US 2011-0141114-A1

Projects

Intelligent Vision Analysis

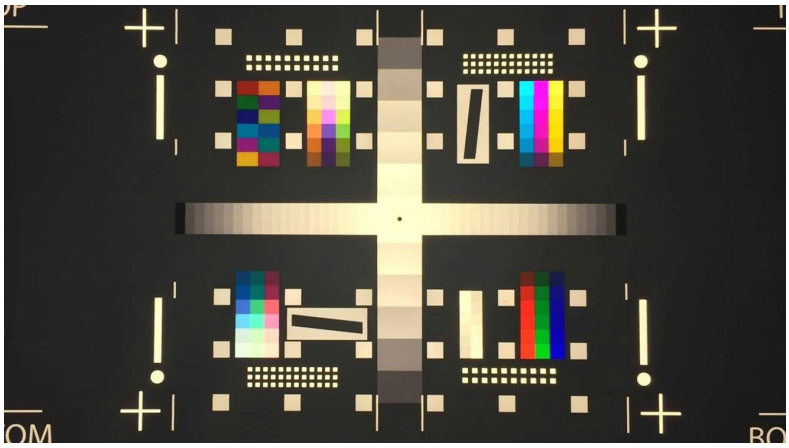
October 2013 – Present, Quanta Computer Inc.



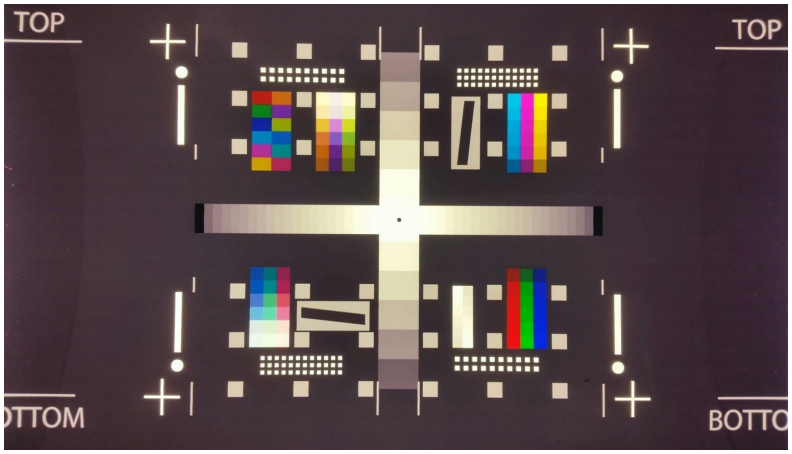
In this project, we develop intelligent vision/video analysis (IVA) techniques for IP cameras in smart home and smart retail applications. Motion detection is used to find motions from environment. Region-of-interest can be set according to user scenarios. Object detection such as face and people detection provides recognition capabilities and space information. Object tracking is applied to record moving histories. These IVA techniques can then be applied to applications such as video synopsis and surveillance. We also implement our IVA in embedded systems for real-time requirements.

Advanced ISP

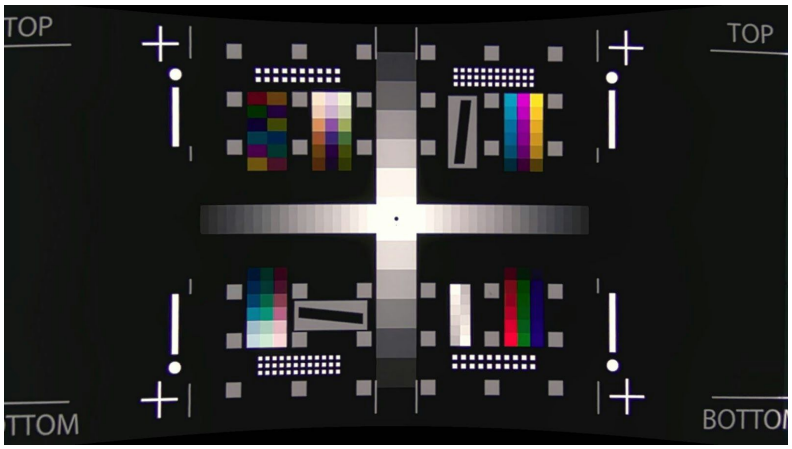
October 2013 – Present, Quanta Computer Inc.



iPhone 5S



Samsung S5

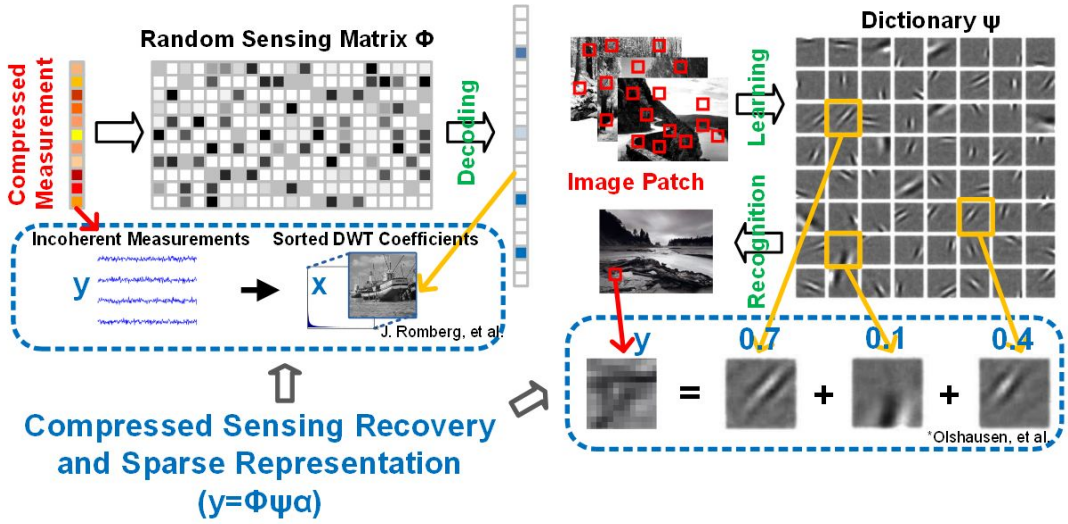


AISP

In this project, we develop an advanced ISP (AISP) pipeline for HDR video/image. AISP supports various HDR sensors, including native, interlaced, and staggered sensors. The features of AISP include texture-aware noise reduction, adaptive exposure fusion, perceptual local tone-mapping, saturation adjustment, and region-based AE/AWB. The AISP dynamically adjusts low-light exposure curve and outperforms other ISP in low-light details. The AISP IP is also verified through FPGA implementation.

Compressive Sensing and Sparse Representation

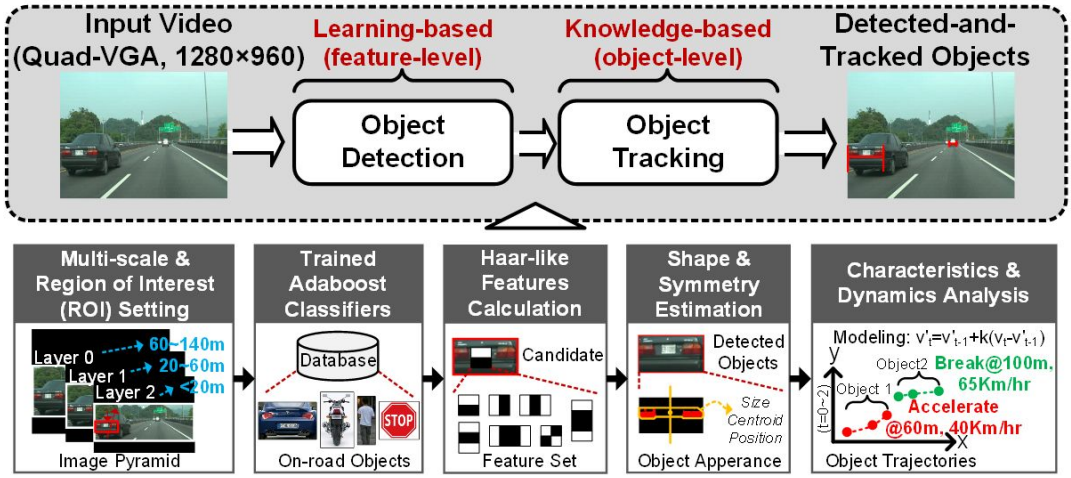
March 2011 – June 2013, National Taiwan University



Compressive sensing is a new signal processing paradigm that can acquire a sparse signal representation with linear random projections. It allows encoding a signal with sparsity constraints and recovering the signal with only few compressed measurements. An object pattern can be represented by a small set of atoms of an over-complete dictionary through sparse approximation. The sparsity constraint enforces such efficient expressions of visual patterns. In this project, we apply compressive sensing and sparse representation for visual recognition tasks.

Intelligent Vehicle

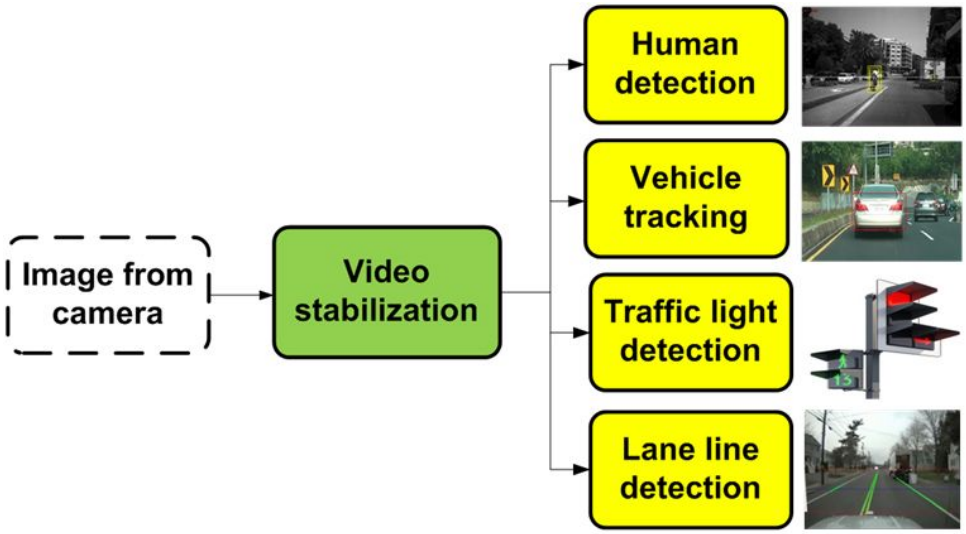
April 2009 – July 2011, National Taiwan University

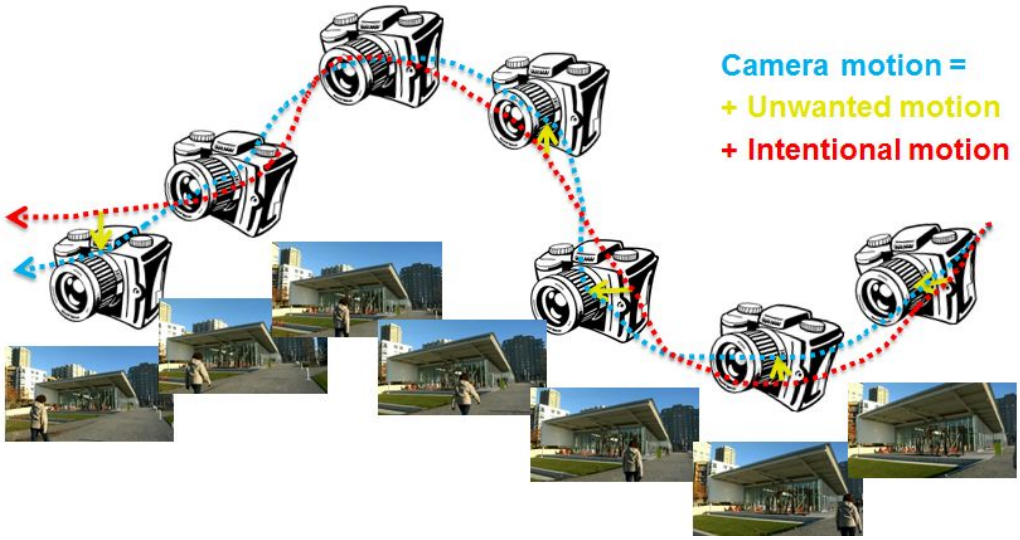


Owing to the maturity of vision sensors, vision-based systems play an essential role in many vehicular applications. Intelligent Cruise Control (ICC) provides semi-automatic driving mechanism. Collision Warning Systems (CWS) prevent vehicles from sudden crashes. These applications require detection and tracking of on-road vehicles to estimate distance between host and preceding vehicles or to monitor vehicles' behaviors on different lanes. We develop an intelligent vision-based on-road preceding vehicle detection-and-tracking system based on computer vision and machine learning techniques.

Video Stabilization

January 2009 – June 2011, National Taiwan University
October 2013 – December 2013, Quanta Computer Inc.

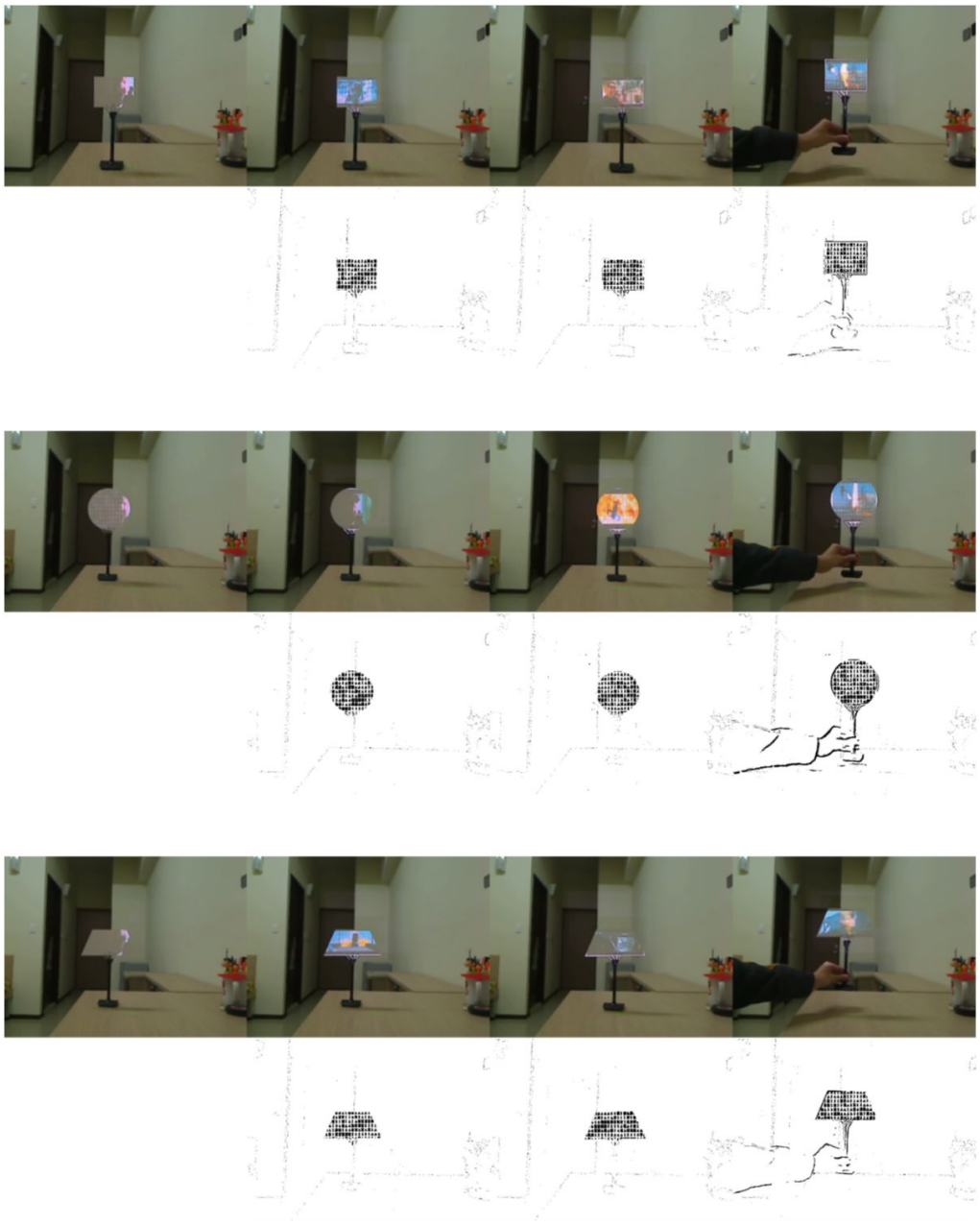




Video camera becomes smaller and eventually portable in many applications. However, the captured video may be blurred and shaky owing to unstable camera platforms. Many real-time applications need on-the-fly video stabilization to provide steady video inputs for further processing. We develop a feature-based real-time video stabilization framework in this project.

Smart Interface

September 2010 – February 2011, National Taiwan University



Augmented reality (AR) is a technique trying to build a bridge connecting the real world and the virtual world. By equipping a camera with a micro-projector, a mobile AR system is constructed. Owing to the diversity of projection surfaces, an effective mobile display system must be adaptive to the surface to avoid introducing a clipped scene. We propose a smart mobile display system which automatically adapts to the location and motion of a surface.

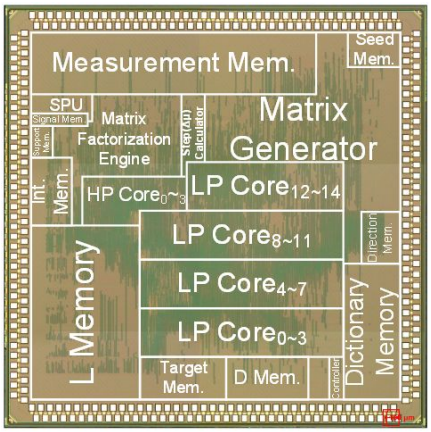
3D Video Processing

June 2007 – September 2008, National Taiwan University

For 2D to 3D conversion, monocular depth cues are utilized to generate the scene depth. In this project, we construct depth information from a single-view video sequence. By clustering vanishing lines and points, we can rebuild space structure and assign relative depth values to the 2D image.

Decoding Chip for Compressive Sensing and Sparse Representation

March 2011 – June 2013, National Taiwan University

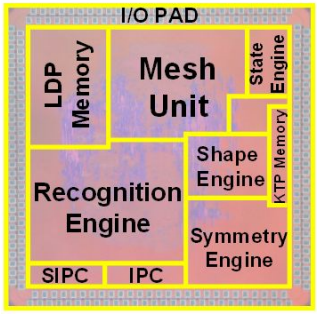


Technology Process	40nm 1P10M CMOS
Die / Core Area	3.7×3.7 / 2.6×2.6 mm^2
Core / IO Power Supply	0.9V / 2.5V
Gate Count (NAND2) / SRAM	1.85M (1.40M for MPC) / 232.5KB
Operating Frequency	250MHz
Processing Capability	141.8 GFlops
Power Consumption	353.3mW (15 LP cores, 4HP cores) 319.3mW (8 LP cores) 292.3mW (4 LP cores) 275.0mW (2 LP cores) 265.0mW (1 LP core)
Supported Sparsity Level	~0.01% ($N=2^{20}-1$) ~0.25% ($N=2^{16}-1$) ~1.50% ($N=2^{14}-1$) ~5.00% ($N=2^{12}-1$) ~25.0% ($N=2^{10}-1$)

A versatile signal reconstruction platform designed in a 40nm CMOS process is presented. The chip supports high-dimensional sparse signal reconstruction for compressed sensing and sparse representation. A 4G entries/s (8Gbps) high-throughput sensing matrix generation engine is proposed. It reduces over 75% external bandwidth and 77% processing cycles. The chip achieves 401GFlops/W power efficiency with 16 multi-processing cores. The chip also yields over 1000× improvement of computing time compared to software implementations.

Intelligent Vision SoC for Versatile Automotive Applications

April 2009 – July 2011, National Taiwan University

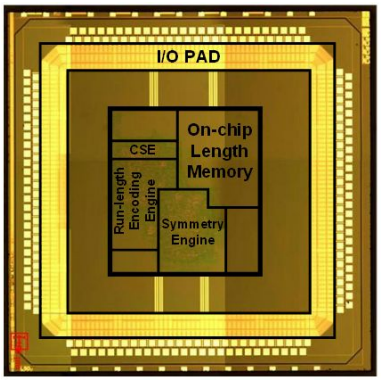


Technology Process	40nm 1P10M CMOS	
Die / Core Area	3.0×3.1 / 2.6×2.6 mm^2	
Core / IO Power Supply	0.9V / 2.5V	
Gate Count (NAND2) / SRAM	1.34M / 25.3KB (LDP: 23.75KB)	
Operating Frequency	Max. 220MHz (2 clock domains)	
Average / Peak Power	69.3mW / 172.2mW	
Peak Performance	Total: 517GOPS (LDP: 356GOPS)	
Processing Capability	LDP: 0.248G feature/s KTP: 0.2G pixel/s	
Frame Rate*	1280×960 (13 Layers)	61fps(DT) 34fps(D)
	640×480 (9 Layers)	199fps(DT) 72fps(D)

A machine-learning based intelligent vision SoC implemented on a 9.3 mm^2 die in a 40nm CMOS process is presented. The architecture realizes 140 meters active distance at 60fps and 60 meters at 300fps under Quad-VGA (1280×960) resolution while maintaining above 90% detection rate for versatile automotive applications. The system supports 64 object tracking and prediction. It raises 1.62× improvement on power efficiency and at least 1.79× increase on frame rate with the proposed knowledge-based tracking processor. The chip achieves 354.2fps/W and 3.01TOPS/W power efficiency with 69mW average power consumption.

Intelligent Vehicle Tracking Engine

April 2009 – July 2011, National Taiwan University



Technology	90nm CMOS
Chip Size	4.84 mm^2
Core Size	1.23 mm^2
Core V_{dd} / IO V_{dd}	1.2 V / 2.5V
On-chip Memory	12.8 Kbits
Operating Frequency	100 MHz
Supported Frame Rate	81.4 FPS@1280x960 11.3 FPS@4096x2160
Maximum Tracking Target #	5

We exploit a vision-based intelligent vehicle cruise control system via chip design. The knowledge-based vehicle tracking processor is implemented in an UMC 90nm Low-K SP CMOS process. The chip size is 2.2×2.2mm^2. The throughput is 5× to 10× compared to software implementation. Chip power dissipation has relations with number of targets. It consumes about 645mW for maximum 5 tracking tasks and 23mW for single-target tracking. For 4096×2160 specification, two memory banks are combined to support an object with maximum height 400 pixels. The chip operates at 100MHz frequency with 2.5V core voltage.

Services

Teaching Assistant

Graduate Institute of Electronics Engineering, National Taiwan University

- Innovation Venture and Entrepreneurship, 2012 Spring
- High-Tech Entrepreneurship and Operation, 2009 Fall, 2010 Fall
- Computer-Aided VLSI System Design, 2009 Fall, 2010 Fall
- GIEE Seminar, 2011 Fall, 2012 Spring, 2012 Fall

Teaching Assistant

Department of Electrical Engineering, National Taiwan University

- Integrated Circuit Design, 2010 Spring, 2011 Spring
- Switching Circuit and Logic Design, 2008 Fall
- Electronic Circuits Experiment (II), 2008 Spring

Website Designer

Acer Longterm-Smile Contest

- Chief Designer, 3rd Contest, 2008
- Chief Designer, 4th Contest, 2009

Workstation Manager

National Taiwan University SoC Center

- Administrator, June 2007 – December 2008

Languages

English

Full professional proficiency

Chinese

Native or bilingual proficiency