Chris Yim

EDUCATION

University of Illinois at Urbana-Champaign

Masters of Science, Electrical Engineering

GPA: 4.00/4.00

Graduating, May 2019

University of Illinois at Urbana-Champaign

Bachelor of Science, Electrical Engineering

Honors: Chancellor's Scholar, James Scholar

GPA: 3.74/4.00 Completed May 2017

COURSEWORK

(ECE 482) Digital IC Design	(ECE 310) Digital Signal Processing	(ECE 453) Wireless Communication Systems
(ECE 483) Analog IC Design	(ECE 385) Digital Systems Laboratory	(ECE 457) Passive Microwave Devices
(ECE 464) Power Electronics	(ECE 527) System-on-Chip Design (Fall 2017)	(ECE 447) Active Microwave Devices
(ECE 486) Control Systems	(ECE 459) Communications I (Fall 2017)	(ECE 451) Advanced Microwave Measurements

RESEARCH

Hanumolu Research Group

Analog/Mixed-Signal Graduate Student

• Exploring possible research topics through literature review

Urbana, IL August 2017 - Present

• Exploring possible research topics through iterature review

Shanbhag Research Group

Undergraduate Research Assistant

Urbana, IL January 2016 – May 2017

- Analyzed different radial basis function circuits for on-chip support vector machine classification
- Implemented a statistical error compensation scheme for digital ICs in a Verilog to MATLAB interface

Bretl Research Group

Undergraduate Research Assistant

Urbana, IL July 2014 – December 2015

• Designed a PCB which interfaced an analog front-end with a microprocessor for an EMG controlled prosthetic arm

o Published a paper for IEEE EMBC 2016

INTERNSHIPS

ViaSat RF/Microwave Engineering Intern Tempe, AZ

May 2017 - August 2017

- · Completed electrical stress analysis of a frequency converter module in the satellite
- Improved an HFSS model of an SMA to microstrip connection interface

Ecolab

Eagen, MN

RD&E Intern June 2016 – August 2016

Explored the feasibility of current signature analysis for detection of failures in solenoid valves and peristaltic pumps

PROJECTS

Binary Classifier

Fall 2015

- Developed a circuit that compares the Hamming distances between two pairs of input vectors
 - o Layout drawn in cadence with a 250nm process technology
 - o Optimized for minimum energy-delay product

Low-Dropout Voltage Regulator

Spring 2016

• Designed a voltage regulator that outputs 1.2 V - 1.5 V for 1mA - 10mA load current with specs on DC Line/Load regulation

INVOLVEMENT

Electronics Circuits Laboratory (ECE 343)

Teaching Assistant

University of Illinois August 2017 – Present

IEEE Technical Advancement Group for Circuits

Club Leader

University of Illinois Fall 2016 – May 2017

· Gave weekly lectures/workshops and supervised projects for students interested in circuits

TECHNICAL SKILLS

cadence, SystemVerilog, C/C++, MATLAB, EAGLE, ADS, HFSS